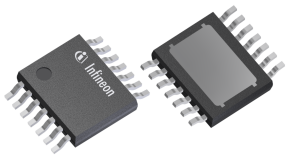
# PROFET™ Wire Guard smart power high-side switch

## Features



- High-side switch with diagnosis and embedded protection
- Selectable integrated I2t function for wire harness protection
- Operating current < 60 µA for active supply in key-off mode
- IDL pin for microcontroller wake-up in idle mode
- Adjustable overcurrent threshold
- Capacitive load switching mode
- Sequential diagnosis for status readout
- Reverse ON for low power dissipation in reverse polarity
- Switch-on capability while inverse current condition (Inverse ON)

AEC Qualified

RoHS

ISO 26262 compliant

## Potential applications

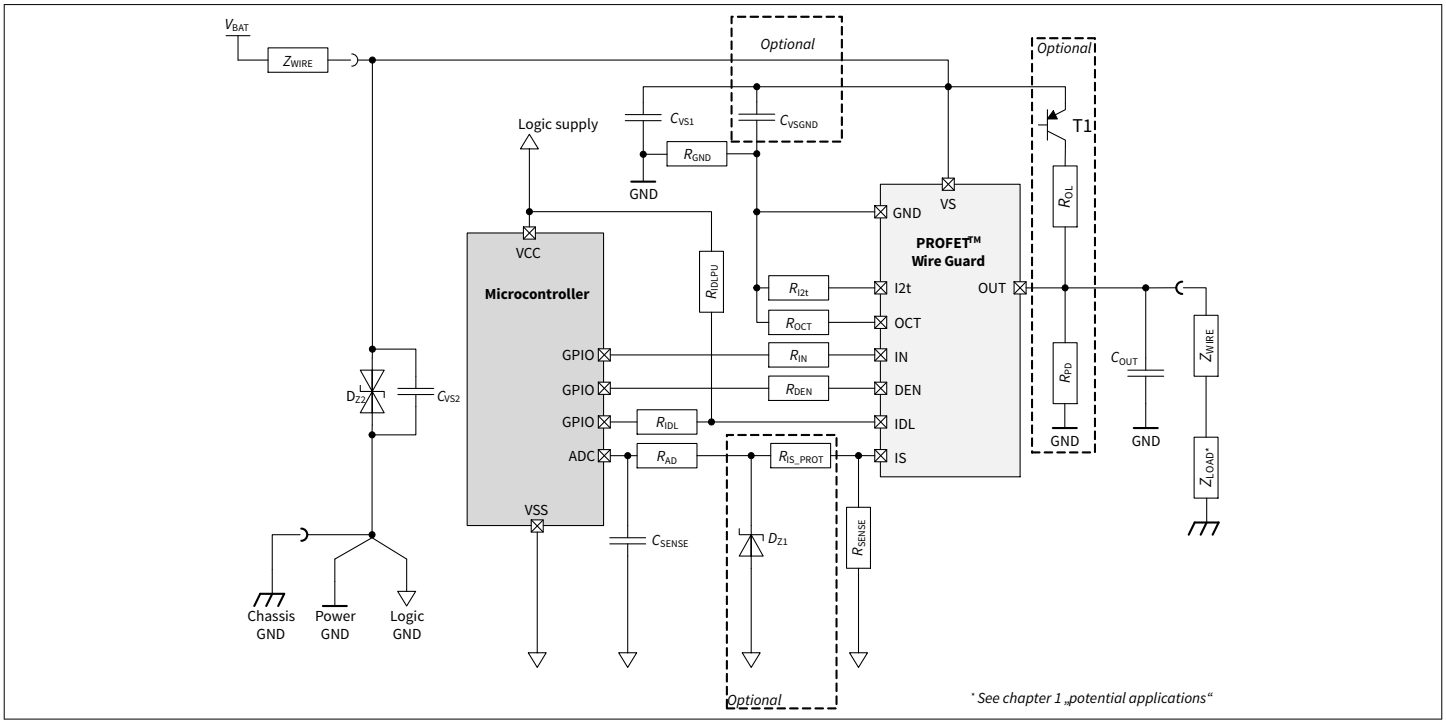
- Replaces electromechanical relays, fuses and discrete circuits
- Protection of  wire harness and system supply
- Main switch for ECU power supplies
- Switch for active power supplies in key-off mode
- Suitable for resistive, inductive and capacitive loads up to 10.3 A

## Product validation

Qualified for automotive applications. Product validation according to AEC-Q100 Grade 1.

## Description

The device is a smart power high-side switch, providing enhanced protection and diagnosis functions. Besides standard device protection functions it offers a selectable I2t protection, an adjustable overcurrent protection, an idle mode as well as a sequential diagnosis mode via IS pin.




| Product type | Package | Marking |
|---|---|---|
| BTG7007A-1EPW | PG-TSDSO-14 | 7007A1W |

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# 1 Product description

## 1.1 Product summary

**Table 1 Product summary**

| Parameter | Symbol | Values |
|---|---|---|
| Minimum operating voltage | $V_{S(OP)}$ | 4.1 V |
| Minimum operating voltage (cranking) | $V_{S(UV)}$ | 2.75 V |
| Maximum operating voltage | $V_S$ | 28 V |
| Minimum overvoltage protection ($T_J$ = 25°C) | $V_{DS(CLAMP)\_25}$ | 35 V |
| Maximum current in sleep mode ($T_J \leq$ 85°C) | $I_{VS(SLEEP)\_85}$ | 0.4 µA |
| Operating current in idle mode (channel ON) | $I_{GND(IDLE)}$ | 60 µA |
| Maximum operating current | $I_{GND(I2t\_D)}$ | 7.4 mA |
| Typical ON-state resistance ($T_J$ = 25°C) | $R_{DS(ON)\_25}$ | 8.0 mΩ |
| Maximum ON-state resistance ($T_J$ = 150°C) | $R_{DS(ON)\_150}$ | 14.7 mΩ |
| Nominal load current ($T_A$ = 85°C) | $I_{L(NOM)\_85}$ | 10.3 A |
| Highest configurable overcurrent detection threshold ($T_J$ = -40°C, $I_{OCT}$ = 50 µA) | $I_{L(HOCT)\_-40}$ | 66 A |
| Typical current sense ratio at $I_L = I_{L(NOM)\_85}$ | $k_{ILIS}$ | 13900 |

## 1.2 Further features

Further features are named in detail as follows:

- Green product (RoHS compliant)
- Proportional load current sense
- Open load in ON and OFF state
- Short circuit protection to ground and battery
- Readout of I2t and overcurrent protection settings
- Readout of wire harness protection status
- Absolute and dynamic temperature limitation with intelligent latch
- Adjustable overcurrent protection (tripping) with intelligent latch
- Selectable I2t function for wire harness protection with intelligent latch
- Undervoltage shutdown
- Overvoltage protection with external components

# 2 Block diagram and terms

## 2.1 Block diagram

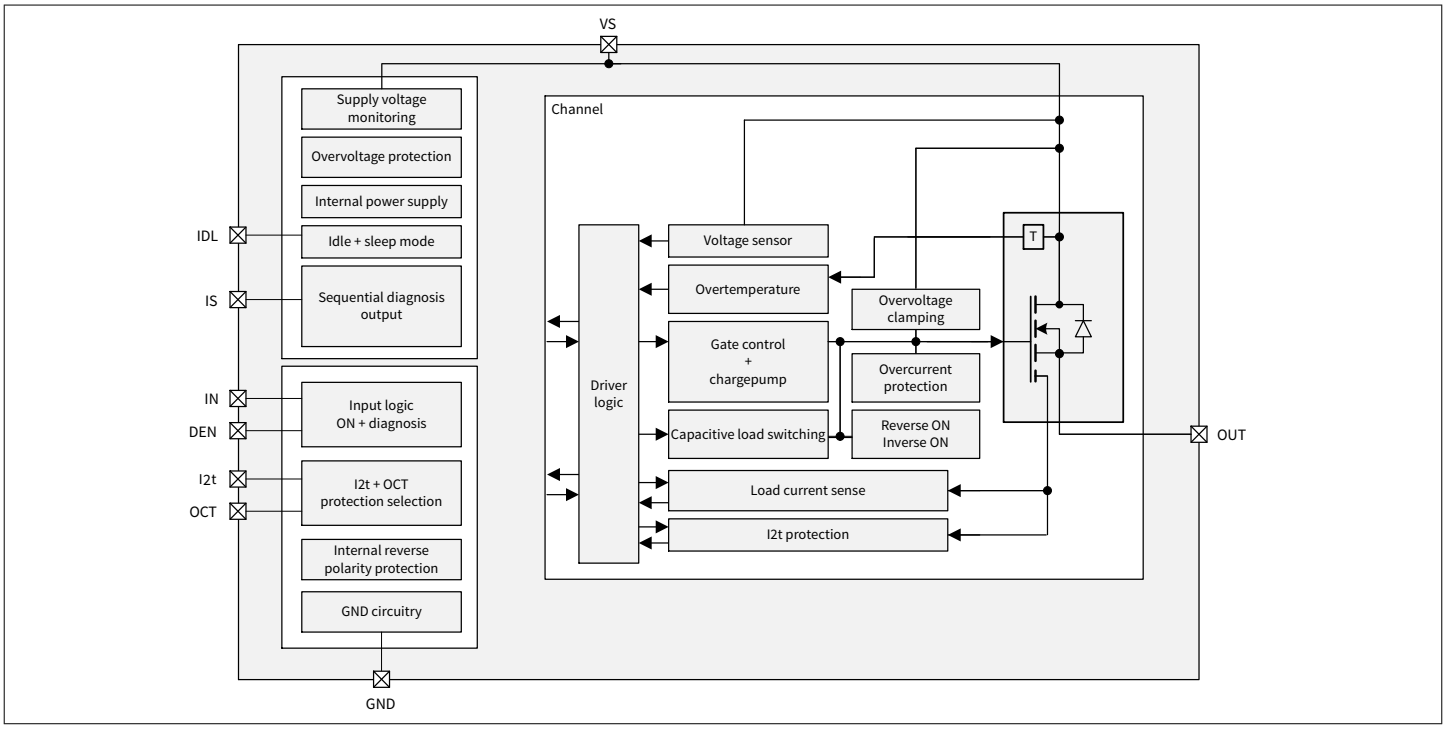



**Figure 1 Block diagram**

## 2.2 Terms

Figure 2 shows all terms used in this datasheet, with associated convention for positive values.

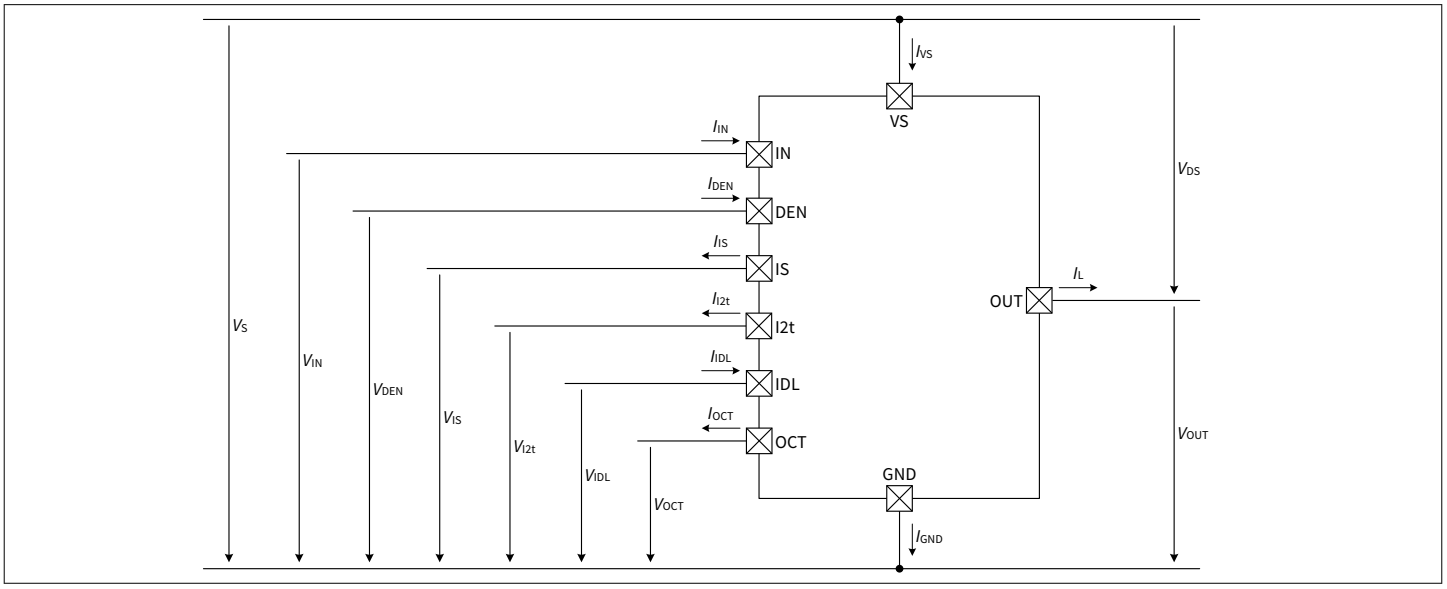



**Figure 2 Voltage and current convention**

# 3 Pin configuration

## 3.1 Pin assignment

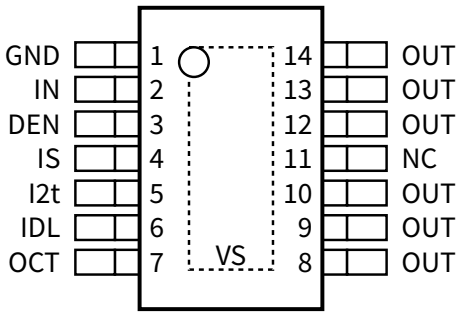



**Figure 3 Pin configuration**

## 3.2 Pin definitions and functions

| Pin | Symbol | Function |
|---|---|---|
| EP | VS (exposed pad) | **Supply voltage**<br>Battery voltage. |
| 1 | GND | **Ground**<br>Ground connection for the internal logic. |
| 2 | IN | **Input channel**<br>Digital signal to switch ON the channel (“high” active).<br>If not used: connect with a 10 kΩ resistor either to GND pin or to module ground. |
| 3 | DEN | **Diagnostic enable**<br>Digital signal to enable device diagnosis (“high” active) and to clear the protection latch of channel.<br>If not used: connect with a 10 kΩ resistor either to GND pin or to module ground. |
| 4 | IS | **SENSE current output**<br>Analog/digital signal for diagnosis.<br>If not used: left open. |
| 5 | I2t | **Selectable I2t protection curve**<br>A resistor $R_{I2t}$ needs to be connected between I2t pin and GND pin to select one of the available I2t protection curves.<br>If not used: left open. Curve selection as described in Chapter 9.1. |
| 6 | IDL | **Idle mode open drain output**<br>Digital signal to inform / wake-up the microcontroller in case of idle mode ("high impedance" in idle/sleep mode; "low" in all other modes).<br>If not used: left open. |

| Pin | Symbol | Function |
|---|---|---|
| 7 | OCT | **Adjustable overcurrent threshold**<br>A resistor $R_{OCT}$ needs to be connected between OCT pin and GND pin to adjust the overcurrent threshold.<br>If not used: left open. Threshold selection as described in Figure 27. |
| 11 | NC | Not connected, internally not bonded. |
| 8-10, 12-14 | OUT | **Output**<br>Protected high-side power output channel[1)]. |

1) All output pins of the channel must be connected together on the PCB. All pins of the output are internally connected together. PCB traces have to be designed to withstand the maximum current which can flow.

# 4 General product characteristics

## 4.1 Absolute maximum ratings

**Table 2 Absolute maximum ratings**

$T_J$ = -40°C to +150°C; all voltages and currents according to the voltage and current conventions, specified in Chapter 2.2 (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Supply pins** | | | | | | | |
| Power supply voltage | $V_S$ | -0.3 | – | 28 | V | 1) | PRQ-128 |
| Load dump voltage | $V_{BAT(LD)}$ | – | – | 35 | V | 1)<br>Suppressed load dump acc. to ISO16750-2 (2012)<br>$R_i$ = 2 Ω | PRQ-130 |
| Supply voltage for short circuit protection | $V_{BAT(SC)}$ | 0 | – | 24 | V | 1)<br>Setup acc. to AEC-Q100-012 | PRQ-132 |
| Reverse polarity voltage | $V_{BAT(REV)}$ | -18 | – | – | V | 1)<br>$t \leq$ 5 min<br>$T_A$ = 25 °C<br>Setup as described in Figure 54 | PRQ-134 |
| Current through GND pin | $I_{GND}$ | -50 | – | 50 | mA | 1)<br>$R_{GND}$ according to Chapter 11 | PRQ-138 |
| **Logic & control pins (digital input = DI) DI = IN, DEN** | | | | | | | |
| Current through DI pin | $I_{DI}$ | -1 | – | 2 | mA | 1) 2) | PRQ-141 |
| Current through DI pin - reverse battery condition | $I_{DI(REV)}$ | -1 | – | 10 | mA | 1) 2)<br>$t \leq$ 5 min | PRQ-142 |
| **Analog & control pins (analog input = AI) AI = I2t, OCT** | | | | | | | |
| Current through AI pin | $I_{AI}$ | -2 | – | 1 | mA | 1) 2) | PRQ-359 |
| Current through AI pin - reverse battery condition | $I_{AI(REV)}$ | -10 | – | 1 | mA | 1) 2)<br>$t \leq$ 5 min | PRQ-362 |

**(table continues...)**

**Table 2 (continued) Absolute maximum ratings**

$T_J$ = -40°C to +150°C; all voltages and currents according to the voltage and current conventions, specified in Chapter 2.2 (unless otherwise specified)

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Logic & control pins (digital output = DO)** | | | | | | | |
| **DO = IDL** | | | | | | | |
| Voltage at DO pin | $V_{DO}$ | -0.3 | – | 5.5 | V | 1) 2) | PRQ-828 |
| Current through DO pin | $I_{DO}$ | -1 | – | 2 | mA | 1) 2) | PRQ-360 |
| Current through DO pin - reverse battery condition | $I_{DO(REV)}$ | -1 | – | 10 | mA | 1) 2) $t \leq 5$ min | PRQ-361 |
| **IS pin** | | | | | | | |
| Voltage at IS pin | $V_{IS}$ | -1.5 | – | $V_S$ | V | 1) $I_{IS} < I_{IS(OFF)}$ | PRQ-144 |
| Current through IS pin | $I_{IS}$ | -25 | – | $I_{IS(SAT)}$, MAX | mA | 1) | PRQ-146 |
| **Temperatures** | | | | | | | |
| Junction temperature | $T_J$ | -40 | – | 150 | °C | 1) | PRQ-147 |
| Storage temperature | $T_{STG}$ | -55 | – | 150 | °C | 1) | PRQ-148 |
| **ESD robustness** | | | | | | | |
| ESD robustness all pins (HBM) | $V_{ESD\_HBM1}$ | -2 | – | 2 | kV | 1) HBM3) | PRQ-149 |
| ESD robustness OUT vs. GND and VS connected (HBM) | $V_{ESD\_HBM2}$ | -4 | – | 4 | kV | 1) HBM3) | PRQ-150 |
| ESD robustness all pins (CDM) | $V_{ESD\_CDM1}$ | -500 | – | 500 | V | 1) CDM4) | PRQ-151 |
| ESD robustness corner pins (CDM) - (pins 1, 7, 8, 14) | $V_{ESD\_CDM2}$ | -750 | – | 750 | V | 1) CDM4) | PRQ-152 |

1) Not subject to production test - specified by design.
2) Maximum VDI/VDO/VAI to be considered for latch-up tests: 5.5 V.
3) Human body model (HBM) robustness according to AEC - Q100-002.
4) Charged device model (CDM) robustness according to AEC - Q100-011 Rev-D; voltage level refers to test condition (TC) mentioned in the standard.

***Notes**:*

***1.*** *Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

***2.*** *Integrated protection functions are designed to prevent IC destruction under fault conditions described in the datasheet. Fault conditions are considered as "outside" normal operating range. Protection functions are not designed for continuous repetitive operation.*

**Table 3 Absolute maximum ratings - power stages**

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Load current | $\|I_L\|$ | – | – | $I_{L(HOCT),MAX}$ | A | 1) | PRQ-157 |
| Maximum energy dissipation - single pulse | $E_{AS}$ | – | – | 60 | mJ | 1)<br>$I_L = 2 \cdot I_{L(NOM)\_85}$<br>$T_{J(0)} = 150°C$<br>$V_S = 28$ V | PRQ-955 |
| Maximum energy dissipation - repetitive pulse | $E_{AR}$ | – | – | 17 | mJ | 1)<br>$I_L = I_{L(NOM)\_85}$<br>$T_{J(0)} = 85°C$<br>$V_S = 13.5$ V<br>1M cycles | PRQ-956 |

1) Not subject to production test - specified by design.

## 4.2 Functional range

**Table 4 Functional range**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Supply voltage range for normal operation | $V_{S(NOR)}$ | 5 | 13.5 | 20 | V | 1) | PRQ-158 |
| Lower extended supply voltage range for operation (normal) | $V_{S(EXT,LOW)}$ | 2.75 | – | 5 | V | 1) 2) 3) 4) (Parameter deviations possible) | PRQ-159 |
| Upper extended supply voltage range for operation | $V_{S(EXT,UP)}$ | 20 | – | 28 | V | 1) 4) (Parameter deviations possible) | PRQ-160 |
| Junction temperature | $T_J$ | -40 | – | 150 | °C | 1) | PRQ-161 |

1) Not subject to production test - specified by design.
2) In case of $V_S$ voltage decreasing refer to the maximum voltage of $V_{S(UV)}$. In case of $V_S$ voltage increasing refer to the maximum voltage of $V_{S(OP)}$.
3) Calculation of I2t protection curve with $I_L$ = 0 A for $V_S$ < 2.75 V (GND resistor voltage drop not included).
4) Device protection functions still operative.

## 4.3 Thermal resistance

**Table 5 Thermal resistance**

This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to www.jedec.org

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Thermal characterization parameter junction to top | $\Psi_{JTOP}$ | – | 2.2 | 3.8 | K/W | 1) 2) | PRQ-960 |
| Thermal resistance junction to case | $R_{thJC}$ | – | 2.4 | 4.1 | K/W | 1) 2) Simulated at exposed pad | PRQ-961 |
| Thermal resistance junction to ambient | $R_{thJA}$ | – | 32.9 | – | K/W | 1) 2) | PRQ-962 |

1) Not subject to production test - specified by design.
2) According to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; the product (chip + package) was simulated on a 76.2 × 114.3 × 1.5 mm board with 2 inner copper layers (2 × 70 µm Cu, 2 × 35 µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer. Simulation done at $T_A$ = 105°C, $P_{DISSIPATION}$ = 1 W.

## 4.4 PCB setup


70 µm modeled (traces, cooling area)

70 µm, 5% metalization*

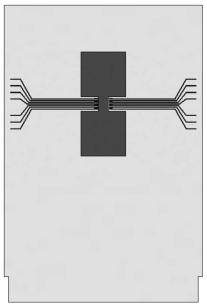
*: means percentual Cu metalization on each layer

**Figure 4 1s0p PCB cross section**

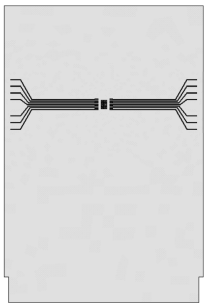

70 µm modeled (traces)
35 µm, 90% metalization*
35 µm, 90% metalization*
70 µm, 5% metalization*

*: means percentual Cu metalization on each layer

**Figure 5 2s2p PCB cross section**



PCB 1s0p + 600 mm² cooling



PCB 2s2p / 1s0p footprint

**Figure 6 PCB setup for thermal simulations**

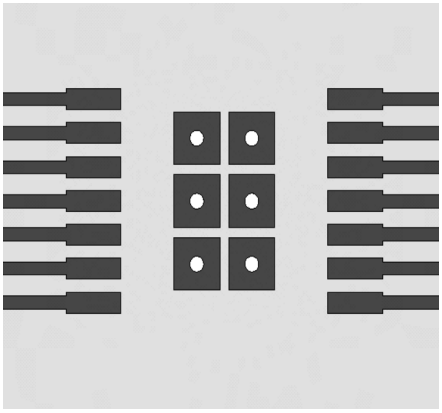


**Figure 7 Thermal vias on PCB for 2s2p PCB setup**

## 4.5 Thermal impedance

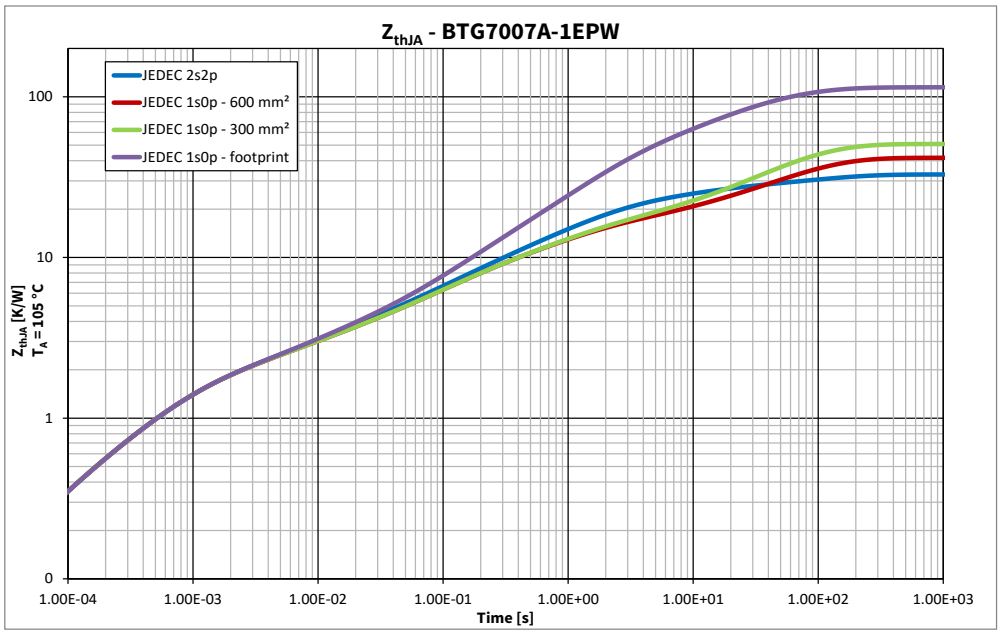



**Figure 8 Typical thermal impedance**

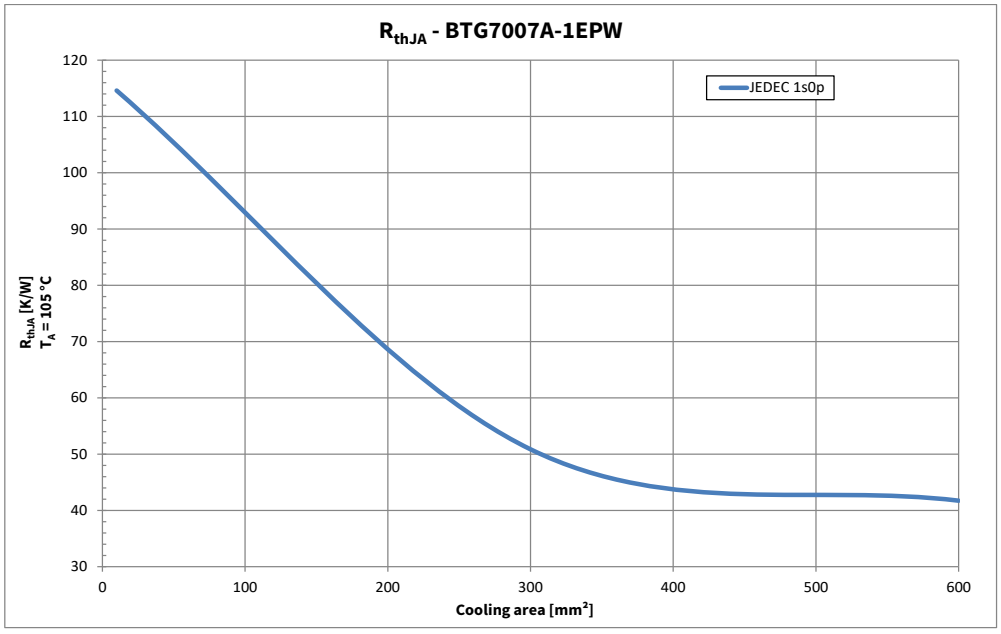



**Figure 9 Typical thermal resistance**

# 5 Logic pins

The device has two digital pins: One to control the output stage and the other one to control the diagnosis. Furthermore, there are two analog input pins for either selecting a generic I2t protection curve, or adjusting the overcurrent threshold; one open drain output pin for idle mode indication is available.

## 5.1 Latched input pin (IN)

The input pin IN activates the output channel. The input circuitry is compatible with 3.3 V and 5 V microcontrollers. The Latched Input feature activates an internal pull up current source in order to keep the input high after it's activation. This feature is deactivated when the DEN pin is set to high. The electrical equivalent of the input circuitry is shown in Figure 10. Indicating the behavior of the digital input current at IN pin $I_{IN(H)}$ by the change of the DEN and IN pin. In case the pin is not used, it must be connected with a 10 kΩ resistor either to GND pin or module ground.

The latched input feature allows the microcontroller to switch the GPIO controlling the IN pin into high impedance, while keeping the mode of the input status unchanged.

The input latch maintains the last mode of the input status as long as:

- Either the IN pin is not actively driven above or below the input thresholds
- The DEN pin is kept low

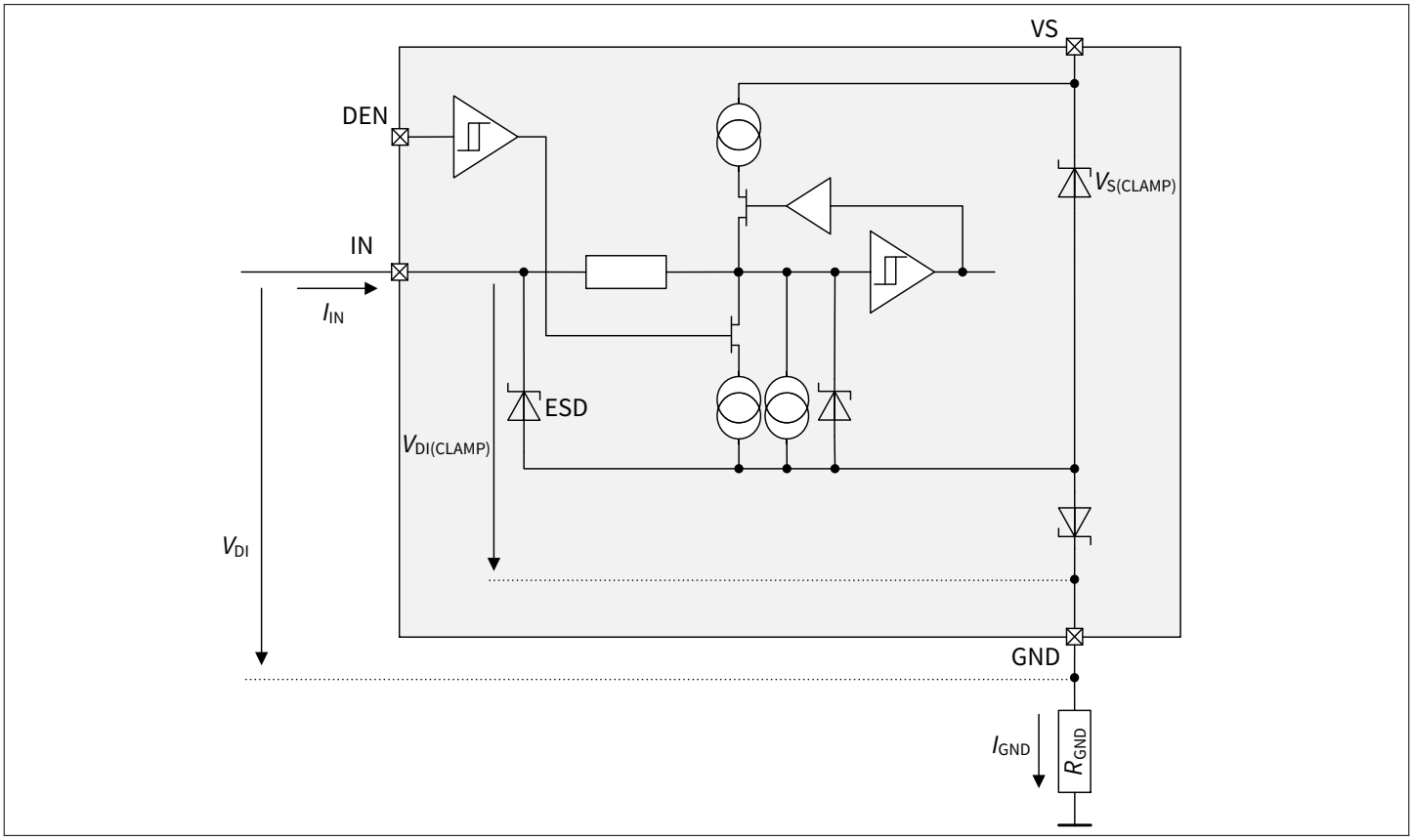



**Figure 10 IN pin circuitry**

The logic thresholds for "low" and "high" states are defined by parameters $V_{DI(TH)}$ and $V_{IN(HYS)}$. The relationship between these two values is shown in Figure 11. The voltage $V_{IN}$ needed to ensure a "high" state is always higher than the voltage needed to ensure a "low" state.

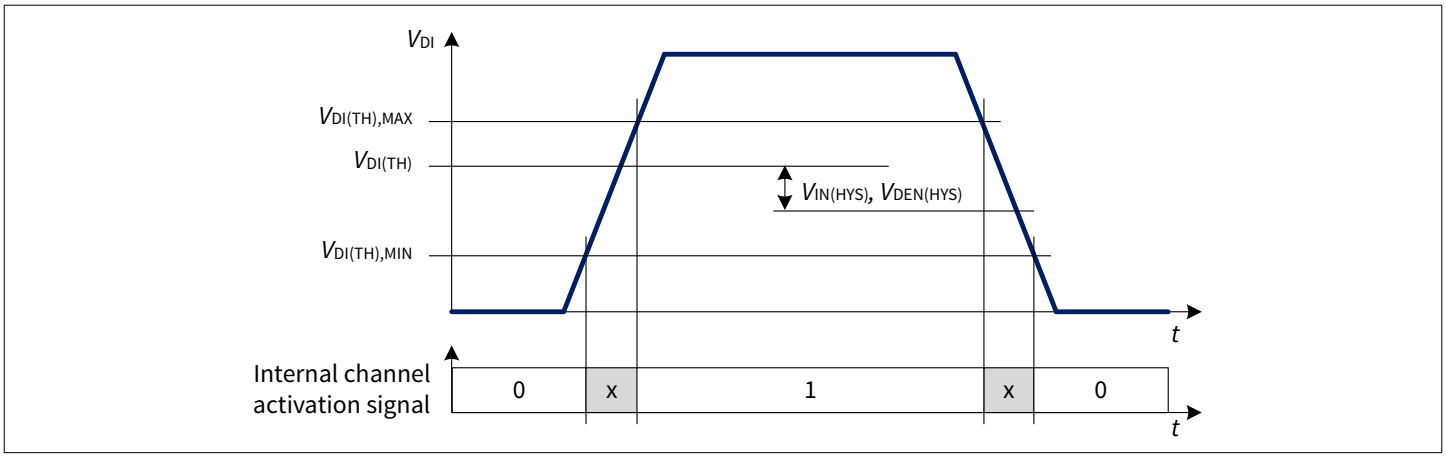



**Figure 11 Input threshold voltages and hysteresis**

## 5.2 Diagnosis pin (DEN)

The diagnosis enable (DEN) pin controls the diagnosis circuitry and can be used to reset the latched protection. The protection circuitry is not disabled by the DEN pin. When the DEN pin is set to “high”, the diagnosis is enabled (see Chapter 10.1.1 for more details) as well as the sequential diagnosis by applying a dedicated DEN "low" pulse (see Figure 42 for more details). When it is set to “low”, the diagnosis is disabled and the IS pin is set to high impedance. The latched protection is reset with a dedicated DEN "high" pulse (see Figure 32).

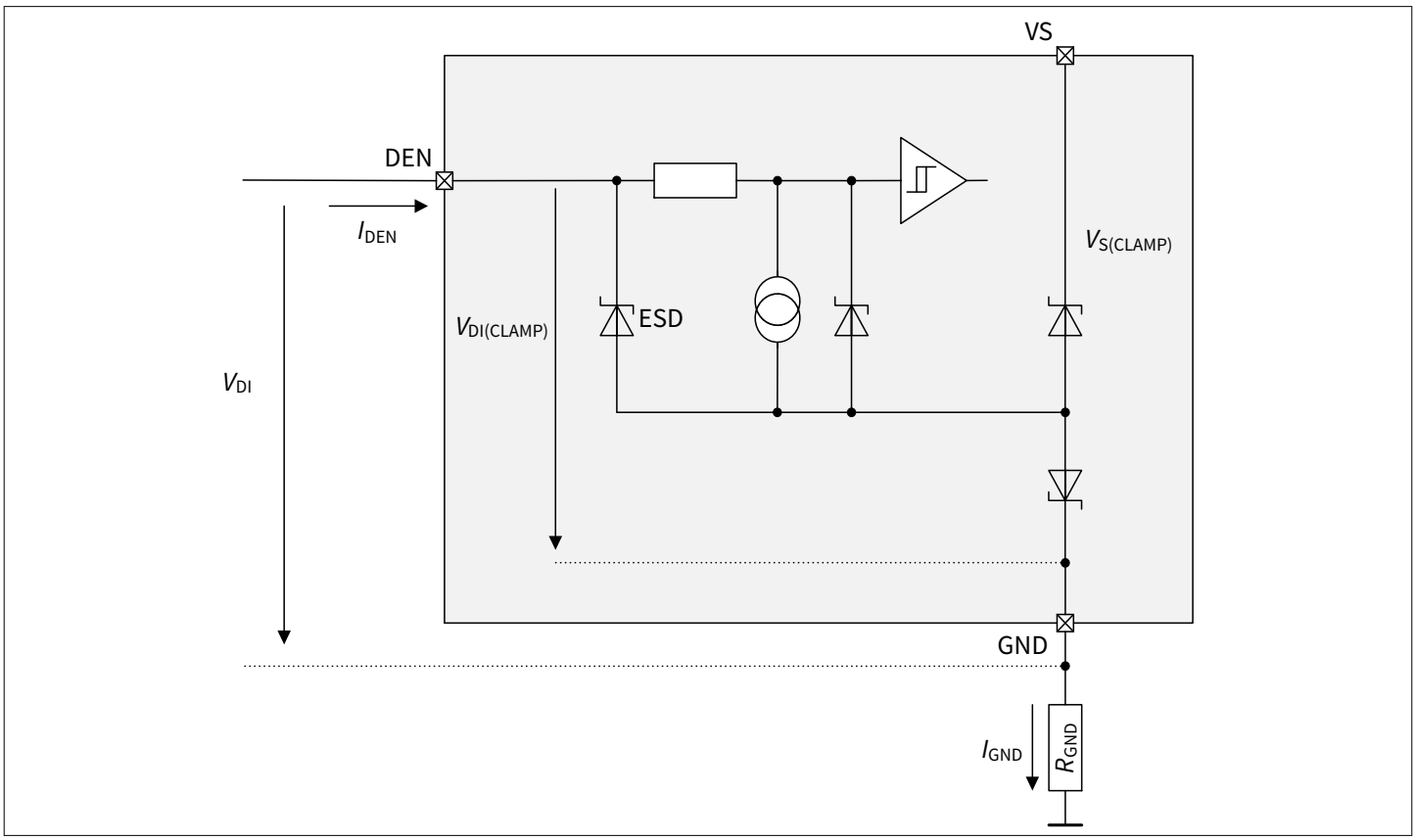



**Figure 12 DEN pin circuitry**

When the device is in idle mode and the DEN pin is set to "high", the diagnosis is enabled (change from idle mode either to I2t with diagnosis mode or active with diagnosis mode). When the DEN pin is set to "low" and all idle mode conditions are fulfilled, the device changes to idle mode.

The protection latch is reset by applying a pulse (rising edge followed by a falling edge) at the DEN pin while the IN pin is "low" (see Chapter 8.3 and Figure 32 for more details).

## 5.3 I2t selection pin (I2t)

The I2t selection pin (I2t) is used to select one of the six available I2t protection curves. The selection is made by the value of the resistor connected between I2t pin and GND pin.

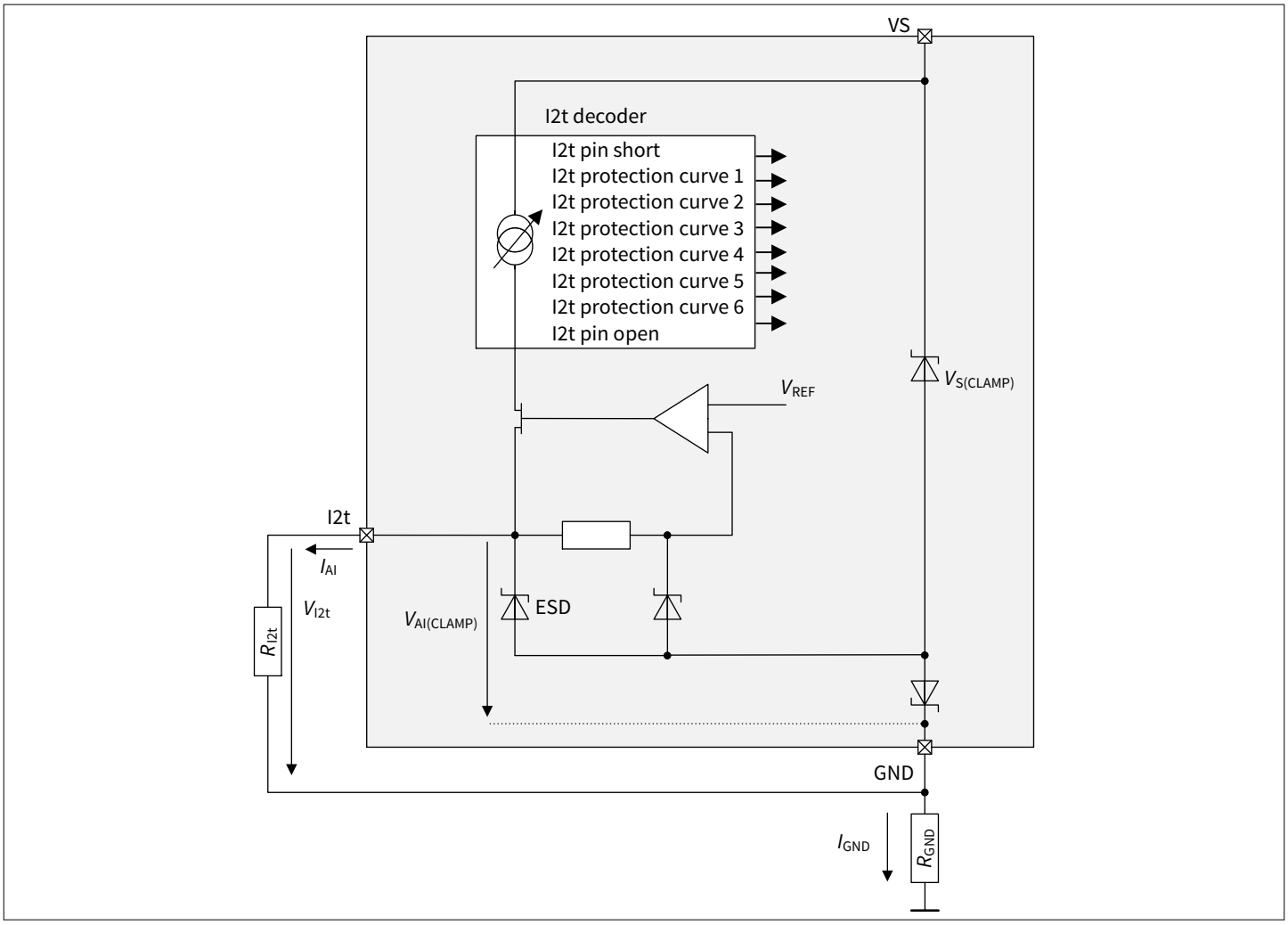



**Figure 13 I2t selection circuitry**

The device recognizes an I2t pin short if the resistance between I2t pin and GND is lower than $R_{I2t\_SHORT}$. In this case the I2t protection changes to I2t protection curve 1 and additionally a sense current of $I_{IS(I2t\_SHORT)}$ is sent out at the IS pin when the sequential diagnosis address #2 is selected.

If the resistance between I2t pin and GND is higher than $R_{I2t\_OPEN}$ an I2t pin open is detected by the device. In this case the I2t protection curve 1 is internally selected and additionally a sense current of $I_{IS(I2t\_OPEN)}$ is sent out at the IS pin when the sequential diagnosis address #2 is selected.

## 5.4 Overcurrent threshold pin (OCT)

The overcurrent threshold (OCT) pin is used for an analog adjustment of the overcurrent threshold by connecting a resistor between the OCT pin and GND pin.

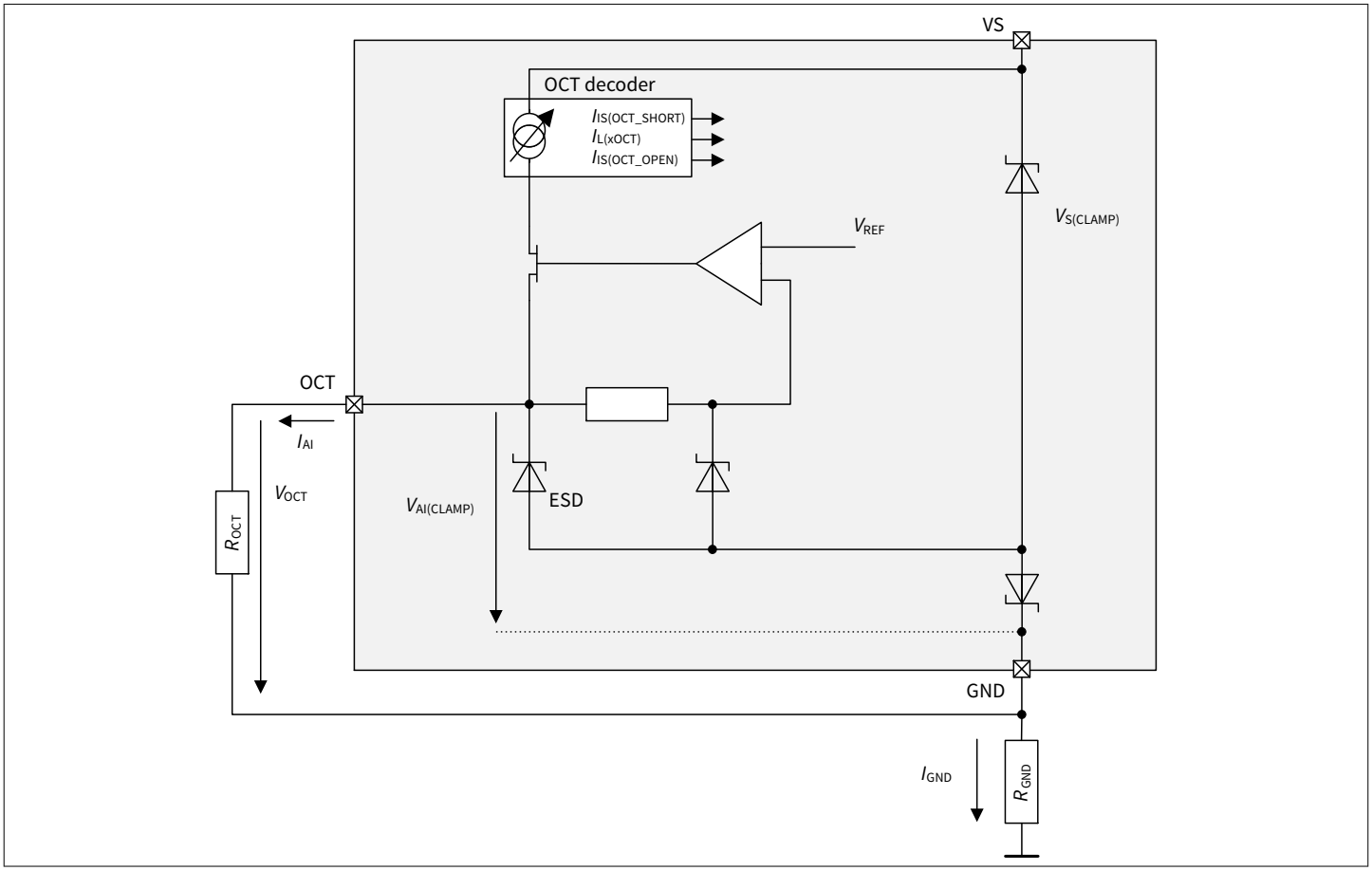



**Figure 14 OCT adjustment circuitry**

The device recognizes an OCT pin short if the current between the OCT pin and GND is higher than $I_{OCT\_SHORT}$. In this case the overcurrent threshold is internally set to the highest configurable overcurrent threshold $I_{L(HOCT)}$. Additionally, a sense current of $I_{IS(OCT\_SHORT)}$ is sent out at the IS pin when the sequential diagnosis address #4 is selected.

If the current between the OCT pin and GND is lower than $I_{OCT\_OPEN}$ an OCT pin open is detected by the device. In this case the overcurrent threshold is internally set to the highest configurable overcurrent threshold $I_{L(HOCT)}$. Additionally, a sense current of $I_{IS(OCT\_OPEN)}$ is sent out at the IS pin when the sequential diagnosis address #4 is selected.

## 5.5 Idle mode pin (IDL)

The idle mode output pin (IDL) is an open drain output. It is set to high impedance in case of idle mode and sleep mode, and it is pulled down in all other modes.

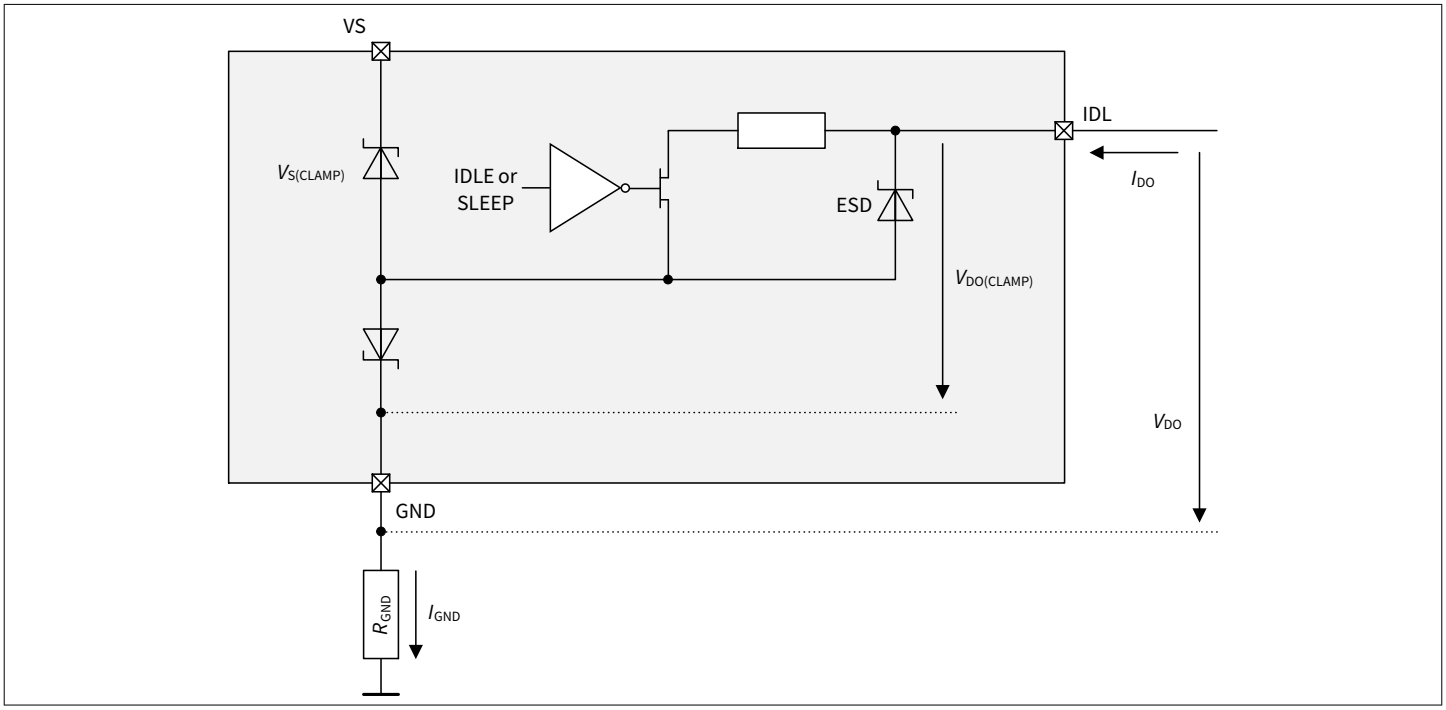



**Figure 15 Idle mode pin circuitry**

## 5.6 Electrical characteristics logic pins

**Table 6 Electrical characteristics - logic pins**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Digital input (DI) pins: IN, DEN** | | | | | | | |
| Digital input voltage threshold | $V_{DI(TH)}$ | 0.8 | 1.3 | 2 | V | See Figure 10, Figure 11 and Figure 12 | PRQ-168 |
| Digital input clamping voltage | $V_{DI(CLAMP1)}$ | – | 7 | – | V | 1) $I_{DI}$ = 1 mA See Figure 10 and Figure 12 | PRQ-169 |
| Digital input clamping voltage | $V_{DI(CLAMP2)}$ | 6.5 | 7.5 | 8.5 | V | $I_{DI}$ = 2 mA See Figure 10 and Figure 12 | PRQ-170 |
| Digital input hysteresis at IN pin | $V_{IN(HYS)}$ | 0.30 | 0.45 | – | V | 1) See Figure 10, Figure 11 | PRQ-172 |

**(table continues...)**

**Table 6 (continued) Electrical characteristics - logic pins**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Digital input hysteresis at DEN pin | $V_{DEN(HYS)}$ | 0.20 | 0.35 | – | V | 1) See Figure 10, Figure 11 and Figure 12 | PRQ-1244 |
| Digital input current at IN pin ("high") | $I_{IN(H)}$ | 1 | 10 | 25 | µA | $V_{DI}$ = 2 V<br>DEN = "high"<br>See Figure 10 | PRQ-173 |
| Digital input current at IN pin ("high") | $I_{IN(H)}$ | -25 | -8 | -1 | µA | $V_{DI}$ = 1.4 V<br>DEN = "low"<br>See Figure 10 | PRQ-930 |
| Digital input current at IN pin ("low") | $I_{IN(L)}$ | 1 | 10 | 25 | µA | $V_{DI}$ = 0.8 V<br>DEN = "high"<br>See Figure 10 | PRQ-174 |
| Digital input current at DEN pin ("high") | $I_{DEN(H)}$ | 1 | 10 | 25 | µA | $V_{DI}$ = 2 V<br>See Figure 12 | PRQ-931 |
| Digital input current at DEN pin ("low") | $I_{DEN(L)}$ | 1 | 10 | 25 | µA | $V_{DI}$ = 0.8 V<br>See Figure 12 | PRQ-932 |
| **Digital output (DO) pin: IDL** | | | | | | | |
| Digital output clamping voltage | $V_{DO(CLAMP1)}$ | – | 7 | – | V | 1) $I_{DO}$ = 1 mA<br>Sleep or idle mode (where IDL is highohmic)<br>See Figure 15 | PRQ-880 |
| Digital output voltage ("low") | $V_{DO(L)}$ | 0 | – | 0.4 | V | $I_{DO}$ = 0.2 mA<br>Not in sleep or idle mode (then IDL is low ohmic) | PRQ-367 |
| **Analog input (AI) pin: I2t, OCT** | | | | | | | |
| Analog input clamping voltage | $V_{AI(CLAMP1)}$ | – | 6.5 | – | V | 1) $I_{AI}$ = -1 mA<br>See Figure 13 and Figure 14 | PRQ-881 |
| Maximum analog input current | $I_{AI\_MAX}$ | 100 | 300 | 500 | µA | – | PRQ-371 |
| OCT pin reference voltage | $V_{OCT}$ | 0.44 | 0.50 | 0.55 | V | $I_{OCT\_MIN} \le I_{OCT} \le I_{OCT\_MAX}$ | PRQ-891 |

**(table continues...)**

**Table 6 (continued) Electrical characteristics - logic pins**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| I2t pin reference voltage | $V_{I2t}$ | 0.48 | 0.59 | 0.69 | V | $R_{I2t\_MIN} \le R_{I2t} \le R_{I2t\_MAX}$ | PRQ-892 |

*1)* Not subject to production test - specified by design.

# 6 Power supply

The device is supplied by $V_S$, which is used for the internal logic as well as supply for the power output stage. $V_S$ has an undervoltage detection circuit, which prevents the activation of the power output stage and diagnosis in case the applied voltage is below the undervoltage threshold ($V_S < V_{S(UV)}$). During power up, the internal power-on signal is set when supply voltage ($V_S$) exceeds the minimum operating voltage ($V_S > V_{S(OP)}$).

## 6.1 Operation modes

The device has the following operation modes in case of $V_S > V_{S(OP)}$:

- Sleep mode
- I2t mode
- I2t with diagnosis mode
- Inactive with diagnosis mode
- Idle mode
- Active with diagnosis
- Capacitive load switching (CLS) mode
- Capacitive load switching (CLS) with diagnosis mode
- Inactive mode

The transition between operation modes is determined according to these variables:

- Logic level at IN pin
- PWM signal at IN pin
- Logic level at DEN pin
- Internal protection latch
- Load current $I_L$ level
- $V_{DS}$ voltage level
- Junction temperature
- Status of the selected I2t protection curve

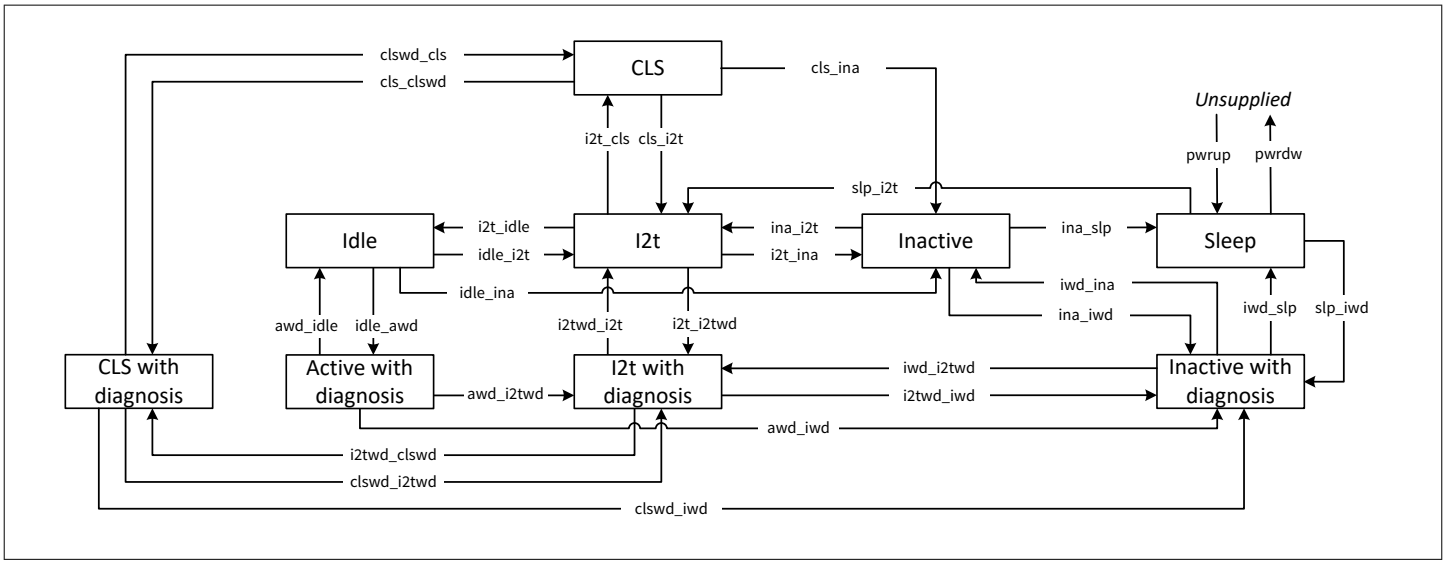



**Figure 16 Operation mode state diagram**

A more detailed description of the transitions, including the transition conditions and duration times are provided in the following table.

**Table 7 Transition descriptions**

| Name | Start state | End state | Transition condition | Duration time |
|---|---|---|---|---|
| pwrdw | Sleep | Unsupplied | $V_{VS} < V_{VS(UV)}$ | n.a. |
| pwrup | Unsupplied | Sleep | $V_{VS} > V_{VS(UV)}$ | n.a. |
| iwd_slp | Inactive with diagnosis | Sleep | DEN = "low" AND $S_{I2t\_A} < (S_{I2t\_I} - S_{I2t\_HYST})$ | $t_{T(iwd\_slp)}$ |
| ina_slp | Inactive | Sleep | $S_{I2t\_A} < (S_{I2t\_I} - S_{I2t\_HYST})$ | $t_{T(F10u)}$ |
| slp_i2t | Sleep | I2t | IN = "high" | $t_{ON}$ |
| cls_i2t | CLS | I2t | (IN = "high" OR $V_{DS} < V_{DS(OLOFF)}$) AND DEN = "low" | $t_{T(CLS\_I2t)}$ |
| idle_I2t | Idle | I2t | $I_L > I_{L(IDLE)}$ | $t_{T(IDLE\_I2t)}$ |
| i2twd_i2t | I2t with diagnosis | I2t | DEN = "low" | $t_{T(F10u)}$ |
| ina_i2t | Inactive | I2t | IN = "high" | $t_{ON}$ |
| i2t_cls | I2t | CLS | IN = "pwm" AND $V_{DS} > V_{DS(OLOFF)}$ | $t_{T(I2t\_CLS)}$ |
| clswd_cls | CLS with diagnosis | CLS | DEN = "low" | $t_{T(F10u)}$ |
| i2t_idle | I2t | Idle | $I_L < (I_{L(IDLE)} - I_{L(IDLE\_HYST)})$ AND $S_{I2t\_A} < (S_{I2t\_I} - S_{I2t\_HYST})$ | $t_{T(I2t\_IDLE)}$ |
| awd_idle | Active with diagnosis | Idle | DEN = "low" | $t_{T(AWD\_IDLE)}$ |
| idle_awd | Idle | Active with diagnosis | DEN = "high" | $t_{T(F10u)}$ |
| i2t_i2twd | I2t | I2t with diagnosis | DEN = "high" | $t_{sIS(ON15)}$ |
| awd_i2twd | Active with diagnosis | I2t with diagnosis | $I_L > I_{L(IDLE)}$ | $t_{sIS(ON15)}$ |
| clswd_i2twd | CLS with diagnosis | I2t with diagnosis | IN = "high" OR $V_{DS} < V_{DS(OLOFF)}$ | $t_{T(CLS\_I2t)}$ |
| iwd_i2twd | Inactive with diagnosis | I2t with diagnosis | IN = "high" | $t_{ON}$ |
| cls_clswd | CLS | CLS with diagnosis | DEN = "high" | $t_{sIS(ON234)}$ |
| i2twd_clswd | I2t with diagnosis | CLS with diagnosis | IN = "pwm" AND $V_{DS} > V_{DS(OLOFF)}$ | $t_{T(I2t\_CLS)}$ |
| slp_iwd | Sleep | Inactive with diagnosis | DEN = "high" | $t_{sIS(ON234)}$ |
| awd_iwd | Active with diagnosis | Inactive with diagnosis | IN = "low" | $t_{OFF}$ |
| i2twd_iwd | I2t with diagnosis | Inactive with diagnosis | IN = "low" | $t_{OFF}$ |

**(table continues...)**

**Table 7 (continued) Transition descriptions**

| Name | Start state | End state | Transition condition | Duration time |
|---|---|---|---|---|
| clswd_iwd | CLS with diagnosis | Inactive with diagnosis | IN = "low" | $t_{OFF}$ |
| ina_iwd | Inactive | Inactive with diagnosis | DEN = "high" | $t_{sIS(ON234)}$ |
| i2t_ina | I2t | Inactive | IN = "low" | $t_{OFF}$ |
| cls_ina | CLS | Inactive | IN = "low" | $t_{OFF}$ |
| idle_ina | Idle | Inactive | IN = "low" | $t_{OFF}$ |
| iwd_ina | Inactive with diagnosis | Inactive | DEN = "low" | $t_{T(F10u)}$ |

### 6.1.1 Unsupplied

In this state the device is either unsupplied (no voltage applied to VS pin) or the supply voltage is below the undervoltage threshold.

### 6.1.2 Power-up

The power-up condition is entered when the supply voltage ($V_S$) is applied to the device. The supply is rising until it is above the minimum operating output voltage $V_{S(OP),}$ therefore the internal power-on signals are set.

### 6.1.3 Sleep mode

The device is in sleep mode when all digital input pins (IN, DEN) are set to “low” and the I2t status calculation is below the initial status $S_{I2t\_I}$ minus the I2t status hysteresis $S_{I2t\_HYST}$. When the device is in sleep mode, the output is OFF. The current consumption is minimum (see parameter $I_{VS(SLEEP)}$). No overtemperature or overcurrent protection mechanism is active when the device is in sleep mode. If a protection was previously triggered and has not been reset, the device will not enter sleep mode (see Chapter 8.3.1 for further details).

### 6.1.4 I2t mode

The I2t mode is entered as soon as the IN pin is set to “high”. The device is calculating the I2t status $S_{I2t}$ and switches the channel OFF as soon as the I2t protection function (selected curve) is triggered. A detailed explanation of the I2t status calculation can be found in Chapter 9.1. The current consumption is specified with $I_{GND(I2t\_D)}$ (measured at GND pin because the current at VS pin includes the load current). Overcurrent, overtemperature and overvoltage protections are active. Since the DEN pin is set to "low" the diagnosis is not available.

### 6.1.5 Inactive with diagnosis mode

The device is in inactive with diagnosis mode as long as DEN pin is set to “high” while input pin is set to “low”. The channel is OFF. The initial I2t status value for the I2t status calculation depends on the actual I2t status. A detailed explanation of the I2t status calculation can be found in Chapter 9.1. The current consumption is specified by the parameter operating current in inactive with diagnosis mode $I_{GND(INACT\_D)}$. Additionally, the sequential diagnosis is enabled and depending on the address the selected setting is present at the IS pin (for further information see Figure 42).

### 6.1.6 I2t with diagnosis mode

The device enters I2t with diagnosis mode as soon as the IN and DEN pin are set to “high”. Similar to I2t mode the device is calculating the I2t status $S_{I2t}$ and switches the channel OFF as soon as the I2t protection function (selected curve) is triggered. A detailed explanation of the I2t status calculation can be found in Chapter 9.1. The current

consumption is specified with $I_{GND(I2t\_D)}$ (measured at GND pin because the current at VS pin includes the load current). Overcurrent, overtemperature and overvoltage protections are active. Additionally, the sequential diagnosis is enabled and depending on the address the selected setting is present at the IS pin (for further information see Figure 42).

### 6.1.7 Idle mode

Idle mode is the low power mode of the device where the current consumption is reduced to $I_{GND(IDLE)}$ while the output channel stays ON. Idle mode is entered automatically when the device fulfills the following idle mode entry conditions:

- IN pin is set to "high"
- Load current level is below $I_{L(IDLE)}$ - $I_{L(IDLE\_HYST)}$
- DEN pin is set to "low"
- I2t protection status calculation $S_{I2t\_A} < (S_{I2t\_I} - S_{I2t\_HYST})$

The idle mode is left when the device fulfills one of the following idle mode exit conditions:

- IN pin is set to "low"
- Load current level is above $I_{L(IDLE)}$
- DEN pin is set to "high"

During idle mode the I2t protection as well as the temperature protection and sequential diagnosis function is not active.

### 6.1.8 Active with diagnosis

The active with diagnosis state is entered out of idle mode when the DEN pin is set to “high” and $I_L < I_{L(IDLE)}$. The transition time from active with diagnosis to idle is defined by $t_{T(awd\_idle)}$. During this state the I2t calculation is not active since $I_L < I_{L(IDLE)}$ and no $I_{L(I2t\_I)}$ is applied. The current consumption is specified with $I_{GND(I2t\_D)}$ (measured at GND pin because the current at VS pin includes the load current). Overcurrent, overtemperature and overvoltage protections are active. Additionally, the sequential diagnosis is enabled and depending on the address the selected setting is present at the IS pin (for further information see Figure 42).

### 6.1.9 CLS mode

The device has a capacitive load switching (CLS) mode implemented to charge capacitive loads. To enter the CLS mode an input frequency of $f_{VIN(CLS)}$ with the duty cycle of $DC_{VIN(CLS)}$ has to be applied at the input pin (for more details see Chapter 7.2.3). The device current consumption in CLS mode is specified by the parameter $I_{GND(I2t\_D)}$.

### 6.1.10 CLS with diagnosis mode

The CLS with diagnosis mode is entered as soon as the pwm signal for CLS mode ($f_{VIN(CLS)}$ and $DC_{VIN(CLS)}$) is applied at the IN pin and the DEN pin is set to "high". The device calculates the I2t status $S_{I2t}$ (with $I_L$=0 A). Overcurrent, overtemperature and overvoltage protections are active. Additionally, the sequential diagnosis is enabled. Depending on the address several settings are present at the IS pin (for further information see Figure 42). The device current consumption is specified by the parameter $I_{GND(I2t\_D)}$.

### 6.1.11 Inactive mode

The inactive mode is a transition mode between I2t mode to sleep mode or idle mode to sleep mode. The device enters inactive mode as soon as the IN pin is set to “low” while the DEN pin is “low”. The device stays in this mode until the I2t status calculation has reached a value below the I2t hysteresis curve. The channel is OFF and the current consumption is specified by the parameter $I_{GND(I2t\_D)}$.

### 6.1.12 Fault mode

The device is in fault mode as soon as a device protection or I2t protection event happen. The output then switches off. In fault mode, with IN="high" and DEN="high", $I_{IS(FAULT)}$ is present and no sequential diagnosis is available at the IS pin. With IN = "low" and DEN = "high" sequential diagnosis is available (for details see Chapter 10) at the IS pin.

## 6.2 Undervoltage on VS

The undervoltage mechanism is triggered below $V_{S(UV)}$ or $V_{S(UV\_IDLE)}$.

If the device is operative (in I2t mode, I2t with diagnosis mode, CLS mode, CLS with diagnosis mode, inactive mode or inactive with diagnosis mode, active with diagnosis mode) and the supply voltage drops below the undervoltage threshold $V_{S(UV)}$, the internal logic switches OFF the output channel and the I2t calculation is reset.

The power supply undervoltage shutdown in idle mode is triggered when the supply voltage drops below $V_{S(UV\_IDLE)}$ during idle mode, resulting in the switch OFF of the output channel.

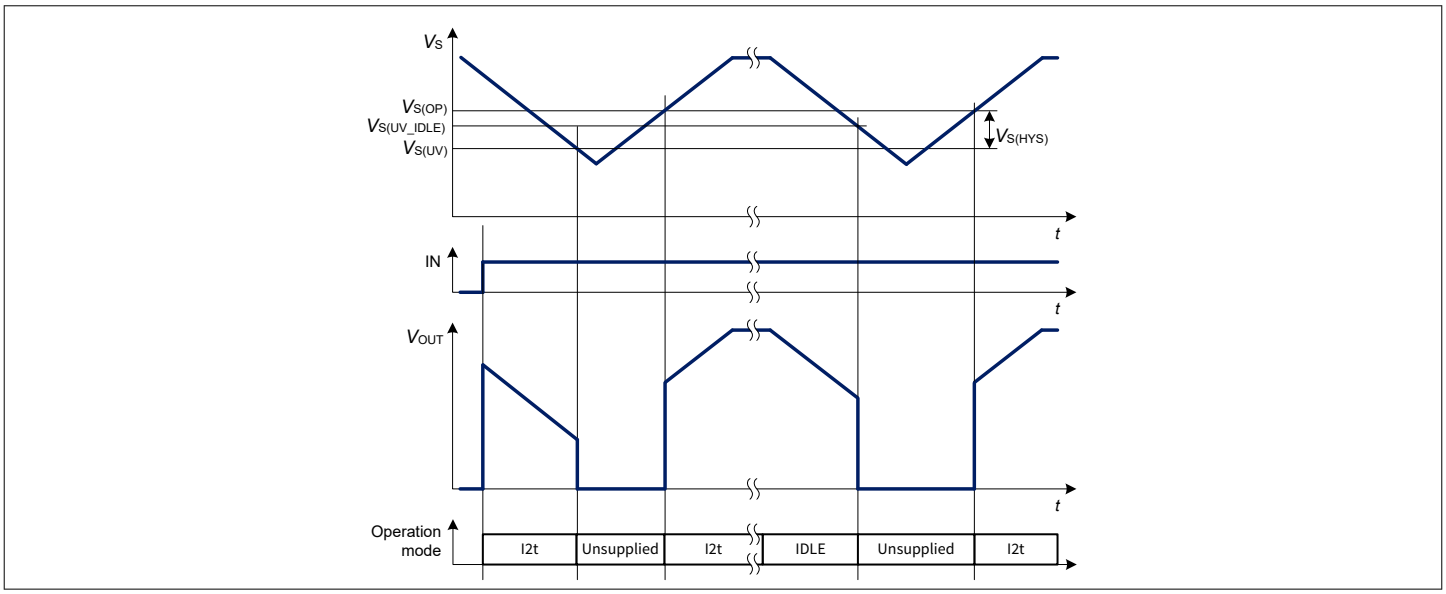



**Figure 17 $V_S$ undervoltage behavior**

## 6.3 Electrical characteristics power supply

**Table 8 Electrical characteristics - power supply**

$T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **VS pin** | | | | | | | |
| Power supply undervoltage shutdown (normal) | $V_{S(UV)}$ | 2.0 | 2.4 | 2.75 | V | $V_S$ decreasing<br>IN = "high"<br>From $V_{DS} \leq 0.5$ V to $V_{DS} = V_S$ | PRQ-186 |
| Power supply undervoltage shutdown in idle | $V_{S(UV\_IDLE)}$ | 2.3 | 2.6 | 2.9 | V | $V_S$ decreasing<br>Idle mode<br>IN = "high"<br>From $V_{DS} \leq 0.5$ V to $V_{DS} = V_S$ | PRQ-1434 |

**(table continues...)**

**Table 8 (continued) Electrical characteristics - power supply**

$T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Power supply minimum operating voltage | $V_{S(OP)}$ | 2.2 | 3.1 | 4.1 | V | $V_S$ increasing<br>IN = "high"<br>From $V_{DS}$ = $V_S$ to $V_{DS}$ ≤ 0.5 V | PRQ-188 |
| Power supply undervoltage shutdown hysteresis | $V_{S(HYS)}$ | – | 0.75 | – | V | 1)<br>$V_{S(OP)}$ - $V_{S(UV)}$ | PRQ-190 |

1) Not subject to production test - specified by design.

## 6.3.1 Electrical characteristics - power supply

**Table 9 Power supply**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Transition times** | | | | | | | |
| Transition time for fast transition | $t_{T(F10u)}$ | – | 15 | 25 | µs | 1) | PRQ-1377 |
| Transition time cls mode to I2t mode | $t_{T(CLS\_I2t)}$ | – | 40 | 80 | µs | 1) | PRQ-1376 |
| Transition time idle mode to I2t mode | $t_{T(IDLE\_I2t)}$ | 9 | 15.5 | 24 | µs | 1) | PRQ-1378 |
| Transition time active with diagnosis mode to idle mode | $t_{T(AWD\_IDLE)}$ | 210 | 280 | 350 | µs | 1) | PRQ-1379 |
| Transition time I2t mode to cls mode | $t_{T(I2t\_CLS)}$ | 30 | 70 | 140 | µs | 1) | PRQ-1380 |
| Transition time inactive with diagnosis mode to sleep mode | $t_{T(iwd\_slp)}$ | 150 | 210 | 300 | µs | 1) | PRQ-1410 |

**(table continues...)**

**Table 9 (continued) Power supply**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Current consumption** | | | | | | | |
| Supply current consumption in sleep mode with loads at TJ ≤ 85°C | $I_{VS(SLEEP)\_85}$ | – | 0.05 | 0.4 | µA | 1)<br>$V_S$ = 20 V<br>$V_{OUT}$ = $V_{I2t}$ = $V_{OCT}$ = 0 V<br>IN = DEN = “low”<br>$T_J$ ≤ 85°C | PRQ-963 |
| Supply current consumption in sleep mode with loads at TJ = 150°C | $I_{VS(SLEEP)\_150}$ | – | 0.5 | 10 | µA | $V_S$ = 20 V<br>$V_{OUT}$ = $V_{I2t}$ = $V_{OCT}$ = 0 V<br>IN = DEN = “low”<br>$T_J$ = 150°C | PRQ-964 |
| Operating current in inactive with diagnosis mode | $I_{GND(INACT\_D)}$ | – | 1.5 | 2.3 | mA | $V_S$ = 20 V<br>IN = “low”<br>DEN = “high” | PRQ-197 |
| Operating current in I2t with diagnosis mode (channel ON) | $I_{GND(I2t\_D)}$ | – | 5 | 7.4 | mA | $V_S$ = 20 V<br>IN = DEN = “high” | PRQ-195 |
| Operating current in idle mode (channel ON) | $I_{GND(IDLE)}$ | – | 50 | 60 | µA | $V_S$ = 20 V<br>IN = "high"<br>DEN = "low"<br>$I_L < I_{L(IDLE)}$ | PRQ-355 |
| **Idle currents** | | | | | | | |
| Load current hysteresis for idle mode entry | $I_{L(IDLE\_HYST)}$ | – | 0.055 | – | A | 1)<br>See Chapter 6.1.7 | PRQ-1461 |
| Load current threshold for idle mode exit | $I_{L(IDLE)}$ | 0.8 | 2.0 | 3.2 | A | See Chapter 6.1.7 | PRQ-966 |

1) Not subject to production test - specified by design.

# 7 Power stages

The high-side power stage is built using an N-channel vertical power MOSFET with charge pump.

## 7.1 Output ON-state resistance

The ON-state resistance $R_{DS(ON)}$ depends mainly on junction temperature $T_J$. Figure 18 shows the variation of $R_{DS(ON)}$ across the whole $T_J$ range. The value “2” on the y-axis corresponds to the maximum $R_{DS(ON)}$ measured at $T_J$ = 150°C.

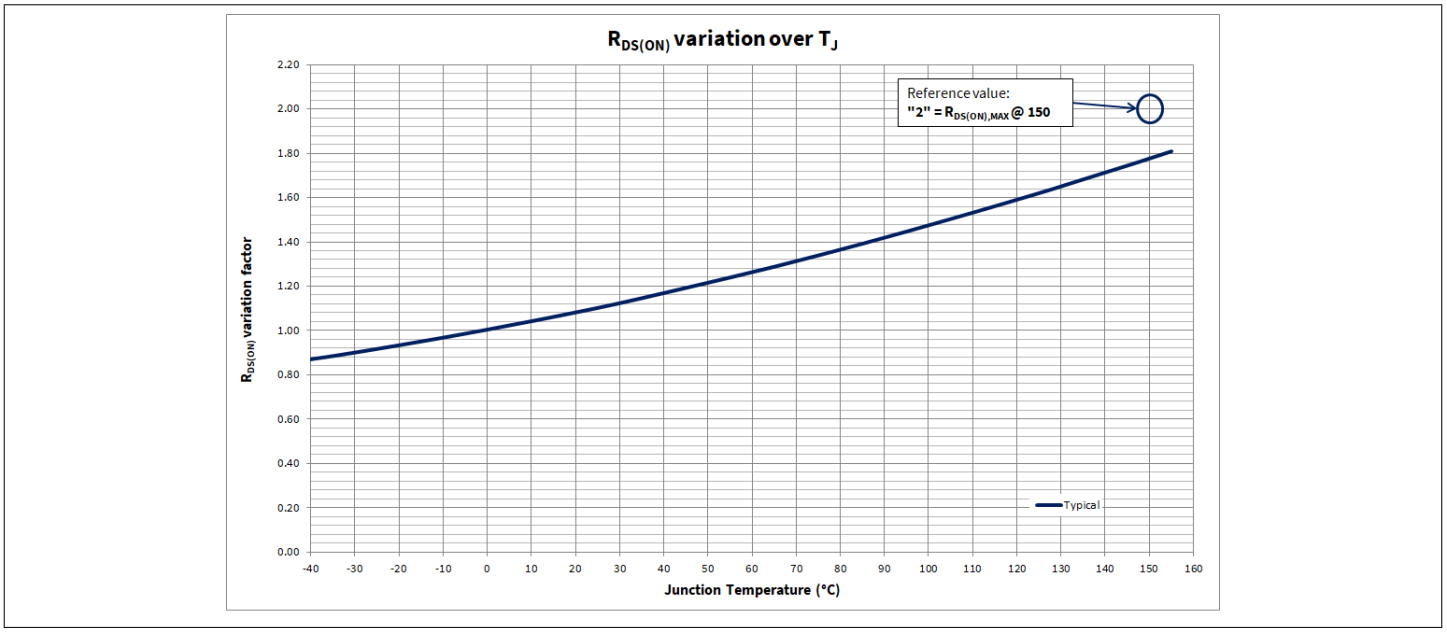



**Figure 18 $R_{DS(ON)}$ variation factor**

The behavior in reverse polarity is described in Chapter 8.4.1.

## 7.2 Switching loads

### 7.2.1 Switching resistive loads

When switching resistive loads, the switching times and slew rates shown in Figure 19 can be considered. The switch energy values $E_{ON}$ and $E_{OFF}$ are proportional to load resistance and times $t_{ON}$ and $t_{OFF}$.

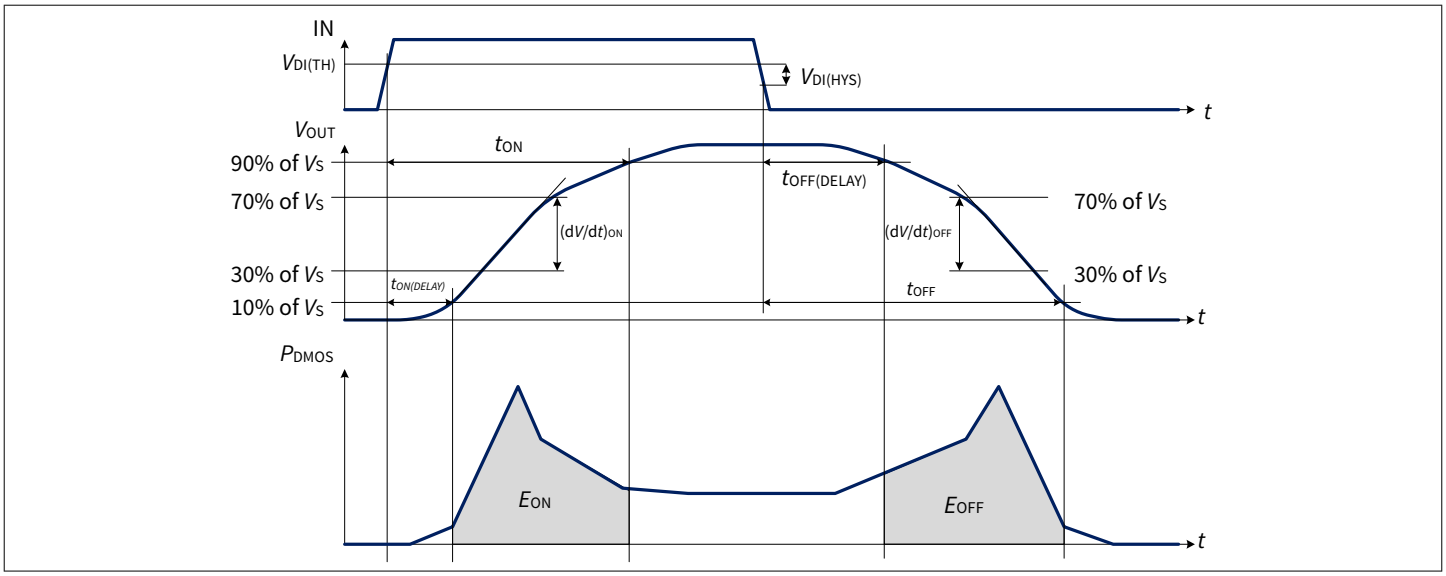



**Figure 19 Switching a resistive load**

## 7.2.2 Switching inductive loads

When switching OFF inductive loads with high-side switches, the voltage $V_{OUT}$ drops below ground potential because the inductance intends to continue driving the current. To prevent the destruction of the device due to overvoltage, a voltage clamp mechanism is implemented. The clamping structure limits the negative output voltage so that $V_{DS}$ = $V_{DS(CLAMP)}$. Figure 20 shows a concept drawing of the implementation.

The clamping structure is available in all operation modes listed in Chapter 6.1.

All clamping structures ($V_{IS(CLAMP)}$, $V_{S(CLAMP)}$, $V_{DS(CLAMP)}$) are implemented with respect to $V_S$ supply.

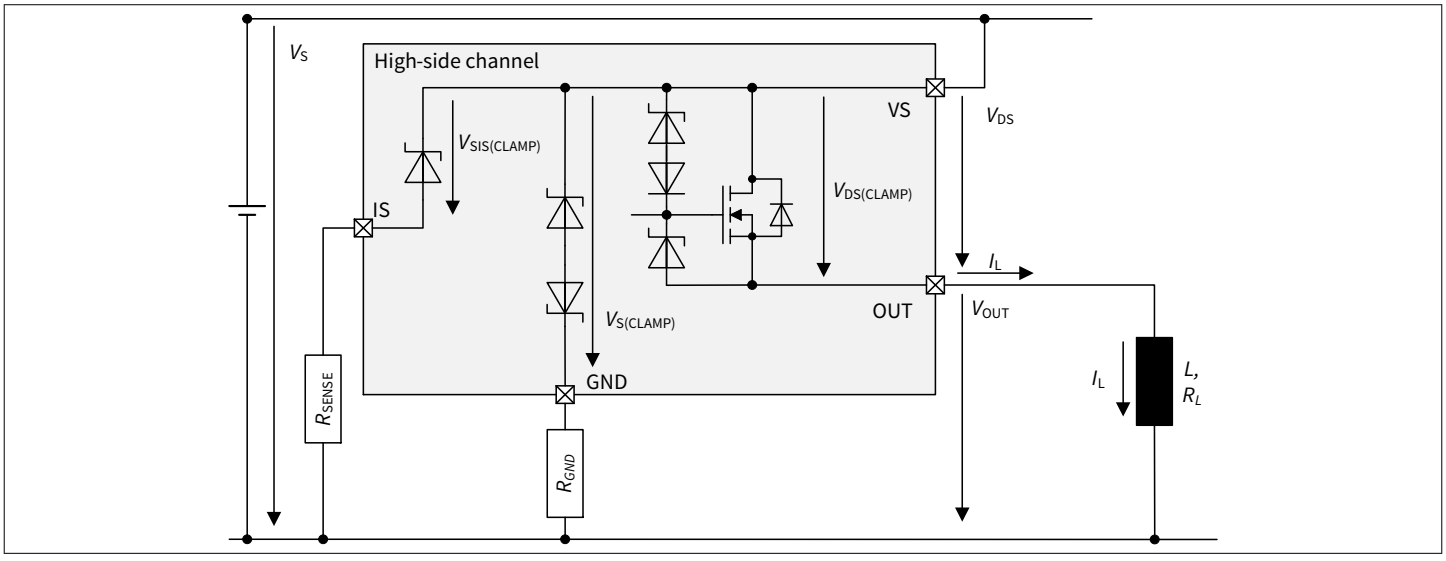



**Figure 20 Output clamp concept**

During demagnetization of inductive loads, energy has to be dissipated in the device. The energy can be calculated using:

$$E = V_{DS(CLAMP)} \cdot \left[ \frac{V_S - V_{DS(CLAMP)}}{R_L} \cdot \ln\left(1 - \frac{R_L \cdot I_L}{V_S - V_{DS(CLAMP)}}\right) + I_L \right] \cdot \frac{L}{R_L} \quad (1)$$

The maximum energy, therefore the maximum inductance for a given current, is limited by the thermal design of the component. Please refer to Table 3 for the maximum allowed values of $E_{AS}$ (single pulse energy) and $E_{AR}$ (repetitive energy).

### 7.2.3 Capacitive load switching

When switching a resistive load with the capacitive load switching (CLS) mode the switching times as well as the slew rate will change to $t_{ON\_CLS}$, $t_{ON\_CLS(DELAY)}$, $(dV/dt)_{ON\_CLS}$ as shown in Figure 21. The CLS mode is entered by applying a PWM signal at the IN pin with a frequency of $f_{VIN(CLS)}$ and a duty cycle of $DC_{VIN(CLS)}$.

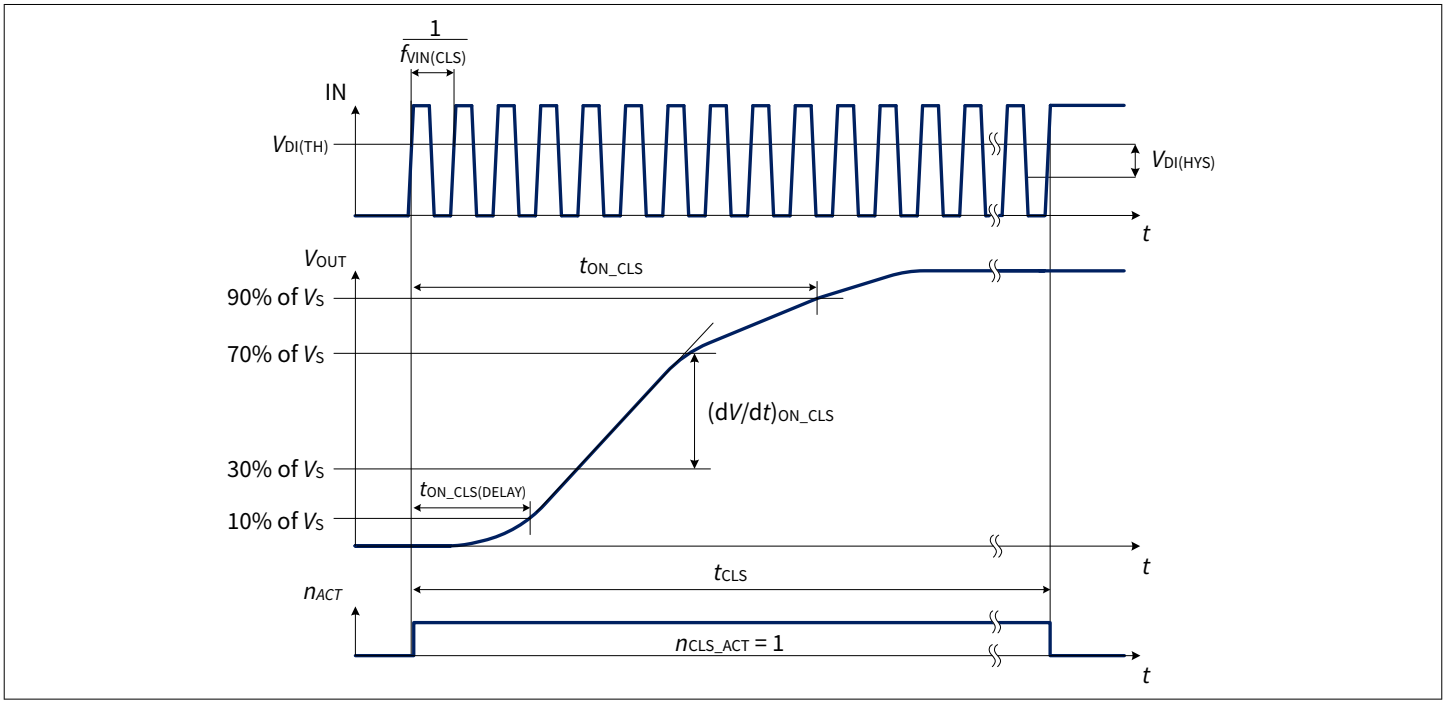



**Figure 21 Capacitive load switching timings**

During this mode the dynamic thermal shut down temperature is reduced to $T_{J\_CLS(DYN)}$ and the device is set to auto-restart.

The CLS mode and CLS with diagnosis mode has to be left after a maximum time of $t_{CLS}$ by setting the input to "high" or "low" state. The highest configurable overcurrent detection threshold $I_{L(HOCT)}$ (for $I_{OCT}$ = 50 µA) is enabled and the overtemperature protections are active (see Figure 29).

The device calculates the I2t status $S_{I2t}$ (with $I_L$ = 0 A).

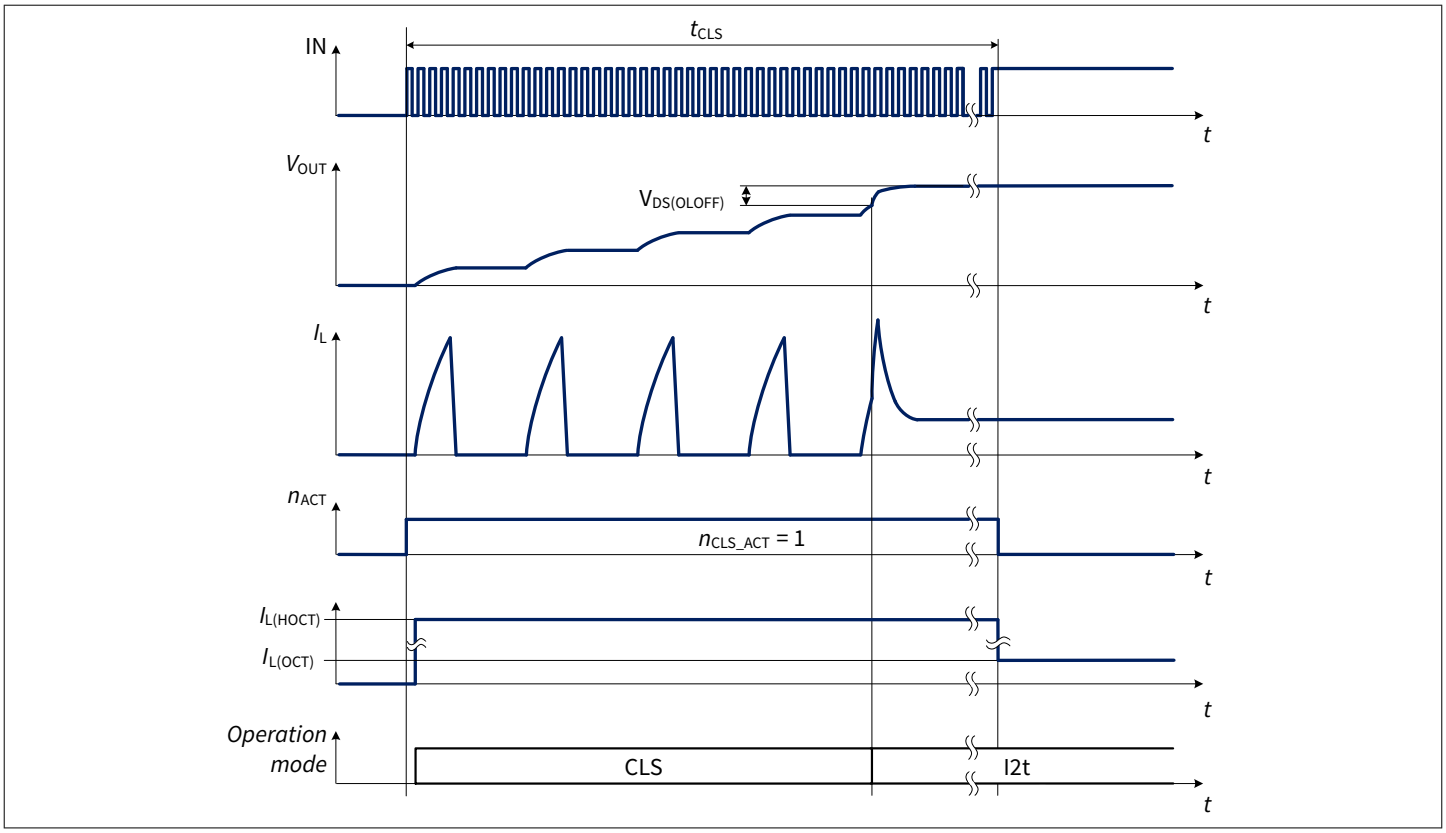



**Figure 22 Capacitive load switching activations**

A transition from the CLS mode to the ON mode is automatically done when $V_{DS} < V_{DS(OLOFF)}$. Before changing from CLS mode (IN = ”pwm”) to I2t mode (IN = ”high”), it must be ensured that there is no short circuit at the output. To distinguish between short circuit and normal load, a current sense measurement must be performed before leaving CLS mode. If the current measurement delivers an expected value, the transition from CLS mode to normal mode is possible. If the current measurement delivers an open load value (no output current), it has to be assumed that there is either an open load or a short circuit at the output. Additionally, a short circuit condition can be excluded by an external voltage measurement at the output.

## 7.3 Advanced switching characteristics

### 7.3.1 Inverse current behavior

If $V_{OUT} > V_S$, a current $I_{L(INV)}$ flows into the power output transistor (see Figure 23). This condition is known as “inverse current”.

If the channel is in OFF state, the current flows through the intrinsic body diode generating high power losses. Therefore, the overall device temperature increases. If the channel is in ON state, $R_{DS(INV)}$ can be expected and power dissipation in the output stage is comparable to normal operation in $R_{DS(ON)}$.

During Inverse ON condition, the channel remains in ON or OFF state as long as $|-I_L| < |-I_{L(INV)}|$. It is possible to switch ON the channel during inverse current condition as long as $|-I_L| < |-I_{L(INV)}|$ (see Figure 24).

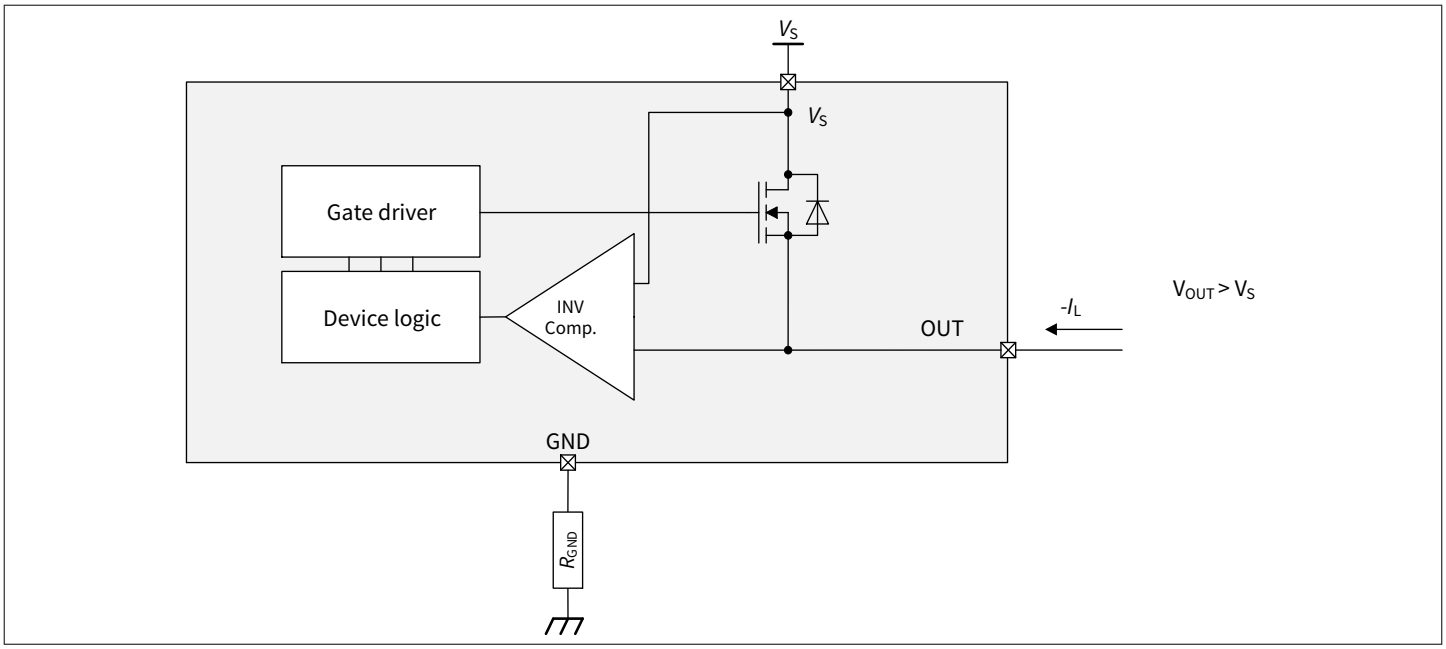



**Figure 23 Inverse current circuitry**

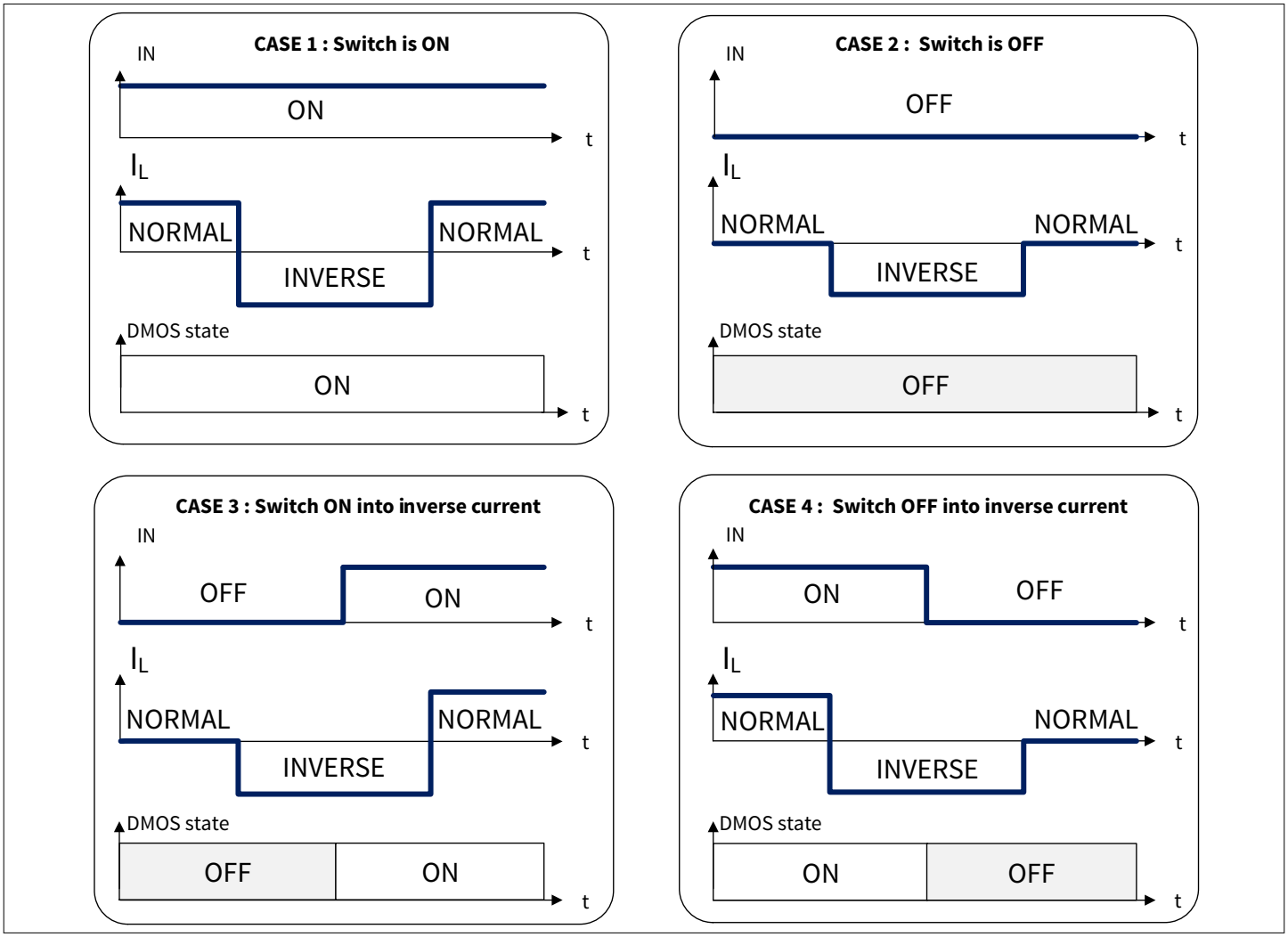



**Figure 24 Inverse ON - channel behavior in case of applied inverse current**

No protection mechanism like overtemperature or overcurrent protection is active during applied inverse currents.

## 7.4 Electrical characteristics power stages

**Table 10 Electrical characteristics power stages**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Voltages** | | | | | | | |
| Drain to source clamping voltage at TJ = -40°C | $V_{DS(CLAMP)\_-40}$ | 33 | 36.5 | 42 | V | $I_L$ = 5 mA<br>$T_J$ = -40°C<br>See Figure 20 | PRQ-203 |
| Drain to source clamping voltage at TJ ≥ 25°C | $V_{DS(CLAMP)\_25}$ | 35 | 38 | 44 | V | 1)<br>$I_L$ = 5 mA<br>$T_J$ ≥ 25°C<br>See Figure 20 | PRQ-204 |
| **Timings** | | | | | | | |
| Switch-ON delay | $t_{ON(DELAY)}$ | 10 | 50 | 90 | µs | $V_S$ = 13.5 V<br>$V_{OUT}$ = 10% $V_S$<br>See Figure 19 | PRQ-205 |
| Switch-ON delay in CLS | $t_{ON\_CLS(DELAY)}$ | 150 | 500 | 850 | µs | $V_S$ = 13.5 V<br>$V_{OUT}$ = 10% $V_S$<br>See Figure 21 | PRQ-591 |
| Switch-OFF delay | $t_{OFF(DELAY)}$ | 10 | 75 | 140 | µs | $V_S$ = 13.5 V<br>$V_{OUT}$ = 90% $V_S$<br>See Figure 19 | PRQ-206 |
| Switch-ON time | $t_{ON}$ | 40 | 100 | 160 | µs | $V_S$ = 13.5 V<br>$V_{OUT}$ = 90% $V_S$<br>See Figure 19 | PRQ-207 |
| Switch-ON time in CLS | $t_{ON\_CLS}$ | 350 | 1075 | 1800 | µs | $V_S$ = 13.5 V<br>$V_{OUT}$ = 90% $V_S$<br>See Figure 21 | PRQ-592 |
| Switch-OFF time | $t_{OFF}$ | 50 | 120 | 190 | µs | $V_S$ = 13.5 V<br>$V_{OUT}$ = 10% $V_S$<br>See Figure 19 | PRQ-208 |
| Switch-ON/OFF matching (tON - tOFF) | $\Delta t_{SW}$ | -90 | -20 | 50 | µs | $V_S$ = 13.5 V | PRQ-209 |

**(table continues...)**

**Table 10 (continued) Electrical characteristics power stages**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Input frequency for capacitive load switching mode | $f_{VIN(CLS)}$ | 22 | 30 | 38 | kHz | 2)<br>$DC_{VIN(CLS)}$ = 50% | PRQ-588 |
| Duty cycle for capacitive load switching | $DC_{VIN(CLS)}$ | 30% | 50% | 70% | – | 2)<br>$f_{VIN(CLS)}$ = 30 kHz | PRQ-589 |
| **Voltage slope** | | | | | | | |
| Switch-ON slew rate | $(dV/dt)_{ON}$ | 0.16 | 0.27 | 0.39 | V/µs | $V_S$ = 13.5 V<br>$V_{OUT}$ = 30% $V_S$ to 70% $V_S$<br>See Figure 19 | PRQ-210 |
| Switch-ON slew rate in CLS | $(dV/dt)_{ON\_CLS}$ | 0.012 | 0.023 | 0.037 | V/µs | $V_S$ = 13.5 V<br>$V_{OUT}$ = 30% $V_S$ to 70% $V_S$<br>See Figure 21 | PRQ-590 |
| Switch-OFF slew rate | $(dV/dt)_{OFF}$ | -0.39 | -0.27 | -0.16 | V/µs | $V_S$ = 13.5 V<br>$V_{OUT}$ = 70% $V_S$ to 30% $V_S$<br>See Figure 19 | PRQ-211 |
| Slew rate matching (dV/dt)ON - (dV/dt)OFF | $\Delta(dV/dt)_{SW}$ | -0.15 | 0 | 0.15 | V/µs | $V_S$ = 13.5 V | PRQ-212 |
| **CLS** | | | | | | | |
| Maximum time in CLS mode | $t_{CLS}$ | – | – | 100 | ms | 2)<br>See Figure 21 | PRQ-872 |
| Maximum number of CLS mode activations | $n_{CLS\_ACT}$ | – | – | 50 | kcycles | 2)<br>See Figure 21 | PRQ-873 |
| Thermal shut down temperature in CLS (dynamic) | $T_{J\_CLS(DYN)}$ | – | 20 | – | K | 2) | PRQ-874 |
| **Output characteristics** | | | | | | | |
| ON-state resistance at TJ = 25°C | $R_{DS(ON)\_25}$ | – | 8.0 | – | mΩ | 2)<br>$T_J$ = 25°C | PRQ-967 |
| ON-state resistance at TJ = 150°C | $R_{DS(ON)\_150}$ | – | – | 14.7 | mΩ | $T_J$ = 150°C | PRQ-968 |
| ON-state resistance in cranking | $R_{DS(ON)\_CRANK}$ | – | – | 16.7 | mΩ | $T_J$ = 150°C<br>$V_S$ = 3.1 V | PRQ-969 |

**(table continues...)**

**Table 10 (continued) Electrical characteristics power stages**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| ON-state resistance in idle mode at TJ = 150°C | $R_{DS(ON)\_IDLE}$ | – | 16.7 | – | mΩ | $T_J$ = 150°C | PRQ-970 |
| ON-state resistance in inverse current at TJ = 25°C | $R_{DS(INV)\_25}$ | – | 8.2 | – | mΩ | 2)<br>$T_J$ = 25°C<br>$V_S$ = 13.5 V<br>$I_L$ = -4 A<br>DEN = “low”<br>See Figure 24 | PRQ-971 |
| ON-state resistance in inverse current at TJ = 150°C | $R_{DS(INV)\_150}$ | – | – | 16.7 | mΩ | $T_J$ = 150°C<br>$V_S$ = 13.5 V<br>$I_L$ = -4 A<br>DEN = “low”<br>See Figure 24 | PRQ-972 |
| ON-state resistance in reverse polarity at TJ = 25°C | $R_{DS(REV)\_25}$ | – | 16.7 | – | mΩ | 2)<br>$T_J$ = 25°C<br>$V_S$ = -13.5 V<br>$I_L$ = -4 A<br>See Figure 34 | PRQ-973 |
| ON-state resistance in reverse polarity at TJ = 150°C | $R_{DS(REV)\_150}$ | – | – | 22.5 | mΩ | 2)<br>$T_J$ = 150°C<br>$V_S$ = -13.5 V<br>$I_L$ = -4 A | PRQ-974 |
| Nominal load current | $I_{L(NOM)\_85}$ | – | 10.3 | – | A | 2)<br>$T_A$ = 85°C<br>$T_J$ ≤ 150°C | PRQ-975 |
| Output leakage current at TJ ≤ 85°C | $I_{L(OFF)\_85}$ | – | 0.05 | 0.4 | µA | 2)<br>$V_{OUT}$ = 0 V<br>$V_{IN}$ = "low"<br>$T_J$ ≤ 85°C | PRQ-976 |
| Output leakage current at TJ = 150°C | $I_{L(OFF)\_150}$ | – | – | 10 | µA | $V_{OUT}$ = 0 V<br>$V_{IN}$ = "low"<br>$T_J$ = 150°C | PRQ-977 |

**(table continues...)**

**Table 10 (continued) Electrical characteristics power stages**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Inverse current capability | $I_{L(INV)}$ | – | -10.3 | – | A | 2)<br>$V_S < V_{OUT}$<br>IN = "high"<br>See Figure 24 | PRQ-978 |
| **Voltages** | | | | | | | |
| Drain source diode voltage | $\lvert V_{DS(DIODE)} \rvert$ | – | 550 | 700 | mV | $I_L$ = -190 mA<br>$T_J$ = 150°C | PRQ-224 |
| **Switching energy** | | | | | | | |
| Switch-ON energy | $E_{ON}$ | – | 1.5 | – | mJ | 2)<br>$V_S$ = 20 V<br>See Figure 19 | PRQ-225 |
| Switch-OFF energy | $E_{OFF}$ | – | 1.65 | – | mJ | 2)<br>$V_S$ = 20 V<br>See Figure 19 | PRQ-226 |

1) Tested at $T_J$ = 150°C.
2) Not subject to production test - specified by design.

# 8 Device protection

The device is protected against overtemperature, overcurrent, reverse battery (with Reverse ON) and overvoltage.

Overtemperature and overcurrent protections are disabled when the device is in sleep mode.

When the device is in idle mode the overtemperature protection is disabled and the overcurrent protection is enabled.

Overtemperature and overcurrent protections are not active during inverse current and in reverse battery condition.

Overvoltage protection works in all operation modes.

Reverse battery protection works when the GND and VS pins are reverse supplied.

## 8.1 Overtemperature protection

The device incorporates an absolute ($T_{J(ABS)}$) as well as a dynamic ($T_{J(DYN)}$) temperature protection circuitry for the channel.

An increase of junction temperature $T_J$ above either one of the two thresholds ($T_{J(ABS)}$ or $T_{J(DYN)}$) switches OFF the overheated channel to prevent destruction. The channel remains switched OFF until the junction temperature has reached the “reactivation” condition and a reset was applied as described in Table 11. The behavior is shown in Figure 25 and Figure 26. $T_{J(REF)}$ is the reference temperature used for dynamic temperature protection.

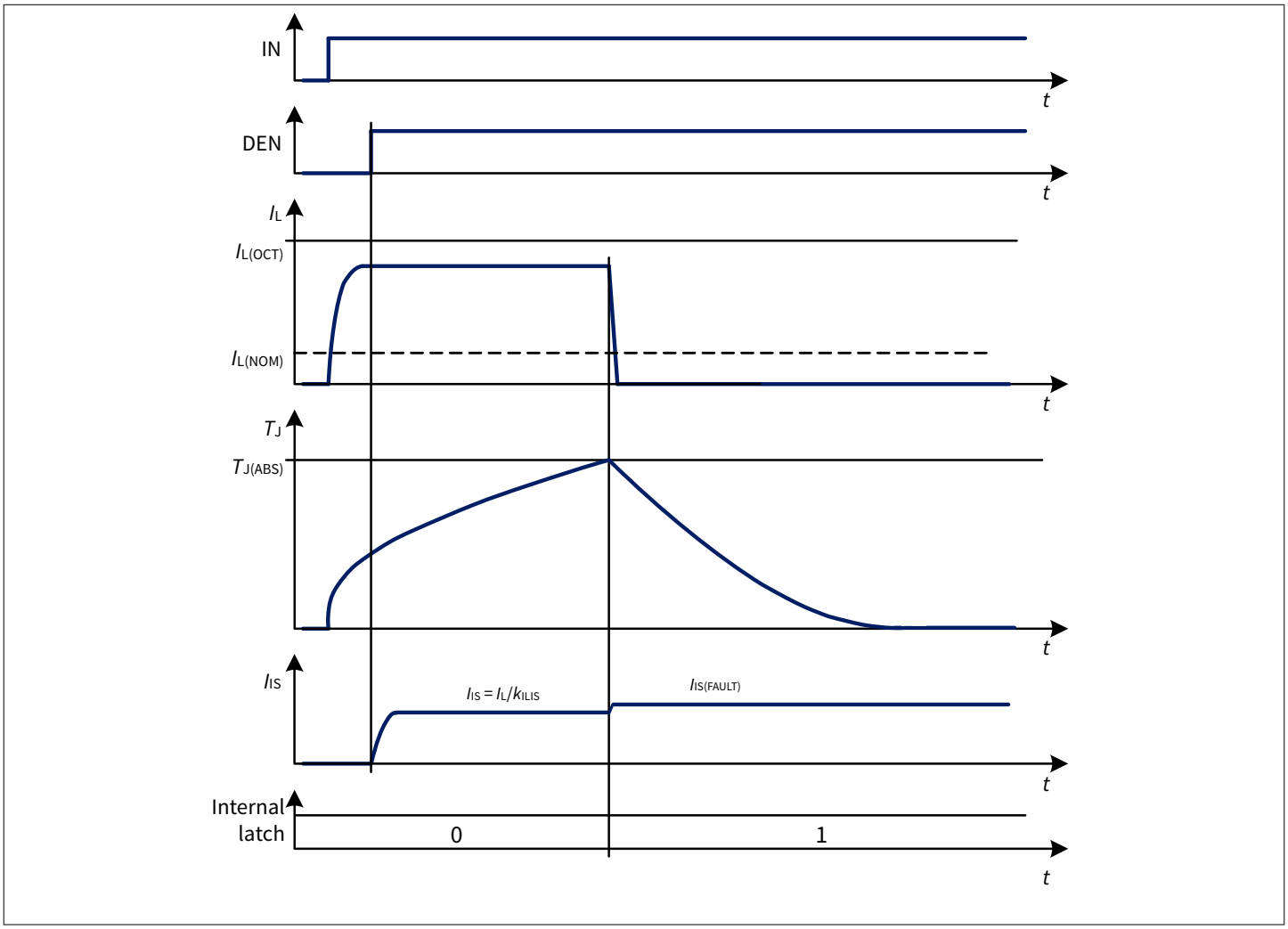



**Figure 25 Overtemperature protection (absolute)**

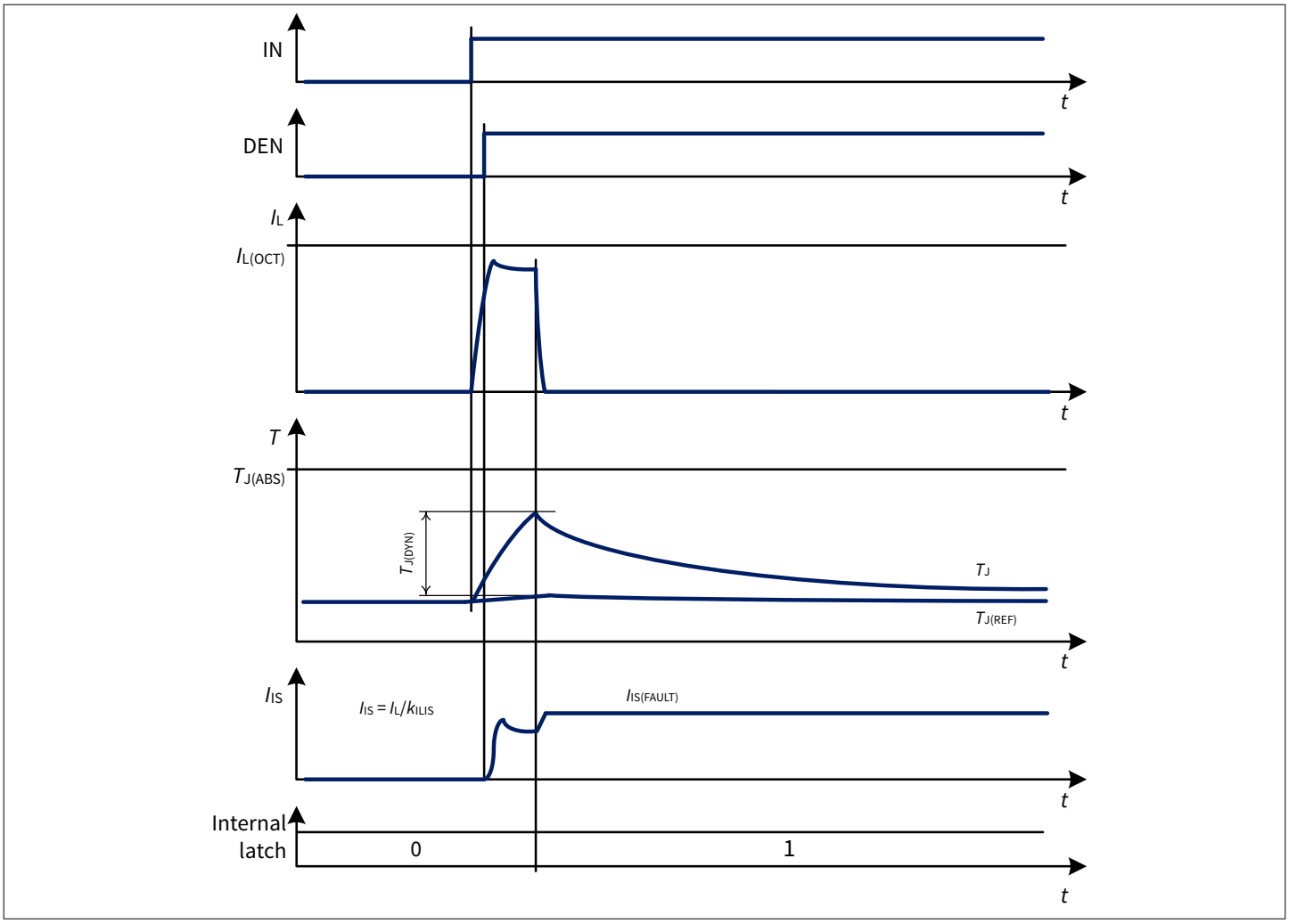



**Figure 26 Overtemperature protection (dynamic)**

When the overtemperature protection circuitry allows the channel to be switched ON again, the intelligent latch strategy described in Chapter 8.3 is followed.

## 8.2 Overcurrent threshold protection

The device is protected in case of overload or short circuit to ground by the overcurrent protection $I_{L(OCT)}$.

Furthermore, the overcurrent threshold $I_{L(OCT)}$ can be adjusted from the lowest configurable overcurrent detection threshold $I_{L(LOCT)}$ to the highest configurable overcurrent detection threshold $I_{L(HOCT)}$ by connecting a resistor between the OCT pin and the GND pin of the device. The adjustment of the overcurrent threshold (without considering the $V_{DS}$ reduction) could be done according to formula:

$$I_{L(OCT)\_TJ}[A] = \left[(I_{OCT}[\mu A] - 7.5[\mu A]) \cdot k_{OCT}[A/\mu A] + I_{L(LOCT)\_-40}[A]\right] \cdot \left[(T_J[°C] + 40[°C]) \cdot k_{TJ} \cdot 10^{-3} + 1\right] \quad (2)$$

To select the proper resistor value $R_{OCT}$ connected between the OCT pin and device ground, the following equation can be considered:

$$I_{OCT} = \frac{V_{OCT}}{R_{OCT}} \quad (3)$$

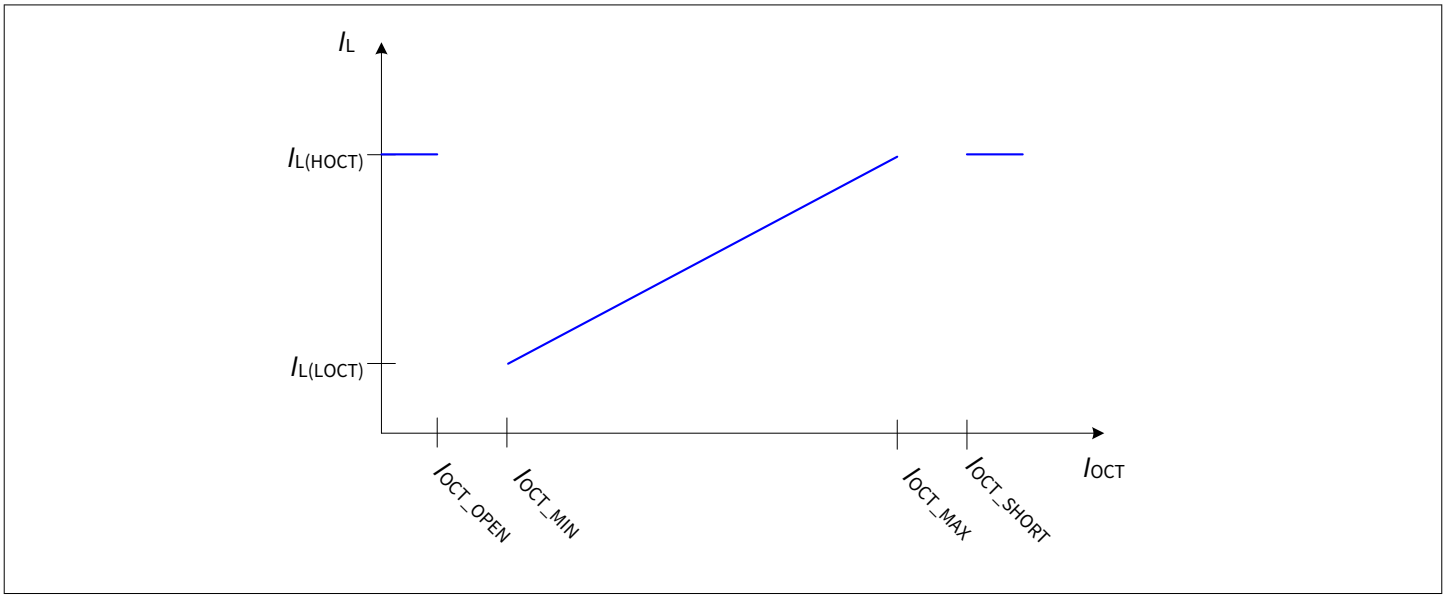



**Figure 27 Overcurrent threshold adjustment by $I_{OCT}$**

In case of an open or short detection of the OCT adjustment current $I_{OCT}$ at the pin the device changes to the highest configurable overcurrent detection threshold $I_{L(HOCT)}$.

The overcurrent thresholds are depending on the voltage $V_{DS}$ across the power DMOS.

If an overcurrent threshold adjustment current $I_{OCT}$ < 30 µA (Typical value) is selected no reduction of the $I_{L(OCT)}$ over $V_{DS}$ takes place (see Figure 28).

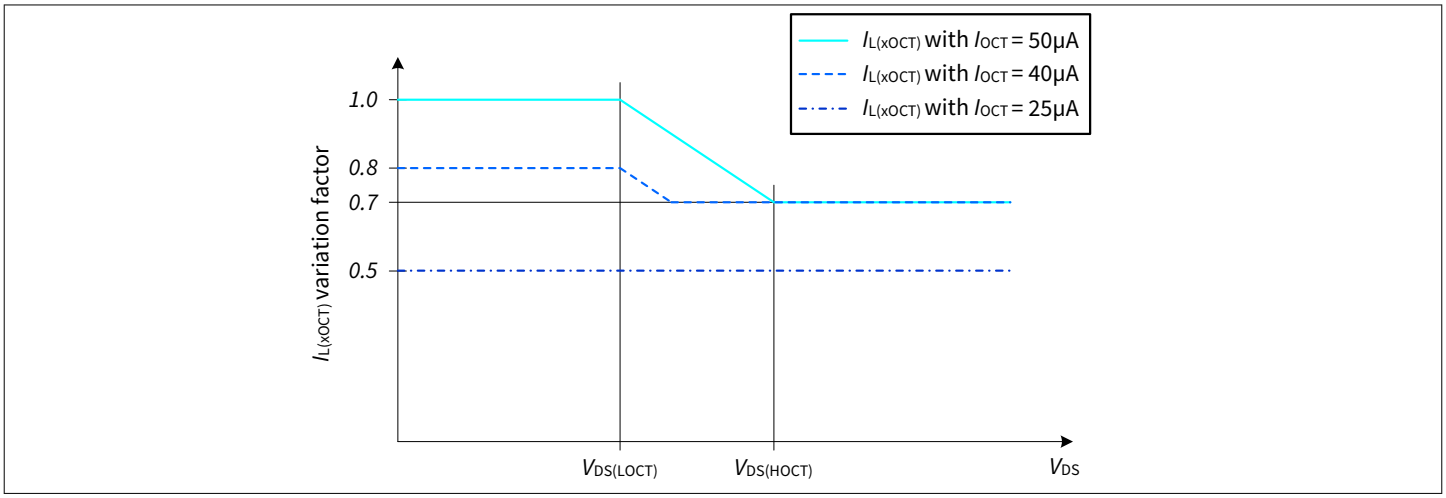



**Figure 28 Adjustable overcurrent threshold variation with $V_{DS}$**

In order to allow a higher load inrush current at low ambient temperature, the overcurrent threshold is maximum at low temperature and decreases when $T_J$ increases (see Figure 29).

Overcurrent detection threshold decreases linearly with increasing temperature.

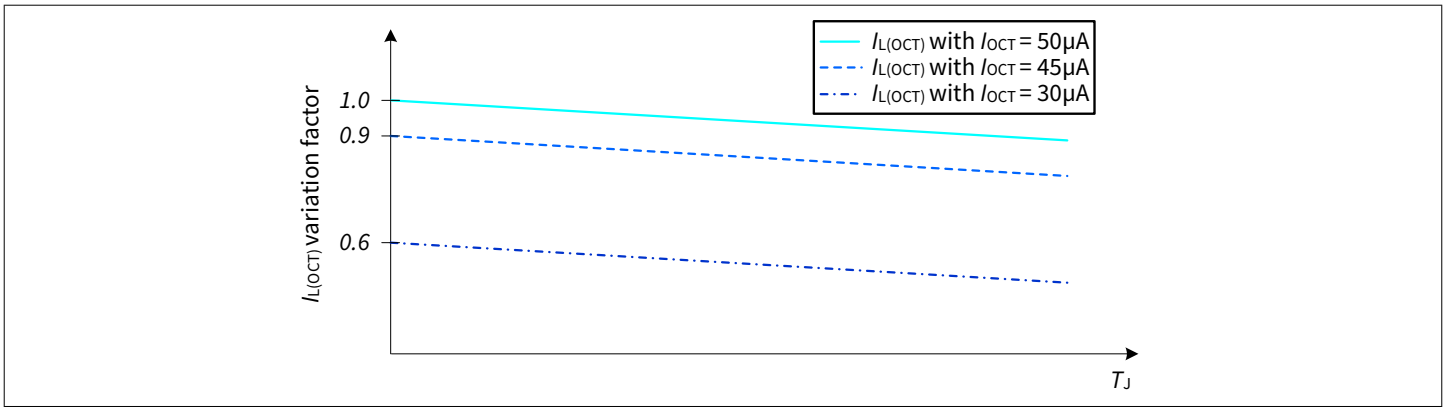



**Figure 29 Adjustable overcurrent threshold variation with $T_J$**

Power supply voltage $V_S$ can increase above 18 V for short time, for instance in load dump or in jump start condition. Whenever $V_S \geq V_{S(JS)}$ during switch ON, the overcurrent detection current is set to $I_{L(OCT\_JS)}$.

If an overcurrent threshold adjustment current $I_{OCT} < 30$ µA (Typical value) is selected no reduction of the $I_{L(OCT)}$ with $V_S$ takes place (see Figure 30).

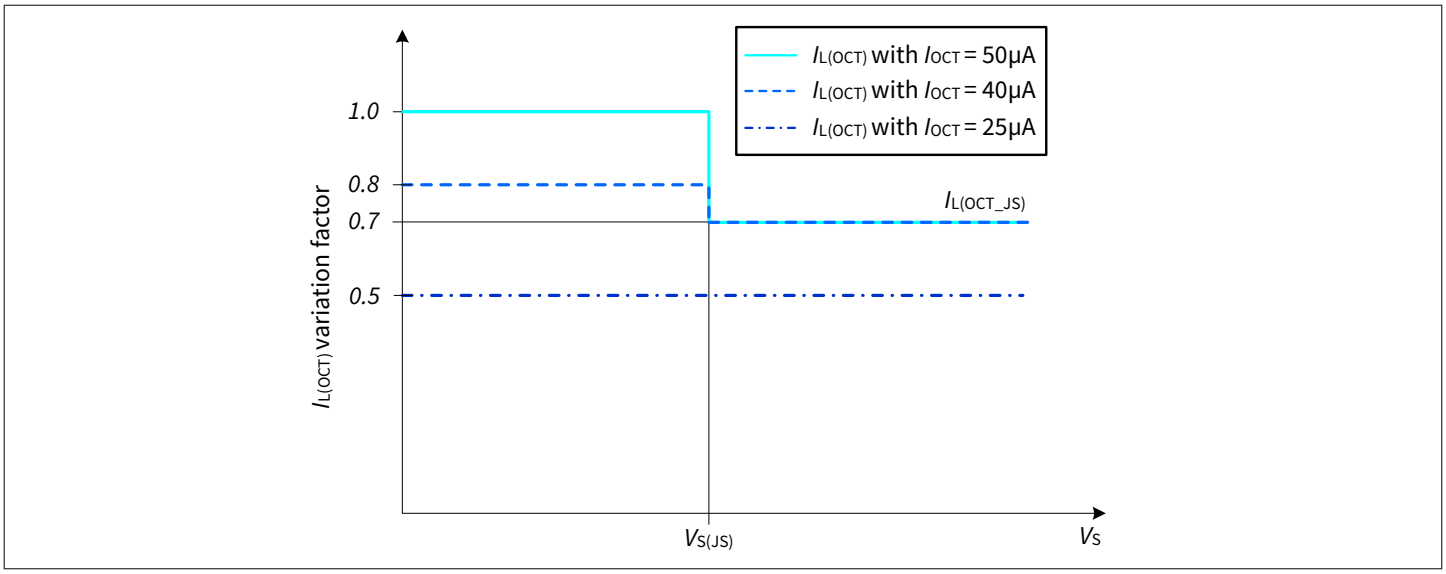



**Figure 30 Adjustable overcurrent with $V_S$ voltage**

When $I_L \geq I_{L(OCT)}$ the channel is switched OFF. The channel is allowed to be reactivated according to the intelligent latch strategy described in Chapter 8.3.

## 8.3 Device protection and diagnosis in case of fault

Any fault event (either overtemperature or overcurrent) that triggers a device protection mechanism has two consequences:

- The channel switches OFF and remains latched OFF (internal latch set to "1")
- If the sequential diagnosis is active for the channel, the current $I_{IS(FAULT)}$ is provided in case of IN = "high" (see Chapter 10.1.1) and for IN = "low" the current $I_{IS(DEVOFF)}$ is provided at address #1 (see Chapter 10.1.2 for further details)

The channel can be switched ON again if all the protection mechanisms fulfill the "reactivation" conditions described in Table 11 and a reset by DEN or IN was applied.

Furthermore, the device has the intelligent latch to protect itself against unwanted repetitive reactivation in fault condition.

**Table 11 Protection "reactivation" condition**

| Fault condition | Switch OFF event | "Reactivation" condition |
|---|---|---|
| Overtemperature | $T_J \geq T_{J(ABS)}$ or $(T_J - T_{J(REF)}) \geq T_{J(DYN)}$ | $T_J < T_{J(ABS)}$ and $(T_J - T_{J(REF)}) < T_{J(DYN)}$ (including hysteresis) |
| Overcurrent | $I_L \geq I_{L(OCT)}$ | |

### 8.3.1 Intelligent latch reset strategy after device protection triggered

In normal condition, when IN is set to "high", the channel is switched ON. In case the device protection is triggered, the output stage is switched OFF. It remains OFF until the channel is reset. There are two ways to reset the channel:

With IN pin: By setting the input pin to "low" for a time longer than $t_{DELAY(LR)}$ ("latch reset delay" time), the channel is reset if the "reactivation" conditions for the protection mechanisms are fulfilled (see Table 11). If the input is set to "high" during the "latch reset delay" time the channel remains switched OFF and the timer $t_{DELAY(LR)}$ is reset. The timer $t_{DELAY(LR)}$ restarts as soon as the input pin is set to "low" again.

With DEN pin: It is possible to "force" a reset of the internal latch without waiting for $t_{DELAY(LR)}$ by applying a pulse (rising edge followed by a falling edge) to the DEN pin while IN pin is "low". The pulse applied to DEN pin must have a duration longer than $t_{DEN(LR)}$ to ensure a reset of the internal latch.

Intelligent latch reset strategy after device protection triggered is shown in Figure 31, Figure 32 and Figure 33.

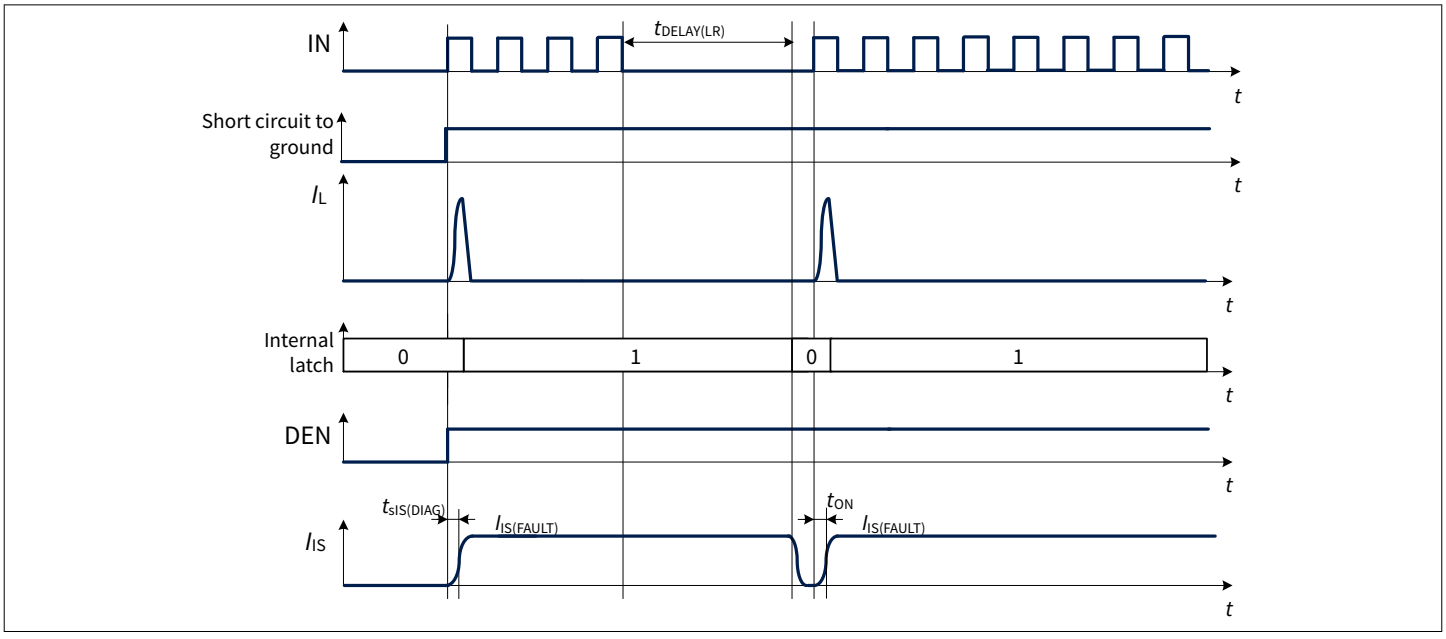



**Figure 31 Intelligent latch timing diagram for IN reset in case of triggered device protection**

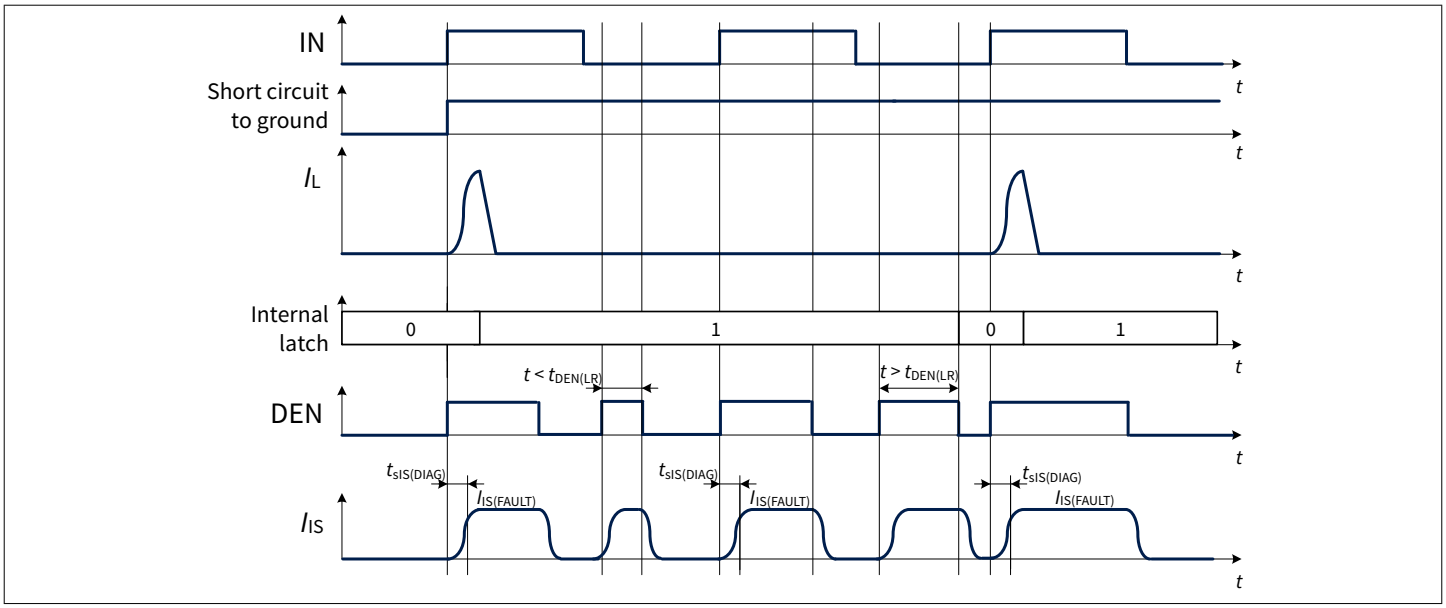



**Figure 32 Intelligent latch timing diagram for DEN reset in case of triggered device protection**

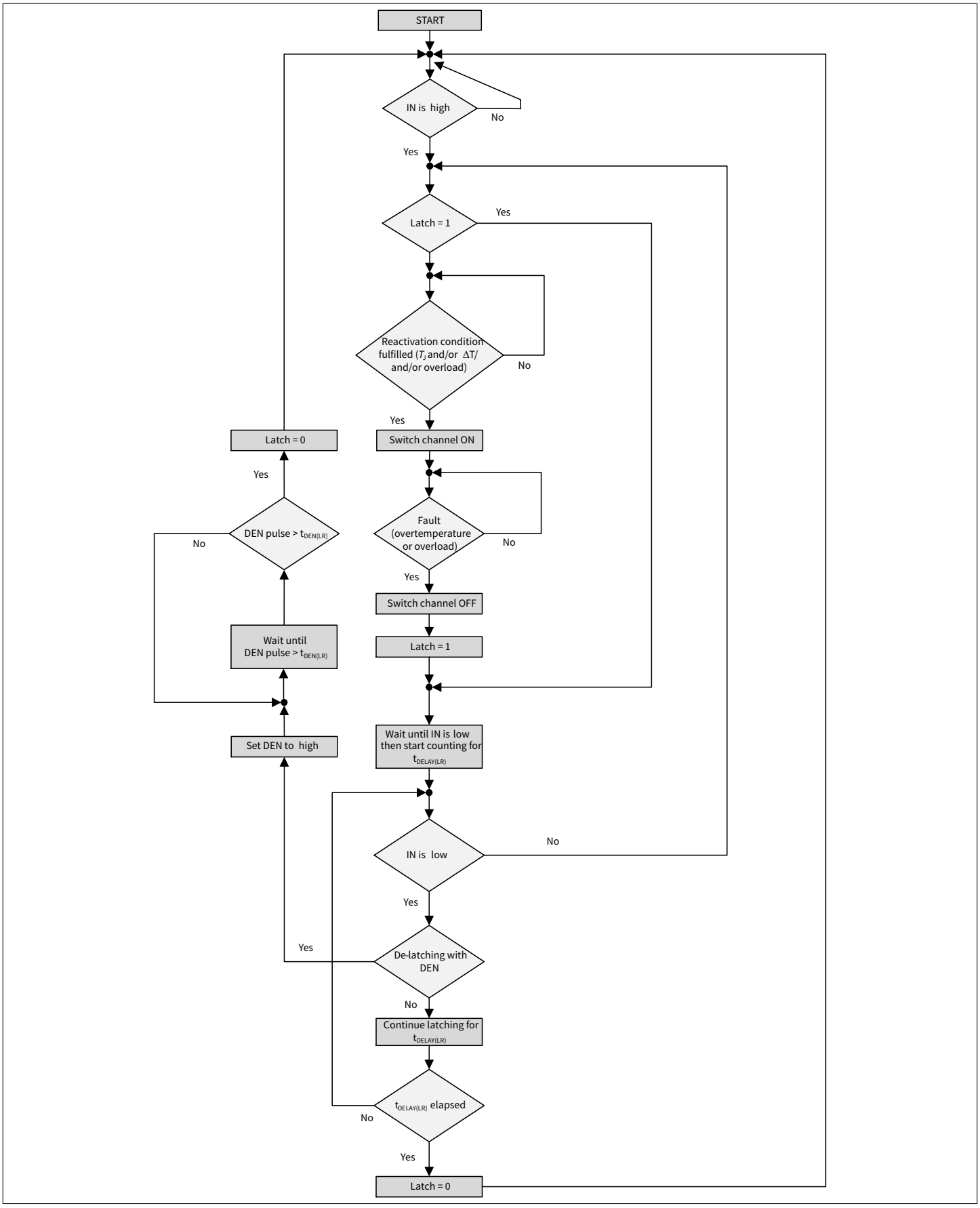



**Figure 33 Intelligent latch flowchart in case of triggered device protection**

## 8.4 Additional protections

### 8.4.1 Reverse polarity protection

In reverse polarity condition (also known as reverse battery), the output stage is switched ON (see parameter $R_{DS(REV)}$) because of the Reverse ON feature, which limits the power dissipation in the output stage. Each ESD diode of the logic contributes to total power dissipation. The reverse current through the output stage must be limited by the connected load. The current through digital input pins has to be limited as well by an external resistor (please refer to the absolute maximum ratings listed in Table 2 and to application information in Chapter 11). Figure 34 shows a typical application including a device with Reverse ON. A current flowing into GND pin ($-I_{GND}$) during reverse polarity condition is necessary to activate Reverse ON, therefore a resistive path between module ground and device GND pin must be present.

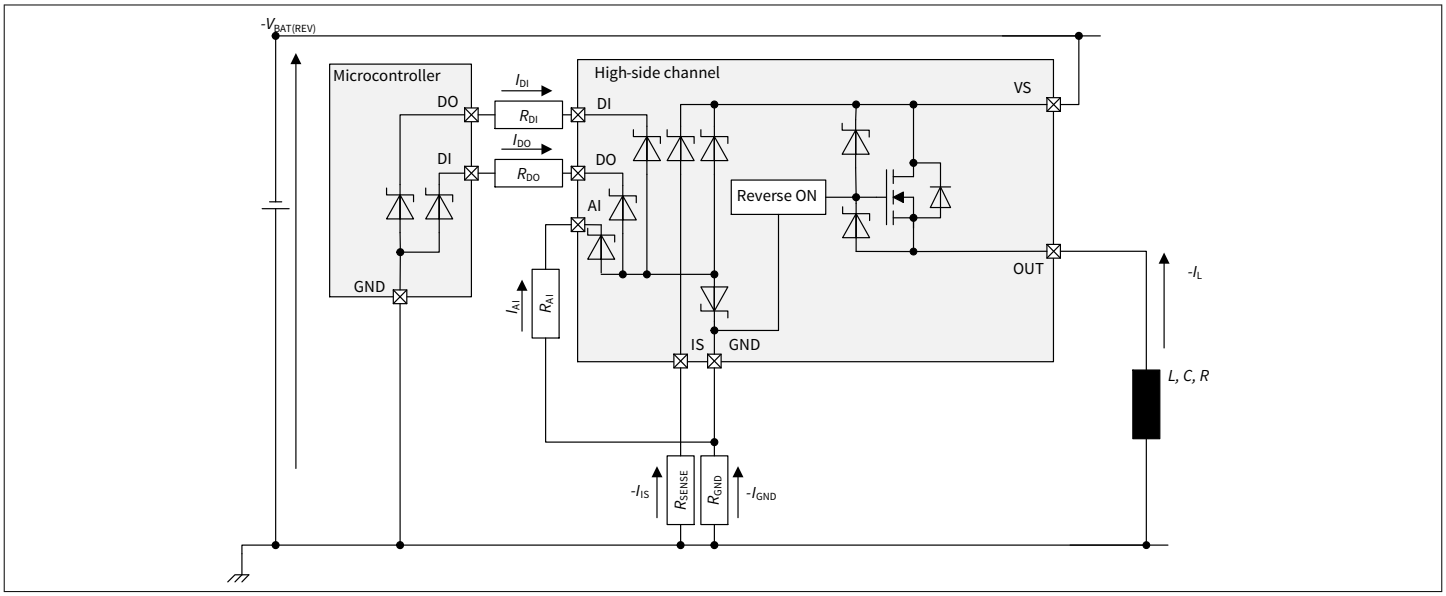



**Figure 34 Reverse battery protection (application example)**

### 8.4.2 Overvoltage protection

In case of supply voltages between $V_{S(EXT,UP)}$ and $V_{BAT(LD)}$, the output transistor is still operational and follows the input pin.

In addition to the output clamp for inductive loads as described in Chapter 7.2.2, there is a clamp mechanism available for overvoltage protection for the logic circuit and the output channels, monitoring the voltage between VS and GND pins ($V_{S(CLAMP)}$).

## 8.5 Protection against loss of connection

### 8.5.1 Loss of battery and loss of load

The loss of connection to battery or load has no influence on device robustness when load and wire harness are purely resistive. In case of driving an inductive load, the energy stored in the inductance must be handled.

PROFET™ Wire Guard devices handle the inductivity of the wire harness up to 10 µH with $I_{L(NOM)\_85}$.

In case of applications where currents and / or the aforementioned inductivity are exceeded, an external suppressor diode (like diode $D_{Z2}$ shown in Chapter 11) is recommended to handle the energy and to provide a well-defined path to the load current.

### 8.5.2 Loss of ground

In case of loss of device ground, it is recommended to have a resistor connected between any digital input pin and the microcontroller to ensure a channel switch OFF (as described in Chapter 11).

***Note**: In case that any digital input pin is pulled to ground (either by a resistor or active) a parasitic ground path is available, which could keep the device operational during loss of device ground.*

## 8.6 Electrical characteristics device protection

**Table 12 Electrical characteristics device protection**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Thermal** | | | | | | | |
| Thermal shutdown temperature (absolute) | $T_{J(ABS)}$ | 150 | 175 | 200 | °C | 1) 2)<br>See Figure 25 | PRQ-246 |
| Thermal shutdown hysteresis (absolute) | $T_{HYS(ABS)}$ | – | 30 | – | K | 3) | PRQ-247 |
| Thermal shutdown temperature (dynamic) | $T_{J(DYN)}$ | – | 80 | – | K | 3)<br>See Figure 26 | PRQ-248 |
| **Voltages** | | | | | | | |
| Power supply clamping voltage at TJ = -40°C | $V_{S(CLAMP)\_-40}$ | 33 | 36.5 | 42 | V | $I_{VS}$ = 10 mA<br>$T_J$ = -40°C<br>See Figure 20 | PRQ-251 |
| Power supply clamping voltage at TJ ≥ 25°C | $V_{S(CLAMP)\_25}$ | 35 | 38 | 44 | V | 2)<br>$I_{VS}$ = 10 mA<br>$T_J$ ≥ 25°C<br>See Figure 20 | PRQ-252 |
| Low level of overcurrent threshold depending on drain source voltage | $V_{DS(LOCT)}$ | 13.5 | 15.0 | 16.5 | V | 3) | PRQ-1248 |
| High level of overcurrent threshold depending on drain source voltage | $V_{DS(HOCT)}$ | 18 | 20 | 22 | V | 3) | PRQ-1249 |

**(table continues...)**

**Table 12 (continued) Electrical characteristics device protection**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Power supply voltage threshold for overcurrent threshold reduction in case of short circuit | $V_{S(JS)}$ | 20.5 | 22.5 | 24.5 | V | 3)<br>Setup acc. to AEC-Q100-012 | PRQ-253 |
| **Timings** | | | | | | | |
| Latch reset delay time after fault condition | $t_{DELAY(LR)}$ | 40 | 70 | 100 | ms | 1)<br>See Figure 31 | PRQ-254 |
| Minimum DEN pulse duration for latch reset | $t_{DEN(LR)}$ | 50 | 100 | 150 | µs | 3)<br>See Figure 32 | PRQ-255 |

1) Functional test only.
2) Tested at $T_J$ = 150°C only.
3) Not subject to production test - specified by design.

**Table 13 Electrical characteristics protection - power output stages**

$V_S$ = 5 V to 20 V, $T_J$ = -40 °C to +150 °C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Highest configurable overcurrent detection threshold at TJ = -40°C | $I_{L(HOCT)\_-40}$ | 66.0 | 77.5 | 89.0 | A | 1)<br>$T_J$ = -40°C<br>d$I$/d$t$ = 0.2 A/µs<br>$I_{OCT}$ = 50 µA | PRQ-979 |
| Highest configurable overcurrent detection threshold at TJ = 25°C | $I_{L(HOCT)\_25}$ | 62.0 | 73.0 | 84.0 | A | 1) 2)<br>$T_J$ = 25°C<br>d$I$/d$t$ = 0.2 A/µs<br>$I_{OCT}$ = 50 µA | PRQ-980 |
| Highest configurable overcurrent detection threshold at TJ = 150°C | $I_{L(HOCT)\_150}$ | 53.5 | 63.0 | 72.5 | A | 1) 2)<br>$T_J$ = 150°C<br>d$I$/d$t$ = 0.2 A/µs<br>$I_{OCT}$ = 50 µA | PRQ-981 |

**(table continues...)**

**Table 13 (continued) Electrical characteristics protection - power output stages**

$V_S$ = 5 V to 20 V, $T_J$ = -40 °C to +150 °C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25 °C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Overcurrent detection at high VDS | $I_{L(OCT\_VDS)}$ | – | 52 | – | A | 1) 2)<br>$I_{OCT}$ = 50 µA<br>$V_{DS} > V_{DS(HOCT)}$<br>See Figure 28 | PRQ-982 |
| Overcurrent detection - jump start condition | $I_{L(OCT\_JS)}$ | – | 52 | – | A | 1) 2)<br>$V_S > V_{S(JS)}$<br>$I_{OCT}$ = 50 µA<br>See Figure 30 | PRQ-983 |
| Lowest configurable overcurrent detection threshold | $I_{L(LOCT)\_-40}$ | 7.6 | 12.8 | 18 | A | 1)<br>$T_J$ = -40°C<br>d$I$/d$t$ = 0.05 A/µs<br>$I_{OCT}$ = 7.5 µA | PRQ-985 |
| Overcurrent threshold ratio at TJ = -40°C | $k_{OCT}$ | – | 1.52 | – | – | 2)<br>$T_J$ = -40°C | PRQ-1316 |
| OCT current threshold for short detection | $I_{OCT\_SHORT}$ | 83.3 | – | – | µA | – | PRQ-885 |
| OCT adjustment current | $I_{OCT}$ | 7.2 | – | 52.6 | µA | – | PRQ-599 |
| OCT current threshold for open detection | $I_{OCT\_OPEN}$ | – | – | 3.8 | µA | – | PRQ-886 |
| Overcurrent threshold temperature coefficient | $k_{TJ}$ | – | -0.985 | – | – | 2) | PRQ-1497 |

1) Functional test only.
2) Not subject to production test - specified by design.

# 9 System protection

## 9.1 I2t protection

The integrated I2t protection supports the protection of the system including the wire harness and the PCB traces.

The I2t protection function is active in I2t mode and I2t with diagnosis mode. While the I2t status calculation (with $I_L$ = 0 A) is as well present in Inactive mode, Inactive with diagnosis mode, CLS mode and CLS with diagnosis mode.

The I2t protection feature calculates an I2t status $S_{I2t}$, which is based on the load current $I_L$, the time constant of all I2t protection curves $\tau_{I2t}$ and the dedicated IDC of the I2t protection curve $I_{L(I2t\_x)}$.

The channel is switched off as soon as the I2t status $S_{I2t}$ calculation reaches 100% (see Figure 35).

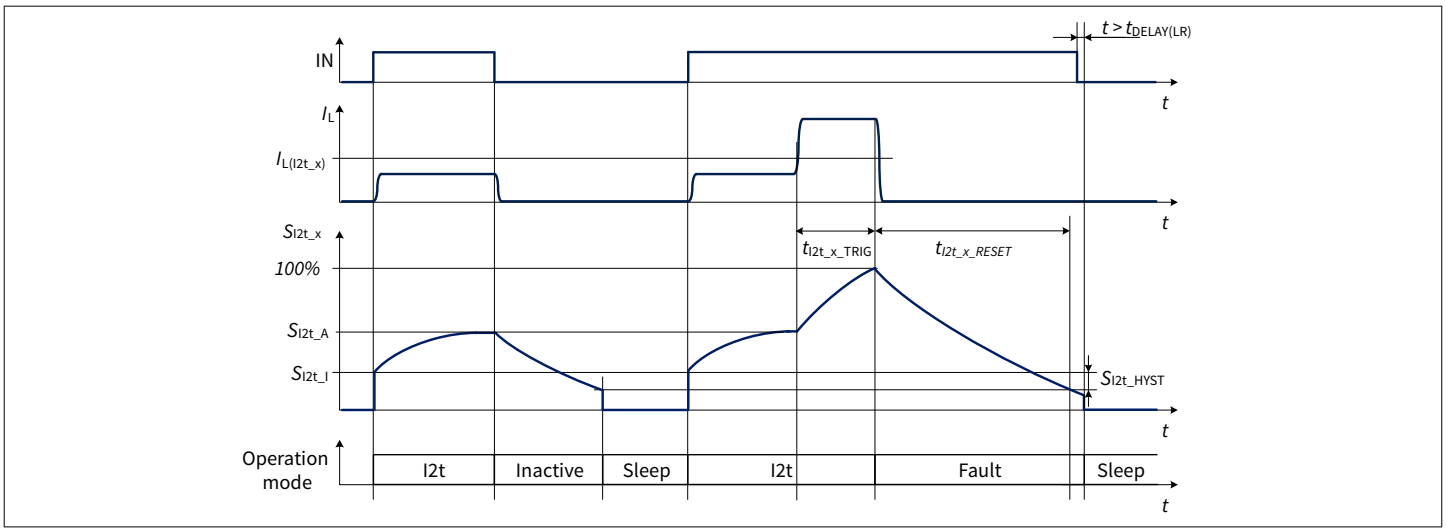



**Figure 35 I2t protection timing**

When the power stage is switched off due to an I2t protection event, the channel is latched off and the I2t status is further calculated with $I_L$ = 0 A.

The dedicated trigger time of the I2t protection curve depends on the actual I2t status $S_{I2t\_A}$ and can be calculated for constant load currents by:

$$t_{I2t\_x\_TRIG} = \begin{cases} \infty & \text{for } I_L \leq I_{L(I2t\_x)} \\ \tau_{I2t} \cdot \ln\left(\dfrac{I_L^2 - I_{L(I2t\_x)}^2 \cdot S_{I2t\_A}}{I_L^2 - I_{L(I2t\_x)}^2}\right) & \text{for constant } I_L > I_{L(I2t\_x)} \end{cases} \quad (4)$$

The steady state value of the actual I2t status $S_{I2t\_A}$ can be calculated with the actual steady state current $I_{L\_A}$ by:

$$S_{I2t\_A} = \frac{I_{L\_A}^2}{I_{L\_(I2t\_x)}^2} \quad (5)$$

The initial value of the I2t status calculation depends on the mode transition and the actual I2t status $S_{I2t\_A}$. In case the I2t status calculation is resumed from a value lower than the initial status $S_{I2t\_I}$ minus the I2t status hysteresis $S_{I2t\_HYST}$ (for instance the I2t mode is entered for the first time) the I2t calculation is pre-loaded with the initial status value $S_{I2t\_I}$. In case the I2t status calculation is resumed from a value higher than the initial status $S_{I2t\_I}$ minus the I2t status hysteresis $S_{I2t\_HYST}$, the I2t status $S_{I2t}$ calculation will be resumed from the actual I2t status $S_{I2t\_A}$.

The initial status value $S_{I2t\_I}$ is preloaded for the following transition conditions slp_i2t, slp_iwd, idle_i2t, idle_ina, awd_i2twd and awd_iwd (see Figure 16). In all other transition conditions, the I2t status calculation is resumed from the actual $S_{I2t\_A}$ value.

In case the actual I2t status $S_{I2t\_A}$ is preloaded by the initial I2t status $S_{I2t\_I}$ it has to be replaced in equation 3 (dedicated trigger time of the I2t protection curve) by the initial I2t status $S_{I2t\_I}$ which can be calculated by:

$$S_{I2t\_I} = \frac{I^2_{L(I2t\_I)}}{I^2_{L\_(I2t\_x)}} \tag{6}$$

To enter sleep mode after the I2t protection feature was triggered the I2t status calculation has to be below the initial status $S_{I2t\_I}$ minus the I2t status hysteresis $S_{I2t\_HYST}$ (see Figure 35). This transition time $t_{I2t\_x\_RESET}$ is given by the following formula (assuming $I_L$= 0 A):

$$t_{I2t\_x\_RESET} = \tau_{I2t} \cdot \ln\left(\frac{I^2_{L(I2t\_x)}}{\left(I_{L(I2t\_I)} - I_{L(I2t\_HYST)}\right)^2}\right) \tag{7}$$

As the ambient temperature and the PCB layout influences the thermal behavior of the device, the overtemperature protection might be triggered before $t_{I2t\_x\_TRIG}$ is reached (see Figure 36) ). Therefore, the maximum time for a given current is potentially limited by the thermal design of the component. For more information, refer to Table 5.

The device has six different I2t protection curves $I_{L(I2t\_x)}$ implemented (see Figure 36). The I2t protection curves $I_{L(I2t\_x)}$ can be selected by placing the corresponding selection resistor $R_{I2t\_x}$. The resistor must be connected between the I2t pin and the ground pin of the device. See Table 14 for detailed information. In case of an open or short of the selection resistor the device selects the I2t protection curve 1.

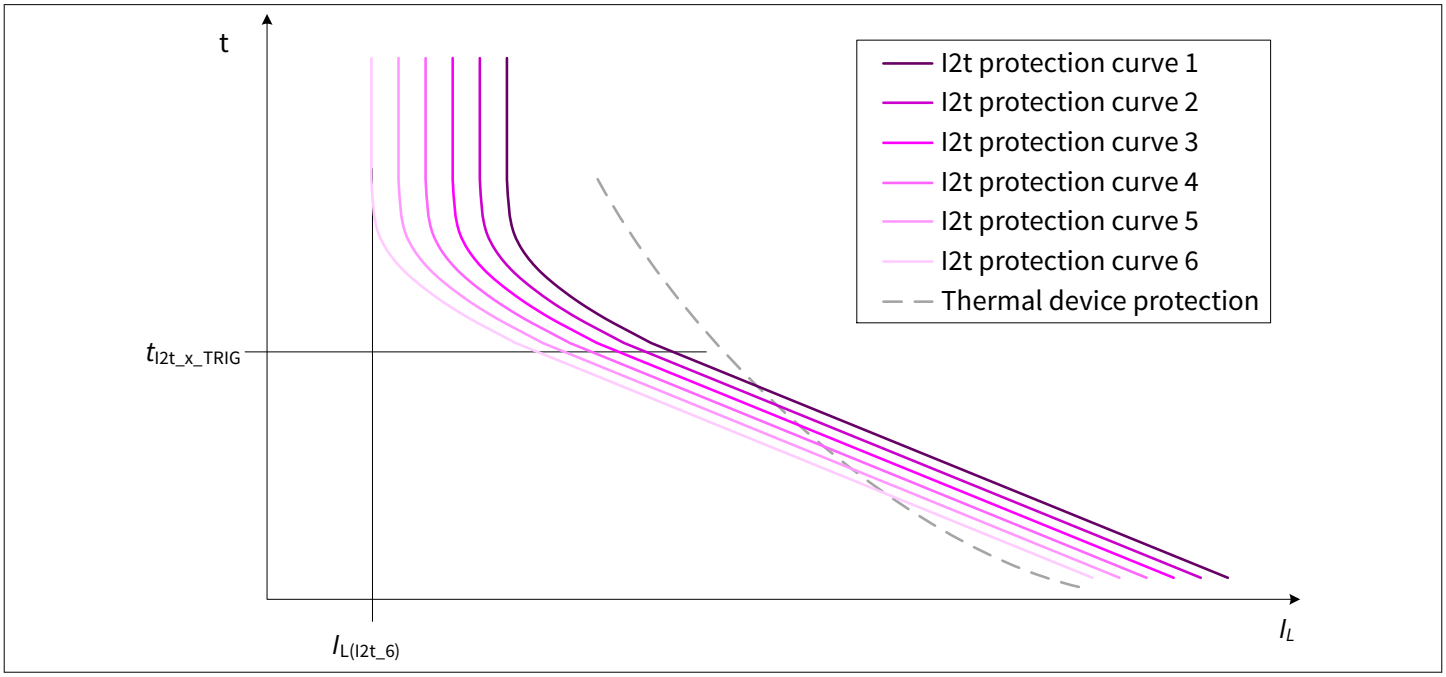



**Figure 36 Energy graph of I2t protection curves**

***Note**: This is a very simplified overview of the implemented system protection function. For detailed trigger behavior, refer to Table 14.*

The synchronization time $t_{SYNC(RI2t)}$ for I2t programming resistor setting is a time at which the device internally updates the I2t protection curve setting.

During inverse current operation the I2t calculation assumes no load current flowing.

In reverse battery condition the I2t calculation is reset and disabled.

### 9.1.1 I2t protection and idle mode

In idle mode as well as in active with diagnosis mode, the I2t protection calculation is disabled.

To change from I2t mode to idle mode the idle mode entry conditions have to be fulfilled (see Chapter 6.1.7).

The minimum transition time from I2t mode to idle mode for $I_L$ = 0 A could be calculated by:

$$t_{T(I2t\_IDLE)} = \tau_{I2t} \cdot \ln\left(\frac{I^2_{L(I2t\_I)}}{\left(I_{L(I2t\_I)} - I_{L(I2t\_HYST)}\right)^2}\right) \quad (8)$$

When the device changes from idle mode into I2t mode, I2t with diagnosis mode (over active with diagnosis mode) and inactive mode, the initial value of the I2t status calculation becomes again pre-loaded with the initial current for I2t protection value $I_{L(I2t\_I)}$ (see Figure 37).

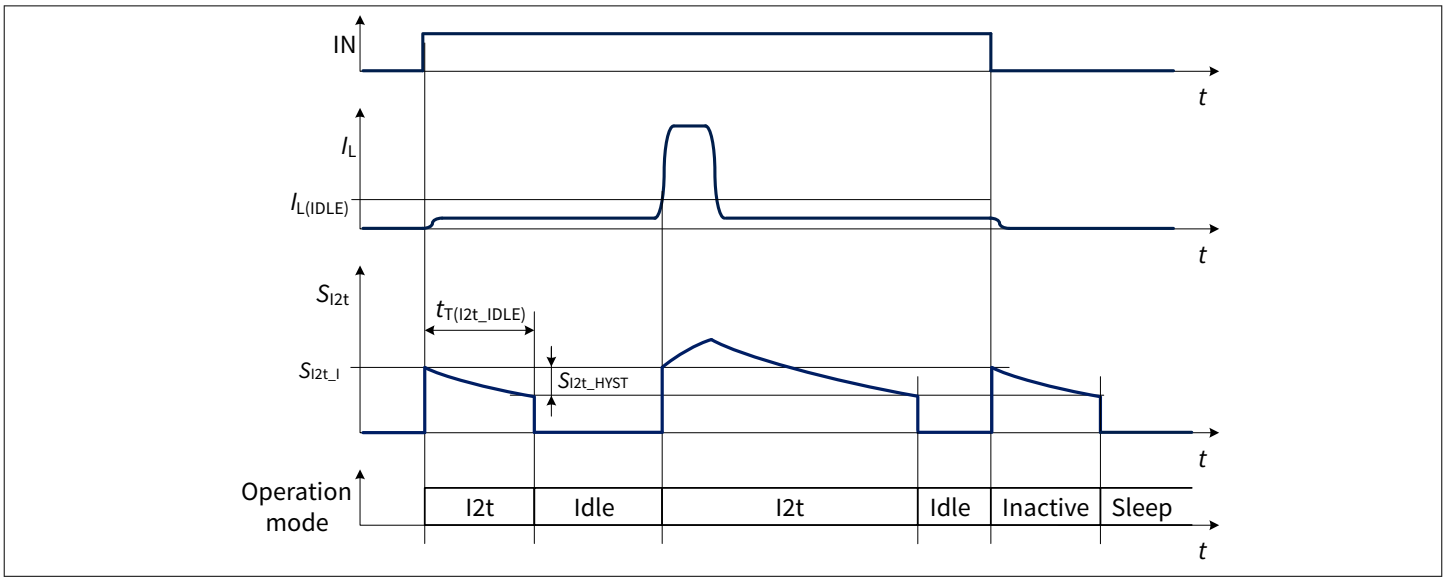



**Figure 37 Idle mode timing**

### 9.1.2 Intelligent latch reset strategy after I2t protection triggered

Any fault event that triggers the I2t protection mechanism has the following consequences:

- The channel switches OFF and remains latched OFF (internal latch set to "1")
- The calculation of I2t protection curve will be continued
- If the diagnosis is active for the channel, depending on the sequential diagnosis address and IN status, different $I_{IS}$ currents are provided at the IS pin (for further details see Figure 44)
  - Address #1 & IN = "high" - the $I_{IS(FAULT)}$ current is provided showing that the channel is switched OFF
  - Address #1 & IN = "low" - the $I_{IS(I2tOFF)}$ current is provided showing that the channel is switched OFF due to triggered I2t protection
  - Address #2 - #5 & IN = "low" - the $I_{IS}$ currents are provided as described in Figure 44

The intelligent latch can be reset by IN or DEN at any time of the I2t status calculation. After the reset the channel can be switched ON again and the I2t status will be further calculated.

With IN pin: By setting the input pin to “low” for a time longer than $t_{DELAY(LR)}$ (“latch reset delay” time) the channel is reset. If the input is set to “high” during the “latch reset delay” time, the channel remains switched OFF and the timer $t_{DELAY(LR)}$ is reset. The timer $t_{DELAY(LR)}$ restarts as soon as the input pin is set to “low” again (see Figure 38).

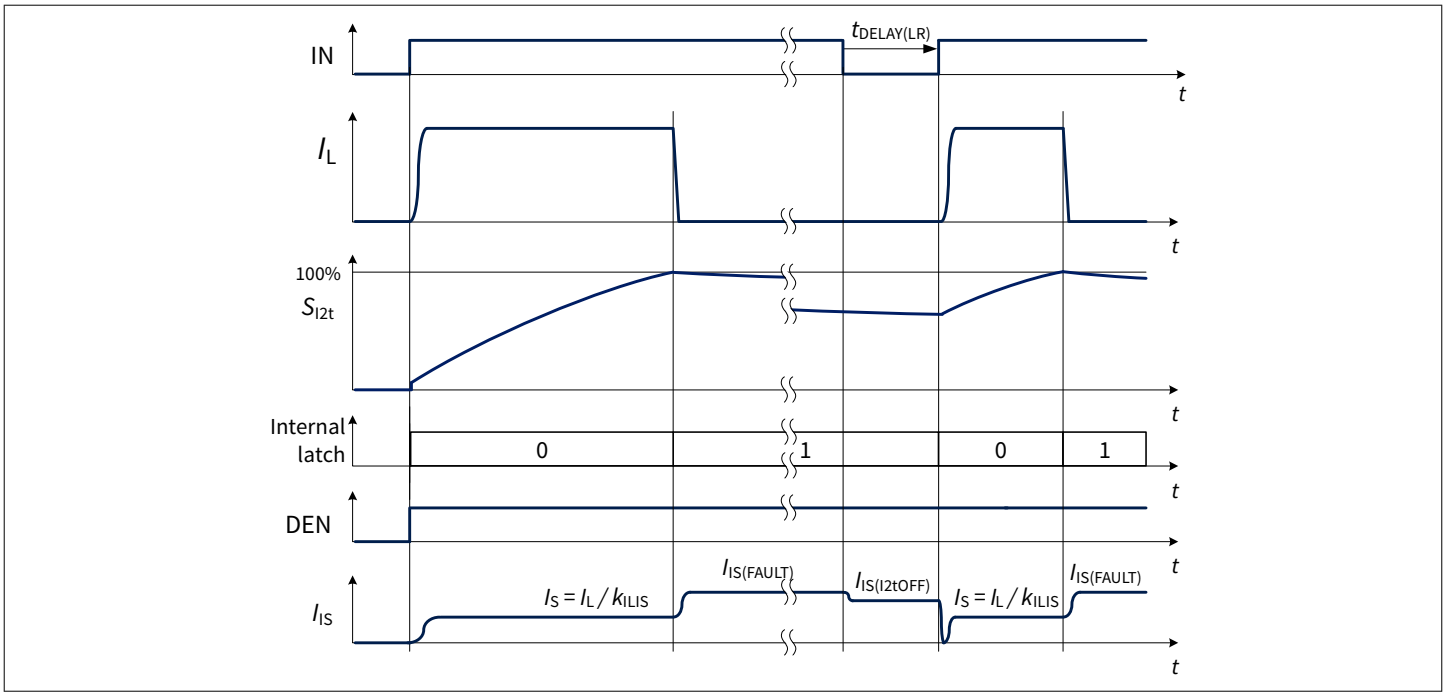



**Figure 38 Intelligent latch timing diagram for IN reset in case of triggered I2t protection**

With DEN pin: It is possible to “force” a reset of the internal latch without waiting for $t_{DELAY(LR)}$ by applying a pulse (rising edge followed by a falling edge) to the DEN pin while IN pin is “low”. The pulse applied to DEN pin must have a duration longer than $t_{DEN(LR)}$ to ensure a reset of the internal latch (see Figure 39).

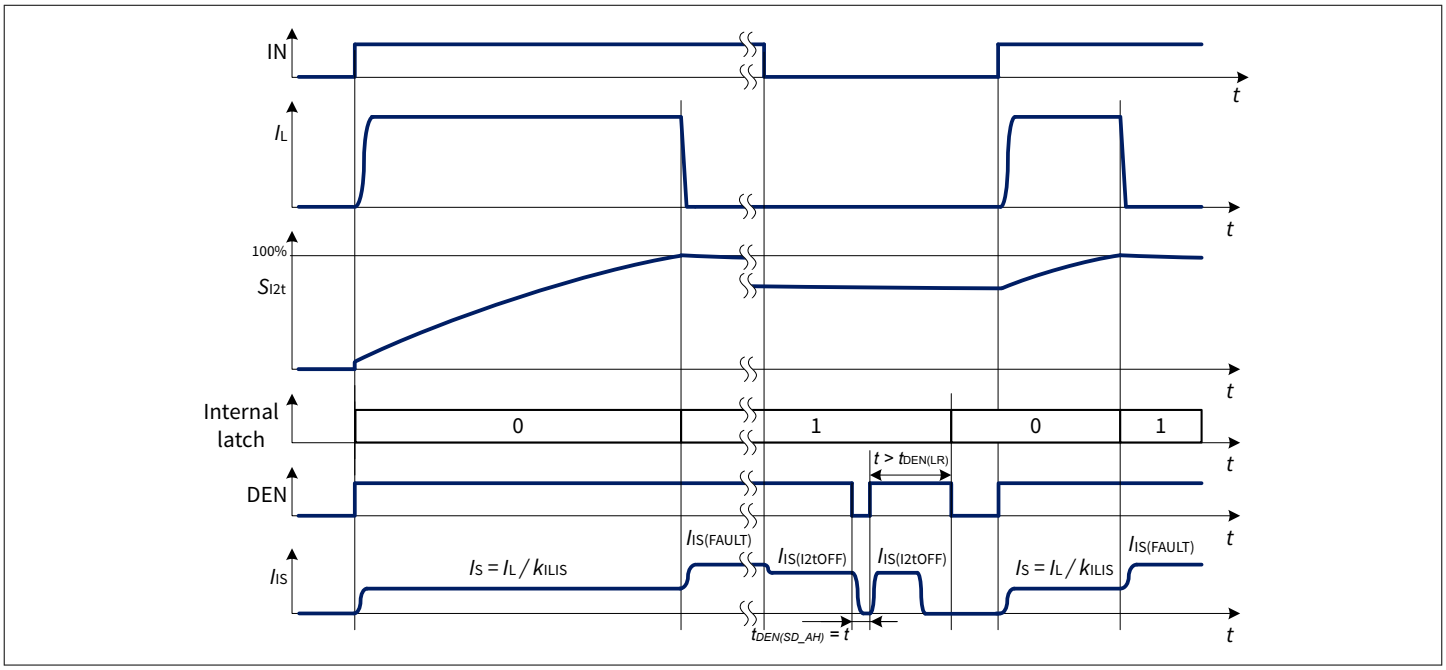



**Figure 39 Intelligent latch timing diagram for DEN reset in case of triggered I2t protection**

The intelligent latch strategy in case of device protection triggering is shown in Figure 40.

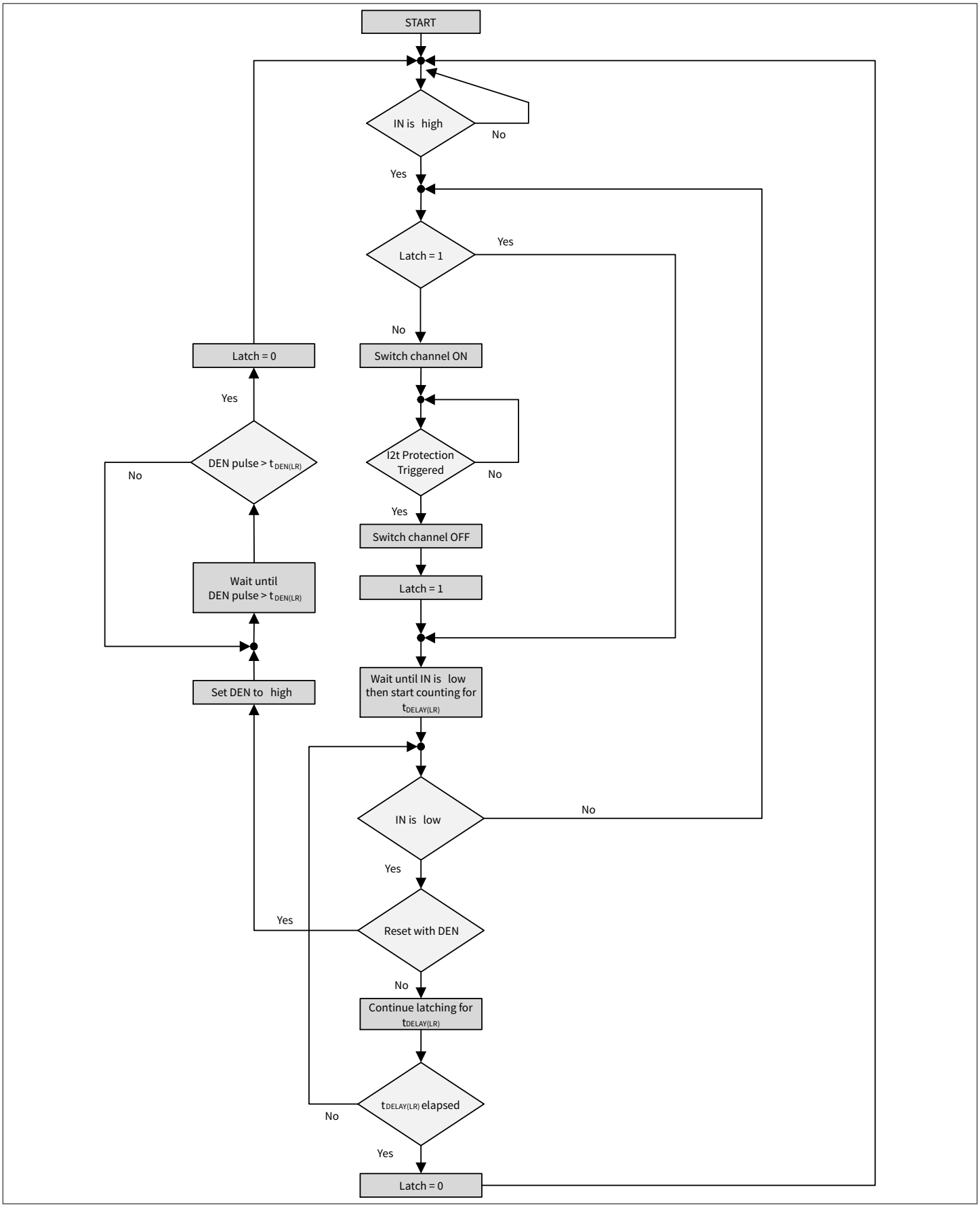



**Figure 40 Intelligent latch flowchart in case of triggered I2t protection**

## 9.2 Electrical characteristics protection

**Table 14 Electrical characteristics I2t protection**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| I2t resistor threshold for short detection | $R_{I2t\_SHORT}$ | – | – | 6 | kΩ | 1) | PRQ-890 |
| Selection resistor for I2t protection curve 1 | $R_{I2t\_1}$ | 9.31 | 9.76 | 10.20 | kΩ | – | PRQ-573 |
| Selection resistor for I2t protection curve 2 | $R_{I2t\_2}$ | 14.06 | 14.70 | 15.30 | kΩ | – | PRQ-574 |
| Selection resistor for I2t protection curve 3 | $R_{I2t\_3}$ | 20.74 | 21.50 | 22.46 | kΩ | – | PRQ-575 |
| Selection resistor for I2t protection curve 4 | $R_{I2t\_4}$ | 30.91 | 32.40 | 33.66 | kΩ | – | PRQ-576 |
| Selection resistor for I2t protection curve 5 | $R_{I2t\_5}$ | 44.39 | 46.40 | 48.09 | kΩ | – | PRQ-577 |
| Selection resistor for I2t protection curve 6 | $R_{I2t\_6}$ | 65.38 | 68.10 | 70.82 | kΩ | – | PRQ-578 |
| I2t resistor threshold for open detection | $R_{I2t\_OPEN}$ | 130 | – | – | kΩ | 1) | PRQ-889 |
| Synchronization time of selection resistor for I2t protection curve setting | $t_{SYNC(RI2t)}$ | 12.8 | 19.2 | 25.6 | µs | 1) | PRQ-944 |
| Time constant of all I2t protection curves | $\tau_{I2t}$ | 7.0 | 10.0 | 13.0 | s | 1) | PRQ-986 |
| IDC of I2t protection curve 1 | $I_{L(I2t\_1)}$ | 10.3 | 11.4 | 12.5 | A | 1) 2) | PRQ-987 |
| IDC of I2t protection curve 2 | $I_{L(I2t\_2)}$ | 9.2 | 10.3 | 11.3 | A | 1) 2) | PRQ-988 |
| IDC of I2t protection curve 3 | $I_{L(I2t\_3)}$ | 8.3 | 9.2 | 10.2 | A | 1) 2) | PRQ-989 |
| IDC of I2t protection curve 4 | $I_{L(I2t\_4)}$ | 7.5 | 8.3 | 9.1 | A | 1) 2) | PRQ-990 |
| IDC of I2t protection curve 5 | $I_{L(I2t\_5)}$ | 6.7 | 7.5 | 8.2 | A | 1) 2) | PRQ-991 |
| IDC of I2t protection curve 6 | $I_{L(I2t\_6)}$ | 6.1 | 6.7 | 7.4 | A | 1) 2) | PRQ-992 |

**(table continues...)**

**Table 14 (continued) Electrical characteristics I2t protection**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| IDC of I2t Hysteresis Curve | $I_{L(I2t\_HYST)}$ | 0.08 | 0.1 | 0.12 | A | 1) 2) | PRQ-1311 |
| Initial current for I2t protection | $I_{L(I2t\_I)}$ | 2.2 | 2.6 | 3.0 | A | 1) 2) | PRQ-993 |
| **Transition times** | | | | | | | |
| Transition time I2t to idle | $t_{T(I2t\_IDLE)}$ | 0.6 | 0.78 | 1.0 | s | 1) $I_L$ < 10 mA | PRQ-965 |

1) Not subject to production test - specified by design.
2) I2t DC trigger level specified for times longer than 200s.

# 10 Diagnosis

For diagnosis purposes the device provides a sense current signal ($I_{IS}$) at IS pin. In case of disabled diagnostics (DEN pin set to “low”), IS pin becomes high impedance.

A sense resistor $R_{SENSE}$ must be connected between IS pin and module ground if the diagnosis is used.

$R_{SENSE}$ value has to be higher than 820 Ω (or 400 Ω when a central reverse battery protection is externally present on the battery feed) to limit the power losses in the sense circuitry.

A typical value is $R_{SENSE}$ = 1.2 kΩ.

Due to the internal connection between IS pin and $V_S$ supply voltage, it is not recommended to connect the IS pin to the sense current output of other devices if they are supplied by a different battery feed.

See Figure 41 for details as an overview.

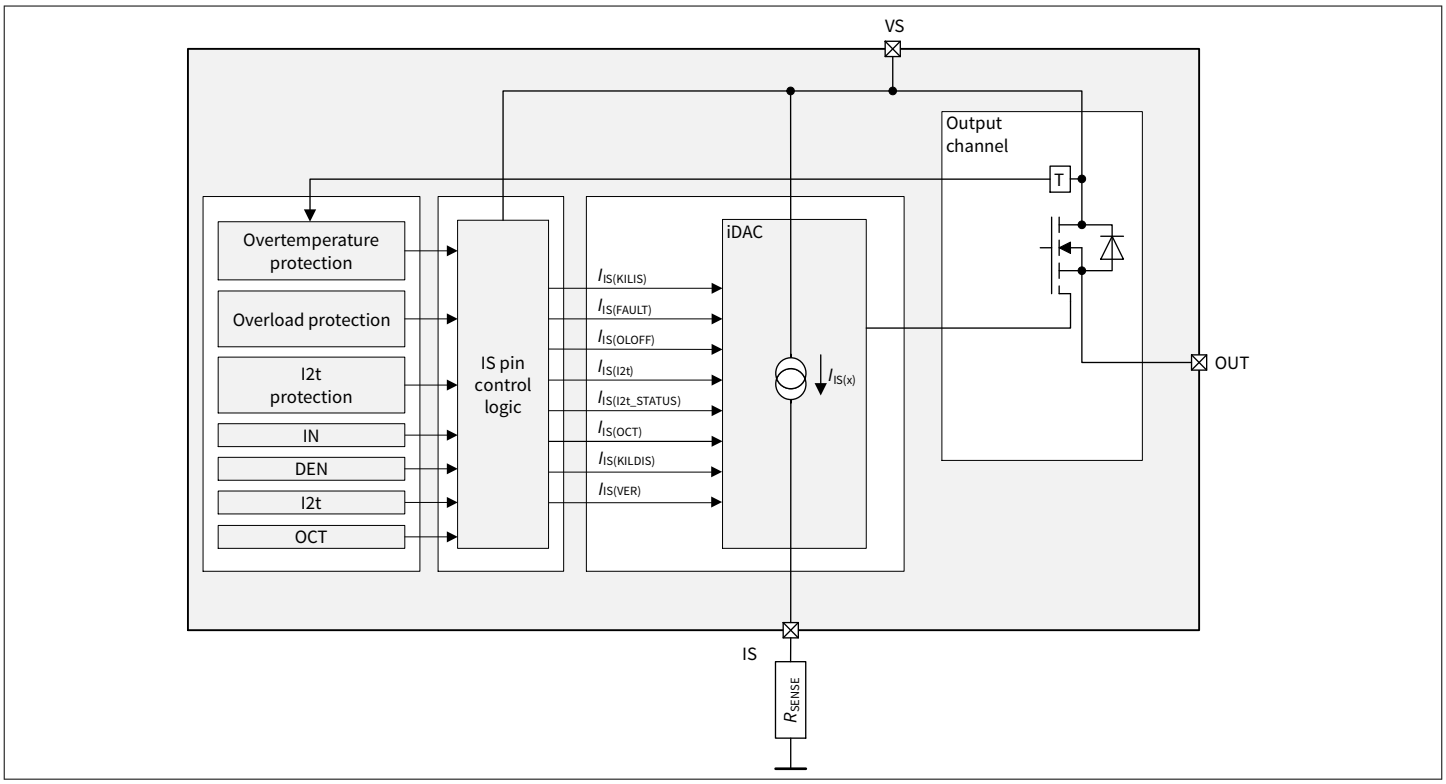



**Figure 41 Diagnosis block diagram**

Table 15 gives a reference to the state of the IS pin during the operation of the device.

**Table 15 SENSE signal, function of application condition**

| Application condition | Input level | DEN level | $V_{OUT}$ | Diagnostic input |
|---|---|---|---|---|
| Normal operation and short circuit to GND | "low" | "high" | ~GND | #1: Z |
| | | | | $I_{IS(DEVOFF)}$, $I_{IS(I2tOFF)}$ if latch ≠ 0 |
| | | | | #2: $I_{IS(I2t)}$ |
| | | | | #3: $I_{IS(STATUS\_I2t)}$ |
| | | | | #4: $I_{IS(OCT)}$ |
| | | | | #5: $I_{IS(VER)}$ |
| Overtemperature | | | Z | #1: $I_{IS(DEVOFF)}$ |

**(table continues...)**

**Table 15 (continued) SENSE signal, function of application condition**

| Application condition | Input level | DEN level | $V_{OUT}$ | Diagnostic input |
|---|---|---|---|---|
| | | | | #2: $I_{IS(I2t)}$ |
| | | | | #3: $I_{IS(STATUS\_I2t)}$ |
| | | | | #4: $I_{IS(OCT)}$ |
| | | | | #5: $I_{IS(VER)}$ |
| Short circuit to $V_S$ | | | $V_S$ | #1: $I_{IS(OLOFF)}$ |
| | | | | $I_{IS(DEVOFF)}$, $I_{IS(I2tOFF)}$ if latch ≠ 0 |
| | | | | #2: $I_{IS(I2t)}$ |
| | | | | #3: $I_{IS(STATUS\_I2t)}$ |
| | | | | #4: $I_{IS(OCT)}$ |
| | | | | #5: $I_{IS(VER)}$ |
| Open load | | | < $V_S$ - $V_{DS(OLOFF)}$ [1)] | #1: Z |
| | | | > $V_S$ - $V_{DS(OLOFF)}$ [1)] | #1: $I_{IS(OLOFF)}$ |
| | | | | (in both cases $I_{IS(DEVOFF)}$) |
| | | | | $I_{IS(I2tOFF)}$ if latch ≠ 0) |
| | | | | #2: $I_{IS(I2t)}$ |
| | | | | #3: $I_{IS(STATUS\_I2t)}$ |
| | | | | #4: $I_{IS(OCT)}$ |
| | | | | #5: $I_{IS(VER)}$ |
| Inverse current | | | ~ $V_{INV}$ = $V_{OUT}$ > $V_S$ | #1: $I_{IS(OLOFF)}$ |
| | | | | $I_{IS(DEVOFF)}$, $I_{IS(I2tOFF)}$ if latch ≠ 0 |
| | | | | #2: $I_{IS(I2t)}$ |
| | | | | #3: $I_{IS(STATUS\_I2t)}$ |
| | | | | #4: $I_{IS(OCT)}$ |
| | | | | #5: $I_{IS(VER)}$ |
| Normal operation | "high" | | ~$V_S$ | #1: $I_{IS}$ = $I_L$ / $k_{ILIS}$ |
| | | | | #2: $I_{IS(I2t)}$ |
| | | | | #3: $I_{IS(STATUS\_I2t)}$ |
| | | | | #4: $I_{IS(OCT)}$ |
| | | | | #5: $I_{IS}$ = $I_L$ / $k_{ILDIS}$ |
| Overload | | | < $V_S$ | #1: $I_{IS(FAULT)}$ |
| Short circuit to GND | | | ~GND | #1: $I_{IS(FAULT)}$ |
| Overtemperature | | | Z | #1: $I_{IS(FAULT)}$ |
| Short circuit to $V_S$ | | | $V_S$ | #1: $I_{IS}$ < $I_L$ / $k_{ILIS}$ |

**(table continues...)**

**Table 15 (continued) SENSE signal, function of application condition**

| Application condition | Input level | DEN level | $V_{OUT}$ | Diagnostic input |
|---|---|---|---|---|
| | | | | #2: $I_{IS(I2t)}$ |
| | | | | #3: $I_{IS(STATUS\_I2t)}$ |
| | | | | #4: $I_{IS(OCT)}$ |
| | | | | #5: $I_{IS} = I_L / k_{ILDIS}$ |
| Open load | | | ~VS[2)] | #1: $I_{IS} = I_{IS(EN)}$ |
| | | | | #2: $I_{IS(I2t)}$ |
| | | | | #3: $I_{IS(STATUS\_I2t)}$ |
| | | | | #4: $I_{IS(OCT)}$ |
| | | | | #5: $I_{IS} = I_{IS(EN)}$ |
| Inverse current | | | ~ $V_{INV} = V_{OUT} > V_S$ | #1: $I_{IS} = I_{IS(EN)}$ |
| | | | | #2: $I_{IS(I2t)}$ |
| | | | | #3: $I_{IS(STATUS\_I2t)}$ |
| | | | | #4: $I_{IS(OCT)}$ |
| | | | | #5: $I_{IS} = I_{IS(EN)}$ |
| CLS mode | "pwm" | "high" | < $V_S$ - $V_{DS(OLOFF)}$ | #1: Z |
| | | | | #2: $I_{IS(I2t)}$ |
| | | | | #3: $I_{IS(STATUS\_I2t)}$ |
| | | | | #4: $I_{IS(OCT)}$ |
| | | | | #5: Z |
| All conditions | n.a. | "low" | n.a. | Z |

*1)* With additional pull-up resistor

*2)* The output current has to be smaller than $I_{L(OL)}$.

## 10.1 Sequential diagnosis

In ON and OFF state the device differentiates between the following diagnosis functions:

| Address | IN | Function |
|---|---|---|
| #1 | "high" | Current sense |
| #1 | "low" | Open load in OFF |
| #2 | "x" | I2t setting |
| #3 | "x" | I2t status |
| #4 | "x" | OCT setting |
| #5 | "high" | Digital current sense |
| #5 | "low" | Sense verification current |

To sequentially change to the next diagnosis address (for example, "current sense" to "I2t setting") a pulse at the DEN pin (falling edge followed by a rising edge) has to be applied for a time of $t_{DEN(SD\_AC)}$ ("DEN pulse duration for sequential diagnosis address change"). If the pulse is shorter than $t_{DEN(SD\_AH)}$ ("DEN pulse duration for sequential diagnosis address hold)" no address change is performed. The timing and modes are shown in Figure 42. After sweeping through the last diagnosis address the device starts again at the first diagnosis address.

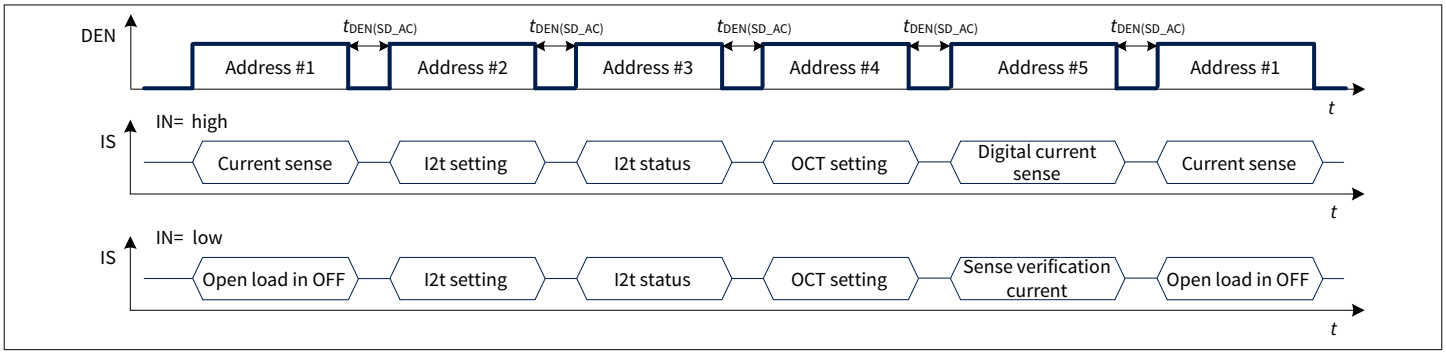



**Figure 42 Sequential diagnosis function**

If the pulse applied at the DEN pin is "low" for a duration longer than the DEN pulse duration for sequential diagnosis timeout $t_{DEN(SD\_TO)}$, the actual diagnosis address is reset (see Figure 43). With the next DEN pin "high" signal the sequential diagnosis starts at the first diagnosis address (depending on the IN pin set to "high" or "low").

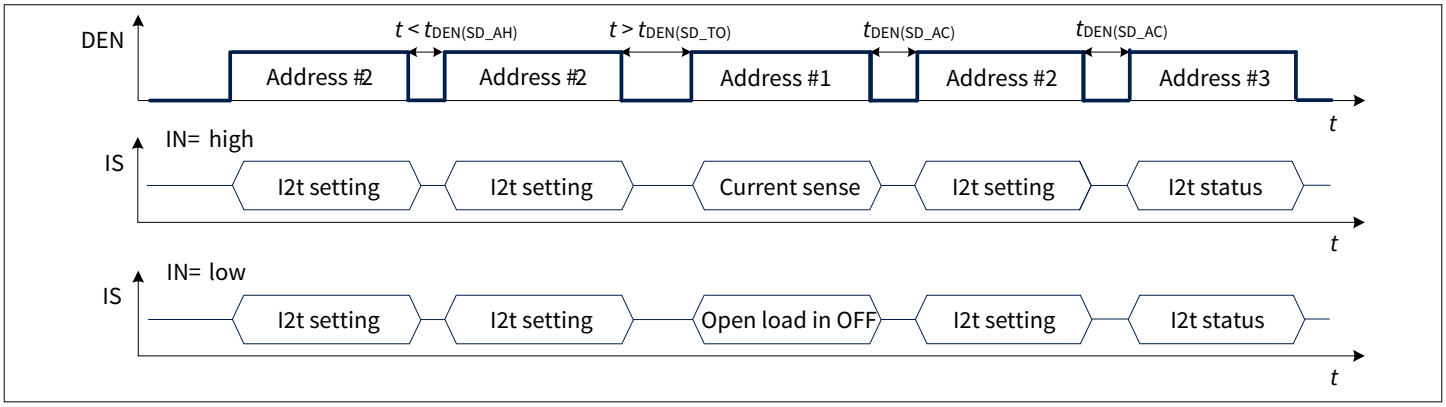



**Figure 43 Sequential diagnosis timing**

The PWM signal ($f_{VIN(CLS)}$ with $DC_{VIN(CLS)}$) which needs to be applied at the input pin in order to enter the CLS mode will be decoded from the diagnosis as IN equal to "high".

The states as well as the corresponding sense currents of the sequential diagnosis function are depicted in Figure 44.

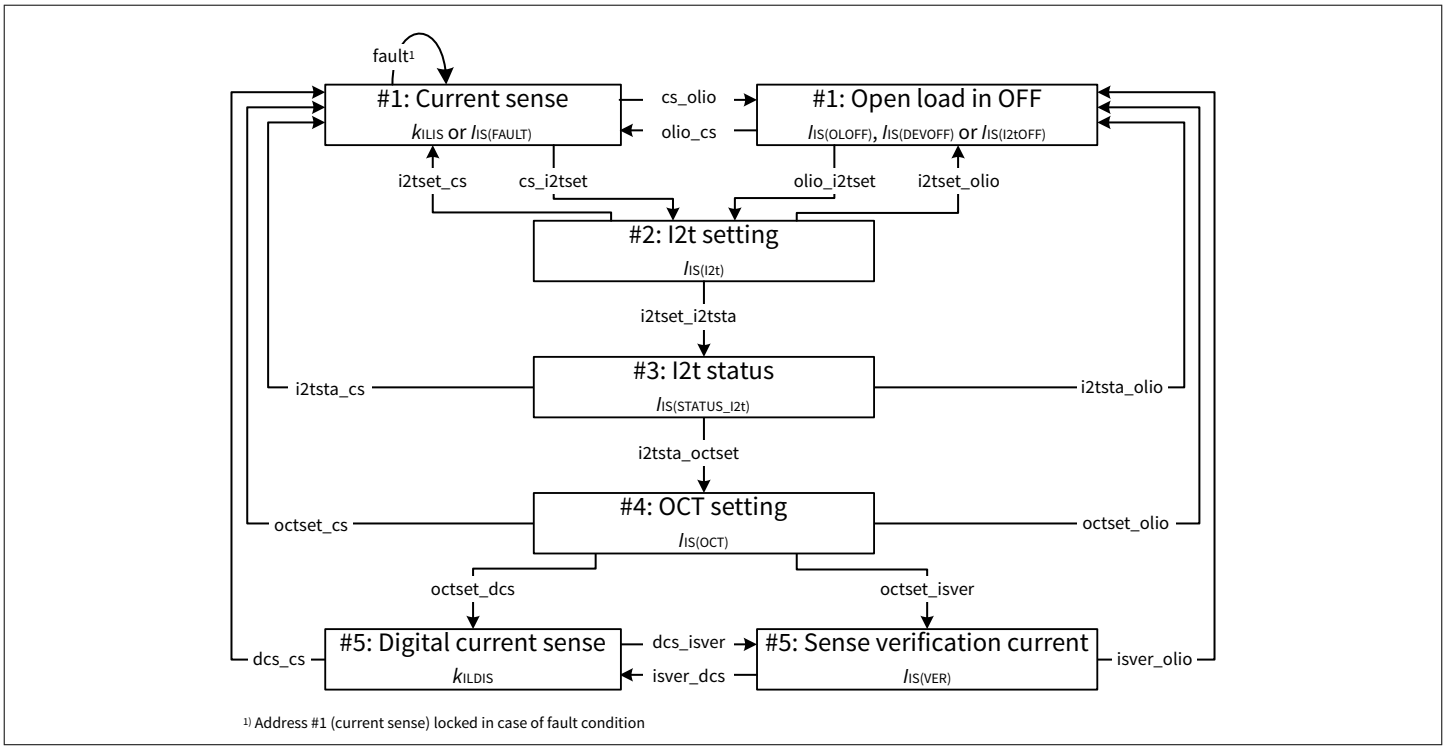



**Figure 44 Sequential diagnosis modes**

A more detailed description of the transitions, including the transition conditions and duration times are provided in the following table.

**Table 16 Transition descriptions**

| Name | Start state | End state | Transition condition | Duration time |
|---|---|---|---|---|
| olio_cs | Open load in OFF | Current sense | IN = "high" [1] | $t_{sIS(DIAG)}$ |
| i2tset_cs | I2t setting | Current sense | (DEN = "low" for $t_{DEN(SD\_TO)}$ OR FAULT) AND IN = "high" [1] | $t_{sIS(ON15)}$ |
| i2tsta_cs | I2t status | Current sense | (DEN = "low" for $t_{DEN(SD\_TO)}$ OR FAULT) AND IN = "high" [1] | $t_{sIS(ON15)}$ |
| octset_cs | OCT setting | Current sense | (DEN = "low" for $t_{DEN(SD\_TO)}$ OR FAULT) AND IN = "high" [1] | $t_{sIS(ON15)}$ |
| dcs_cs | Digital current sense | Current sense | (DEN = "low" for ($t_{DEN(SD\_AC)}$ OR $t_{DEN(SD\_TO)}$) OR FAULT) AND IN = "high" | $t_{sIS(ON15)}$ |
| cs_olio | Current sense | Open load in OFF | IN = "low" | $t_{sIS(ON234)}$ |
| i2tset_olio | I2t setting | Open load in OFF | (DEN = "low" for $t_{DEN(SD\_TO)}$) AND IN = "low" | $t_{sIS(ON234)}$ |

**(table continues...)**

**Table 16 (continued) Transition descriptions**

| Name | Start state | End state | Transition condition | Duration time |
|---|---|---|---|---|
| i2tsta_olio | I2t status | Open load in OFF | (DEN = "low" for $t_{DEN(SD\_TO)}$) AND IN = "low" | $t_{sIS(ON234)}$ |
| octset_olio | OCT setting | Open load in OFF | (DEN = "low" for $t_{DEN(SD\_TO)}$) AND IN = "low" | $t_{sIS(ON234)}$ |
| isver_olio | Sense verification current | Open load in OFF | (DEN = "low" for ($t_{DEN(SD\_AC)}$ OR $t_{DEN(SD\_TO)}$)) AND IN = "low" | $t_{sIS(ON234)}$ |
| cs_i2tset | Current sense | I2t setting | DEN = "low" for $t_{DEN(SD\_AC)}$ | $t_{sIS(ON234)}$ |
| olio_i2tset | Open load in OFF | I2t setting | DEN = "low" for $t_{DEN(SD\_AC)}$ | $t_{sIS(ON234)}$ |
| i2tset_i2tsta | I2t setting | I2t status | DEN = "low" for $t_{DEN(SD\_AC)}$ | $t_{sIS(ON234)}$ |
| i2tsta_octset | I2t status | OCT setting | DEN = "low" for $t_{DEN(SD\_AC)}$ | $t_{sIS(ON234)}$ |
| octset_dcs | OCT setting | Digital current sense | (DEN = "low" for $t_{DEN(SD\_AC)}$) AND IN = "high" [1)] | $t_{sIS(ON15)}$ |
| isver_dcs | Sense verification current | Digital current sense | IN = "high" [1)] | $t_{sIS(DIAG)}$ |
| octset_isver | OCT setting | Sense verification current | (DEN = "low" for $t_{DEN(SD\_AC)}$) AND IN = "low" [1)] | $t_{sIS(ON234)}$ |
| dcs_isver | Digital current sense | Sense verification current | IN = "low" | $t_{sIS(ON234)}$ |

*1)* CLS mode with IN = “pwm“ are decoded as IN = “high“

### 10.1.1 Current sense (address #1 - IN=high)

A current proportional to the load current according to

$$k_{ILIS} = \frac{I_L}{I_{IS}} \quad (9)$$

is provided at IS pin when the following conditions are fulfilled:

- Address #1 and IN = "high"
- The diagnosis (current sense) is enabled with $V_{DS} < V_{DS(OLOFF)}$
- No fault (as described in Chapter 8.3) is present or was latched (see Figure 46 for further details)

A fault current $I_{IS(FAULT)}$ is provided at the IS pin when a fault is present or was latched.

The accuracy of the sense current $I_{IS}$ depends on the load current $I_L$. The sense current $I_{IS}$ increases linearly with $I_L$ output current until it reaches the saturation current $I_{IS(SAT)}$. In case of open load at the output stage ($I_L$ close to 0 A), the maximum sense current $I_{IS(EN)}$ (no load, diagnosis enabled) is specified. This condition is shown in Figure 45. The blue line represents the ideal $k_{ILIS}$ line, while the red lines show the behavior of a typical product.

An external RC filter between IS pin and microcontroller ADC input pin is recommended to reduce the signal ripple and oscillations (a minimum time constant of 1 µs for the RC filter is recommended).

The $k_{ILIS}$ factor is specified with limits that take into account effects due to temperature, supply voltage and manufacturing process. Tighter limits are possible (within a defined current window) with calibration:

- A well-defined and precise current ($I_{L(CAL)}$) is applied at the output during end-of-line test at customer side
- The corresponding current at IS pin is measured and the $k_{ILIS}$ is calculated ($k_{ILIS}$ @ $I_{L(CAL)}$)
- Within the current range going to $I_{L(CAL)\_L}$ to $I_{L(CAL)\_H}$ the $k_{ILIS}$ is equal to $k_{ILIS}$ @ $I_{L(CAL)}$ with limits defined by $\Delta k_{ILIS}$

The derating of $k_{ILIS}$ after calibration is specified by $\Delta k_{ILIS}$, calculated using the following formulas:

$$\Delta k_{ILIS,MAX} = 100 \cdot MAX\left(\frac{k_{ILIS} @ I_{L(CAL)\_L}}{k_{ILIS} @ I_{L(CAL)}} - 1, \frac{k_{ILIS} @ I_{L(CAL)\_H}}{k_{ILIS} @ I_{L(CAL)}} - 1\right) \quad (10)$$

$$\Delta k_{ILIS,MIN} = 100 \cdot MIN\left(\frac{k_{ILIS} @ I_{L(CAL)\_L}}{k_{ILIS} @ I_{L(CAL)}} - 1, \frac{k_{ILIS} @ I_{L(CAL)\_H}}{k_{ILIS} @ I_{L(CAL)}} - 1\right)$$

The calibration is intended to be performed at $T_{A(CAL)}$ = 25°C. The parameter $\Delta k_{ILIS}$ includes the drift over temperature as well as the drift over the current range from $I_{L(CAL)\_L}$ to $I_{L(CAL)\_H}$.

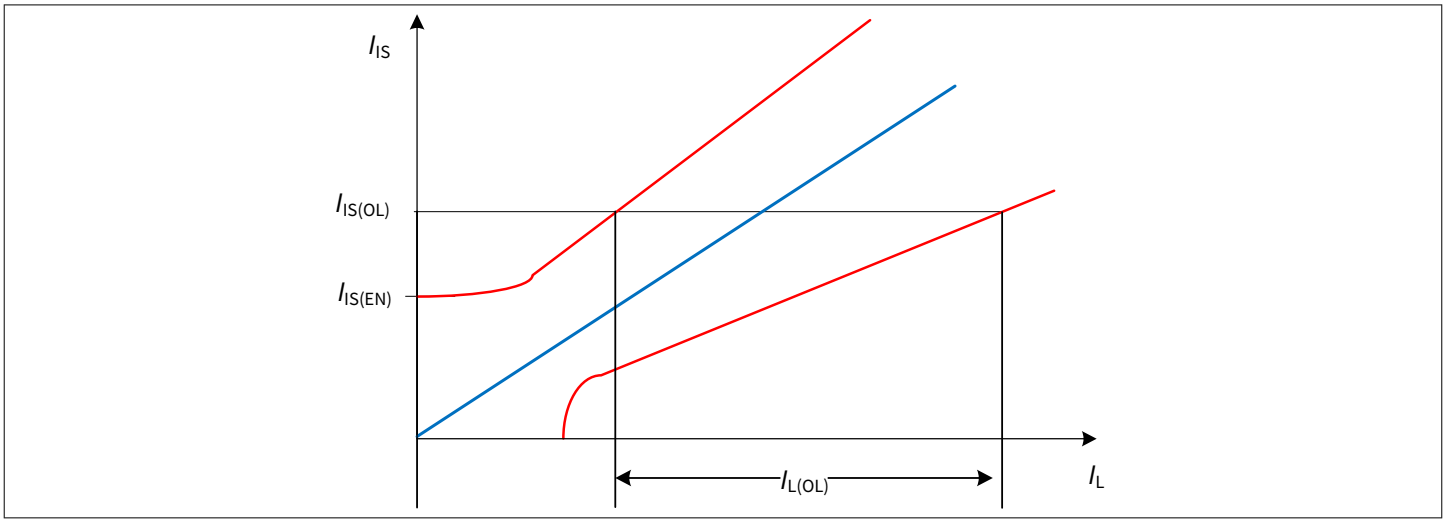



**Figure 45 Current sense ratio in open load at ON condition**

As soon as a protection event occurs the device is switched OFF and a fault current $I_{IS(FAULT)}$ is provided by the IS pin if DEN is set to high (see Chapter 8.3 for more details). In fault condition the current $I_{IS(FAULT)}$ is provided each time the device diagnosis is activated by DEN = "high".

Figure 46 shows the relation between $I_{IS} = I_L / k_{ILIS}$, $I_{IS(SAT)}$ and $I_{IS(FAULT)}$.

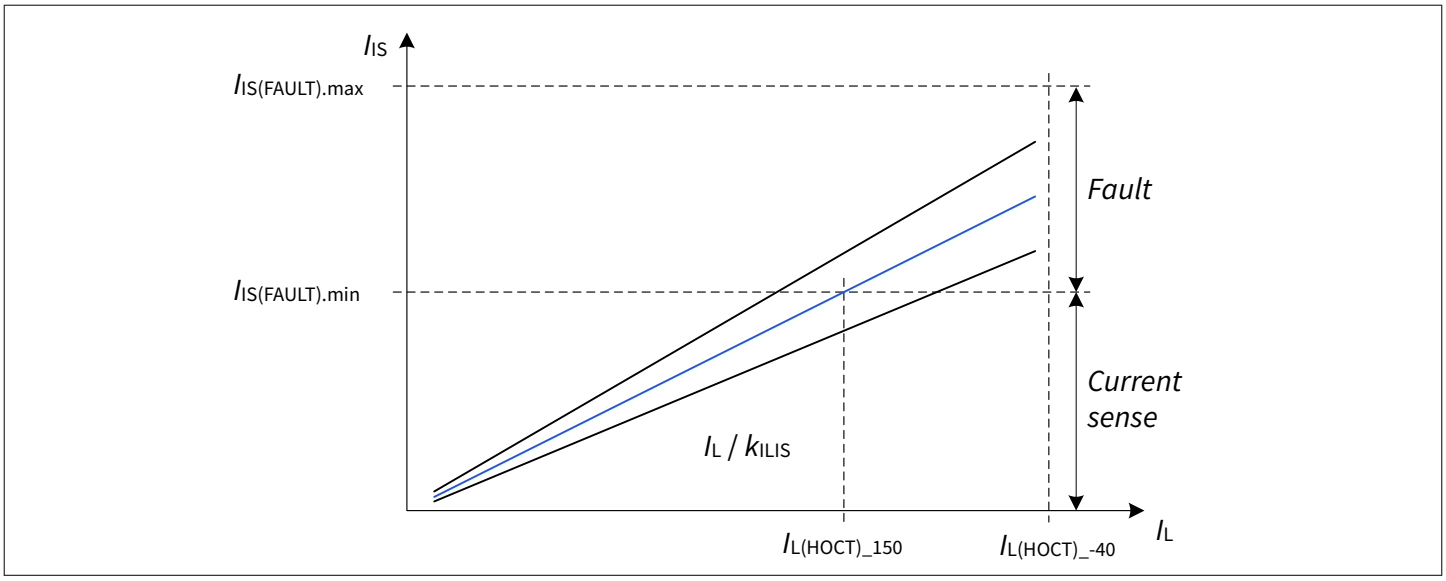



**Figure 46 Current sense behavior - overview**

## 10.1.2 Open load in OFF (address #1 - IN = low)

When the input signal is "low" and the address #1 is selected, the device will measure the drain-source voltage and compare it with the open load $V_{DS}$ detection threshold in OFF state $V_{DS(OLOFF)}$. By the use of external components (see Figure 54), it is possible to detect if the load is missing or if there is a short circuit to battery.

If a fault condition was detected by the device either the device protection fault current $I_{IS(DEVOFF)}$ or the I2t protection fault current $I_{IS(I2tOFF)}$ is provided by the IS pin each time the channel diagnosis is checked in OFF state. See Figure 47 for further details.

In OFF state, when DEN pin is set to “high” the $V_{DS}$ voltage is compared with a threshold voltage $V_{DS(OLOFF)}$. If the load is properly connected and there is no short circuit to battery, $V_{DS} \sim V_S$ therefore $V_{DS} > V_{DS(OLOFF)}$. When the diagnosis is active and $V_{DS} \leq V_{DS(OLOFF)}$, a current $I_{IS(OLOFF)}$ is provided by IS pin. Figure 47 shows the relationship between $I_{IS(OLOFF)}$, $I_{IS(DEVOFF)}$ and $I_{IS(I2tOFF)}$ as functions of $V_{DS}$. By the fact that the three currents do not overlap, it is always possible to differentiate between open load in OFF, I2t protection and device protection triggered. Furthermore, the first and highest prioritization has the I2t protection fault current $I_{IS(I2tOFF)}$, second has the device protection fault current $I_{IS(DEVOFF)}$ and third has the open load in OFF current $I_{IS(OLOFF)}$.

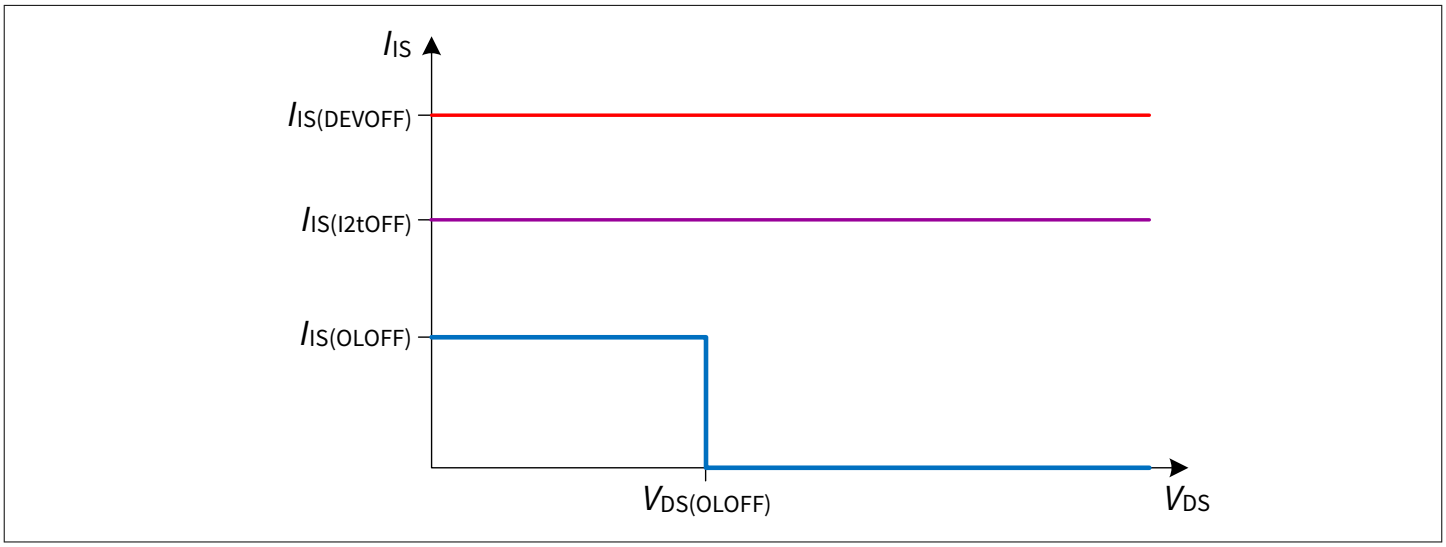



**Figure 47 $I_{IS}$ in OFF state**

It is necessary to wait a time $t_{IS(OLOFF)\_D}$ between the falling edge of the input pin and the sensing at IS pin for open load in OFF diagnosis to allow the internal comparator to settle. In Figure 48 the timings for an open load detection are shown - the load is always disconnected.

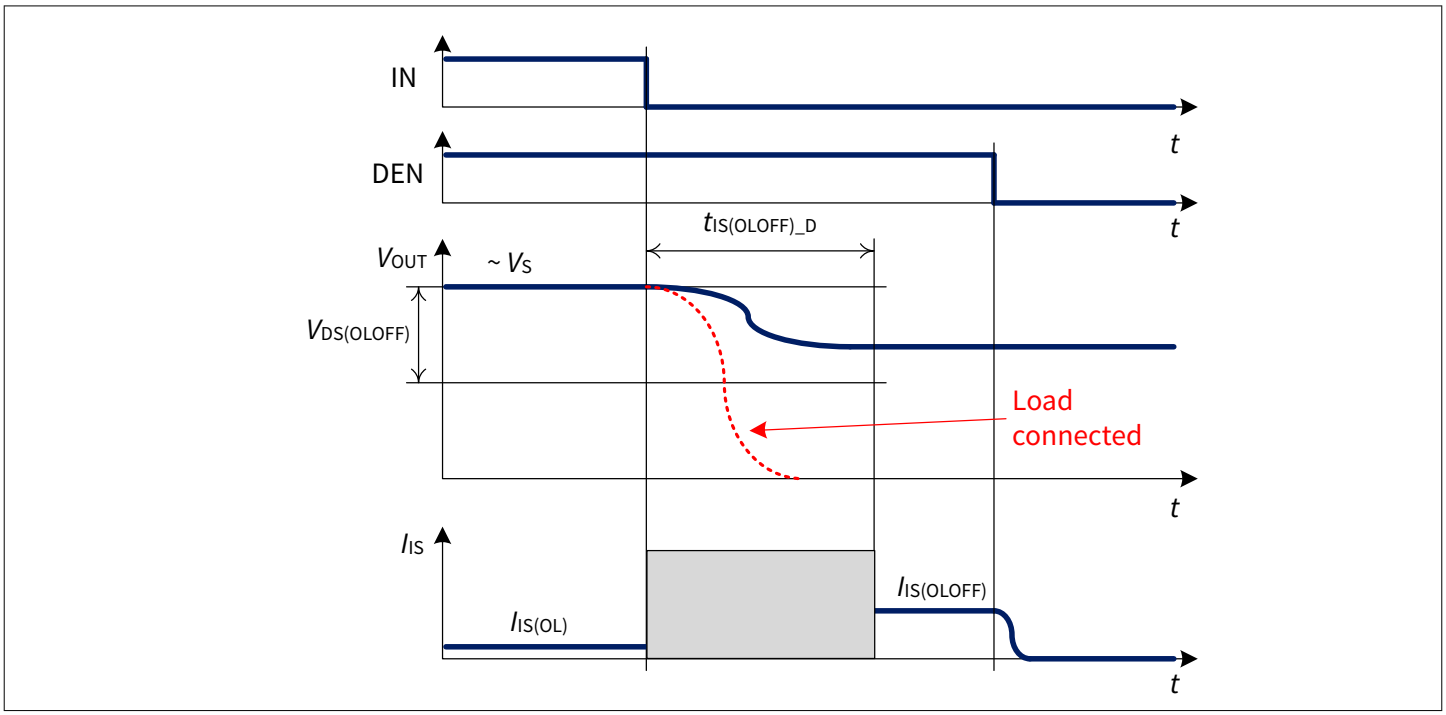



**Figure 48 Open load in OFF timings - load disconnected**

### 10.1.3 I2t setting (address #2 - IN = x)

The device provides for each I2t protection curve setting a corresponding sense current $I_{IS(I2t\_x)}$ at the IS pin in case of setting the sequential diagnosis mode to address #2. The I2t settings are set by the resistor at the I2t pin (see Figure 49).

The device offers an open and short detection of the I2t pin at the IS pin. In this case a pin short current $I_{IS(I2t\_SHORT)}$ or a pin open current $I_{IS(I2t\_OPEN)}$ will be distributed during the diagnosis of the I2t setting.

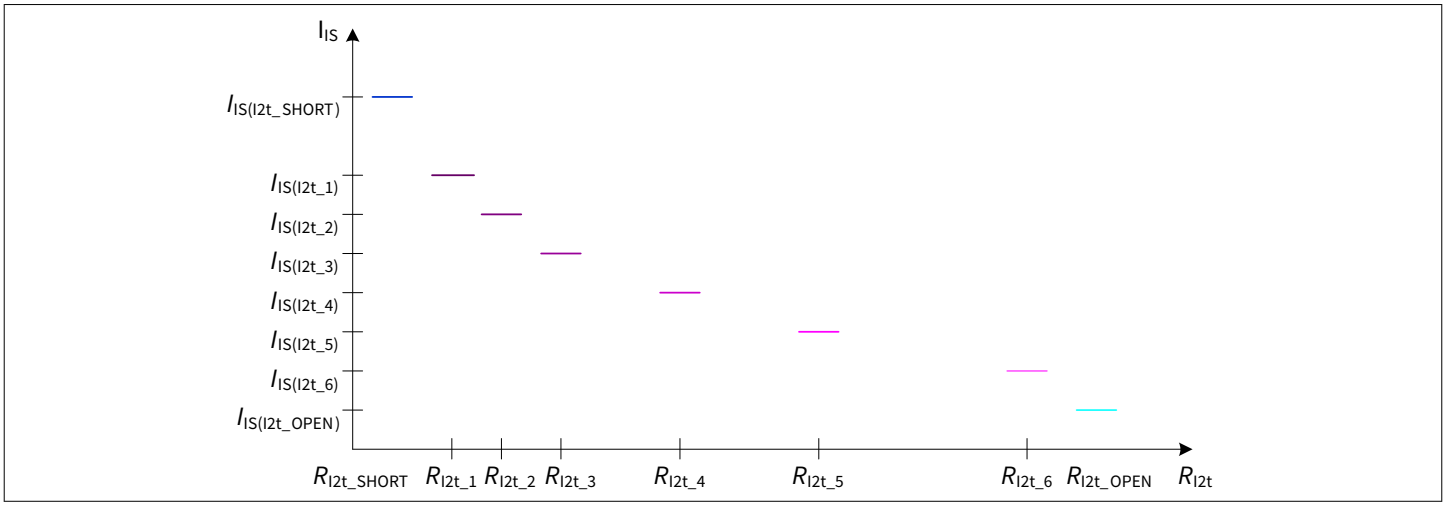



**Figure 49 Diagnosis of I2t setting**

### 10.1.4 I2t status (address #3 - IN = x)

A current proportional to the actual I2t status $S_{I2t\_A}$ according to

$$I_{IS(STATUS\_I2t\_x)} = S_{I2t\_A} \cdot I_{IS(I2t\_x\_100\,\%)} \quad (11)$$

is provided at the IS pin depending on the selected I2t protection curve (see Figure 50). When the I2t protection curve status has reached 100% the $I_{IS(STATUS\_I2t\_x)}$ is equal to $I_{IS(I2t\_x\_100\%)}$.

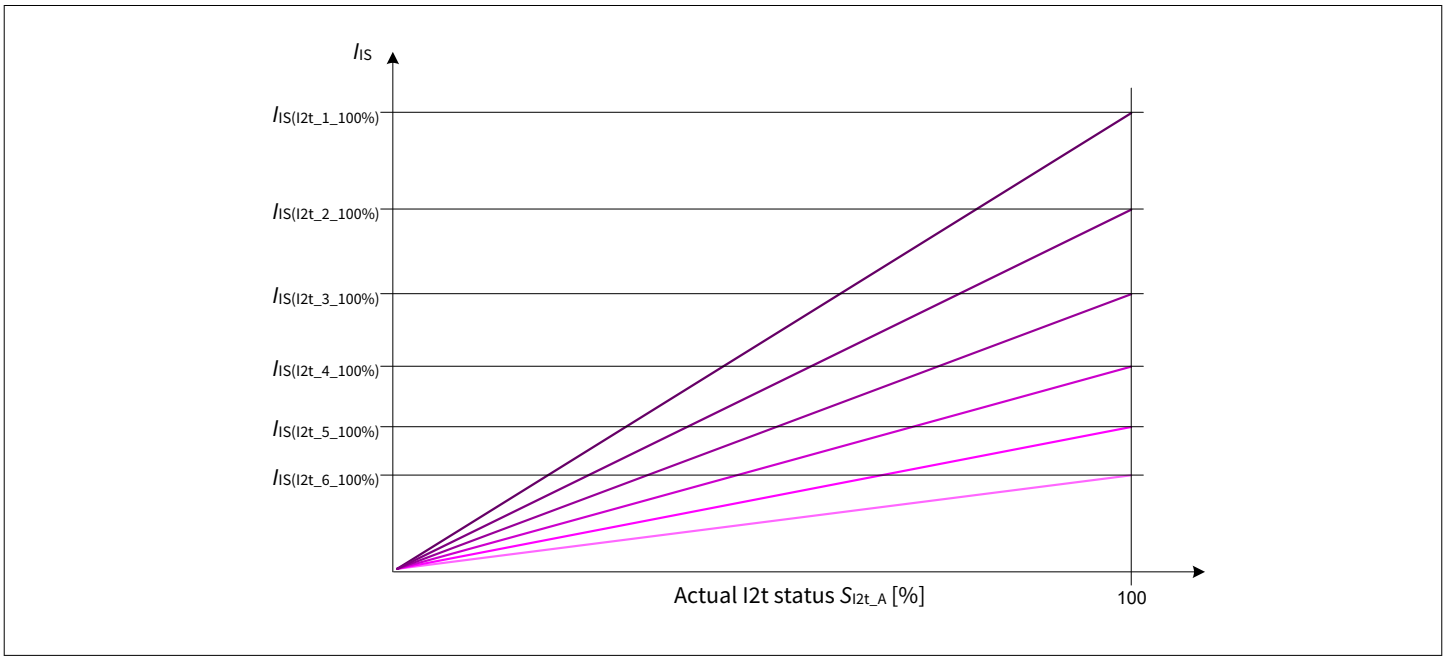



**Figure 50 Diagnosis of I2t status calculation**

### 10.1.5 OCT setting (address #4 - IN = x)

A current according to

$$I_{IS(OCT)}\ [A] = 54.5 \cdot I_{OCT}\ [A] \quad (12)$$

is provided at the IS pin depending on the selected OCT setting during readout of sequential diagnosis address #4 (see Figure 51). The $I_{OCT}$ range is limited by $I_{OCT,MAX}$ and $I_{OCT,MIN}$ for highest and and lowest configurable overcurrent threshold respectively.

The device offers an open and short detection of the OCT pin at the IS pin. In this case a pin short current $I_{IS(OCT\_SHORT)}$ or a pin open current $I_{IS(OCT\_OPEN)}$ will be distributed during the diagnosis of the OCT setting.

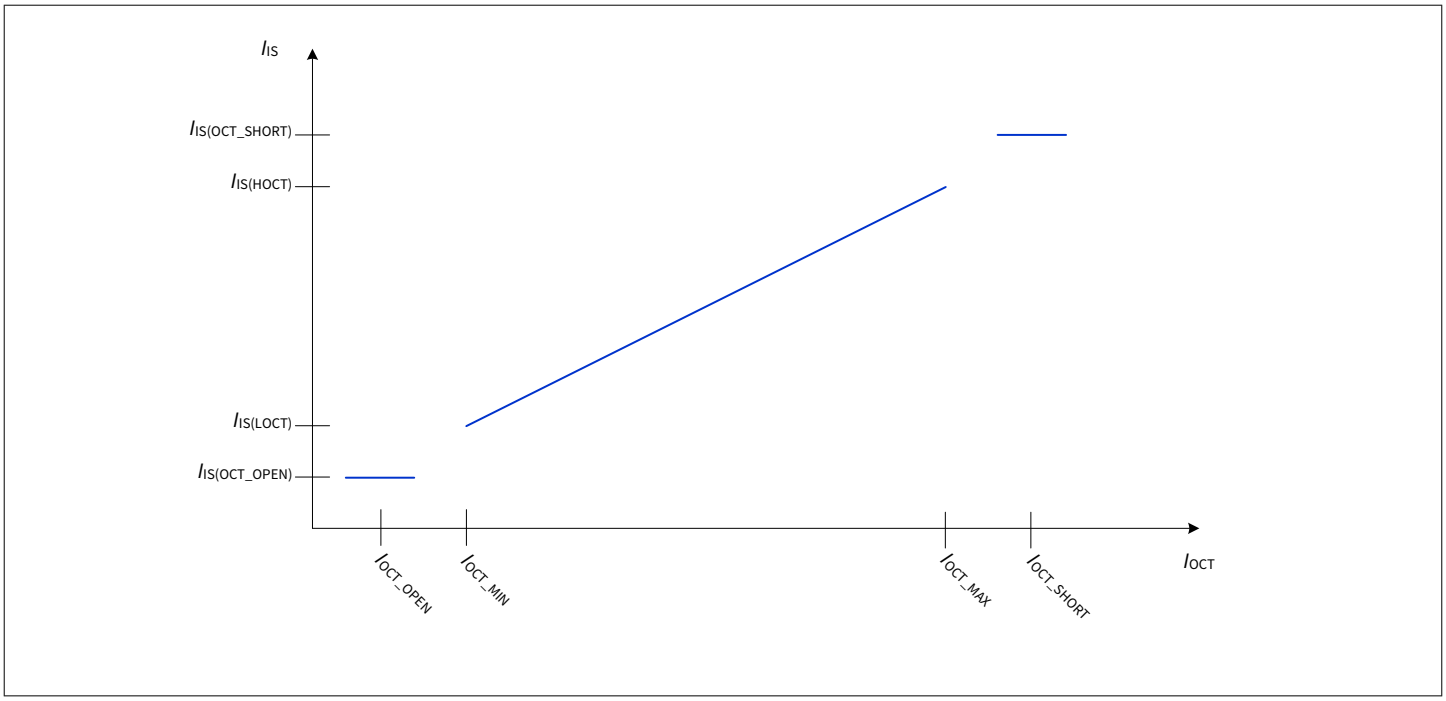



**Figure 51 Diagnosis of overcurrent threshold setting**

### 10.1.6 Digital current sense (address #5 - IN = high)

A current proportional to the load current according to

$$k_{ILDIS} = \frac{I_L}{I_{DIS}} \quad (13)$$

is provided at IS pin when the following conditions are fulfilled:

- Address #5 and IN = "high"
- The diagnosis (current sense) is enabled with $V_{DS} < V_{DS(OLOFF)}$
- No fault (as described in Chapter 8.3) is present or was latched (see Figure 46 for further details)

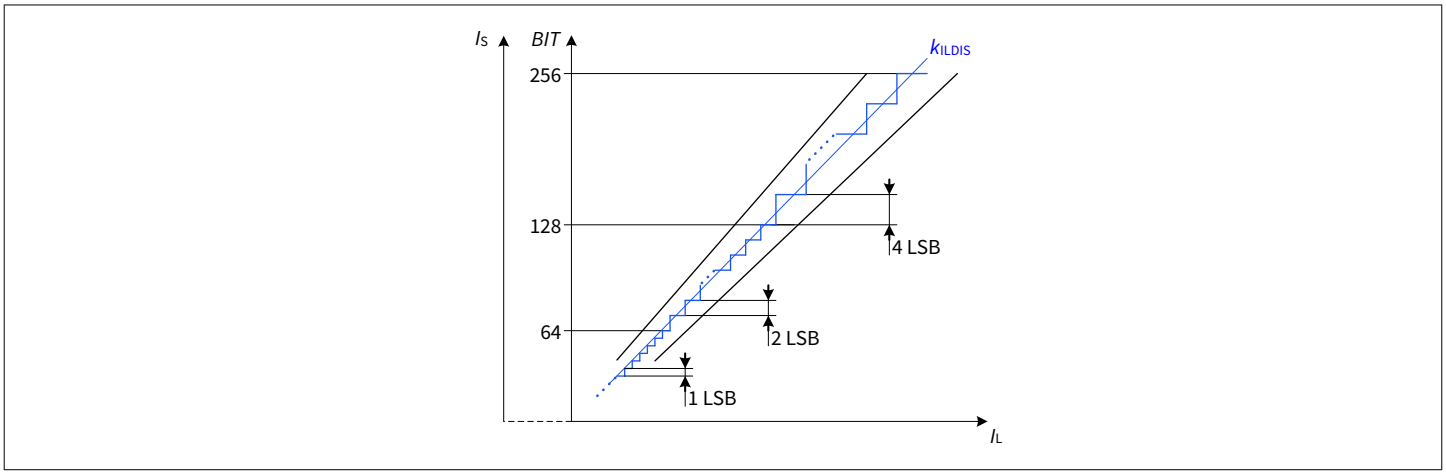



**Figure 52 Digital current sense behavior - overview**

The digital current sense settling time for an infinite fast current ramp is determined by:

$$t_{DIS\_SET} = \begin{cases} I_L \leq 64 \cdot LSB, & \frac{I_L}{LSB} \cdot t_{CON} \\ 65 \cdot LSB < I_L \leq 128 \cdot LSB, & \left(64 + \frac{I_L - 64 \cdot LSB}{2LSB}\right) \cdot t_{CON} \\ 129 \cdot LSB < I_L \leq 256 \cdot LSB, & \left(96 + \frac{I_L - 128 \cdot LSB}{4LSB}\right) \cdot t_{CON} \end{cases} \quad (14)$$

### 10.1.7 Sense verification current (address #5 - IN = low)

To verify the function of the current sensing path in OFF state, the device offers a sense verification adress. In this mode a predefined current $I_{IS(VER)}$ is provided at the current sense pin independent of the load condition.

## 10.2 SENSE timings

Figure 53 shows the timing during settling $t_{sIS(ON)}$ and disabling $t_{sIS(OFF)}$ of the SENSE (including the case of load change). As a proper signal cannot be established before the load current is stable (therefore before $t_{ON}$), the SENSE settling time after start-up is defined by $t_{sIS(DIAG)}$.

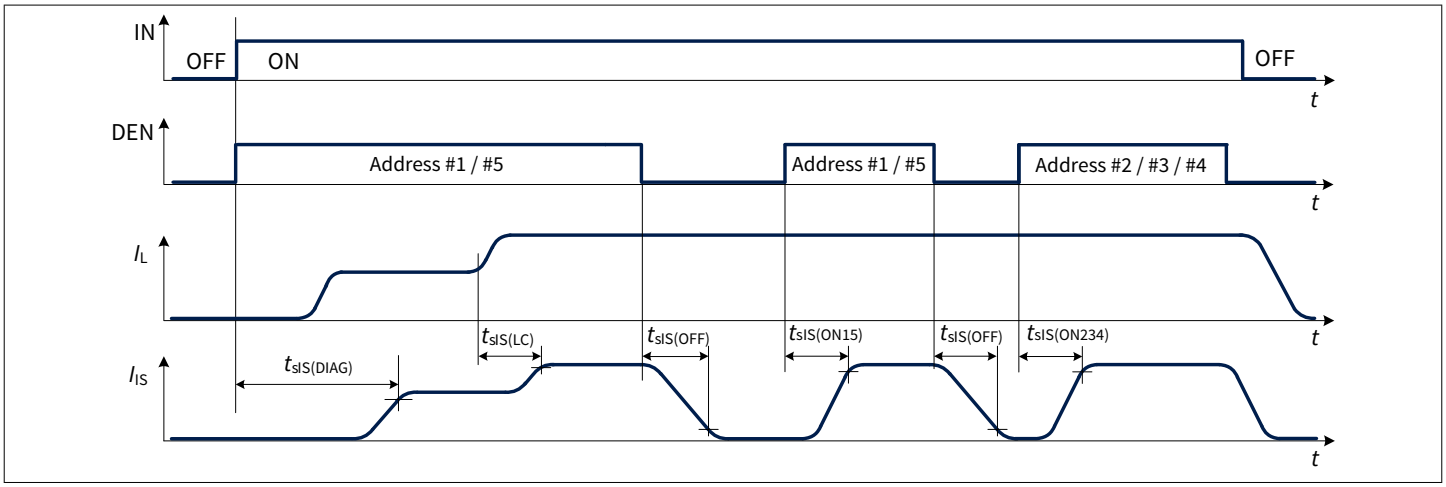



**Figure 53 SENSE settling/disabling timing**

## 10.3 Electrical characteristics diagnosis

**Table 17 Electrical characteristics diagnosis**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| SENSE fault current | $I_{IS(FAULT)}$ | 4.4 | 5.5 | 10 | mA | IN = "high"<br>Device or I2t protection triggered<br>Address #1<br>$V_S$ = 6 V | PRQ-287 |
| Device protection fault current | $I_{IS(DEVOFF)}$ | 4.4 | 6.1 | 10 | mA | IN = "low"<br>Device protection triggered<br>Address #1<br>$V_S$ = 6 V | PRQ-893 |
| I2t protection fault current | $I_{IS(I2tOFF)}$ | 2.56 | 3.20 | 3.84 | mA | 1)<br>IN = "low"<br>I2t protection triggered<br>Address #1 | PRQ-631 |
| SENSE open load in OFF current | $I_{IS(OLOFF)}$ | 0.8 | 1.15 | 1.5 | mA | IN = "low"<br>Address #1 | PRQ-288 |
| Sense verification current | $I_{IS(VER)}$ | 400 | 500 | 600 | µA | IN = "low"<br>Address #5 | PRQ-1333 |
| SENSE open load in OFF delay time (from ON to OFF) | $t_{IS(OLOFF)\_D}$ | – | 5 | 20 | µs | $V_{DS} < V_{OL(OFF)}$<br>from IN falling edge to $V_{IS} = R_{SENSE} \cdot 0.9 \cdot I_{IS(OLOFF),MIN}$<br>DEN = “high”<br>Address #1 | PRQ-290 |
| Open load VDS detection threshold in OFF state | $V_{DS(OLOFF)}$ | 1.3 | 1.8 | 2.3 | V | IN="low"<br>Address #1 | PRQ-292 |
| SENSE settling time with nominal load current stable | $t_{sIS(ON15)}$ | – | 5 | 40 | µs | $I_L = I_{L(NOM)\_85}$<br>DEN from “low” to “high”<br>IN = "high"<br>Address #1, #5 | PRQ-293 |

**(table continues...)**

**Table 17 (continued) Electrical characteristics diagnosis**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| SENSE settling time with nominal load current stable after startup | $t_{sIS(DIAG)}$ | – | 400 | 750 | µs | 1)<br>$I_L = I_{L(NOM)\_85}$ IN, DEN from “low” to “high”<br>Address #1, #5 | PRQ-276 |
| SENSE settling time for sequential diagnosis | $t_{sIS(ON234)}$ | – | 5 | 20 | µs | 1)<br>DEN from “low” to “high”<br>IN = "high"<br>Address #2, #3, #4<br>IN = "low"<br>Address #1, #2, #3, #4, #5 | PRQ-1201 |
| SENSE disable time | $t_{sIS(OFF)}$ | – | 5 | 20 | µs | 1)<br>From DEN falling edge to $I_{IS} = I_{IS(OFF)}$<br>See Figure 53<br>IN="high"<br>Address #1 | PRQ-295 |
| SENSE settling time after load change | $t_{sIS(LC)}$ | – | 5 | 20 | µs | 1)<br>From 10% $I_{L(NOM)\_85}$ to $I_{L(NOM)\_85}$<br>See Figure 53<br>IN="high"<br>Address #1 | PRQ-296 |
| Load jump duration in Address 5 | $t_{sIS(LC\_Address5)}$ | 19 | 25 | 31 | µs | 1)<br>From 10% $I_{L(NOM)\_85}$ to $I_{L(NOM)\_85}$*x for x=1,2,3,4.<br>See Figure 53<br>IN="high"<br>Address #5 | PRQ-1488 |
| Digital SENSE conversion time | $t_{CON}$ | 720 | 800 | 880 | ns | 1) | PRQ-1455 |

**(table continues...)**

**Table 17 (continued) Electrical characteristics diagnosis**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| DEN pulse duration for sequential diagnosis address change | $t_{DEN(SD\_AC)}$ | 25 | 50 | 75 | µs | 1) | PRQ-610 |
| DEN pulse duration for sequential diagnosis timeout | $t_{DEN(SD\_TO)}$ | 150 | – | – | µs | 1) | PRQ-937 |
| DEN pulse duration for sequential diagnosis address hold | $t_{DEN(SD\_AH)}$ | 0 | 5 | 10 | µs | 1) | PRQ-1468 |

1) Not subject to production test - specified by design.

**Table 18 Electrical characteristics diagnosis**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| SENSE saturation current | $I_{IS(SAT)}$ | 4.4 | – | 15 | mA | 1)<br>$V_{SIS} = V_S - V_{IS} \geq 2$ V<br>See Figure 46 | PRQ-277 |
| SENSE leakage current when disabled | $I_{IS(OFF)}$ | – | 0.01 | 0.5 | µA | DEN = "low"<br>$V_{IS}$ = 0 V | PRQ-279 |
| SENSE leakage current when enabled at TJ ≤ 85°C | $I_{IS(EN)\_85}$ | – | 0.2 | 1 | µA | 1)<br>$T_J \leq 85$°C<br>DEN = "high"<br>$I_L$ = 0 A<br>See Figure 45 | PRQ-280 |
| SENSE leakage current when enabled at TJ = 150°C | $I_{IS(EN)\_150}$ | – | 0.2 | 1 | µA | $T_J$ = 150°C<br>DEN = "high"<br>$I_L$ = 0 A<br>See Figure 45 | PRQ-281 |

**(table continues...)**

**Table 18 (continued) Electrical characteristics diagnosis**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to +150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| Saturation voltage in kILIS operation - (VS - VIS) | $V_{SIS\_k}$ | – | 0.5 | 1 | V | 1)<br>$V_S$ = 5 V<br>IN = DEN = "high"<br>$I_L \le 1.2 * I_{L(NOM)\_85}$ | PRQ-282 |
| Saturation voltage in open load at OFF diagnosis - (VS - VIS) | $V_{SIS\_OL}$ | – | 0.5 | 1 | V | 1)<br>$V_S$ = 5 V<br>$I_{IS} = I_{IS(OLOFF)\_Min}$<br>IN = "low"<br>DEN = "high" | PRQ-283 |
| Saturation voltage in fault diagnosis - (VS - VIS) | $V_{SIS\_F}$ | – | 0.5 | 1 | V | 1)<br>$V_S$ = 5 V<br>$I_{IS} = I_{IS(FAULT)\_Min}$<br>IN = "low"<br>DEN = "high"<br>latch ≠ 0<br>-40°C < $T_J \le$ 150°C | PRQ-284 |
| Saturation voltage in sequential diagnosis - (VS - VIS) | $V_{SIS\_SD}$ | – | 0.5 | 1 | V | 1)<br>$V_S$ = 5 V<br>IN = DEN = "high"<br>Address #2: $R_{I2t}$ = 10 kΩ<br>Address #3: $I_{IS(I2t\_1\_100\%)}$<br>Address #4: $I_{OCT}$ = 50 µA<br>Address #5: $I_L \le 1.2 * I_{L(NOM)\_85}$ | PRQ-1453 |
| Power supply to IS pin clamping voltage at TJ = -40°C | $V_{SIS(CLAMP)\_-40}$ | 33 | 36.5 | 42 | V | $I_{IS}$ = 1 mA<br>$T_J$ = -40°C<br>See Figure 20 | PRQ-285 |
| Power supply to IS pin clamping voltage at TJ ≥ 25°C | $V_{SIS(CLAMP)\_25}$ | 35 | 38 | 44 | V | 2)<br>$I_{IS}$ = 1 mA<br>$T_J \ge$ 25°C<br>See Figure 20 | PRQ-286 |

1) Not subject to production test - specified by design.
2) Tested at $T_J$ = 150°C.

### 10.3.1 Electrical characteristics diagnosis - power output stages

**Table 19 Diagnosis power output stage**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to 150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Open load output current** | | | | | | | |
| Open load output current at IIS = 4 µA | $I_{L(OL)\_4u}$ | 10 | 67 | 124 | mA | IN = "high"<br>Address #1<br>$I_{IS} = I_{IS(OL)}$ = 4 µA | PRQ-1042 |
| **Current sense ratio** | | | | | | | |
| Current sense ratio at - IL = IL02 | $k_{ILIS02}$ | -85% | 16750 | +85% | – | $I_{L02}$ = 60 mA<br>IN = "high"<br>Address #1 | PRQ-1043 |
| Current sense ratio at - IL = IL07 | $k_{ILIS07}$ | -30% | 13900 | +30% | – | $I_{L07}$ = 300 mA<br>IN = "high"<br>Address #1 | PRQ-1044 |
| Current sense ratio at - IL = IL08 | $k_{ILIS08}$ | -20% | 13900 | +20% | – | $I_{L08}$ = 500 mA<br>IN = "high"<br>Address #1 | PRQ-1045 |
| Current sense ratio at - IL = IL12 | $k_{ILIS12}$ | -15% | 13900 | +15% | – | $I_{L12}$ = 3 A<br>IN = "high"<br>Address #1 | PRQ-1046 |
| Current sense ratio at - IL = IL13 | $k_{ILIS13}$ | -8% | 13900 | +8% | – | $I_{L13}$ = 5 A<br>IN = "high"<br>Address #1 | PRQ-1047 |
| Current sense ratio at - IL = IL15 | $k_{ILIS15}$ | -8% | 13900 | +8% | – | $I_{L15}$ = 10 A<br>IN = "high"<br>Address #1 | PRQ-1048 |
| Current sense ratio at - IL = IL16 | $k_{ILIS16}$ | -8% | 13900 | +8% | – | *1)*<br>$I_{L16}$ = 15 A<br>IN = "high"<br>Address #1 | PRQ-1049 |

**(table continues...)**

**Table 19 (continued) Diagnosis power output stage**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to 150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **SENSE current derating** | | | | | | | |
| SENSE current derating with nominal current calibration | $\Delta k_{ILIS(NOM)}$ | -4 | 0 | 4 | % | 1)<br>$I_{L(CAL)} = I_{L15}$<br>$I_{L(CAL)\_H} = I_{L16}$<br>$I_{L(CAL)\_L} = I_{L13}$<br>$T_{A(CAL)}$ = 25°C | PRQ-1192 |
| **I2t setting** | | | | | | | |
| Diagnosis of I2t pin short | $I_{IS(I2t\_SHORT)}$ | 3.40 | 3.68 | 3.97 | mA | Address #2<br>$V_S$ = 6 V<br>$R_{I2t} = R_{I2t\_SHORT}$<br>See Figure 49 | PRQ-613 |
| Diagnosis of I2t_1 setting | $I_{IS(I2t\_1)}$ | 2.57 | 2.83 | 3.09 | mA | Address #2<br>$R_{I2t} = R_{I2t\_1}$<br>See Figure 49 | PRQ-614 |
| Diagnosis of I2t_2 setting | $I_{IS(I2t\_2)}$ | 1.95 | 2.14 | 2.33 | mA | Address #2<br>$R_{I2t} = R_{I2t\_2}$<br>See Figure 49 | PRQ-615 |
| Diagnosis of I2t_3 setting | $I_{IS(I2t\_3)}$ | 1.43 | 1.58 | 1.74 | mA | Address #2<br>$R_{I2t} = R_{I2t\_3}$<br>See Figure 49 | PRQ-616 |
| Diagnosis of I2t_4 setting | $I_{IS(I2t\_4)}$ | 1.01 | 1.13 | 1.26 | mA | Address #2<br>$R_{I2t} = R_{I2t\_4}$<br>See Figure 49 | PRQ-617 |
| Diagnosis of I2t_5 setting | $I_{IS(I2t\_5)}$ | 0.70 | 0.78 | 0.87 | mA | Address #2<br>$R_{I2t} = R_{I2t\_5}$<br>See Figure 49 | PRQ-618 |
| Diagnosis of I2t_6 setting | $I_{IS(I2t\_6)}$ | 0.39 | 0.47 | 0.55 | mA | Address #2<br>$R_{I2t} = R_{I2t\_6}$<br>See Figure 49 | PRQ-619 |
| Diagnosis of I2t pin open | $I_{IS(I2t\_OPEN)}$ | 0.08 | 0.15 | 0.21 | mA | Address #2<br>$R_{I2t} = R_{I2t\_OPEN}$<br>See Figure 49 | PRQ-620 |

**(table continues...)**

**Table 19 (continued) Diagnosis power output stage**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to 150°C
Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C
Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **I2t status** | | | | | | | |
| 100% Status of I2t_1 | $I_{IS(I2t\_1\_100\%)}$ | 3.02 | 3.48 | 3.93 | mA | 1)<br>Address #3<br>See Figure 50 | PRQ-1381 |
| 100% Status of I2t_2 | $I_{IS(I2t\_2\_100\%)}$ | 2.47 | 2.84 | 3.22 | mA | 1)<br>Address #3<br>See Figure 50 | PRQ-1387 |
| 100% Status of I2t_3 | $I_{IS(I2t\_3\_100\%)}$ | 1.96 | 2.26 | 2.55 | mA | 1)<br>Address #3<br>See Figure 50 | PRQ-1391 |
| 100% Status of I2t_4 | $I_{IS(I2t\_4\_100\%)}$ | 1.59 | 1.84 | 2.08 | mA | 1)<br>Address #3<br>See Figure 50 | PRQ-1392 |
| 100% Status of I2t_5 | $I_{IS(I2t\_5\_100\%)}$ | 1.30 | 1.50 | 1.70 | mA | 1)<br>Address #3<br>See Figure 50 | PRQ-1393 |
| 100% Status of I2t_6 | $I_{IS(I2t\_6\_100\%)}$ | 1.04 | 1.20 | 1.36 | mA | 1)<br>Address #3<br>See Figure 50 | PRQ-1394 |
| **OCT setting** | | | | | | | |
| Diagnosis of OCT pin short | $I_{IS(OCT\_SHORT)}$ | 3.33 | 3.64 | 3.94 | mA | Address #4<br>$V_S$ = 6 V<br>$I_{OCT}$ = 83.3 µA<br>See Figure 51 | PRQ-627 |
| Diagnosis of HOCT setting | $I_{IS(HOCT)}$ | 2.45 | 2.72 | 2.99 | mA | Address #4<br>$I_{OCT}$ = 50 µA<br>See Figure 51 | PRQ-628 |
| Diagnosis of LOCT setting | $I_{IS(LOCT)}$ | 0.33 | 0.43 | 0.52 | mA | Address #4<br>$I_{OCT}$ = 7.5 µA<br>See Figure 51 | PRQ-629 |
| Diagnosis of OCT pin open | $I_{IS(OCT\_OPEN)}$ | 0.08 | 0.15 | 0.21 | mA | Address #4<br>$I_{OCT}$ = 3.8 µA<br>See Figure 51 | PRQ-630 |

**(table continues...)**

**Table 19 (continued) Diagnosis power output stage**

$V_S$ = 5 V to 20 V, $T_J$ = -40°C to 150°C

Unless otherwise specified typical values: $V_S$ = 13.5 V, $T_J$ = 25°C

Typical resistive loads connected to the outputs for testing (unless otherwise specified): $R_L$ = 2.1 Ω

| Parameter | Symbol | Values | | | Unit | Note or condition | P-Number |
|---|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | | |
| **Digital current sense ratio** | | | | | | | |
| LSB for KILDIS conversion | LSB | 236 | 278 | 320 | mA | 1) | PRQ-1457 |
| Digital current sense ratio at - IL = IL12 | $k_{ILDIS12}$ | -20% | 13400 | +20% | – | $I_{L12}$ = 3 A<br>IN = "high"<br>Address #5 | PRQ-1334 |
| Digital current sense ratio at - IL = IL13 | $k_{ILDIS13}$ | -17.5% | 13400 | +17.5 % | – | $I_{L13}$ = 5 A<br>IN = "high"<br>Address #5 | PRQ-1335 |
| Digital current sense ratio at - IL = IL15 | $k_{ILDIS15}$ | -15% | 13400 | +15% | – | $I_{L15}$ = 10 A<br>IN = "high"<br>Address #5 | PRQ-1336 |
| Digital current sense ratio at - IL = IL16 | $k_{ILDIS16}$ | -15% | 13400 | +15% | – | $I_{L16}$ = 15 A<br>IN = "high"<br>Address #5 | PRQ-1337 |

1) Not subject to production test - specified by design.

# 11 Application information

***Note**: The following information is given as a hint for the implementation of the device only and shall not be regarded as a description or warranty of a certain functionality, condition or quality of the device.*

## 11.1 Application setup

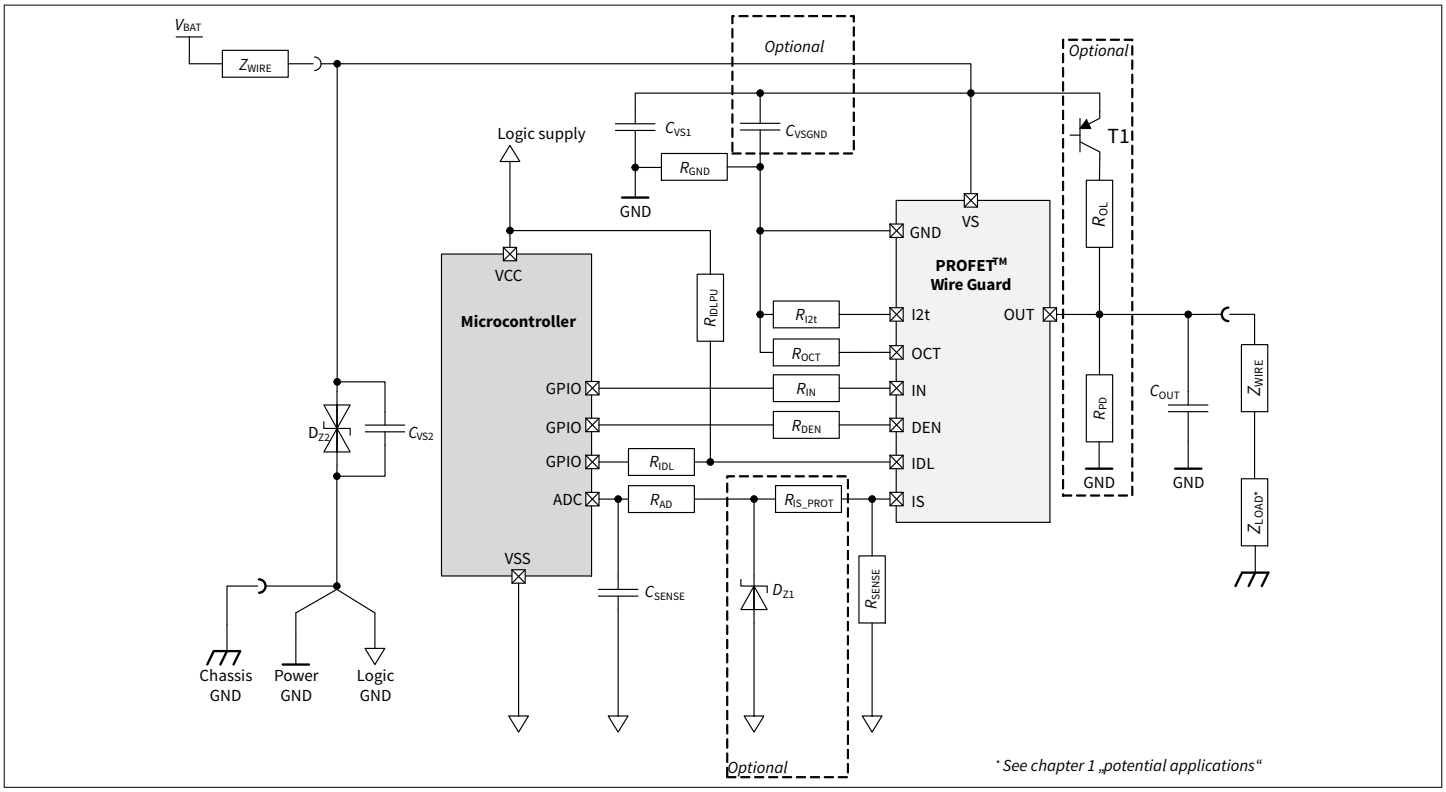



**Figure 54 PROFET™ Wire Guard - application diagram**

***Note**: This is a very simplified example of an application circuit. The function must be verified in the real application.*

## 11.2 External components

| Reference | Value | Purpose |
|---|---|---|
| $R_{IN}$ | 4.7 kΩ | Protection of the microcontroller during overvoltage and reverse polarity.<br>Necessary to switch OFF the device output during loss of ground |
| $R_{DEN}$ | 4.7 kΩ | Protection of the microcontroller during overvoltage and reverse polarity.<br>Necessary to switch OFF the device output during loss of ground |
| $R_{I2t}$ | 10...68 kΩ | Selection of the I2t protection curve.<br>Protection of the device during overvoltage and reverse polarity |
| $R_{OCT}$ | 10...68 kΩ | Selection of the OCT threshold.<br>Protection of the device during overvoltage and reverse polarity |
| $R_{IDL}$ | 4.7 kΩ | Protection of the microcontroller during overvoltage and reverse polarity |
| $R_{IDLPU}$ | 47 kΩ | Pull-up resistor for idle mode diagnosis at microcontroller |

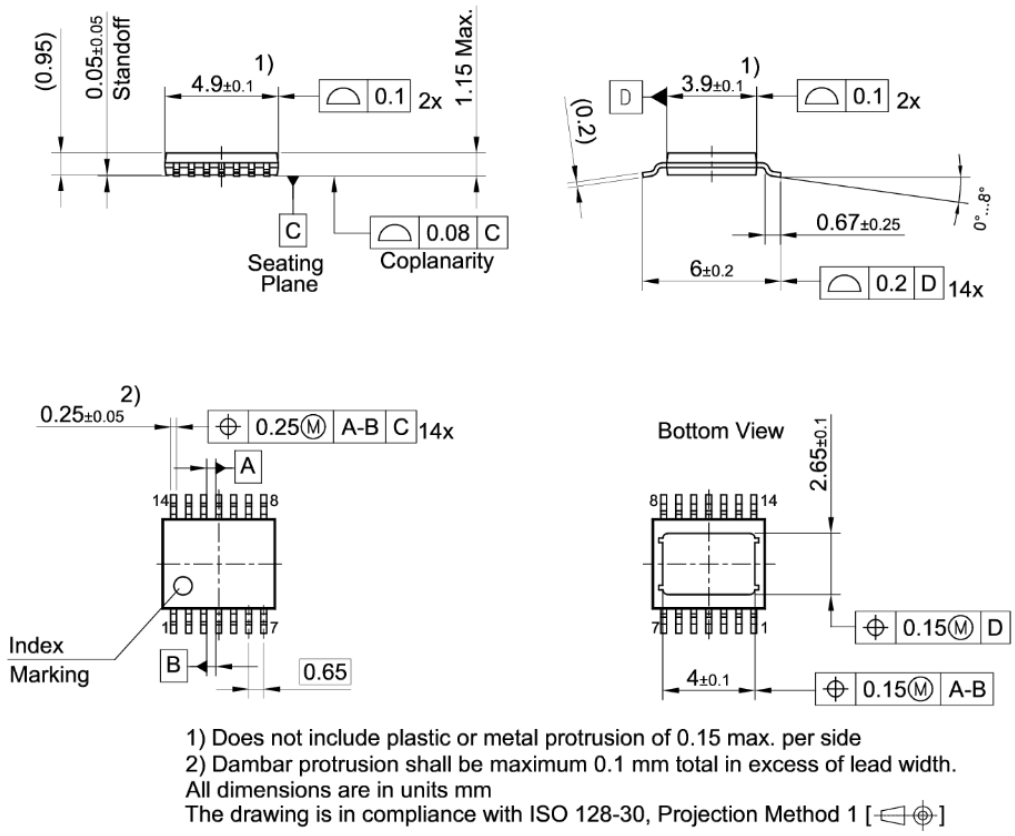
| Reference | Value | Purpose |
|---|---|---|
| $R_{PD}$ | 47 kΩ | Output polarization (pull-down). Ensures polarization of the device output to distinguish between open load and short to $V_S$ in OFF diagnosis |
| $R_{OL}$ | 1.5 kΩ | Output polarization (pull-up). Ensures polarization of the device output during open load in OFF diagnosis |
| $C_{OUT}$ | 10 nF[1)] | Protection of the device output during ESD events and BCI |
| $T_1$ | BC 807 | Switches the battery voltage for open load in OFF diagnosis |
| $C_{VS1}$ | 100 nF | Filtering of voltage spikes on the battery line |
| $C_{VS2}$ | – | Filtering / buffer capacitor located at $V_{BAT}$ connector |
| $C_{VSGND}$ | 22 nF | Buffer capacitor for fast transients.<br>Recommended in case no battery voltage oscillation filter is present |
| $D_{Z2}$ | 33 V Z-Diode | Suppressor diode. Protection during overvoltage and in case of loss of battery while driving an inductive load |
| $R_{SENSE}$ | 1.2 kΩ | SENSE resistor |
| $R_{IS\_PROT}$ | 4.7 kΩ | Protection during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications |
| $D_{Z1}$ | 7 V Z-Diode | Protection of microcontroller during overvoltage |
| $R_{AD}$ | 4.7 kΩ | Protection of microcontroller ADC input during overvoltage, reverse polarity, loss of ground. Value to be tuned according to microcontroller specifications |
| $C_{SENSE}$ | 220 pF | Sense signal filtering. A time constant ($R_{AD}$ + $R_{IS\_PROT}$) * $C_{SENSE}$ longer than 1 µs is recommended |
| $R_{GND}$ | 47 Ω | Protection in case of overvoltage and loss of battery while driving inductive loads |

*1)* In case the CLS mode is used, a $C_{OUT}$ of 100 nF is recommended to additionally improve the EMC performance.

## 11.3 Further application information

- Please contact us for information regarding the pin behavior assessment
- For further information you may contact http://www.infineon.com/

# 12 Package outlines




1) Does not include plastic or metal protrusion of 0.15 max. per side
2) Dambar protrusion shall be maximum 0.1 mm total in excess of lead width.
All dimensions are in units mm
The drawing is in compliance with ISO 128-30, Projection Method 1 [⊕]

**Figure 55 PG-TSDSO-14 (thin (slim) dual small outline 14 pins) package outline**

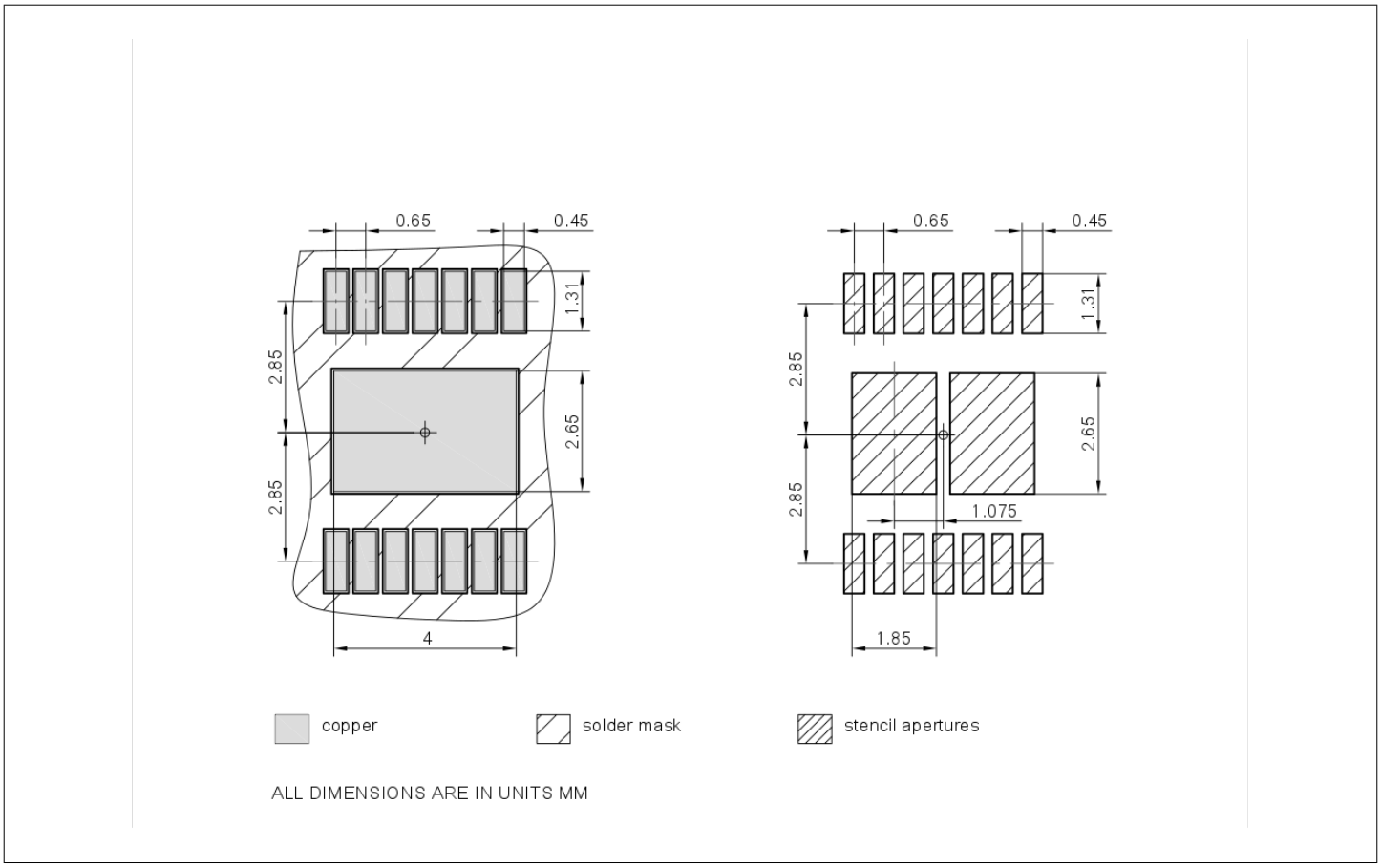



**Figure 56 PG-TSDSO-14 (thin (slim) dual small outline 14 pins) package pads and stencil**

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

# 13 Revision history

| Document version | Date of release | Description of changes |
|---|---|---|
| Rev. 1.00 | 2023-12-07 | Datasheet available |

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