

MOSFET

Small Signal MOSFET, -60 V

Features

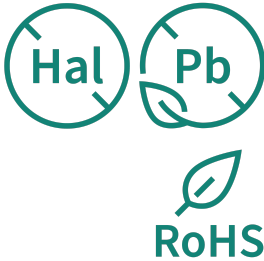
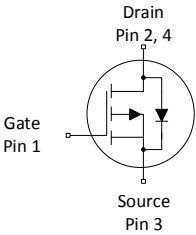
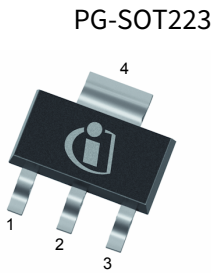
- P-channel
- Very low on-resistance $R_{DS(on)}$
- Superior thermal resistance
- 100% avalanche tested
- Pb-free lead plating; RoHS compliant
- Halogen-free according to IEC61249-2-21

Product validation

Fully qualified according to JEDEC for Industrial Applications

Table 1 Key performance parameters

Parameter	Value	Unit
V_{DS}	-60	V
$R_{DS(on),max}$	250	mΩ
I_D	-3.2	A
Q_{oss}	-4.4	nC
Q_G	-6.7	nC



Part number	Package	Marking	Related links
BSP171I	PG-SOT223	BSP171I	-



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1 Maximum ratings

at $T_A=25\text{ °C}$, unless otherwise specified

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Continuous drain current ¹⁾	I_D	-	-	-3.2	A	$V_{GS}=-10\text{ V}$, $T_C=25\text{ °C}$
				-2		$V_{GS}=-10\text{ V}$, $T_C=100\text{ °C}$
				-1.81		$V_{GS}=-4.5\text{ V}$, $T_C=100\text{ °C}$
				-1.9		$V_{GS}=-10\text{ V}$, $T_A=25\text{ °C}$, $R_{thJA}=70\text{ °C/W}$ ²⁾
Pulsed drain current ³⁾	$I_{D,pulse}$	-	-	-12.8	A	$T_C=25\text{ °C}$
Avalanche energy, single pulse ⁴⁾	E_{AS}	-	-	257	mJ	$I_D=-1.9\text{ A}$, $R_{GS}=25\text{ }\Omega$
Gate source voltage	V_{GS}	-20	-	20	V	-
Power dissipation	P_{tot}	-	-	5	W	$T_C=25\text{ °C}$
				1.8		$T_A=25\text{ °C}$, $R_{thJA}=70\text{ °C/W}$ ²⁾
Operating and storage temperature	T_j, T_{stg}	-55	-	150	°C	-

¹⁾ Rating refers to the product only with datasheet specified absolute maximum values, maintaining case temperature as specified. For other case temperatures please refer to Diagram 2. De-rating will be required based on the actual environmental conditions.

²⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

³⁾ See Diagram 3 for more detailed information

⁴⁾ See Diagram 13 for more detailed information

2 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	-	25	°C/W	-
Thermal resistance, junction - ambient, 6 cm ² cooling area ⁵⁾	R_{thJA}			70		

⁵⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air.

3 Electrical characteristics

at $T_j=25\text{ °C}$, unless otherwise specified

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	-60	-	-	V	$V_{GS}=0\text{ V}$, $I_D=-250\text{ }\mu\text{A}$
Gate threshold voltage	$V_{GS(th)}$	-1.0	-1.5	-2.0	V	$V_{DS}=V_{GS}$, $I_D=-270\text{ }\mu\text{A}$
Zero gate voltage drain current	I_{DSS}	-	-0.1	-1	μA	$V_{DS}=-60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$
			-10	-100		$V_{DS}=-60\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=125\text{ °C}$
Gate-source leakage current	I_{GSS}	-	-10	-100	nA	$V_{GS}=-20\text{ V}$, $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	177.1	250	m Ω	$V_{GS}=-10\text{ V}$, $I_D=-1.9\text{ A}$
			210.7	310		$V_{GS}=-4.5\text{ V}$, $I_D=-1.7\text{ A}$
Gate resistance	R_G	-	5.6	-	Ω	-
Transconductance	g_{fs}	-	4.4	-	S	$ V_{DS} \geq 2 I_D R_{DS(on)max}$, $I_D=-1.9\text{ A}$

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Input capacitance ⁶⁾	C_{iss}	-	420	550	pF	$V_{GS}=0\text{ V}$, $V_{DS}=-30\text{ V}$, $f=1\text{ MHz}$
Output capacitance ⁶⁾	C_{oss}		60	78		
Reverse transfer capacitance ⁶⁾	C_{rss}		15	26		
Turn-on delay time	$t_{d(on)}$	-	4.0	-	ns	$V_{DD}=-30\text{ V}$, $V_{GS}=-10\text{ V}$, $I_D=-1.9\text{ A}$, $R_{G,ext}=6\text{ }\Omega$
Rise time	t_r		2.0			
Turn-off delay time	$t_{d(off)}$		24.0			
Fall time	t_f		11.9			

⁶⁾ Defined by design. Not subject to production test.

Table 6 Gate charge characteristics ⁷⁾

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	-1.21	-	nC	$V_{DD} = -30\text{ V}$, $I_D = -1.9\text{ A}$, $V_{GS} = 0\text{ to } -4.5\text{ V}$
Gate charge at threshold	$Q_{g(th)}$		-0.63	-	nC	
Gate to drain charge ⁸⁾	Q_{gd}		-3.3	-4.9	nC	
Switching charge	Q_{sw}		-3.9	-	nC	
Gate charge total ⁸⁾	Q_g		-6.7	-8.4	nC	
Gate plateau voltage	$V_{plateau}$		-2.9	-	V	
Gate charge total ⁸⁾	Q_g	-	-13.9	-18.5	nC	$V_{DD} = -30\text{ V}$, $I_D = -1.9\text{ A}$, $V_{GS} = 0\text{ to } -10\text{ V}$
Output charge ⁸⁾	Q_{oss}	-	-4.4	-5.9	nC	$V_{DS} = -30\text{ V}$, $V_{GS} = 0\text{ V}$

⁷⁾ See "Gate charge waveforms" for parameter definition

⁸⁾ Defined by design. Not subject to production test.

Table 7 Reverse diode

Parameter	Symbol	Values			Unit	Note / Test condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S	-	-	-3.2	A	$T_C = 25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			-12.8		
Diode forward voltage	V_{SD}	-	-0.81	-1.2	V	$V_{GS} = 0\text{ V}$, $I_F = -1.5\text{ A}$, $T_J = 25\text{ °C}$
Reverse recovery time ⁹⁾	t_{rr}	-	31.8	63.6	ns	$V_R = -30\text{ V}$, $I_F = -1.9\text{ A}$, $di_F/dt = -100\text{ A}/\mu\text{s}$
Reverse recovery charge ⁹⁾	Q_{rr}		42.6	85.2	nC	

⁹⁾ Defined by design. Not subject to production test.

4 Electrical characteristics diagrams

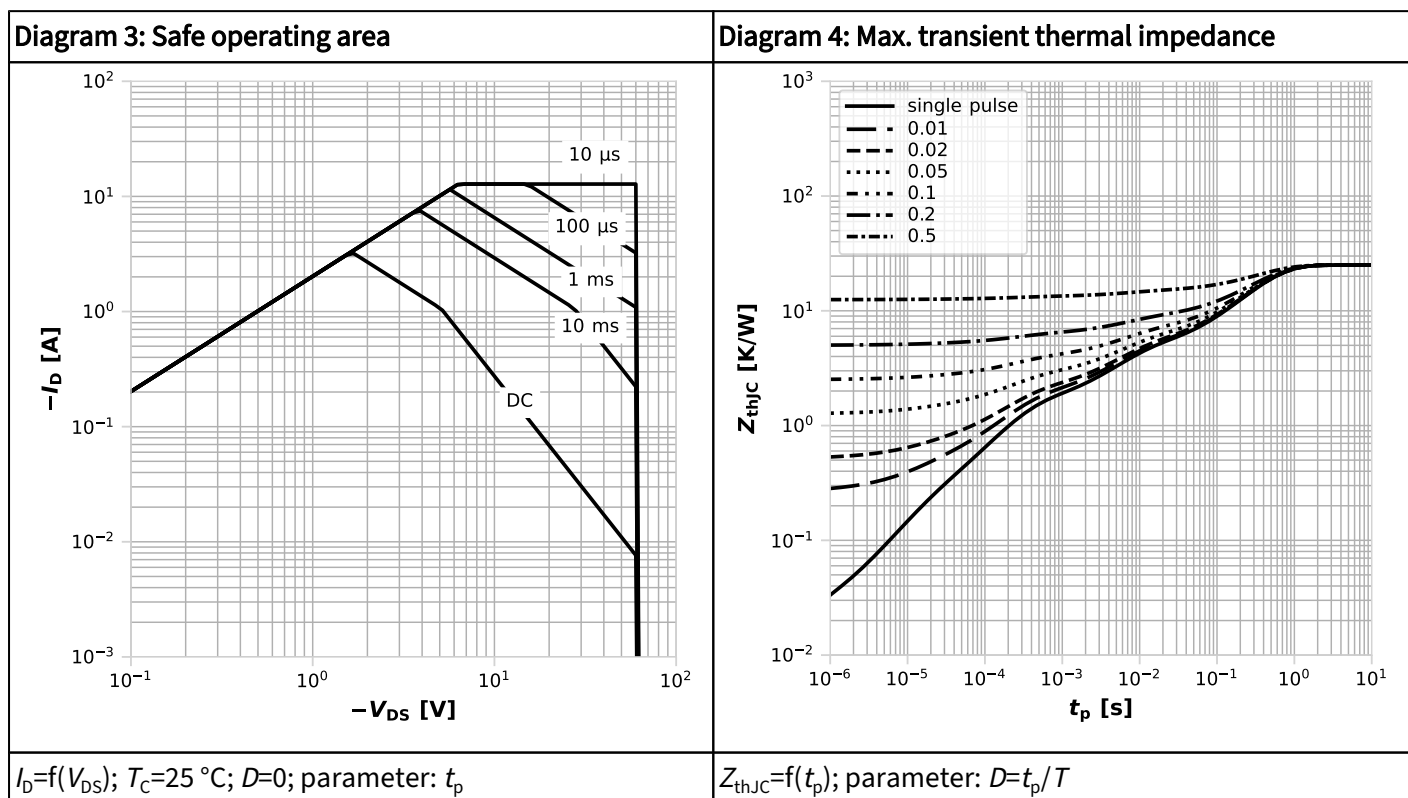
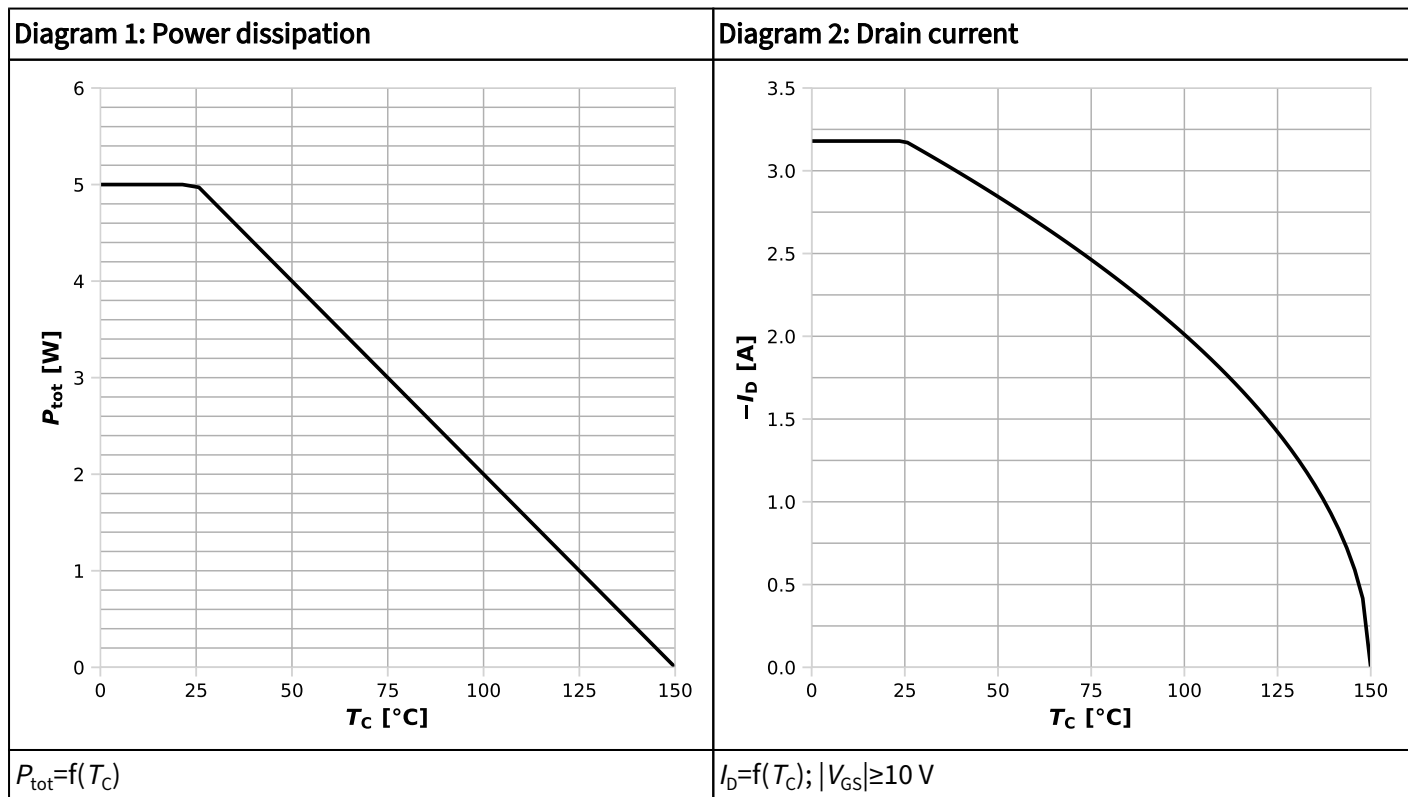
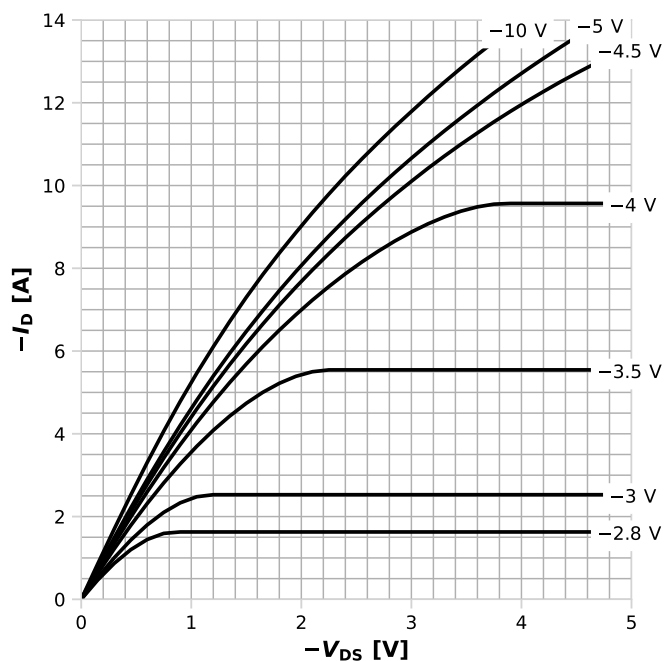
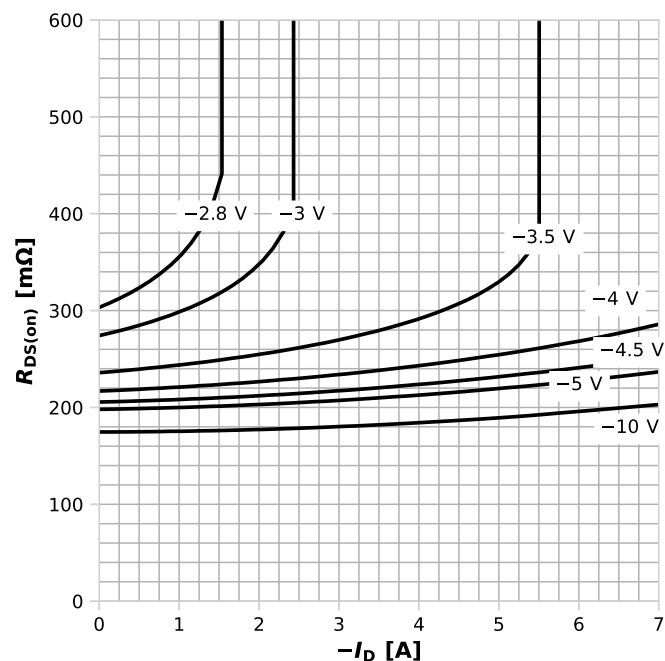


Diagram 5: Typ. output characteristics



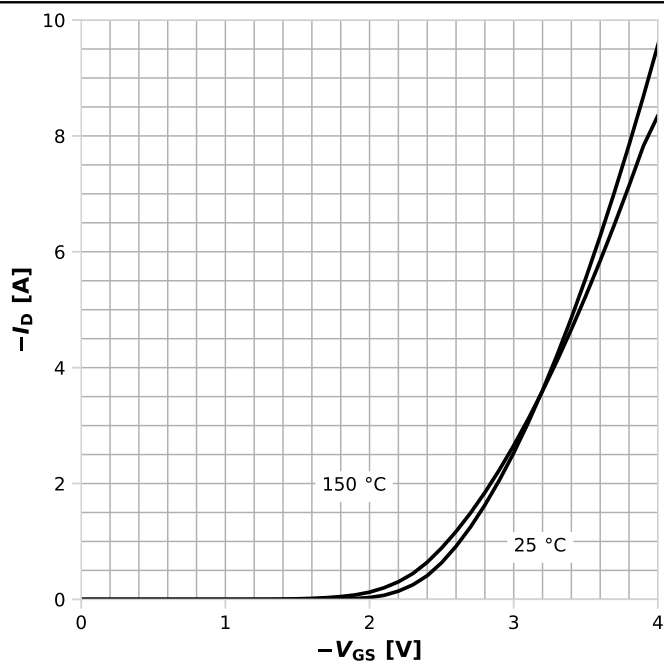
$I_D = f(V_{DS})$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 6: Typ. drain-source on resistance



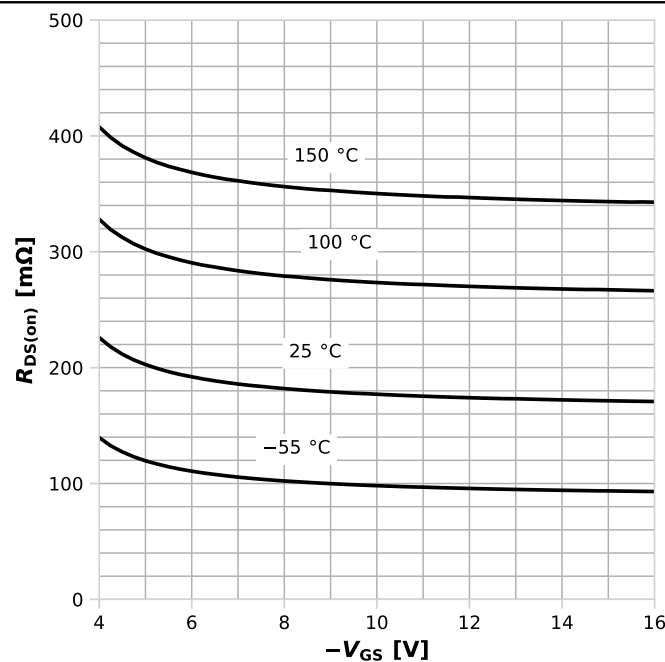
$R_{DS(on)} = f(I_D)$, $T_j = 25^\circ\text{C}$; parameter: V_{GS}

Diagram 7: Typ. transfer characteristics



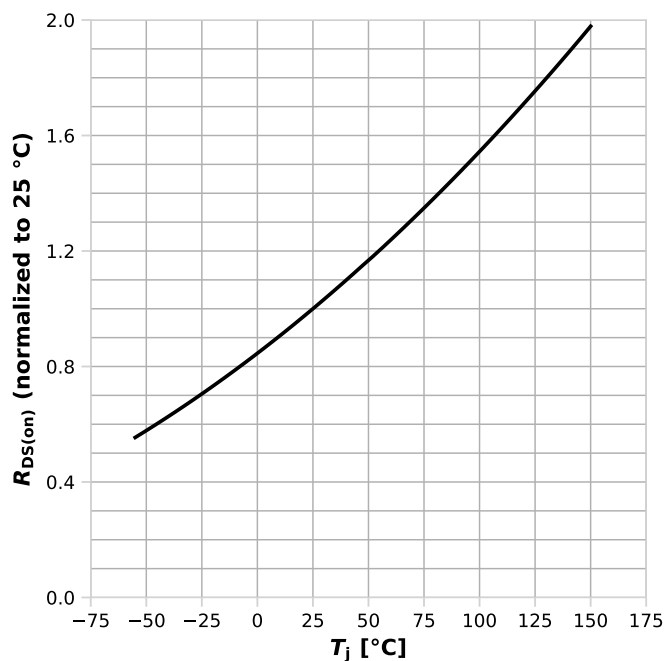
$I_D = f(V_{GS})$, $|V_{DS}| > 2|I_D|R_{DS(on)max}$; parameter: T_j

Diagram 8: Typ. drain-source on resistance



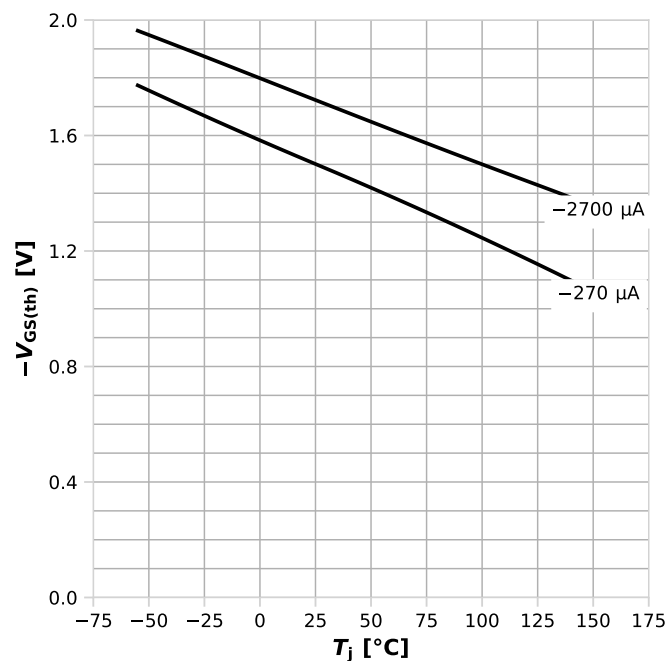
$R_{DS(on)} = f(V_{GS})$, $I_D = -1.9\text{ A}$; parameter: T_j

Diagram 9: Normalized drain-source on resistance



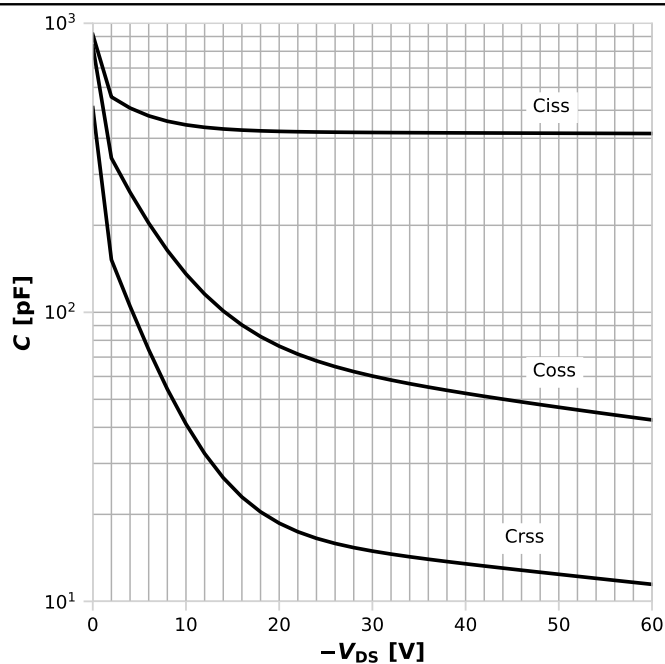
$$R_{DS(on)} = f(T_j), I_D = -1.9 \text{ A}, V_{GS} = -10 \text{ V}$$

Diagram 10: Typ. gate threshold voltage



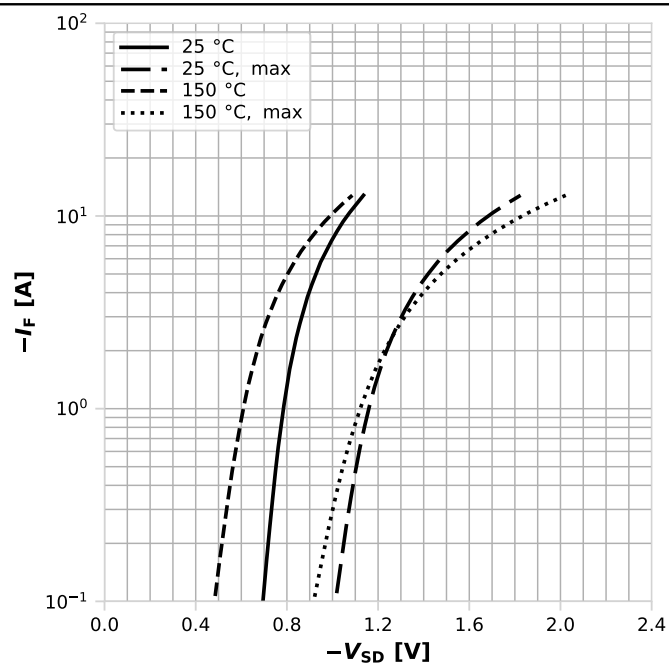
$$V_{GS(th)} = f(T_j), V_{GS} = V_{DS}; \text{ parameter: } I_D$$

Diagram 11: Typ. capacitances



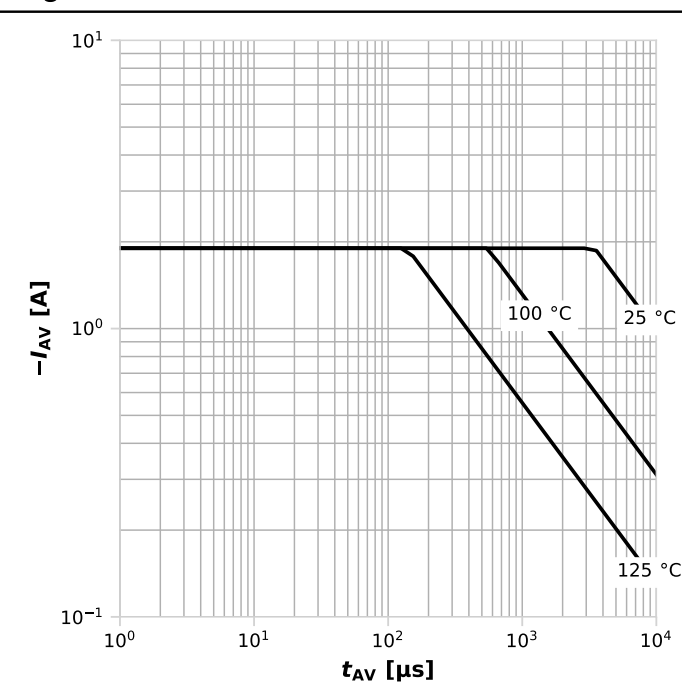
$$C = f(V_{DS}); V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$$

Diagram 12: Forward characteristics of reverse diode



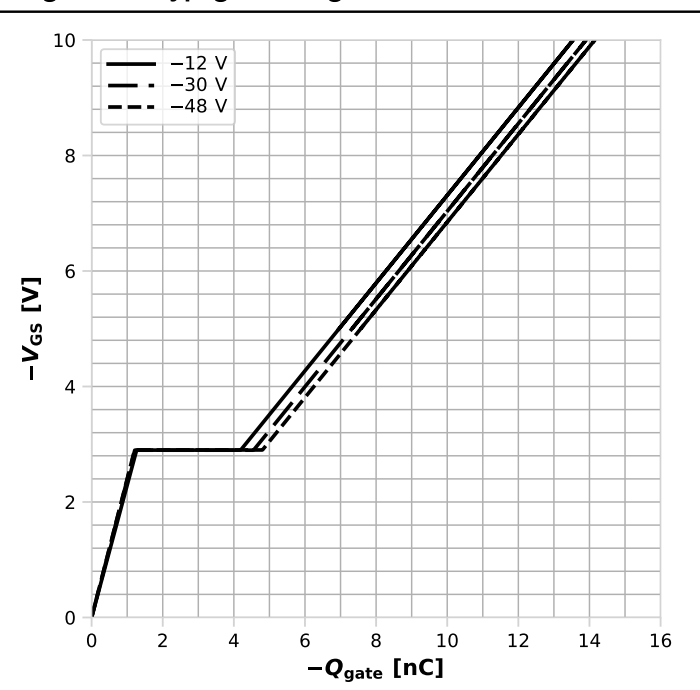
$$I_F = f(V_{SD}); \text{ parameter: } T_j$$

Diagram 13: Avalanche characteristics



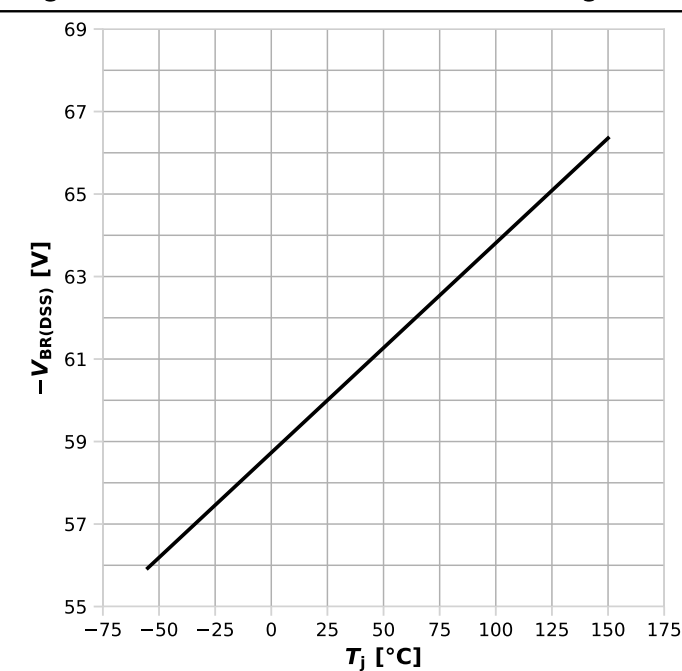
$I_{AS}=f(t_{AV})$; $R_{GS}=25\ \Omega$; parameter: $T_{j,start}$

Diagram 14: Typ. gate charge



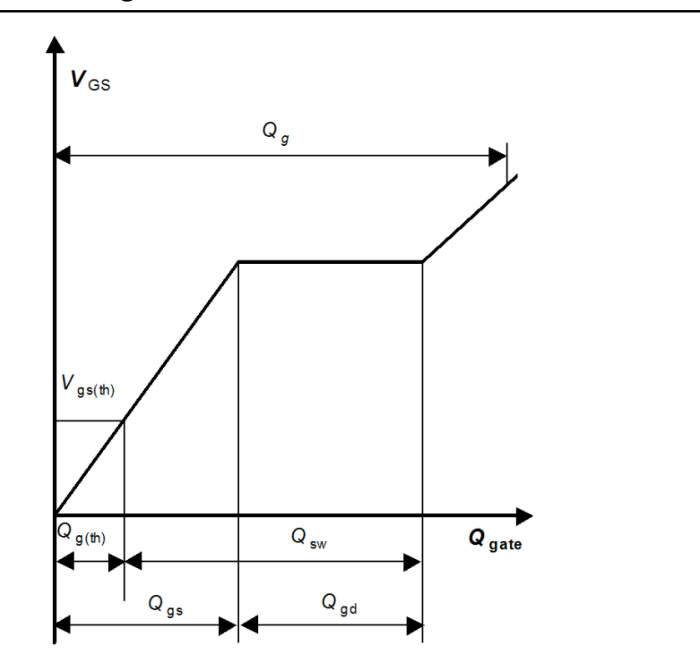
$V_{GS}=f(Q_{gate})$, $I_D=-1.9\text{ A}$ pulsed, $T_j=25\text{ °C}$; parameter: V_{DD}

Diagram 15: Min. drain-source breakdown voltage



$V_{BR(DSS)}=f(T_j)$; $I_D=-250\ \mu$ A

Gate charge waveforms



-

5 Package outlines

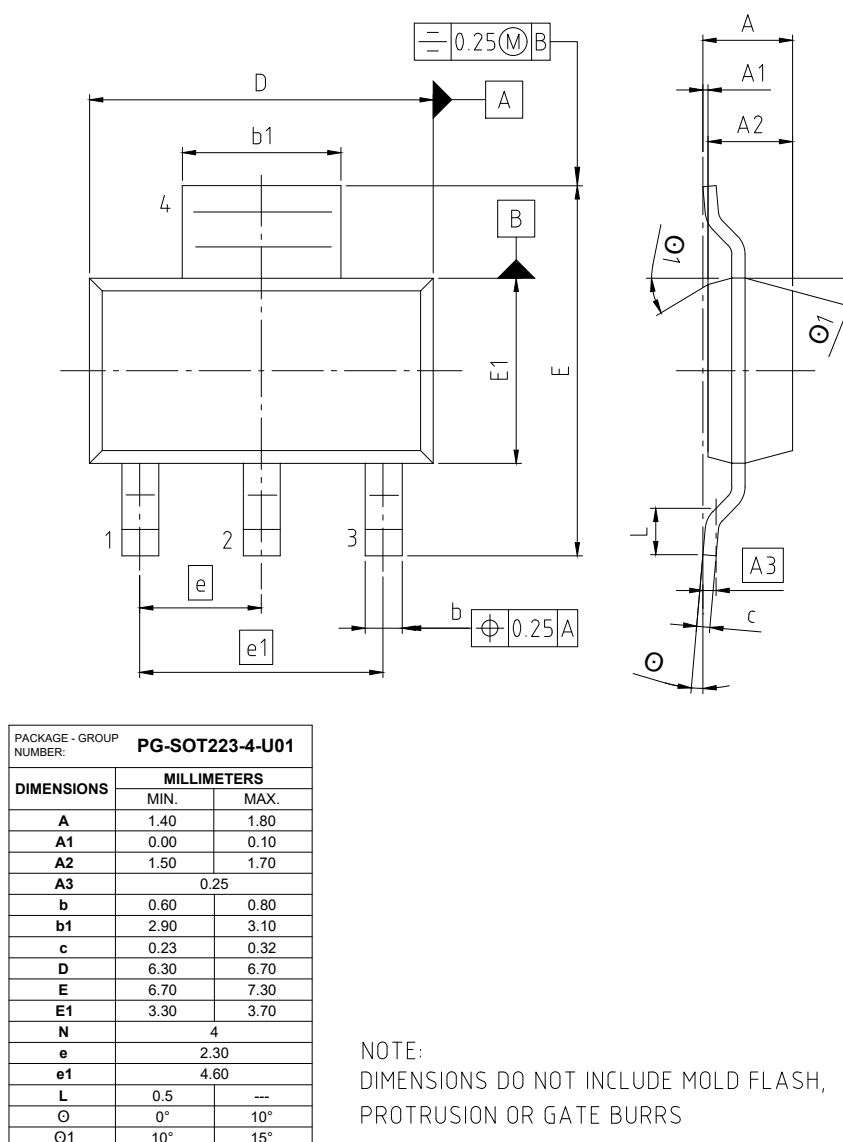


Figure 1 Outline PG-SOT223, dimensions in mm

Revision history

BSP171I

Revision 2025-02-16, Rev. 2.0

Previous revisions

Revision	Date	Subjects (major changes since last revision)
2.0	2025-02-16	Release of final datasheet

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