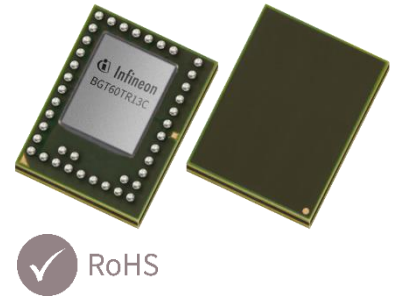


BGT60TR13C

Datasheet V2.4.9

Features

- 60 GHz radar sensor for FMCW operation
- 5.5 GHz bandwidth
- Antenna-in-package (6.5 x 5.0 x 0.9 mm³)
- Digital interface for chip configuration and radar data acquisition
- Optimized power modes for low-power operation
- Integrated state machine for independent operation



Potential applications

- Radar frontend for gesture sensing
- High resolution FMCW radars
- Short range sensing operations
- Hidden sensing applications behind radome

Product validation

Packaged device qualified according to JEDEC 20/22.

Description

The BGT60TR13C, a 60 GHz radar sensor with antenna in package, enables ultra-wide bandwidth FMCW operation in a small package. Sensor configuration and data acquisition are enabled with a digital interface and the integrated state machine enables independent data acquisition with power mode optimization for lowest power consumption.

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Introduction

1 Introduction

New smart sensors for gesture recognition can be based on radar systems, in special case, FMCW radars. Those systems can comprise several blocks: Radio Frequency (RF) front-end, Analog Base Band (ABB), Analog to Digital Converter (ADC), Phase Locked Loop (PLL), memory (FIFO e.g.), Serial Peripheral Interface (SPI) and Antennas. Smart sensors require a high level of integration, thus, the components listed above should be integrated in a single chip solution. BGT60TR13C offers this level of integration in a single chipset.

1.1 Product Overview

The core functionality of BGT60TR13C is to transmit frequency modulated continuous wave (FMCW) signal via the transmitter channel (TX) and receive the echo signals from the target object on the three receiving channels (RX). Each receiver path includes a baseband filtering, a VGA, as well as an ADC. The digitized output is stored in a FIFO. The data are transferred to an external host, microcontroller unit (MCU) or application processor (AP), to run radar signal processing. A typical implementation of a sensor system consists of two main blocks only (see Figure 1):

- BGT60TR13C handles the RF signals and provides the sampled IF signals
- Application Processor which captures and processes the radar signals

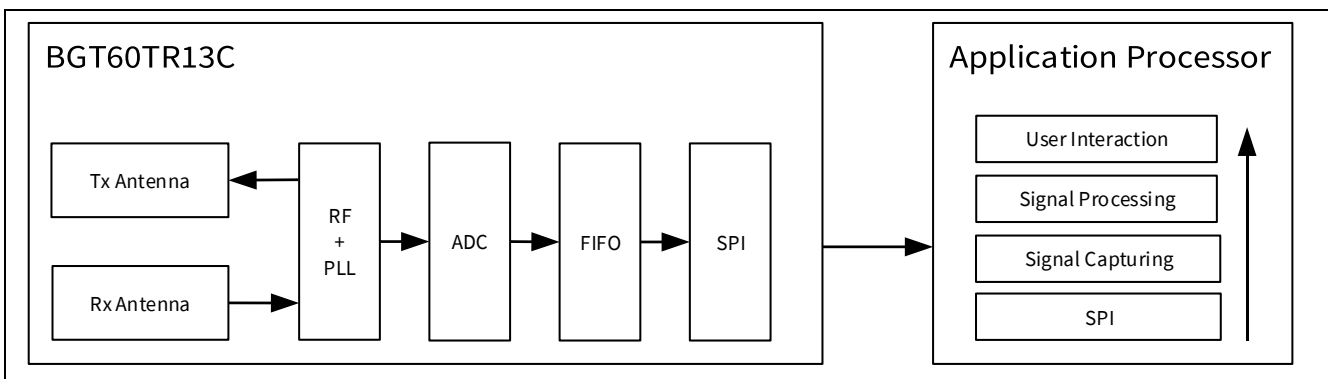


Figure 1 Data flow in the complete radar sensor system

1.2 Potential Applications

The chipset has been designed to address mainly the following potential applications:

- Radar frontend for gesture sensing
- High resolution FMCW radars
- Short range sensing operations
- Hidden sensing applications behind radome

BGT60TR13C

Datasheet

Introduction

1.4 BGT60TR13C Pin Definition and Function

The following Figure 3 shows the bottom view of the BGT60TR13C laminate package with the pin and antenna number assignment.

The function of each pin is described in Table 1 (See also Table 2 and Table 3).

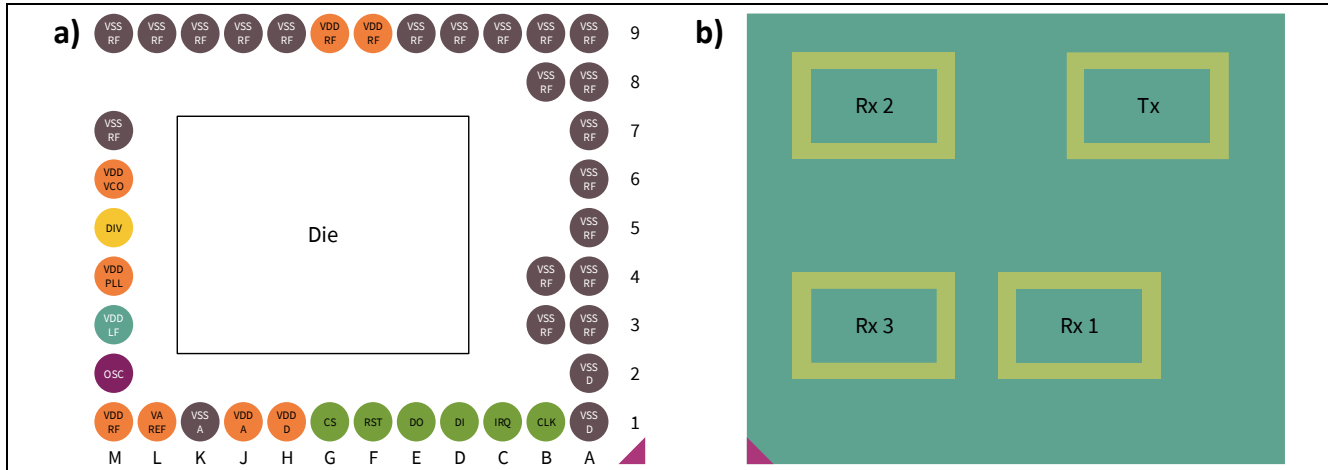


Figure 3 BGT60TR13C pin out in bottom view (a) and antenna numbers assignment in top view (b)

Table 1 Ball and Antenna Definition

| Ball | Function |
|--|--------------|
| A1, A2 | VSSD |
| B1 | CLK |
| C1 | IRQ |
| D1 | DI |
| E1 | DO |
| F1 | DIO3 |
| G1 | CS_N |
| H1 | VDDD |
| J1 | VDDA |
| K1 | VSSA |
| L1 | VAREF |
| M1, F9, G9 | VDDRF |
| M2 | OSC_CLK |
| M3 | VDDLf |
| M4 | VDDPLL |
| M5 | DIV_TEST |
| M6 | VDDVCO |
| M7, M9, L9, K9, J9, H9, E9, D9, C9, B9, B8, A9, A8, A7, A6, A5, B4, A4, B3, A3 | VSSRF |
| Antenna | Function |
| Tx1 | Transmitter |
| Rx1 | Receiver ch1 |

Introduction

Table 1 Ball and Antenna Definition

| Ball | Function |
|------|--------------|
| Rx2 | Receiver ch2 |
| Rx3 | Receiver ch3 |

1.4.1 IO and Supply Pins

The following Table 2 gives an overview on the input/output pins of BGT60TR13C.

Table 2 BGT60TR13C Input/Output Pins

| Symbol | Type | Domain | Description | Domain |
|----------|------------------------------------|--------|-----------------------------------|-------------|
| DIV_TEST | A _{OUT} | VDDRF | VCO divided by 16 output | Analog-RF |
| OSC_CLK | A _{IN} | VDDRF | 80 MHz (e.g.) Xtal input | Analog-RF |
| CLK | D _{IN} | VDDD | SPI CLK input | SPI |
| IRQ | D _{OUT} | VDDD | Interrupt output | Control FSM |
| CS_N | D _{IN} | VDDD | SPI chip select input, active low | SPI |
| DI | D _{IN} | VDDD | SPI signal from the host output | SPI |
| DO | D _{OUT} | VDDD | SPI signal to the host input | SPI |
| DIO3 | D _{IN} / D _{OUT} | VDDD | HW reset pin | SPI |

The power supply pins are described in Table 3.

Table 3 BGT60TR13C Supply Pins

| Symbol | Type | Domain | Description | Domain |
|--------|------------------|--------|---|-----------|
| VDDD | V _{IN} | 1.8 V | Digital supply voltage | Digital |
| VDDA | V _{IN} | 1.8 V | Analog supply voltage | ADC |
| VAREF | V _{OUT} | 1.2 V | Positive reference voltage output; for bypass cap | ADC |
| VDDVCO | V _{IN} | 1.8 V | Analog supply voltage to the VCO | Analog-RF |
| VDDRF | V _{IN} | 1.8 V | Analog supply voltage | Analog-RF |
| VDDLf | V _{IN} | 3.3V | Analog supply voltage for the level shifter for the PLL loop filter | Analog-RF |
| VDDPLL | V _{IN} | 1.8 V | Analog supply voltage to the PLL | Analog-RF |
| VSSRF | GNDA | 0 V | Analog ground connection | Analog-RF |
| VSSA | GNDA | 0 V | Analog ground connection | ADC |
| VSSD | GNDD | 0 V | Digital ground connection | Digital |

Abbreviations:

V_{IN} ... supply voltage input pin

D_{IN} ... digital input pin

D_{OUT} ... digital output pin

V_{OUT} ... supply voltage output pin

Introduction

A_{OUT} ... analog output pin

A_{IN} ... analog input pin

GNDA ... analog ground connection

GNDD ... digital ground connection

1.5 BGT60TR13C Functional Block Diagram

BGT60TR13C consists of some main functional blocks:

- **Antenna** built in package, see Figure 81
- **RF Frontend** consisting of 3ch Rx, 1ch Tx, LO generation, and divider by 4/5, see paragraph 7.1
- **ABB**, analog baseband consisting of high pass filter (HPF), VGA, anti-aliasing filter (AAF), see paragraph 7.2
- **PLL**, 3rd order sigma-delta based to perform FMCW ramp
- **MADC**, 3ch 12 bits differential SAR ADCs interfaced to the ABB via a driver and to the FIFO via a mux, see paragraph 8
- **SADC**, 8 to 10 bits single-ended SAR ADC used to sense the sensor data, see section 9
- **FIFO**, 196 kbit= 8192 words x 24 bits
- **Register banks**, 127 registers, see paragraph 4
- **SPI**, up to 50 MHz clock in standard mode
- **FSM**, finite state machine which manages the complete chip
- Clockwise, two domains can be identified:
 - 80 MHz system clock (SYS_CLK) domain for PLL, MADC, SADC, and FIFO
 - 50 MHz (e.g.) SPI clock

The main FSM syncs those two domains.

Introduction

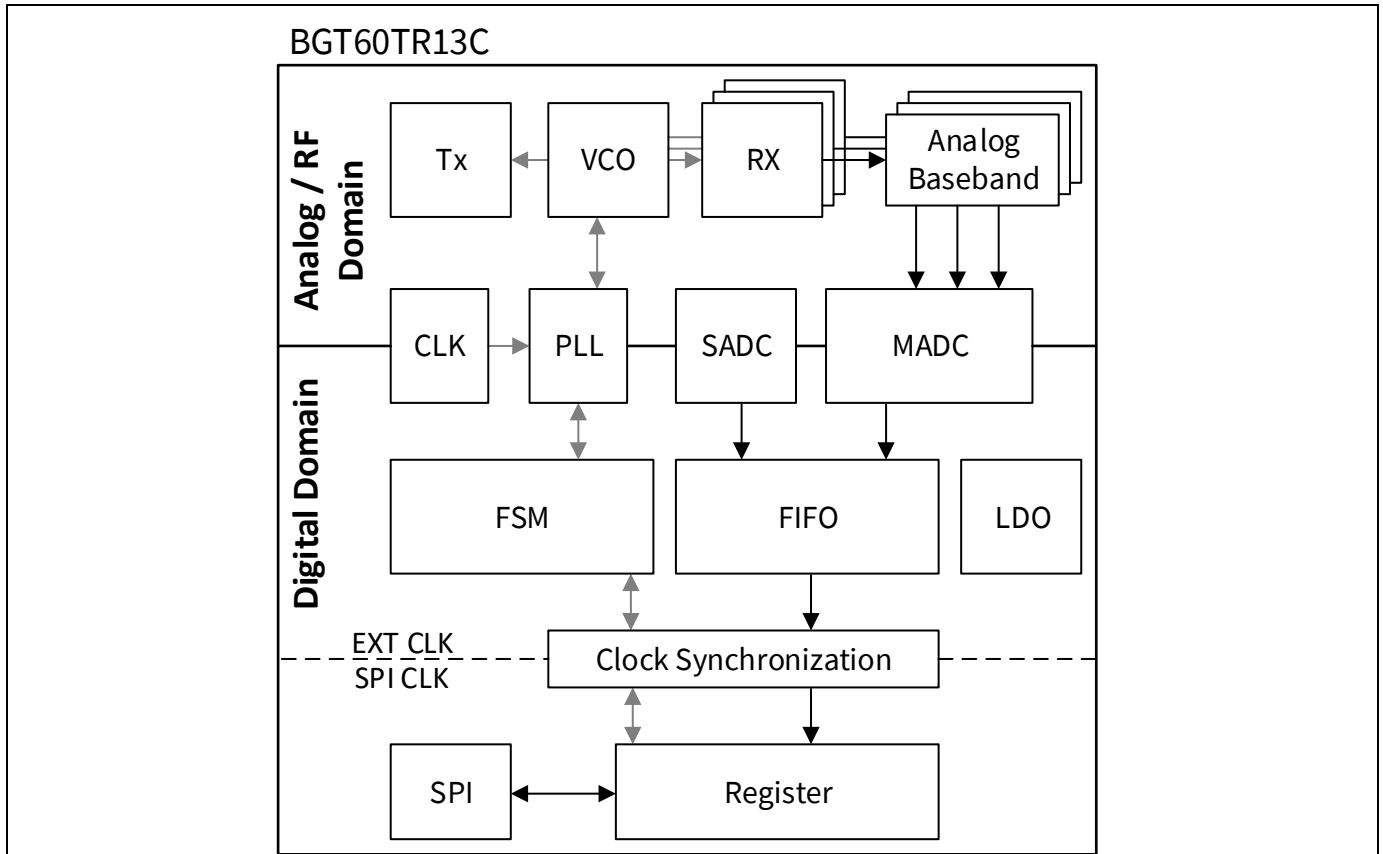


Figure 4 BGT60TR13C functional overview

General Product Specification

2 General Product Specification

The reference for all specified data is the Infineon application board, available on request.

2.1 Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings $T_b = -40\text{ °C}$ to 105 °C , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified). Parameters not subject to production test

| Spec | Symbol | Unit | Value | | | Condition |
|----------------------------|-----------|------|-------|-----|---------|----------------------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Supply Voltage | VDDD | V | -0.3 | | +2 | |
| Supply Voltage | VDDA | V | -0.3 | | +2 | |
| Supply Voltage | VDDRF | V | -0.3 | | +2 | |
| Supply Voltage | VDDVCO | V | -0.3 | | +2 | |
| Supply Voltage | VDDPLL | V | -0.3 | | +2 | |
| Supply Voltage | VDDLf | V | -0.3 | | +3.7 | |
| DC Voltage at all I/O Pins | $V_{I/O}$ | V | -0.3 | | VDD+0.3 | Not exceeding 2V |
| RF Input Power Level | PRF | dBm | | | +10 | At the Rx input-port |
| Junction Temperature | T_j | °C | -40 | | +125 | |
| Storage Temperature | T_{stg} | °C | -40 | | +150 | |

Warning: Stresses above the maximum values listed here may cause permanent damage to the device. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit. Exposure to conditions at or below absolute maximum rating but above the specified maximum operation conditions may affect device reliability and lifetime. Functionality of the device might not be given under these conditions.

2.2 Range of Functionality

Table 5 Range of Functionality, VDDD = 1.71 to 1.89 V, $T_b = -20$ to $+70\text{ °C}$

| Spec | Symbol | Unit | Value | | | Condition |
|---------------------------|----------|------|-------|-----|------|---|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Supply Voltage | VDDD | V | 1.71 | 1.8 | 1.89 | Noise on each supply domain should not exceed the level of 20µVpp in the frequency range 20 kHz – 700 kHz ¹⁾ |
| Supply Voltage | VDDA | V | 1.71 | 1.8 | 1.89 | |
| Supply Voltage | VDDRF | V | 1.71 | 1.8 | 1.89 | |
| Supply Voltage | VDDVCO | V | 1.71 | 1.8 | 1.89 | |
| Supply Voltage | VDDPLL | V | 1.71 | 1.8 | 1.89 | |
| Supply Voltage | VDDLf | V | 2.5 | 3.3 | 3.63 | |
| Chip Backside Temperature | T_b | °C | -20 | | 70 | Measured with the on-chip temperature sensor |
| Frequency Range | f_{RF} | GHz | 58.0 | | 63.5 | |

General Product Specification

| | | | | | | |
|---|------------------------|-----|----|----|----|---|
| System Reference Frequency | $f_{\text{SYS_CLK}}$ | MHz | 75 | 80 | 85 | 1.8 V CMOS clock; 78 MHz not allowed |
| Duty cycle of $f_{\text{SYS_CLK}}$ | f_{DUTSYS} | % | 45 | 50 | 55 | |
| Rise and Fall Time of $f_{\text{SYS_CLK}}$ | $t_{\text{RS,FS,SYS}}$ | ns | | | 6 | |
| Phase Jitter of $f_{\text{SYS_CLK}}$ | J_{PHYSYS} | ps | | 1 | | BW: 12 kHz to 20 MHz |

- ¹⁾ This value will guarantee no artifact/false target in the Range-Doppler map when it is calculated with a minimum of 8 chirps.

2.3 Current Consumption

Table 6 Overall Current Consumption, VDD (all except LF) = 1.71 to 1.89 V and Tb = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|-------------------------------------|-------------------------------|------|-------|------|---------------------|-----------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep ¹⁾ | $I_{\text{dd}_{\text{ds}}}$ | mA | 0.05 | 0.12 | 0.555 ⁵⁾ | |
| Idd Idle ²⁾ | $I_{\text{dd}_{\text{idle}}}$ | mA | 0.05 | 2.8 | 5 | |
| Idd Init0, 3Rx+ 1Tx | $I_{\text{dd}_{\text{int0}}}$ | mA | 136 | 175 | 205 | |
| Idd Init1, 3Rx+ 1Tx ³⁾ | $I_{\text{dd}_{\text{int1}}}$ | mA | 141 | 185 | 215 | |
| Idd Active, 3Rx + 1Tx ⁴⁾ | $I_{\text{dd}_{\text{act}}}$ | mA | 160 | 201 | 230 | |

- ¹⁾ All registers in reset mode, 80 MHz clock path disabled
- ²⁾ MADC band gap running
- ³⁾ Idd for the rest of interchirp similar to Init1
- ⁴⁾ Device set in radar mode; DAC Tx set to 31_D
- ⁵⁾ The value at max refers to the max temperature, +70 °C, and the max supply, 1.89 V

Table 7 VDDD Domain Current Consumption, VDD (any except LF) = 1.71 to 1.89 V and Tb = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|-------------------------------------|---------------------------------|------|-------|-----|--------------------|-----------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep ¹⁾ | $D I_{\text{dd}_{\text{ds}}}$ | mA | 0.05 | 0.1 | 0.48 ⁵⁾ | |
| Idd Idle ²⁾ | $D I_{\text{dd}_{\text{idle}}}$ | mA | 1.5 | 2.5 | 3.5 | |
| Idd Init0, 3Rx+ 1Tx | $D I_{\text{dd}_{\text{int0}}}$ | mA | 2 | 3 | 4 | |
| Idd Init1, 3Rx+ 1Tx ³⁾ | $D I_{\text{dd}_{\text{int1}}}$ | mA | 3 | 4 | 5 | |
| Idd Active, 3Rx + 1Tx ⁴⁾ | $D I_{\text{dd}_{\text{act}}}$ | mA | 3 | 4 | 5 | |

- ¹⁾ All registers in reset mode, 80 MHz clock path disabled
- ²⁾ MADC band gap running
- ³⁾ Idd for the rest of interchirp similar to Init1
- ⁴⁾ Device set in radar mode and FIFO in low power mode; DAC Tx set to 31_D for an output power of +5 dBm

General Product Specification

⁵⁾ The value at max refers to the max temperature +70 °C and the max supply 1.89 V

Table 8 VDDA Domain Current Consumption, VDD (any except LF) = 1.71 to 1.89 V and Tb = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|-------------------------------------|----------------------|------|-------|-------|------|-----------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep ¹⁾ | Aldd _{ds} | mA | 0 | 0.005 | 0.01 | |
| Idd Idle ²⁾ | Aldd _{idle} | mA | 0.01 | 0.2 | 0.3 | |
| Idd Init0, 3Rx+ 1Tx | Aldd _{int0} | mA | 0.5 | 1.6 | 3 | |
| Idd Init1, 3Rx+ 1Tx ³⁾ | Aldd _{int1} | mA | 0.5 | 1.6 | 3 | |
| Idd Active, 3Rx + 1Tx ⁴⁾ | Aldd _{act} | mA | 0.5 | 1.6 | 3 | |

¹⁾ All registers in reset mode, 80 MHz clock path disabled

²⁾ MADC band gap running

³⁾ Idd for the rest of interchirp similar to Init1

⁴⁾ Device set in radar mode; DAC Tx set to 31_D

Table 9 VDDPLL Domain Current Consumption, VDD (any except LF) = 1.71 to 1.89 V and Tb = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|-------------------------------------|------------------------|------|-------|-------|------|-----------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep ¹⁾ | PLLidd _{ds} | mA | 0 | 0.005 | 0.01 | |
| Idd Idle ²⁾ | PLLidd _{idle} | mA | 0 | 0.005 | 0.01 | |
| Idd Init0, 3Rx+ 1Tx | PLLidd _{int0} | mA | 0.6 | 0.9 | 1.2 | |
| Idd Init1, 3Rx+ 1Tx ³⁾ | PLLidd _{int1} | mA | 5 | 8 | 10 | |
| Idd Active, 3Rx + 1Tx ⁴⁾ | PLLidd _{act} | mA | 5 | 8 | 10 | |

¹⁾ All registers in reset mode, 80 MHz clock path disabled

²⁾ MADC band gap running

³⁾ Idd for the rest of interchirp similar to Init1

⁴⁾ Device set in radar mode; DAC Tx set to 31_D

Table 10 VDDLf Domain Current Consumption, VDD (any except LF) = 1.71 to 1.89 V and Tb = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|-------------------------------------|-----------------------|------|-------|-------|------|-----------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep ¹⁾ | LFidd _{ds} | mA | 0 | 0.005 | 0.01 | |
| Idd Idle ²⁾ | LFidd _{idle} | mA | 0 | 0.005 | 0.01 | |
| Idd Init0, 3Rx+ 1Tx | LFidd _{int0} | mA | 0.2 | 0.45 | 0.5 | |
| Idd Init1, 3Rx+ 1Tx ³⁾ | LFidd _{int1} | mA | 0.2 | 0.45 | 0.5 | |
| Idd Active, 3Rx + 1Tx ⁴⁾ | LFidd _{act} | mA | 0.2 | 0.45 | 0.5 | |

General Product Specification

- 1) All registers in reset mode, 80 MHz clock path disabled
- 2) MADC band gap running
- 3) Idd for the rest of interchirp similar to Init1
- 4) Device set in radar mode; DAC Tx set to 31_D

Table 11 VDDRF + VDDVCO Domain Current Consumption, VDD (any except LF) = 1.71 to 1.89 V and Tb = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|-------------------------------------|-----------------------|------|-------|------|-------|-----------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Idd Deep Sleep ¹⁾ | RFIdd _{ds} | mA | 0 | 0.02 | 0.045 | |
| Idd Idle ²⁾ | RFIdd _{idle} | mA | 0 | 0.02 | 0.045 | |
| Idd Init0, 3Rx+ 1Tx | RFIdd _{int0} | mA | 133 | 170 | 196 | |
| Idd Init1, 3Rx+ 1Tx ³⁾ | RFIdd _{int1} | mA | 133 | 170 | 196 | |
| Idd Active, 3Rx + 1Tx ⁴⁾ | RFIdd _{act} | mA | 151 | 187 | 212 | |

- 1) All registers in reset mode, 80 MHz clock path disabled
- 2) MADC band gap running
- 3) Idd for the rest of interchirp similar to Init1
- 4) Device set in radar mode; DAC Tx set to 31_D

2.4 ESD Integrity

Table 12 ESD Integrity, VDD(any) = 1.71 to 1.89 V, Tb = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|---|--------------------------|------|-------|-----|-------|--|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| ESD robustness, HBM All pins | V _{ESD-HBM} | V | -2000 | | +2000 | According to JS-001 (R = 1.5 kΩ, C = 100 pF) |
| ESD robustness, CDM All pins except M2 | V _{ESD-CDM} | V | -500 | | +500 | According to JS-002 |
| ESD robustness, CDM Pin M2 | V _{ESD-CDM, M2} | V | -250 | | +250 | According to JS-002 |

CDM: Field-Induced Charged-Device Model ANSI/ESDA/JEDEC JS-002. Simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occurs whenever there is metal-to-metal contact in manufacturing.

HBM: Human Body Model ANSI/ESDA/JEDEC JS-001 (R = 1.5 kΩ, C=100 pF).

General Product Specification

2.5 Thermal Resistance

Table 13 Thermal Resistance, VDD(any) = 1.71 to 1.89 V, Tb = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|-------------|-----------------|------|-------|-----|-----|--------------------------------------|
| | | | Min | Typ | Max | |
| Parameter | | | | | | |
| Package Rth | R _{th} | K/W | | 35 | | Chip backside to ambient temperature |

2.6 Product Validation

Qualified for potential applications listed in section 1.2 based on the test conditions in the relevant tests of JEDEC20/22.

Shapes, Frames, and Channel Set Definition

3 Shapes, Frames, and Channel Set Definition

This section is intended to provide the user with an overview on the overall modulation and power modes capabilities of BGT60TR13C. Specifically, the structure of timers, counters, shapes, channel set and frames will be presented. The section also gives a description of how the main FSM is setting and controlling the PLL for the expected modulation shapes and sequences programmed by the host.

3.1 Shapes and Frames

The shape is the modulation chirp that should be performed by the PLL. Two basic shapes are allowed (see Figure 5):

- triangular shape: consisting of a frequency Upchirp and a frequency Downchirp
- saw-tooth shape: consisting of a frequency Upchirp followed by a fast-down chirp

The shapes are set and enabled in the PLLx[0..7] registers (see section 4.16 and 4.17) by the bit PLLx7_SH_EN. Up to four different shapes can be programmed. If more than one shape is used, the lower shapes must be programmed (e.g. 3 shapes are needed by the application than x= 1...3).

N_SHAPE_EN is the number of shapes enabled.

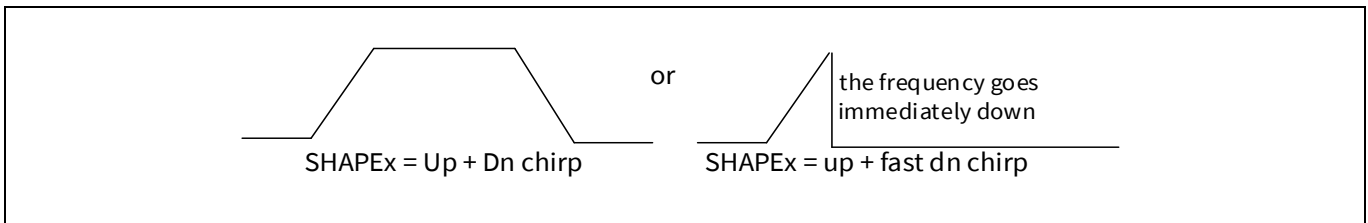


Figure 5 Shape definition

Shape Group

Each shape defined above can be repeated several times (see Figure 6). The same shape repeated several times represents a shape group. The repetition factor for the shape is called REPSx and described in 4.17. Each shape is repeated up to RSx=2^REPSx times.

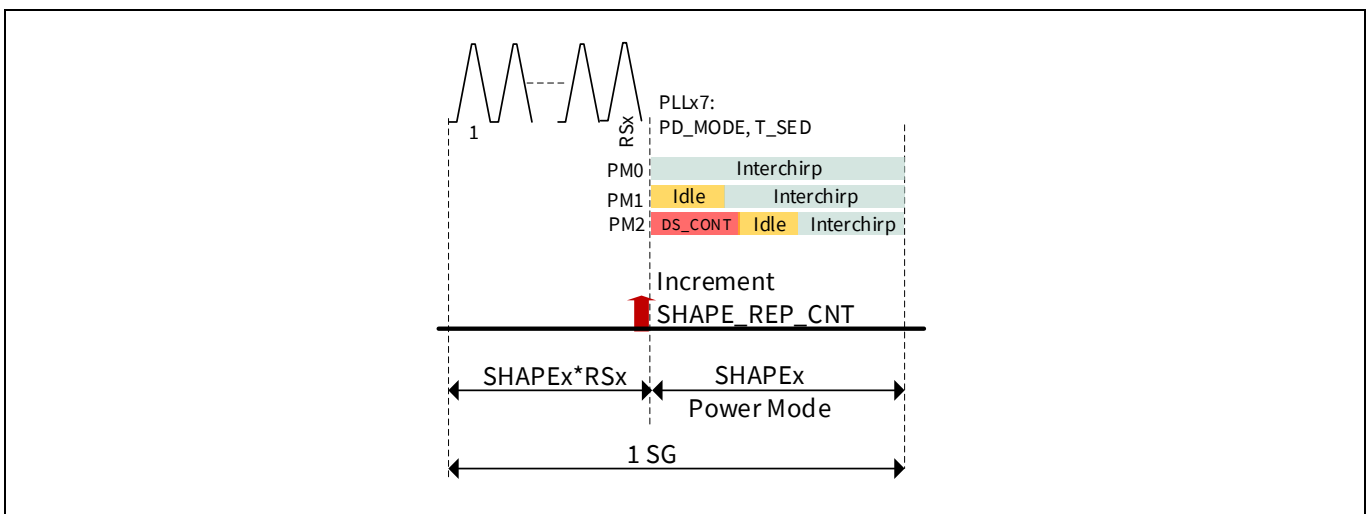


Figure 6 Shape group

Shapes, Frames, and Channel Set Definition

After the last repetitions the FSM will enter, for a period $PLLx7:T_SED$ (see section 4.17), the power mode programmed according to what specified in $PLLx7:PD_MODE$ (see section 4.17).

After a shape group, the shape groups counter $STAT1:SHAPE_GRP_CNT$ is incremented (see section 4.5). In Figure 7 an example of four programmed shape groups is reported. It represents a shape set.

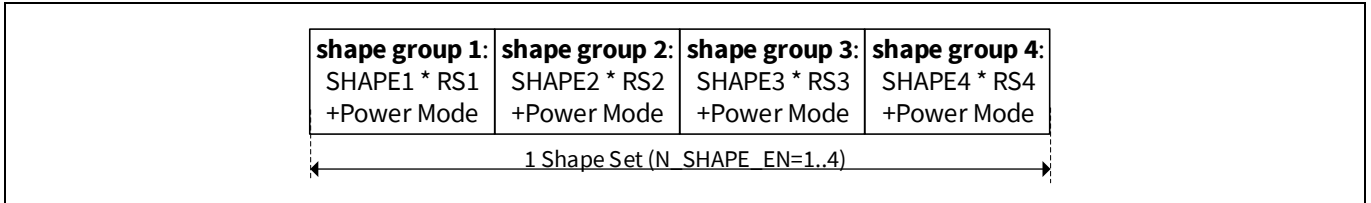


Figure 7 Shape set

Frame

A frame, as shown in Figure 8, is a sequence of shape sets followed by a specific power mode. Each shape set can be then repeated several times. The repetition factor for the shape set is called $REPTx$ and described in 4.12. Each shape is repeated up to $RTx = 2^{REPTx}$ times.

The length of a frame is defined through $CCR2:FRAME_LEN$ (see section 4.14), which is the number of shape groups to be executed.

At each start of a frame, the first shape $SHAPE1$ together with the first channel set, $CSU1+CSC1$ in 0, is loaded.

The number of frame groups the FSM will execute will be:

$$\min(FRAME_LEN, N_SHAPE_EN * RT)$$

With $RT \leq (4096/\text{shape groups})$ and 4095 maximum value allowed for $CCR2:FRAME_LEN$.

After the last shape group in a frame, the power mode from $CCR1:PD_MODE$ is used for the period programmed in $CCR1:T_FED$ instead of $PPLx7:MODE$ for period $PLLx7:T_SED$.

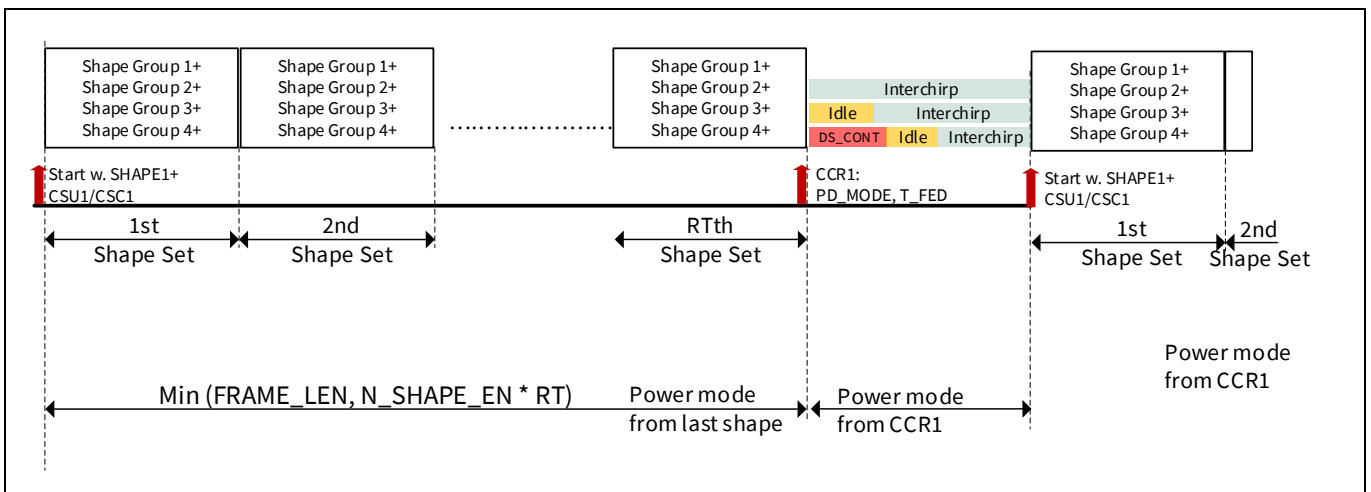


Figure 8 Example of one frame

Maximum Number of Frames

- The overall frame generation starts after the wake-up period with the first frame
- After the last frame $CCR2:MAX_FRAME_CNT$ (see section 4.14) is reached, the FSM will enter the Deep Sleep mode instead of the power mode defined at the end of the last but one frame
 - In order to trigger the chip again, an FSM reset is required.

Shapes, Frames, and Channel Set Definition

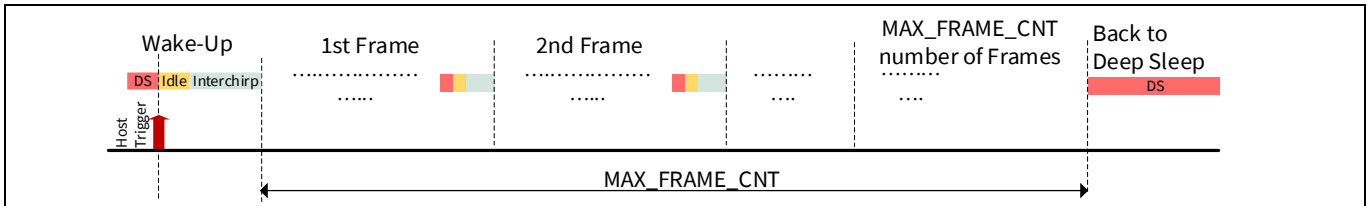


Figure 9 Maximum number of frames

3.2 Channel Set

Each channel set can be then repeated several times. The repetition factor for the channel set is called REPCx and described in section 4.11. Each shape is repeated up to $RCx=2^{REPCx}$ times. There are in total 10 channel sets of 3 different types acting in the specific “modes”. 8 channel sets relate to the shapes (4 shapes x “up” and “down” segment settings) and two to the power modes, Idle and Deep Sleep, respectively:

- Deep Sleep power mode is related to channel set CSDS and CSCDS
- Idle mode is related to channel set CSI and CSCI
- 8 channel sets are defined for the shapes:
 - CSU1 ... CSU4 registers for Upchirp
 - CSD1 ... CSD4 registers for Downchirp
 - CSC1 ... CSC4 channel set registers for up- and Downchirp
- Each shape from above has up to 2 channel sets CSUx and CSDx
 - In case triangular shape is used, CSUx and CSDx are applied
 - In case saw-tooth shape is used, CSD is skipped
- Channel sets are repeating independent of the shapes
- Channel set repetition factor tells how often a single channel set is repeated until the next channel set is loaded
- On the channel set sequence:
 - The lower channel set number is followed by the next higher channel set number
 - In case the highest channel set number is reached, the next channel set loaded is channel set 1
- On the enabling sequence of channel sets:
 - In case not all channel sets are used, the lower number channel sets have to be used
 - In between the enabled channel sets must not be a disabled channel set
 - E.g. 2 channel sets expected: use only CS1 and CS2. In case 3 channel sets are expected, use only CS1, CS2, and CS3
- Start and end of channel set sequences:
 - After reset, the first channel set loaded is CS1.
 - After a frame starts the first channel set loaded will be CS1

Note:

It would be preferable to have REPS=REPC. This is the actual implementation in the driver.

Shapes, Frames, and Channel Set Definition

3.3 Power Modes

The following Figure 10 shows the flow chart on all possible power modes for the FSM.

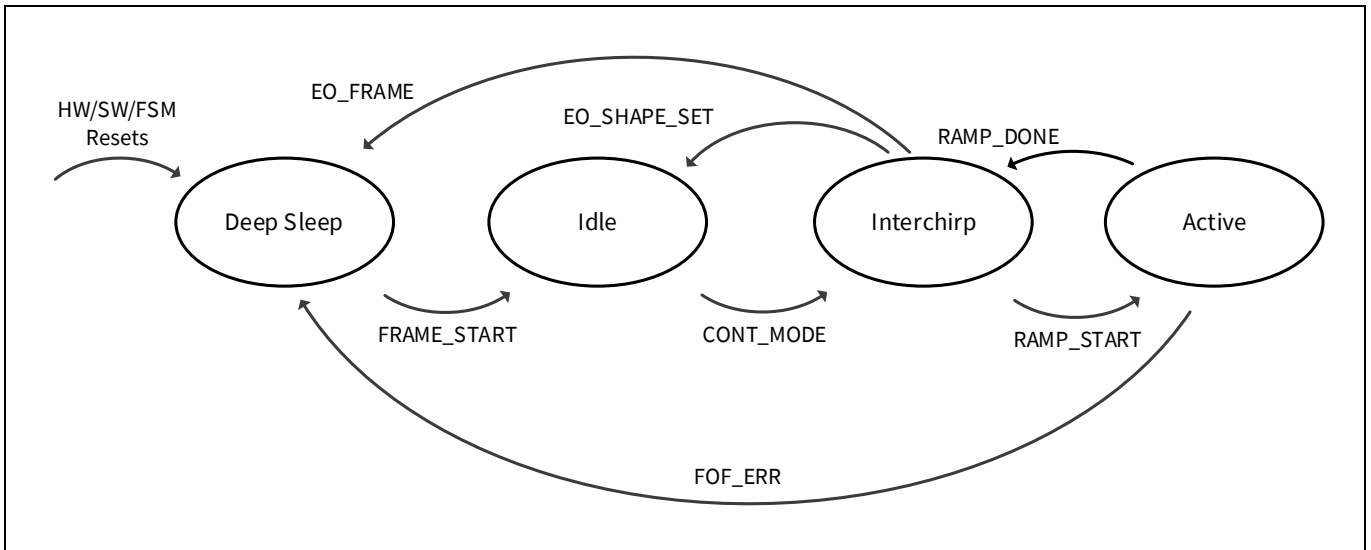


Figure 10 FSM flow chart

Power Management through the Power Modes

The power modes enable the host to have full flexibility on power consumption during each state of radar frame generation. A set of isolation registers (CSCx see section 4.11) enables/disables the different blocks on chip. The power modes are managed by the FSM.

3.3.1 Mode Descriptions

In Active, Idle, and Deep Sleep mode the power mode can be defined in the CSCx register, see section 4.11, for all channel sets: CSC1...4, CSI, CSCDS (CSUx= Channel Set Upchirp, CSDx= Channel Set Downchirp, CSI= Channel Set Idle, CSDS= Channel Set Deep Sleep).

Active Mode Definition:

- During a shape: PLLx7: PD_MODE= 0_b
- Power mode defined through registers CSx (CHS1...CHS4), same mode for Up/Downchirp
- Default Setting: all expected settings are enabled by the host.

Interchirp Mode Definition:

- During a shape: PLLx7: PD_MODE= 0_b
- Power mode basically the same as Active mode, exception: TX1 off (PAOFF).

Idle Mode Definition:

- After a shape: PLLx7: PD_MODE= 1_b
- After a frame: CCR1: PD_MODE= 1_b
- Idle mode is defined through CSCI

Shapes, Frames, and Channel Set Definition

- Wake-up from Deep Sleep for MAIN:TR_WKUP

The Idle mode can be used as a low-power mode in between Interchirp modes or after Deep Sleep mode to further reduce the overall power consumption while not entering the Deep Sleep mode. The wake-up times after Idle mode are faster compared to the ones after Deep Sleep mode.

Entering Deep Sleep Mode:

- After a shape: PLLx7: PD_MODE= 2_D and PLLx7:CONT_MODE= 0_B
- After a frame: CCR1: PD_MODE= 2_D and CCR0:CONT_MODE= 0_B
- Deep sleep mode is defined through CSCDS register (see section 4.11)
- All blocks can be turned off
- Internal 80 MHz clock is also turned off - to achieve extra power saving - when Cont Mode= 0_B otherwise (Cont Mode= 1_B) the clock is kept up to count the internal timer T_FED/T_SED during the deep sleep.
- In order to wake up the FSM from the Deep Sleep, the host has to program:
 - PACR1:OSCCLKEN= 1_B to enable the clock gating
 - Then the first trigger can be applied via FRAME_START.

Entering Deep Sleep Cont Mode:

- After a shape: PLLx7: PD_MODE= 2_D and PLLx7:CONT_MODE= 1_B
- After a frame: CCR1:PD_MODE= 2_D and CCR0:CONT_MODE= 1_B

In case CCR0:CONT_MODE= 1_B is enabled, the wake-up from deep sleep is done automatically. The internal system clock is kept running.

In case of Errors:

If a FIFO overflow condition occurs, the FSM will bring the sensor into the Deep Sleep power mode even if the internal counters are holding the previous value, i.e., the FSM is not reset and a reset is required. In order to reset the FIFO, the host should send at least a MAIN:FIFO_RESET command (see section 4.2).

If the FIFO overflow occurs, the event is reported in FSTAT:FOF_ERR (see section 4.23) or in GSR0:FOF_ERR (see section 4.24).

In this case, the data inside a FIFO can be read from the host as long as no reset occurs.

The flags FSTAT:FOF_ERR and GSR0:FOF_ERR are cleared after a reset.

Note:

Each time the SPI will access the chip, the 80 MHz clock will be enabled internally for synchronization reasons.

3.3.2 Power Modes and Timings

This section presents the power modes and states that can be entered by the BGT60TR13C FSM.

Shapes, Frames, and Channel Set Definition

3.3.3 Wake-Up Phase from “Deep Sleep” to “Idle”

After VDDD power up, the main LDO will require 20 μs to settle VDDC. After the reset, the chip will move to a Deep Sleep state. The following figure describes the timing for waking up the chip.

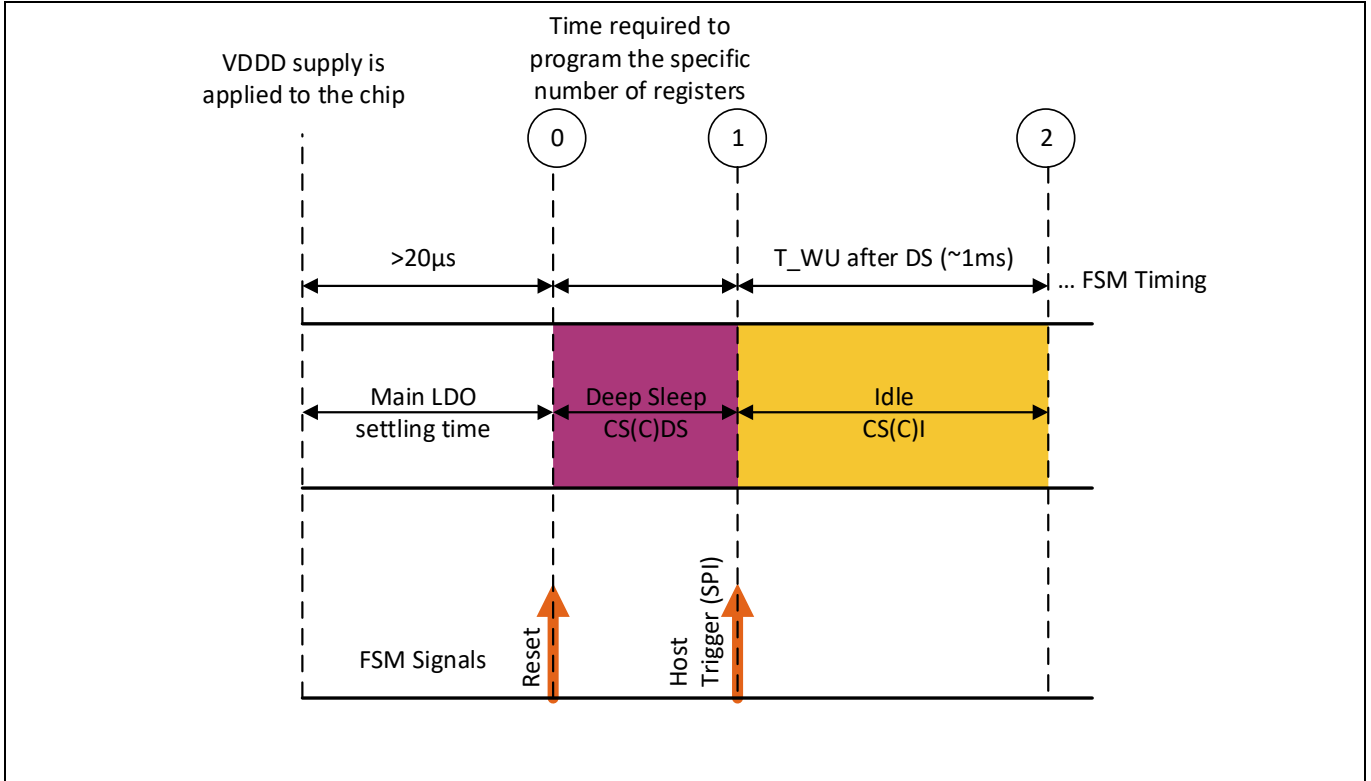


Figure 11 Deep Sleep to Idle transition

Table 14 Transitions from Deep Sleep into Idle

| From # | To # | Description | Signals | Related time |
|--------|------|---|----------|--------------|
| #0 | | Chip is reset by host (see section 5.9). | | |
| #0 | #1 | Host programs all registers needed for expected functionality. | | |
| #1 | | Host enables the oscillator: PACR1:OSCCLKEN= 1 _B to enable the clock gating. | | |
| #1 | | Host starts the first trigger; it can be applied via FRAME_START. | | |
| #1 | | Activate bandgap for MADC. | | |
| #1 | #2 | Time required to settle the ADC BG (charge of external cap). | | T_WU |
| #2 | | Enable PLL, MADC, and SADC. | | |
| #2 | | MADC sends ready signal to FSM. | madc_rdy | |

Shapes, Frames, and Channel Set Definition

3.3.4 Idle to Interchirp then Active

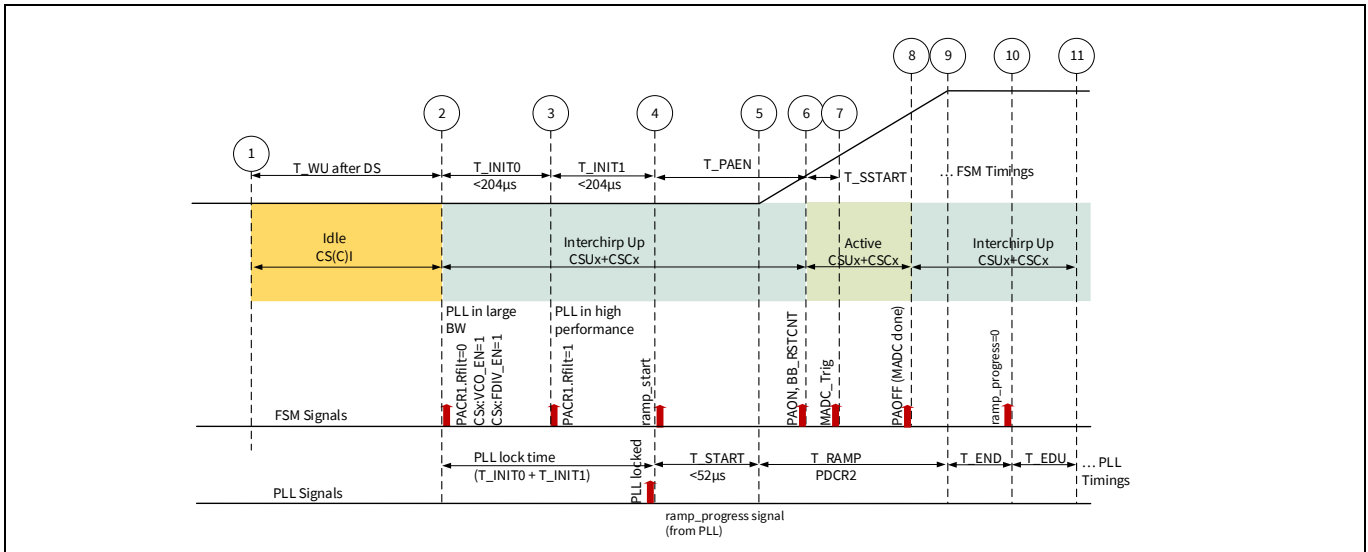


Figure 12 Transition from Idle to Interchirp to Active to Interchirp again

Table 15 Transition from Idle to Interchirp to Active to Interchirp

| Fro m # | To # | Description | Signals | Related time |
|---------|------|--|------------|---------------|
| #1 | | Idle mode is activated. | | |
| #1 | | Host has to enable the bandgap (CSCI:BG_EN= 1 _B in section 4.11). | | |
| #1 | #2 | If Idle mode comes after a Deep Sleep (see transition from Deep Sleep to Idle). | | T_WU |
| #1 | #2 | If Idle mode comes after an Interchirp mode, the bandgap is already running. | | T_SED |
| #2 | | Interchirp Up mode is activated by selecting CSUx + CSCx register depending on the actual channel set (see section 4.10). | | |
| #2 | | Host already enabled the blocks required by the PLL: CSx:VCO_EN= 1 _B CSx:FDIV_EN= 1 _B | | |
| #2 | | FSM sets power mode from CSUx + CSCx. | | |
| #2 | | FSM sets PACR1.RFILTSEL = 0 _B . | | |
| #2 | #3 | The PLL needs some time to initialize the filter settings, 75 μs typ. | | T_INIT0 |
| #3 | #4 | The PLL needs again some time to settle the mode, 15 μs typ. | | T_INIT1 |
| #4 | | PLL sends lock signal to FSM. | PLL_lock | |
| #4 | | FSM gives ramp_start signal to PLL. | RAMP_START | |
| #4 | #5 | PLL needs some settling time before chirp can start. The PLL timer is running in parallel to the FSM timer. T_START will be evaluated during system testing. | | T_START (PLL) |
| #5 | #9 | PLL will run the frequency chirp. | | T_RAMP |

Shapes, Frames, and Channel Set Definition

| From # | To # | Description | Signals | Related time |
|--------|------|---|-----------|--------------|
| | | | | (PLL) |
| #4 | #6 | Some programmable delay | | T_PAEN |
| #6 | | Active mode starts here. | | |
| #6 | | PA is enabled (PAON). Host makes sure that PA is not ON before the chirp starts (>#5). | PAON | |
| #6 | | Baseband reset timer is enabled here based on the CSx:BB_RSTCNT value. | | |
| #6 | #7 | During this phase, the baseband can settle. | | T_SSTART |
| #7 | | MADC is triggered for the active segment (Up). | MADC_TRIG | |
| #7 | | SADC is triggered once here. | | |
| #7 | #8 | MADC starts acquiring the given number of samples (PLLx:APU in section 4.16). See section 3.4. | | T_ACQUx |
| #8 | | MADC has completed the acquisition of the expected number of samples. | MADC_DONE | |
| #8 | | PA is disabled (PAOFF) This condition must be reached before #9 The condition is: $T_PAEN + T_SSTART + T_ACQUx > T_START + T_RAMPx$. | PAOFF | |
| #8 | | Interchirp Up mode is activated again here (CSUx + CSCx). | | |
| #9 | | PLL has completed the Upchirp. | | |
| #9 | #10 | Programmable delay time (eg. 3 μ s). | | T_END |
| #10 | | Ramp completed. | RAMP_DONE | |
| #10 | #11 | Programmable delay time (eg. 1 μ s). | | T_EDU |
| #11 | | Interchirp Up mode ends here. | | |
| #11 | | Interchirp Down mode is programmed here. | | |

Shapes, Frames, and Channel Set Definition

3.3.5 Saw-tooth Shape Timing

In the saw-tooth mode, after a normal Upchirp segment there will be a fast ramp down segment. The saw-tooth shape should be enabled in the bitfield PACR2:FSTDNEN (see section 4.7). For the saw-tooth only CSU (Upchirp) is used (see section 4.10). The time T_EDU (see section 4.16, PLLx2#) is applied after the segment is completed.

See Figure 13.

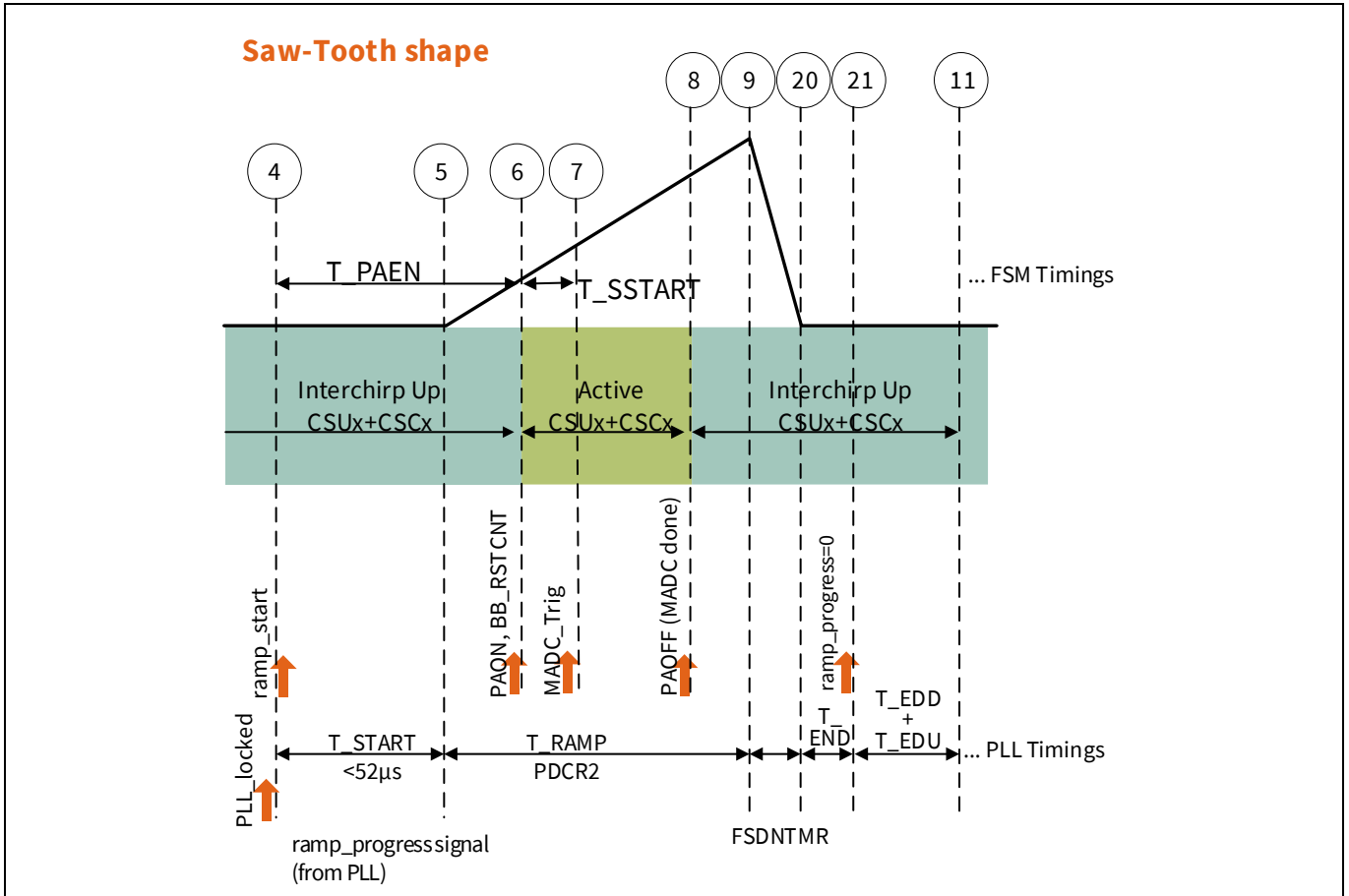


Figure 13 Saw-tooth shape timing

3.3.6 Different Power Modes after Shapes and Shape Groups

After the shape ends with Downchirp, the chip can enter different power modes based on the settings (PLLx, CSx, CSCx, …):

- Interchirp mode in-between shapes – for fast chirp repetitions
- Idle mode after shape groups – in case of longer delay between shape groups and max power saving is required
- Deep Sleep + Idle mode after shape groups in case if very long delays are expected.

3.3.6.1 Idle after Shape or Shape Groups

The Idle mode after a shape or shape groups can be set when a long time in low power mode between shapes is required. Figure 14 represents a time behavior continuation of what presented in Figure 12.

Shapes, Frames, and Channel Set Definition

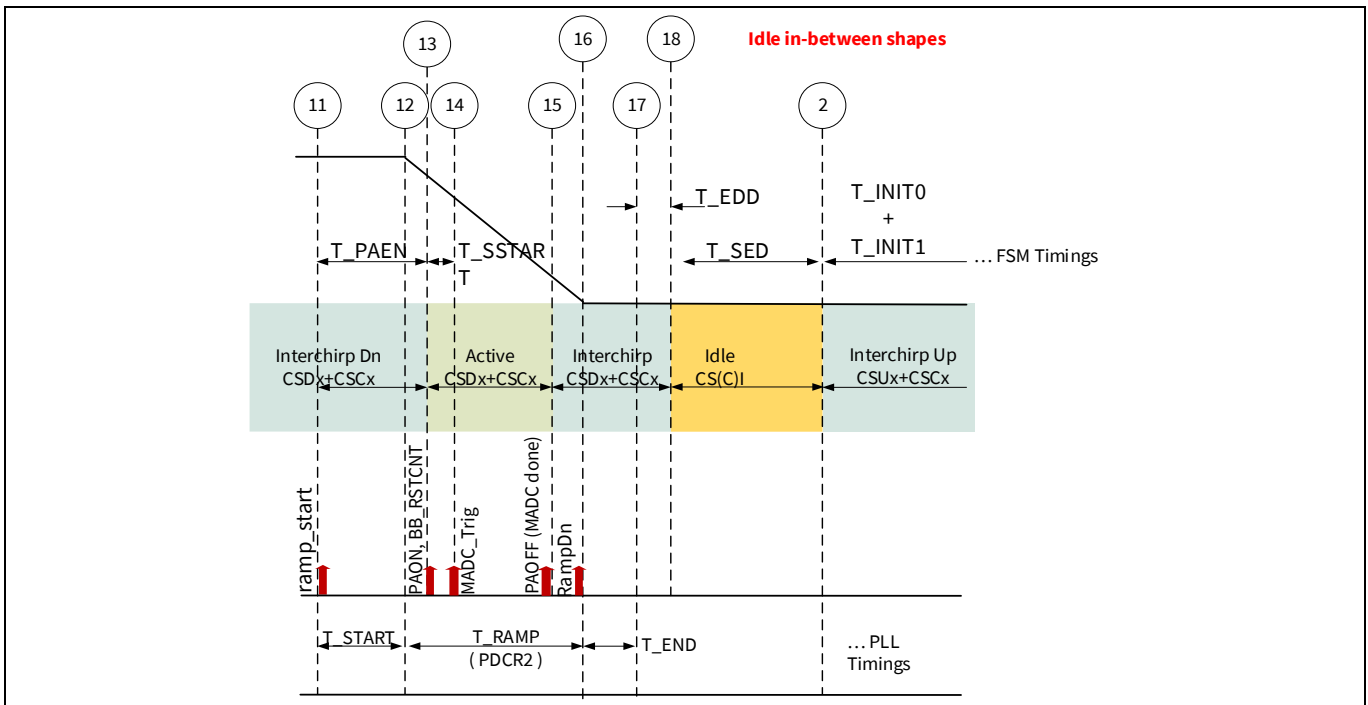


Figure 14 Idle mode after shape groups

Table 16 End of shape and interchirp in-between shapes

| From # | To # | Description | Signals | Related time |
|--------|------|--|------------|--------------|
| #11 | | Interchirp Dn mode is programmed here (CSDx + CSCx). | | |
| #11 | | FSM generates ramp_start signal. | Ramp_start | |
| | | PLL related: | | |
| #11 | #12 | Preparation for Downchirp. | | T_START |
| #12 | #16 | Downchirp time. | | T_RAMP |
| #16 | #17 | Some delay after Downchirp is completed. | | T_END |
| | | FSM related: | | |
| #11 | #13 | Some delay (see above T_PAEN). | | T_PAEN |
| #13 | | Active mode is entered with settings from previous Interchirp Dn mode (CSDx+CSCx). | | |
| #13 | | PA is enabled (PAON). Host ensures that PA is not ON before the chirp starts (>#12). | PAON | |
| #13 | | Baseband reset timer is enabled here based on the CSx:BB_RSTCNT value. | | |
| #13 | #14 | During this phase, the baseband can settle | | T_SSTAR |
| #14 | #15 | MADC starts acquiring the given number of samples (PLLx:APD in section 4.16). See section 3.4. | MADC_TRIG | T_ACQDx |
| #15 | | MADC has completed the acquisition of the expected number of samples. | MADC_DONE | |
| #15 | | PA is disabled (PAOFF) This condition must be reached before #16 The condition is: | PAOFF | |

Shapes, Frames, and Channel Set Definition

| From # | To # | Description | Signals | Related time |
|--------|------|--|---------|--------------|
| | | $T_{PAEN} + T_{SSTART} + T_{ACQDx} > T_{START} + T_{RAMPx}$. | | |
| #15 | | Interchirp Dn mode is activated again here ($CSDx + CSCx$). | | |
| #14 | #16 | FSM waits for PLL if ramp down to calculate #17 (TMREND). | | |
| #16 | | PLL signals the end of the Downchirp (ramp progress). | RampDN | |
| #17 | #18 | Time delay programmed by the host. | | T_{EDD} |
| #18 | #2 | Time programmed by the host to stay in Idle mode. | | T_{SED} |
| #2 | | Same state #2 as in Figure 12 starts here. | | |

3.3.6.2 Interchirp in-between Shapes

Interchirp between shapes can be set when the required gap between two shapes is relatively small (< 25 μs).

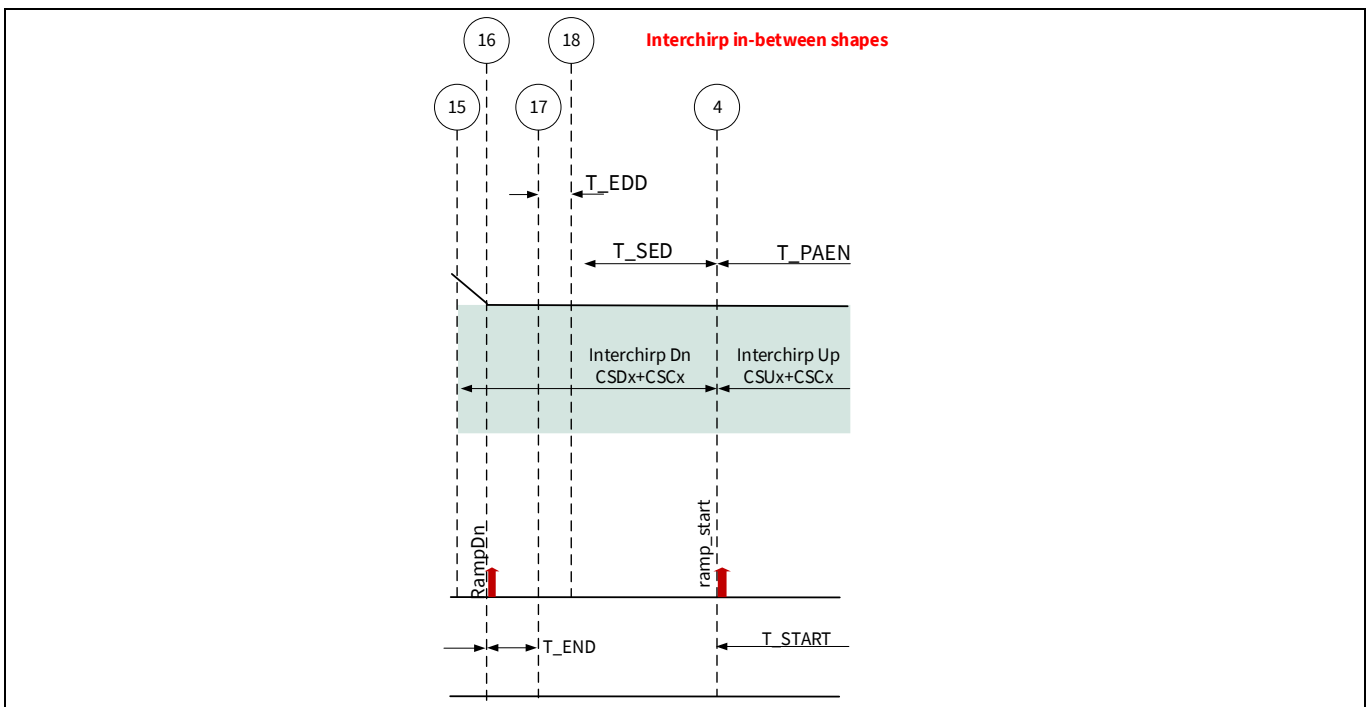


Figure 15 Interchirp in-between shapes

Table 17 Interchirp in-between shapes

| From # | To # | Description | Signals | Related time |
|--------|------|--|---------|--------------|
| #15 | | Interchirp Dn ($CSDx + CSCx$) is activated after Active mode. | | |
| #16 | | PLL signals the end of the Downchirp (ramp progress). | RampDN | |
| #16 | #17 | Some delay after Downchirp is completed. | | T_{END} |
| #17 | | PLL has completed its action. | | |
| #17 | #18 | Time delay programmed by the host. | | T_{EDD} |
| #18 | #4 | The chip will remain in the same interchirp power state for the provided amount of time (T_{EDD}). | | T_{SED} |
| #4 | | Same state #4 as in Figure 12 starts here. | | |
| #4 | | Interchirp Up mode programmed by FSM here ($CSUx + CSCx$). | | |

Shapes, Frames, and Channel Set Definition

3.3.6.3 Deep Sleep Continuous + Idle wake-up after shape groups

In Deep Sleep Cont(inuous) mode after the shape group is completed, the FSM wakes up automatically after the programmed time T_{SED} . The internal clock is kept running during this time. Deep Sleep Cont is the only deep sleep power mode possible between shape groups.

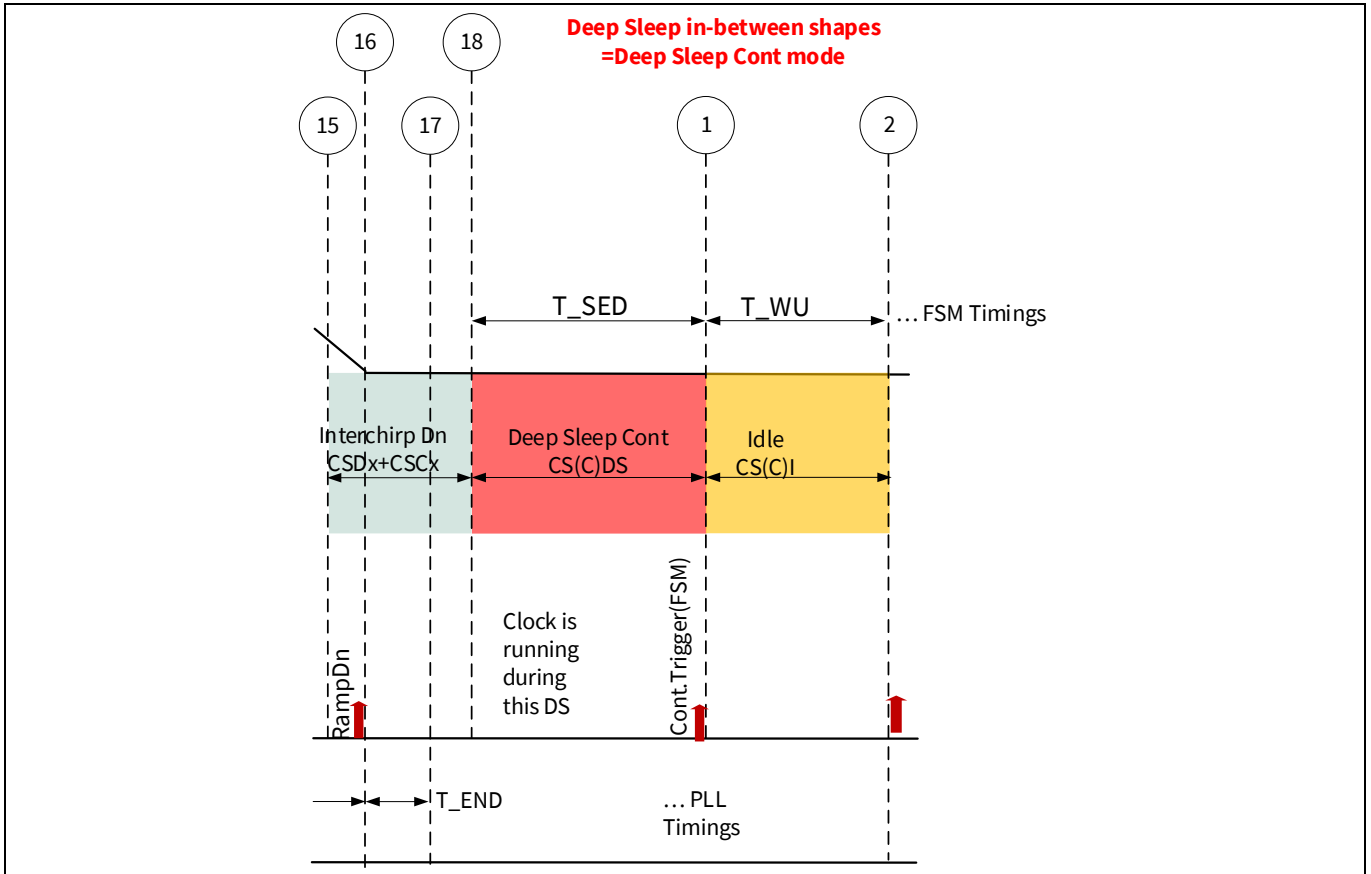


Figure 16 Deep Sleep + Idle wake-up after shape groups

Shapes, Frames, and Channel Set Definition

Table 18 Deep Sleep Cont + Idle wake-up after shape groups

| From # | To # | Description | Signals | Related time |
|--------|------|--|---------|--------------|
| #16 | #17 | Some delay after Downchirp is completed. | | T_END |
| #17 | | PLL is completed its action. | | |
| #17 | #18 | Time delay programmed by the host. | | T_EDD |
| #17 | | Deep Sleep Cont mode is enabled. The difference to the normal Deep Sleep mode is, the f_{SYS_CLK} is kept running to count the internal timers. | | |
| #17 | | The internal system clock f_{SYS_CLK} is kept running. | | |
| #18 | #1 | The chip will be in Deep Sleep Cont mode. | | T_SED |
| #1 | | Continuous trigger coming from the FSM. | | |
| #1 | | Same start-up procedure as Figure 12 starts here. | | |

3.4 System Constraints

3.4.1 MADC Sampling Timing Conditions and Calculations

The number of MADC samples during a frequency chirp (up or down segment of the shape) should fulfil some specific requirements.

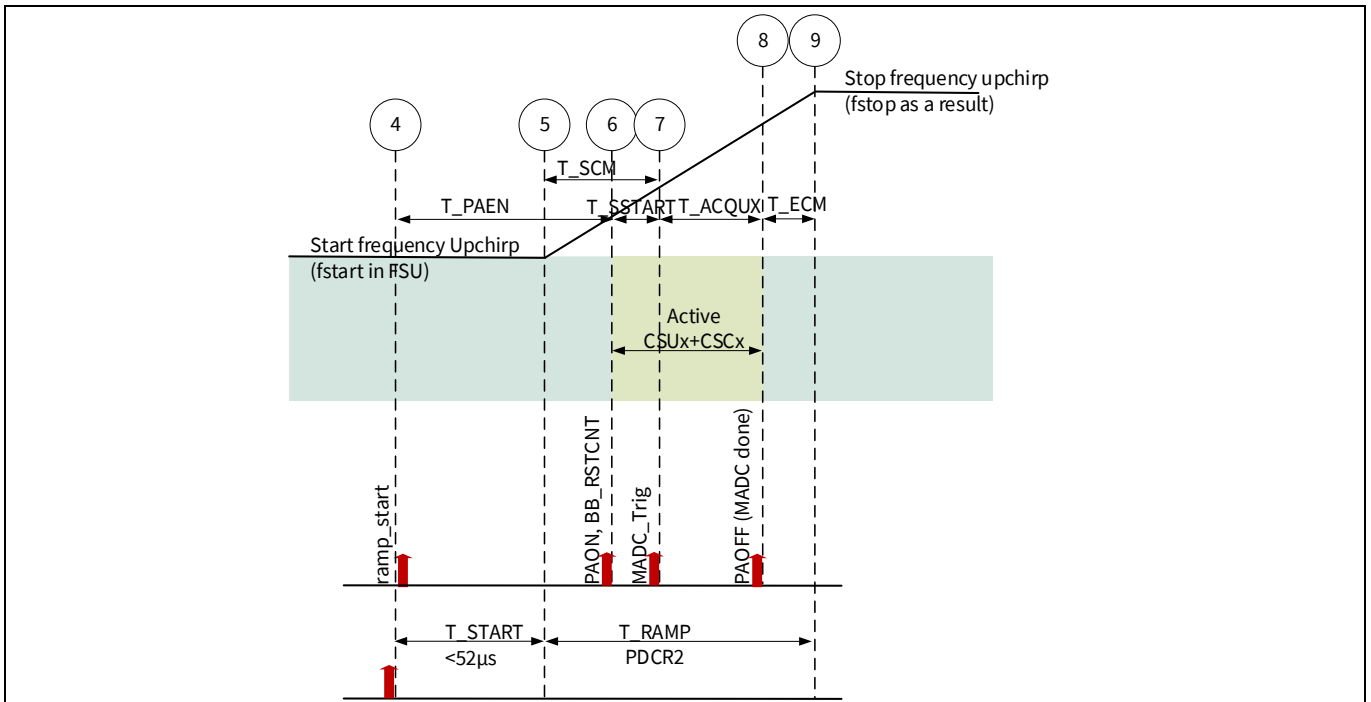


Figure 17 T_RAMP timing conditions

Shapes, Frames, and Channel Set Definition

Table 19 T_RAMP Timing Conditions

| From # | To # | Description | Signals | Related time |
|--------|------|--|---------|-----------------|
| #4 | | PLL starts counting. | | |
| #4 | #5 | PLL starts. | | T_START |
| #5 | #9 | PLL performs the frequency Upchirp, chirp from fstart (PLLx[1]:FSU) to fstop. | | T_RAMP |
| #6 | #8 | Active Phase. | | |
| #4 | #7 | Time to start the MADC. | | T_PAEN+T_SSTART |
| #7 | #8 | MADC sampling time for Upchirp raw data. | | T_ACQUX |
| #8 | #9 | End chirp margin T_ECM is needed to avoid transmission out of band. Empirically derived in System. | | T_ECM |
| #5 | #7 | Start chirp margin T_SCM is needed to avoid transmission out of band. Empirically derived in System. | | T_SCM |

ADC Sampling Rate $f_{\text{ADC_SAMP}}$ (see section 8.5.5):

$$f_{\text{ADC_SAMP}} = f_{\text{ADC_CLK}} / \text{ADC_DIV}$$

ADC acquisition time for Upchirp T_ACQUx:

$$T_{\text{ACQUX}} = \text{APUx} / f_{\text{ADC_SAMP}}$$

Where APU is the number of samples.

End chirp margin T_ECM is tested in system but assumed to be more than 0 μs :

$$T_{\text{ECM}} > 0\mu\text{s}, T_{\text{SCM}} > 0\mu\text{s}$$

Condition on the data acquisition start time:

$$T_{\text{PAEN}} + T_{\text{SSTART}} > T_{\text{START}}$$

Considering the start chirp margin TCM at the beginning:

$$T_{\text{PAEN}} + T_{\text{SSTART}} - T_{\text{SCM}} = T_{\text{START}}$$

Overall timing equation:

$$T_{\text{PAEN}} + T_{\text{SSTART}} + T_{\text{ACQUX}} + T_{\text{ECM}} = T_{\text{START}} + T_{\text{RAMP}}$$

Example, fixed number of samples:

In case the user expects a fixed number of samples, the APU is set and T_RAMP is calculated.

The time for a frequency ramp T_RAMP is:

$$T_{\text{RAMP}} (\text{PLLx2\#:RTU in section 4.16}) = T_{\text{PAEN}} + T_{\text{SSTART}} + T_{\text{ACQUX}} + T_{\text{ECM}} - T_{\text{START}}$$

Example, Fixed chirp-time (T_RAMP):

$$T_{\text{ACQUX}} = T_{\text{RAMP}} - (T_{\text{SCM}} + T_{\text{ECM}})$$

$$\text{APU} = (T_{\text{ACQUX}} * f_{\text{ADC_SAMP}}),$$

$$\text{APU} (\text{PLLx3\#:APU in section 4.16}) = (T_{\text{RAMP}} - (T_{\text{SCM}} + T_{\text{ECM}})) * (f_{\text{SYS_CLK}} / \text{ADC_DIV})$$

Shapes, Frames, and Channel Set Definition

3.4.2 PLL Frequency Ramp Setup

The RF frequency ramps generated by the PLL are controlled through the PLLx registers (see section 4.16), where the bit fields FSU, RSU and RTU control the Upchirp of a shape and the registers FSD, RSD and RTD control the down chirp of a shape. The following description refers only to up chirp ramp setup. The given formulas can be adopted to down chirp ramps by replacing FSU by FSD, RSU by RSD and RTU by RTD.

Each RF frequency ramp is defined by the start frequency programmed to FSU, the ramp slope programmed to RSU and the ramp time programmed to RTU. It must be noted that the slope in RSU is specified as frequency increment per clock cycle while the ramp time in RTU is specified as number of steps where a single step means 8 clock cycles. The relation between RSU and RTU is shown in Figure 18.

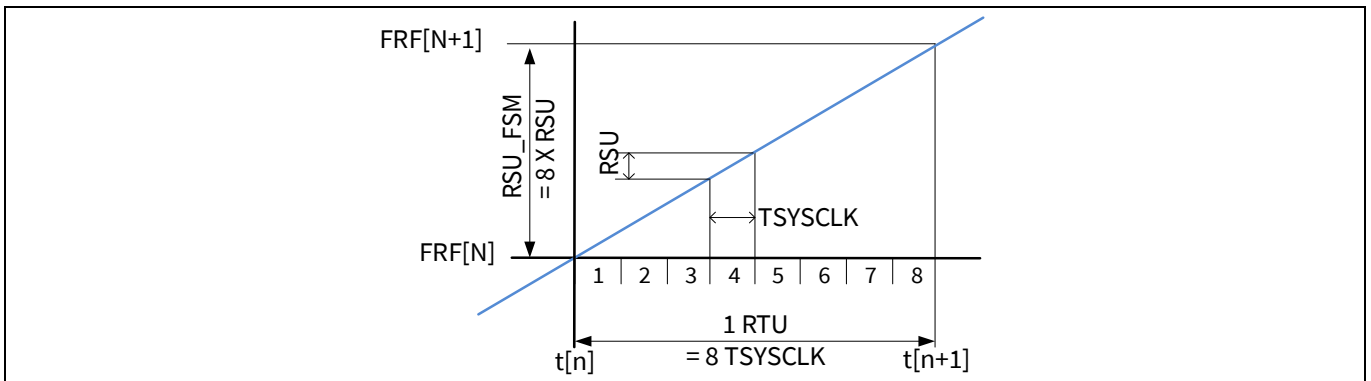


Figure 18 Relationship between RTU and RSU

The value N_{FSU} that is programmed to FSU bit field to control the ramp start frequency is a signed 2's complement number in the range of $[-2^{23} \dots (2^{23} - 1)]$. The relation between the RF frequency f_{RF} and N_{FSU} is given by:

$$f_{RF} = 8f_{SYSCLK} \left[4(N_{DIVSET} + 2) + 8 + \frac{N_{FSU}}{2^{20}} \right]$$

where f_{SYSCLK} is the frequency of the reference clock oscillator (typically 80 MHz) and N_{DIVSET} is the value programmed to the bit field DIVSET in register PACR2 (default 20, see section 4.7). Accordingly, the value N_{FSU} can be calculated by this formula:

$$N_{FSU} = 2^{20} \left[\frac{f_{RF}}{8f_{SYSCLK}} - 4(N_{DIVSET} + 2) - 8 \right]$$

The value N_{RSU} that is programmed to RSU bit field to control the frequency increment per clock cycle is also a signed 2's complement number in the range of $[-2^{23} \dots (2^{23} - 1)]$. The relation between the RF frequency increment Δf_{RF} and N_{RSU} is given by:

$$\Delta f_{RF} = 8f_{SYSCLK} \frac{N_{RSU}}{2^{20}}$$

or

Shapes, Frames, and Channel Set Definition

$$N_{RSU} = 2^{20} \frac{\Delta f_{RF}}{8f_{SYSCLK}}$$

Note:

Both slope bit fields *RSU* and *RSD* can hold positive and negative values, so an up chirp can also be programmed with a falling ramp and a down chirp can be programmed with a rising ramp. The naming convention “up-chirp” and “down-chirp” are based on the assumption that a triangle shape always starts with the rising ramp. Therefore, regardless of the actual ramp slope the up-chirp registers always refer to the first chirp of a shape and the down chirp registers always refer to the 2nd chirp of a shape in triangle mode.

PLL Setup Example 1 ($f_{SYSCLK} = 80 \text{ MHz}$)

With a reference clock frequency of 80 MHz the recommended value for N_{DIVSET} is 20, the default values. With these parameters the conversion formulas simplify to:

$$N_{FSU} = 2^{20} \left[\frac{f_{RF}}{640 \text{ MHz}} - 96 \right]$$

and

$$N_{RSU} = 2^{20} \frac{\Delta f_{RF}}{640 \text{ MHz}}$$

With the PLL's 24 bit 2's complement frequency registers the total programmable RF frequency range is $56.32 \text{ GHz} \leq f_{RF} \leq 66.559 \text{ GHz}$. This may be a wider range than the effectively achievable frequency range (see section 6 for PLL specification).

To achieve a frequency ramp from 58 GHz to 63.5 GHz in 36 μs , the FSU register is programmed to:

$$N_{FSU} = 2^{20} \left[\frac{58 \text{ GHz}}{640 \text{ MHz}} - 96 \right] = -5636096 \hat{=} AA0000_{hex}$$

The ramp time bit field RTU is programmed to:

$$N_{RTU} = \frac{t_{ramp}}{8 \cdot T_{SYSCLK}} = 36 \mu\text{s} \frac{80 \text{ MHz}}{8} = 360.$$

The frequency increment per clock cycle result to:

$$\Delta f_{RF} = \frac{f_{RF,end} - f_{RF,start}}{8 \cdot N_{RTU}} = \frac{63.5 \text{ GHz} - 58 \text{ GHz}}{8 \cdot 360} = \frac{5.5 \text{ GHz}}{2880} = 1.9097\bar{2} \text{ MHz}.$$

Accordingly, the bit field RSU is programmed to:

$$N_{RSU} = 2^{20} \frac{1.9097\bar{2} \text{ MHz}}{640 \text{ MHz}} = 3128.\bar{8} \hat{=} 3128 \hat{=} 000C38_{hex}$$

Due to rounding errors from the above calculation, the ramp will end at a slightly different end frequency:

$$f_{RF,end} = f_{RF,start} + 8 \cdot N_{RTU} \cdot \frac{640 \text{ MHz}}{2^{20}} N_{RSU} = 63.4984375 \text{ GHz}.$$

Shapes, Frames, and Channel Set Definition

PLL Setup Example 2 ($f_{SYSCLK} = 76.8\text{ MHz}$)

With a reference clock frequency of 76.8 MHz the recommended value for N_{DIVSET} is 21. With these parameters the conversion formulas simplify to:

$$N_{FSU} = 2^{20} \left[\frac{f_{RF}}{614.4\text{ MHz}} - 100 \right]$$

and

$$N_{RSU} = 2^{20} \frac{\Delta f_{RF}}{614.4\text{ MHz}}$$

With the PLL's 24 bit 2's complement frequency registers the total programmable RF frequency range is $56.5248\text{ GHz} \leq f_{RF} \leq 66.3552\text{ GHz}$. This may be a wider range than the effectively achievable frequency range (see section 6 for PLL specification).

To achieve a frequency ramp from 58 GHz to 63.5 GHz in $36\ \mu\text{s}$, the FSU register is programmed to:

$$N_{FSU} = 2^{20} \left[\frac{58\text{ GHz}}{614.4\text{ MHz}} - 100 \right] = -5870933.\bar{3} \cong -5870933 \cong A66AAB_{hex}.$$

The ramp time bit field RTU is programmed to:

$$N_{RTU} = \frac{t_{ramp}}{8 \cdot T_{SYSCLK}} = 36\ \mu\text{s} \frac{76.8\text{ MHz}}{8} = 345.6 \cong 346.$$

The frequency increment per clock cycle result to:

$$\Delta f_{RF} = \frac{f_{RF,end} - f_{RF,start}}{8 \cdot N_{RTU}} = \frac{63.5\text{ GHz} - 58\text{ GHz}}{8 \cdot 346} = \frac{5.5\text{ GHz}}{2768} = 1.986994\text{ MHz}.$$

Accordingly the bit field RSU is programmed to:

$$N_{RSU} = 2^{20} \frac{1.986994\text{ MHz}}{614.4\text{ MHz}} = 3391.13680 \cong 3391 \cong 000D3F_{hex}.$$

Due to rounding errors from the above calculation, the ramp will end at a slightly different end frequency:

$$f_{RF,start} = 614.4\text{ MHz} \left[100 + \frac{N_{FSU}}{2^{20}} \right] = 58.0000002\text{ GHz}$$

$$f_{RF,end} = f_{RF,start} + 8 \cdot N_{RTU} \cdot \frac{614.4\text{ MHz}}{2^{20}} N_{RSU} = 63.499778315\text{ GHz}.$$

BGT60TR13C Registers

4 BGT60TR13C Registers

An array of registers visible via the SPI is used to control and program the states of the different blocks inside the chip.

4.1 Register List

The registers are arranged in blocks of 24 bits each. Each block is identified by its unique address. The registers are accessed from the SPI module. The bit fields from each register are arranged in MSB first order.

Table 20 The following table gives an overview on the BGT60TR13C registers. Register Overview / Address Table

| Register Address | Register Name | Description | RST | Section |
|------------------|---------------|-------------------------------------|-----|---------|
| 0x00 | MAIN | Main register | | 4.2 |
| 0x01 | ADC0 | MADC control register | | 4.3 |
| 0x02 | CHIP_ID | Digital and RF version | | 4.3 |
| 0x03 | STAT1 | Status register 1 | | 4.5 |
| 0x04 | PACR1 | PLL analog control register 1 | | 4.6 |
| 0x05 | PACR2 | PLL analog control register 2 | | 4.7 |
| 0x06 | SFCTL | SPI and FIFO Control | | 4.8 |
| 0x07 | SADC_CTRL | Sensor ADC ctrl reg | | 4.9 |
| 0x08 | CSI_0 | Channel set idle mode 0 | | 4.10 |
| 0x09 | CSI_1 | Channel set idle mode 1 | | 4.10 |
| 0x0A | CSI_2 | Channel set idle mode 2 | | 4.10 |
| 0x0B | CSCI | Channel set control idle mode | | 4.11 |
| 0x0C | CSDS_0 | Channel set deep sleep mode 0 | | 4.10 |
| 0x0D | CSDS_1 | Channel set deep sleep mode 1 | | 4.10 |
| 0x0E | CSDS_2 | Channel set deep sleep mode 2 | | 4.10 |
| 0x0F | CSCDS | Channel set control deep sleep mode | | 4.11 |
| 0x10 | CSU1_0 | Channel set 1 (up) | | 4.10 |
| 0x11 | CSU1_1 | Channel set 1 (up) | | 4.10 |
| 0x12 | CSU1_2 | Channel set 1 (up) | | 4.10 |
| 0x13 | CSD1_0 | Channel set 1 (down) | | 4.10 |
| 0x14 | CSD1_1 | Channel set 1 (down) | | 4.10 |
| 0x15 | CSD1_2 | Channel set 1 (down) | | 4.10 |
| 0x16 | CSC1 | Channel set control 1 (up/dn) | | 4.11 |
| 0x17 | CSU2_0 | Channel set 2 (up) | | 4.10 |
| 0x18 | CSU2_1 | Channel set 2 (up) | | 4.10 |
| 0x19 | CSU2_2 | Channel set 2 (up) | | 4.10 |
| 0x1A | CSD2_0 | Channel set 2 (down) | | 4.10 |
| 0x1B | CSD2_1 | Channel set 2 (down) | | 4.10 |
| 0x1C | CSD2_2 | Channel set 2 (down) | | 4.10 |

BGT60TR13C Registers

| | | | |
|------|--------|-------------------------------|------|
| 0x1D | CSC2 | Channel set control 2 (up/dn) | 4.11 |
| 0x1E | CSU3_0 | Channel set 3 (up) | 4.10 |
| 0x1F | CSU3_1 | Channel set 3 (up) | 4.10 |
| 0x20 | CSU3_2 | Channel set 3 (up) | 4.10 |
| 0x21 | CSD3_0 | Channel set 3 (down) | 4.10 |
| 0x22 | CSD3_1 | Channel set 3 (down) | 4.10 |
| 0x23 | CSD3_2 | Channel set 3 (down) | 4.10 |
| 0x24 | CSC3 | Channel set control 3 (up/dn) | 4.11 |
| 0x25 | CSU4_0 | Channel set 4 (up) | 4.10 |
| 0x26 | CSU4_1 | Channel set 4 (up) | 4.10 |
| 0x27 | CSU4_2 | Channel set 4 (up) | 4.10 |
| 0x28 | CSD4_0 | Channel set 4 (down) | 4.10 |
| 0x29 | CSD4_1 | Channel set 4 (down) | 4.10 |
| 0x2A | CSD4_2 | Channel set 4 (down) | 4.10 |
| 0x2B | CSC4 | Channel set control 4 (up/dn) | 4.11 |
| 0x2C | CCR0 | Chirp control register 0 | 4.12 |
| 0x2D | CCR1 | Chirp control register 1 | 4.13 |
| 0x2E | CCR2 | Chirp control register 2 | 4.14 |
| 0x2F | CCR3 | Chirp control register 3 | 4.15 |
| 0x30 | PLL1_0 | FSU1 – shape 1 | 4.16 |
| 0x31 | PLL1_1 | RSU1 – shape 1 | 4.16 |
| 0x32 | PLL1_2 | RTU1 – Shape 1 | 4.16 |
| 0x33 | PLL1_3 | AP1 – shape 1 | 4.16 |
| 0x34 | PLL1_4 | FSD1 – shape 1 | 4.16 |
| 0x35 | PLL1_5 | RSD1 – shape 1 | 4.16 |
| 0x36 | PLL1_6 | RTD1 – shape 1 | 4.16 |
| 0x37 | PLL1_7 | SCR – shape 1 | 4.17 |
| 0x38 | PLL2_0 | FSU1 – shape 2 | 4.16 |
| 0x39 | PLL2_1 | RSU1 – shape 2 | 4.16 |
| 0x3A | PLL2_2 | RTU1 – shape 2 | 4.16 |
| 0x3B | PLL2_3 | AP1 – shape 2 | 4.16 |
| 0x3C | PLL2_4 | FSD1 – shape 2 | 4.16 |
| 0x3D | PLL2_5 | RSD1 – shape 2 | 4.16 |
| 0x3E | PLL2_6 | RTD1 – shape 2 | 4.16 |
| 0x3F | PLL2_7 | SCR – shape 2 | 4.17 |
| 0x40 | PLL3_0 | FSU1 – shape 3 | 4.16 |
| 0x41 | PLL3_1 | RSU1 – shape 3 | 4.16 |
| 0x42 | PLL3_2 | RTU1 – shape 3 | 4.16 |
| 0x43 | PLL3_3 | AP1 – shape 3 | 4.16 |
| 0x44 | PLL3_4 | FSD1 – shape 3 | 4.16 |
| 0x45 | PLL3_5 | RSD1 – shape 3 | 4.16 |

BGT60TR13C Registers

| | | | |
|---------|-------------|----------------------------|------|
| 0x46 | PLL3_6 | RTD1 – shape 3 | 4.16 |
| 0x47 | PLL3_7 | SCR – shape 3 | 4.17 |
| 0x48 | PLL4_0 | FSU1 – shape 4 | 4.16 |
| 0x49 | PLL4_1 | RSU1 – shape 4 | 4.16 |
| 0x4A | PLL4_2 | RTU1 – shape 4 | 4.16 |
| 0x4B | PLL4_3 | AP1 – shape 4 | 4.16 |
| 0x4C | PLL4_4 | FSD1 – shape 4 | 4.16 |
| 0x4D | PLL4_5 | RSD1 – shape 4 | 4.16 |
| 0x4E | PLL4_6 | RTD1 – shape 4 | 4.16 |
| 0x4F | PLL4_7 | SCR – shape 4 | 4.17 |
| 0x55 | RFT0 | RF test register 0 | 4.19 |
| 0x56 | RFT1 | RSVD | 4.20 |
| 0x59 | PLL_DFT0 | PLL DFT register 0 | 4.18 |
| 0x5D | STAT0 | Status register 0 | 4.21 |
| 0x5E | SADC_RESULT | Sensor ADC result register | 4.22 |
| 0x5F | FSTAT | FIFO status register | 4.23 |
| >= 0x60 | | FIFO access | |

Note: Reserved bits (RSVD) in the registers should not be modified. They should be kept in the default/reset state unless otherwise specified.

4.1.1 Abbreviations

Access modes on the registers:

- R ... Readable register or bit field
- W ... Writeable register or bit field
- S ... Status bit can be set to readable mode “R”
- RSVD ... Reserved value which is not assigned at the moment

4.2 MAIN – Main Register

This register controls the top-level behavior of the chip.

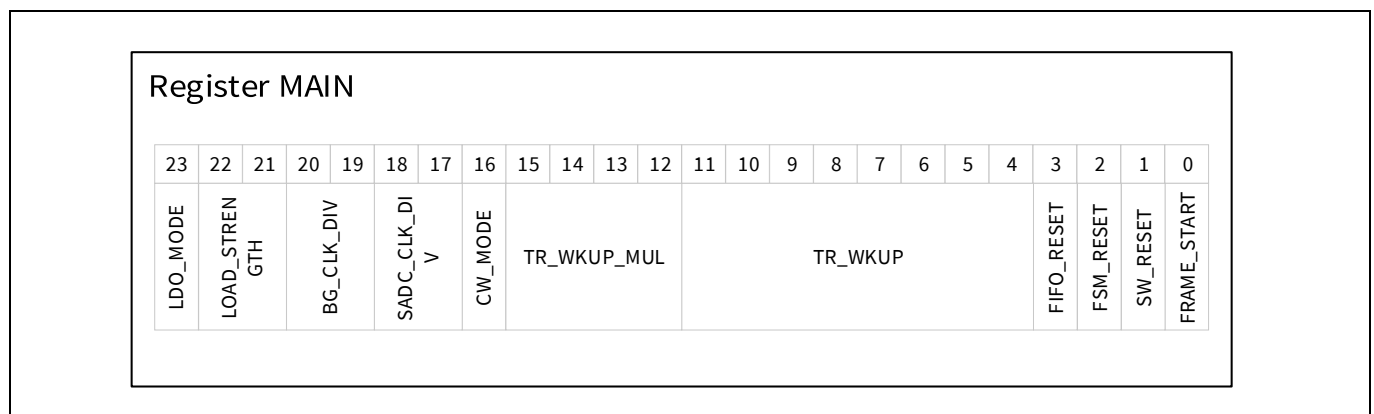


Figure 19 MAIN register

BGT60TR13C Registers

Table 21 MAIN: Register Description

| Symbol | Bits | Type | Description | RST |
|---------------|-------|------|---|----------------|
| LDO_MODE | 23 | RW | The LDO settling time is defined by the LDO_MODE: 0 _B ... Low power (50 µA), slow settling time 1 _B ... High power (100 µA), fast settling time | 0 _B |
| LOAD_STRENGTH | 22:21 | RW | Current spikes, overshoots and undershoots can occur on the VDDC during FSM transitions. Those can be smooth by applying a dummy load at the output of the LDO: 0 _D ... Disabled 1 _D ... 100 µA (current in the dummy load) 2 _D ... 200 µA (current in the dummy load) 3 _D ... 400 µA (current in the dummy load) | 0 _D |
| BG_CLK_DIV | 20:19 | RW | Bandgap clock divider Bandgap clock frequency divider value: 0 _D ... Bandgap clock off 1 _D ... Divider value is 1 2 _D ... Divider value is 2 3 _D ... Divider value is 4 Note: not “clock tree balanced” | 3 _D |
| SADC_CLKDIV | 18:17 | RW | SADC clock divider provides the system clock for the sensing ADC. The divider value is defined as: 0 _D ... SADC clock off 1 _D ... Divider value is 1 2 _D ... Divider value is 2 3 _D ... Divider value is 4 | 3 _D |
| CW_MODE | 16 | RW | Set to 1 _B : “Continuous Wave” mode: no shapes are executed but PLL / RF / ADC runs with values programmed in PDFT[0,1] registers and CS1. | 0 _B |
| TR_WKUP_MUL | 15:12 | RW | Timer multiplier factor for wake-up time delay T_WU. Precise formula provided under MAIN:TR_WKUP. | 0 _D |
| TR_WKUP | 11:4 | RW | Coefficient to calculate T_WU: 0 _D ... T _{SYS_CLK} From 1 _D to 255 _D the time delay T_WU is calculated as follows: $T_WU = (TR_WKUP \times 2^{TR_WKUP_MUL \times 8 + TR_WKUP_MUL + 3}) \times T_{SYS_CLK}$ In typical use-case T_WUTYP= 1ms. | 0 _D |
| FIFO_RESET | 3 | W | Clears and resets data_fifo: 0 _B ... No change 1 _B ... Reset the FIFO and return back to 0 | 0 _B |
| FSM_RESET | 2 | W | Control FSM reset: 0 _B ... No change 1 _B ... Reset the control FSM and return back to 0 _B | 0 _B |
| SW_RESET | 1 | W | Software reset: | 0 _B |

BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|-------------|------|------|---|----------------|
| | | | 0 _B ... No change 1 _B ... Reset the register settings and return back to 0 _B | |
| FRAME_START | 0 | W | Starts frame generation. After the frame generation is started writing 1 _B : 0 _B ... No effect 1 _B ... Starts the frame generation It can be stopped by an FSM_RESET. | 0 _B |

4.3 ADC0 – MADC Control Register

The bits in this register are used to set properly the ADCs in the Rx chain.

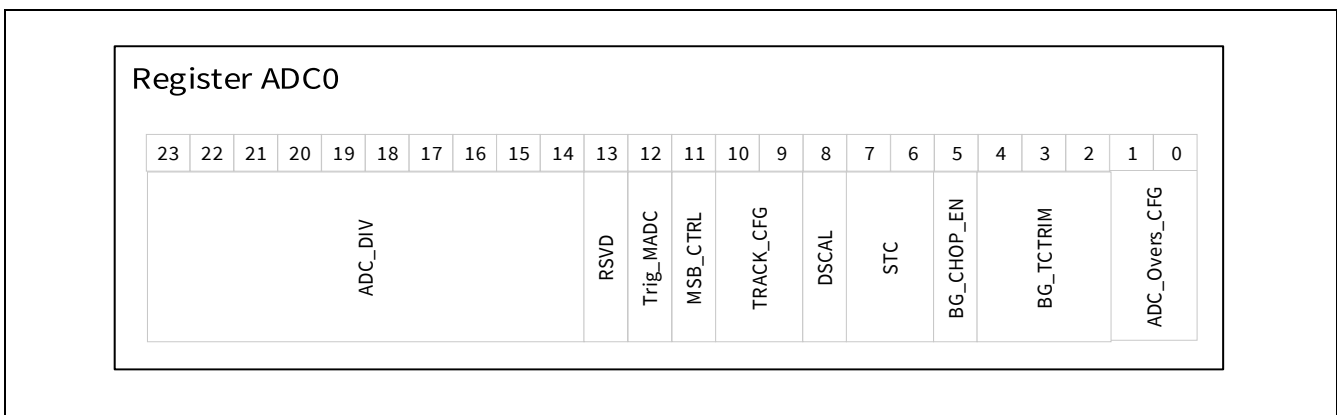


Figure 20 ADC0 register

Table 22 ADC0: Register Description

| Symbol | Bits | Type | Description | RST |
|-----------|-------|------|--|-----------------|
| ADC_DIV | 23:14 | RW | Sampling frequency divider value. The actual sampling frequency will be $f_{ADC_SAMP} = f_{ADC_CLK} / ADC_DIV$: 20 _D ... minimum divider value → $f_{ADC_SAMP} = 4$ Msps 33 _D ... typical value → $f_{ADC_SAMP} = 2.42$ Msps 1023 _D ... max divider value → $f_{ADC_SAMP} = 78.201$ kpsps | 40 _D |
| RSVD | 13 | RW | RSVD | 0 _B |
| TRIG_MADC | 12 | W | Test mode feature for single measurement acquisition. The results can be read through the test bits in registers ADC1 to ADC4: 0 _B ... Return value after trigger is captured internally 1 _B ... Single trigger event | 0 _B |
| MSB_CTRL | 11 | RW | MSB decision time selection during calibration and conversion: 0 _B ... Single MSB decision time 1 _B ... Doubled MSB decision time | 0 _B |
| TRACK_CFG | 10:9 | RW | Tracking conversion configuration bits: 0 _D ... No sub conversions are executed and averaged 1 _D ... 1 sub conversion 2 _D ... 3 sub conversions | 1 _D |

BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|---------------|------|------|---|----------------|
| | | | 3 _D ... 7 sub conversions | |
| DSCAL | 8 | RW | Disable Startup calibration: 0 _B ... startup calibration is enabled 1 _B ... startup calibration is disabled | 0 _B |
| STC | 7:6 | RW | Sample time control: 0 _D ... 50 ns 1 _D ... 100 ns 2 _D ... 200 ns 3 _D ... 400 ns | 1 _D |
| BG_CHOP_EN | 5 | RW | Enable chopping within the bandgap. 0 _B ... No chopping enabled 1 _B ... Chopping enabled | 0 _B |
| BG_TC_TRIM | 4:2 | RW | Static temperature coefficient trimming 0 _D ... Min. value 7 _D ... Max. value | 0 _D |
| ADC_OVERS_CFG | 1:0 | RW | Oversampling configuration: 0 _D ... Standard single 11 bits conversion 1 _D ... Reserved 2 _D ... Reserved 3 _D ... Reserved Note: Oversampling must be set to 0 _D | 0 _D |

4.4 CHIP_ID

The register CHIP_ID provides information regarding the digital code version, the RF block version, and the antenna configuration (number of channels, position of the antennas e.g.).

It is used by the driver to configure the device properly according to the information above.

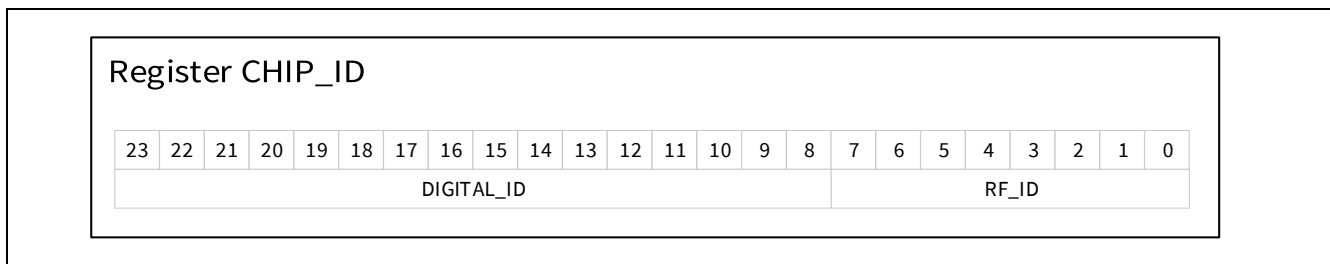


Figure 21 CHIP_ID register

Table 23 CHIP_ID: Register Description

| Symbol | Bits | Type | Description | RST |
|------------|------|------|-----------------------------------|----------------|
| DIGITAL_ID | 23:8 | R | 3 _D | 3 _D |
| RF_ID | 7:0 | R | 3 _D ... 1ch Tx, 3ch Rx | 3 _D |

The Digital_ID as well as the RF_ID will be incremented according to the latest chip release/version.

BGT60TR13C Registers

4.5 STAT1 - Status Register1

The status register provides internal counter values for the actual number of frames and shapes. They are also provided to the data header. However, it should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after eg. 100 μ s.

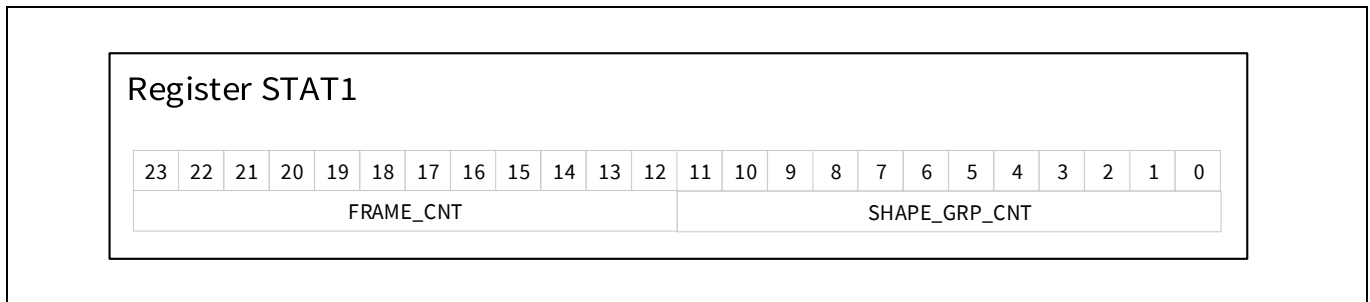


Figure 22 STAT1: status register 1

Table 24 STAT1: Register Description

| Symbol | Bits | Type | Description | RST |
|---------------|-------|------|--|----------------|
| FRAME_CNT | 23:12 | R | Frame counter value: 0 _D ... Reset value / after max. value rollover 4095 _D ... Max. value Note: This field is for debug only. Note: FRAME_CNT info should not be used when endless mode enabled (please check CCR2:MAX_FRAME_CNT). | 0 _D |
| SHAPE_GRP_CNT | 11:0 | R | Shape group counter counts the actual shape groups: 0 _D ... Reset value / after max. value for SHAPE_GRP_CNT reached 4095 _D ... Max. value | 0 _D |

Note:

1. A shape consists of an “Up Chirp” segment and a “Down Chirp” segment.
2. A saw-tooth shape is generated by an “Up Chirp” and a “Fast Down Chirp”.
3. There is no data acquisition in the “Fast Down Chirp”.

BGT60TR13C Registers

4.6 PACR1: PLL Analog Control Registers 1

The bits in this register are used to properly set the PLL.

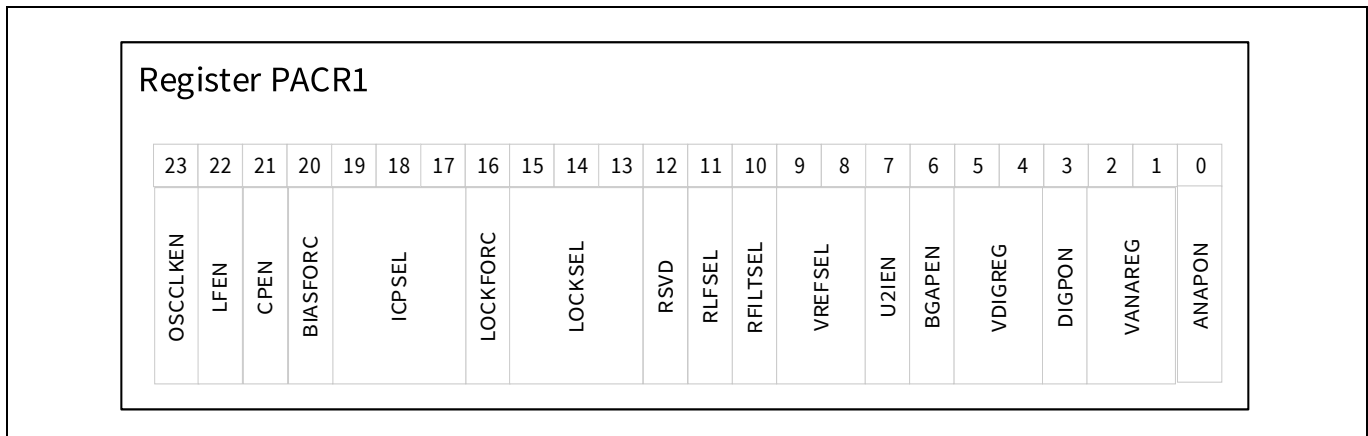


Figure 23 PACR1 register

Table 25 PACR1: Register Description

| Symbol | Bits | Type | Description | RST |
|----------|-------|------|--|----------------|
| OSCCLKEN | 23 | RW | Enable clock path for system clock: 0 _B ... Clock off 1 _B ... Clock path active by default this is disabled This bit is controlled by FSM during operation. After deep sleep this bit should be enabled by the host. Before the MAIN: FRAME_START is raised the OSCCLKEN should be enabled! | 0 _B |
| LFEN | 22 | RW | Enable loop filter: 0 _B ... Off(default) 1 _B ... On | 0 _B |
| CPEN | 21 | RW | Enable charge pump: 0 _B ... Off(default) 1 _B ... On | 0 _B |
| BIASFORC | 20 | RW | Use fixed biasing inside charge pump (= disable bias reg. loop): 0 _B ... Fixed biasing off = bias regulation loop active (default) 1 _B ... Fixed biasing on = bias regulation loop deactivated | 1 _B |
| ICPSEL | 19:17 | RW | Select charge pump current: 0 _D ... 40 μA 1 _D ... 80 μA 2 _D ... 120 μA 3 _D ... 160 μA 4 _D ... 200 μA (default) 5 _D ... 240 μA 6 _D to 7 _D ... 280 μA | 4 _D |
| LOCKFORC | 16 | RW | Force lock signal to high: 0 _B ... Lock signal not forced 1 _B ... Lock forced to high | 1 _B |

BGT60TR13C Registers

4.7 PACR2: PLL Analog Control Registers 2

The bits in this register are used to properly set the PLL.

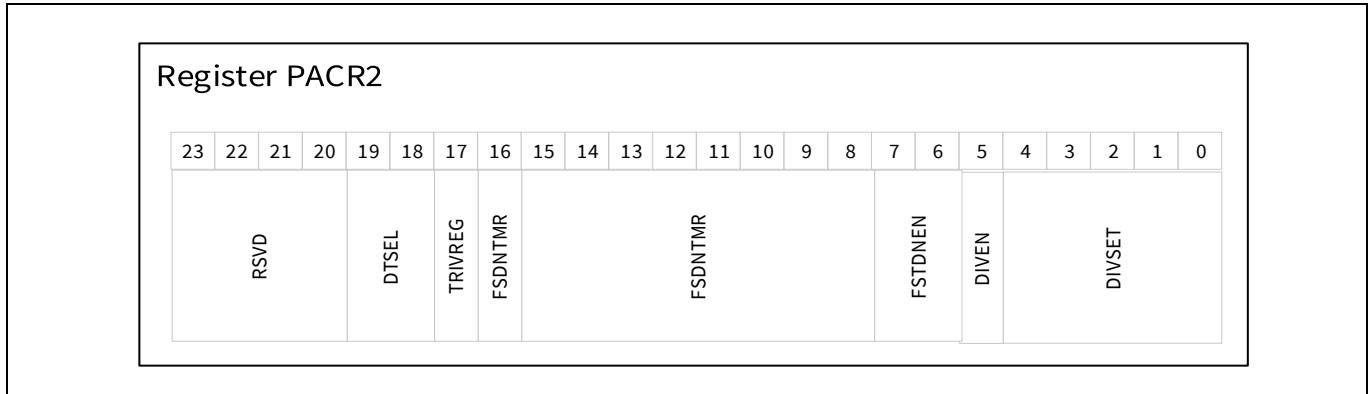


Figure 24 PACR2 PLL register

Table 26 PACR2: Register Description

| Symbol | Bits | Type | Description | RST |
|---------|-------|------|--|----------------|
| RSVD | 23:20 | RW | Reserved | 0 _D |
| DTSEL | 19:18 | RW | Set PFD dead time / dead zone: 0 _D ... 180 ps to 350 ps 1 _D ... 270 ps to 510 ps (default) 2 _D ... 360 ps to 680 ps 3 _D ... 450 ps to 840 ps | 1 _D |
| TRIVREG | 17 | RW | Set regulator off-state to tristate (for both ana- & dig-regulator): 0 _B ... Off state is 0.0V (default) 1 _B ... Off state is to tristate (setting active for dig-regulator if DIGPON = 0 _B ; setting active for ana-regulator if ANAPON= 0 _B) | 0 _B |
| FSDNTMR | 16:8 | RW | Defines the time for the PLL loop filter discharge during fast down chirp operation. When FSTDNTMR = 0 _D and FSTDNEN is ≠ 0 _D , the fast down chirp length is internally assigned to a default value (@typ f _{SYS_CLK}): 0 _D ... 500 ns if FSTDNEN = 1 _D (discharge of the loop filter to the reference voltage set to PACR2:VREFSEL) 0 _D ... 700 ns if FSTDNEN = 2 _D (discharge of the loop filter in a defined time window) 0 _D ... 300 ns if FSTDNEN = 3 _D For FSDNTMR > 0 _D the discharge time will be T _{SYS_CLK} × (FSDNTMR+1): 1 _D ... 25 ns 2 _D ... 37.5 ns ... 511 _D ... 6.4 μs Suggested settings for the discharge time: | 0 _D |

BGT60TR13C Registers

| | | | | |
|---------|-----|----|---|-----------------|
| | | | PACR2:FSDNTMR= 5 _D Together with: PACR2:FSTDNEN= 2 _D Depending on the specific modulation bandwidth set, specific settings can be defined. | |
| FSTDNEN | 7:6 | W | Fast-down chirp enabled (see note below): 00 _B ... Disable (default) 01 _B ... Enable fast down chirp (mode 1) 10 _B ... Enable fast down chirp (mode 2) 11 _B ... Enable fast down chirp (mode 3) Suggested settings for the fast-down mode (active mode between chirps): PACR2:FSDNTMR = 5 _D Together with: PACR2:FSTDNEN = 2 _D Depending on the specific modulation bandwidth set, specific settings can be defined. | 00 _B |
| DIVEN | 5 | RW | Enable divider: 0 _B ... Off: Input clock of divider and 80 MHz clock gated 1 _B ... On: clocks released | 0 _B |
| DIVSET | 4:0 | RW | Set fixed part of integer division factor (consider offset of 2) Default = 20 _D , valid for a 80 MHz system clock. 21 _D should be used for a 76.8 MHz system clock. | 20 _D |

Note:

This bit field is typically used by the FSM. In case not used, the FSM switches the bit field back to the default value.

4.8 SFCTL – SPI and FIFO Control Register

This register is used to configure the SPI and FIFO.

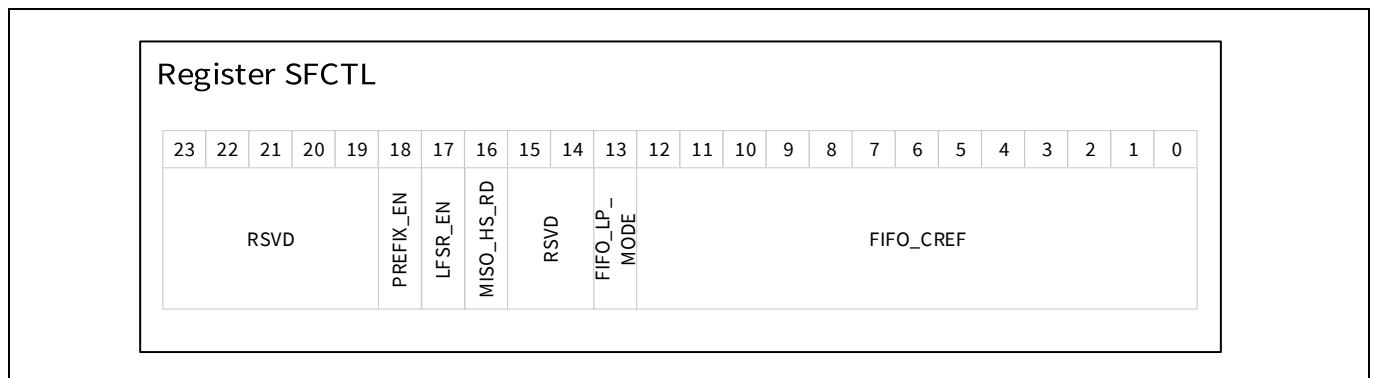


Figure 25 SPI and FIFO Control Register

BGT60TR13C Registers

Table 27 SPI and FIFO Control: Register Description

| Symbol | Bits | Type | Description | RST |
|--------------|-------|------|--|-----------------|
| RSVD | 23:19 | RW | RSVD | 14 _B |
| PREFIX_EN | 18 | RW | Enables the data header written into the FIFO prior to the sampling data of each chirp: 0 _B ... No prefix data header prior to chirp data 1 _B ... Prefix data header added prior to chirp data (see section 5.1 for data header) | 0 _B |
| LFSR_EN | 17 | RW | Enable LFSR register data generation: 0 _B ... Normal data acquisition, LFSR reset 1 _B ... LFSR data generation started LFSR should be enabled after a FIFO reset to ensure an empty FIFO (see also 5.10). | 0 _B |
| MISO_HS_RD | 16 | RW | 0 _B ... MISO data is sent with falling edge of SPI CLK 1 _B ... MISO data is sent with rising edge (½ cycle earlier) Note: HS_RD = 0 _B can only be used for a SPI clock < 25 MHz. For HS-transfer please check the timing of the SPI Master and adjust settings accordingly. The setting becomes active when the last bit of FSCTL is clocked out and it affects MISO immediately. See also section 5.3.1. | 1 _B |
| RSVD | 15:14 | RW | RSVD | 0 _B |
| FIFO_LP_MODE | 13 | RW | FIFO power mode: 0 _B ... FIFO permanently enabled 1 _B ... FIFO activated dynamically | 0 _B |
| FIFO_CREF | 12:0 | RW | FIFO compare reference: it defines the compare filling status for interrupt and CREF reporting When filling status is > FIFO_CREF an interrupt is issued: 0 _D ... minimum value is 0, interrupt generated in case first sample is written into FIFO 8191 _D ... maximum value in case FIFO is full with 8192 memory locations eg. CREF = 0x1000 represents a 50% compare reference | 0 _D |

4.9 SADC_CTRL Sensor ADC Control Register

The bits in this register are used to properly set the sensor ADC (SADC) used to monitor the on-chip sensor outputs, temperature and power, as well as some internal voltage nodes.

BGT60TR13C Registers

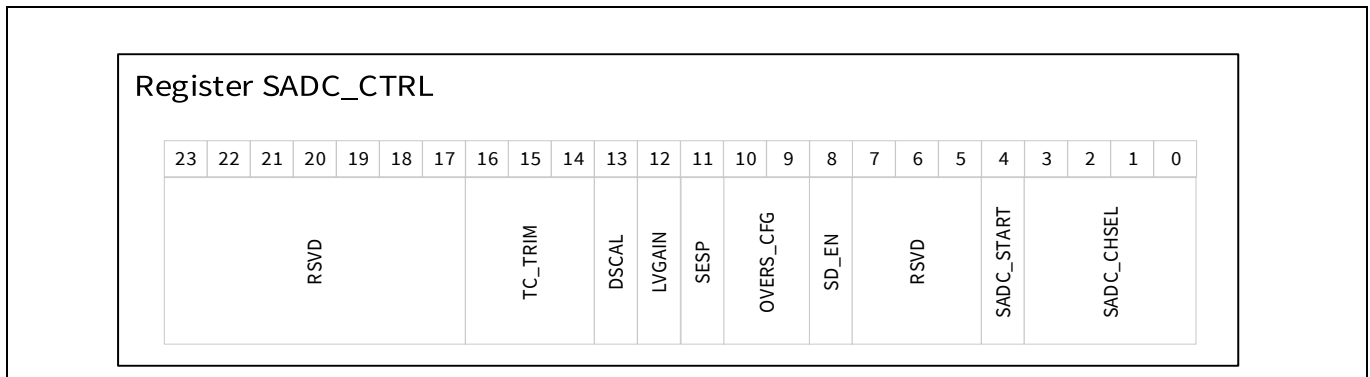


Figure 26 SADC_CTRL registers

Table 28 SADC_CTRL: Register Description

| Symbol | Bits | Type | Description | RST |
|------------|-------|------|---|----------------|
| RSVD | 23:17 | RW | RSVD | 0 _D |
| TC_TRIM | 16:14 | RW | Bandgap trim value: 0 _D ... Min. trim value 7 _D ... Max. trim value | 0 _D |
| DSCAL | 13 | RW | Disable startup calibration: 0 _B ... Startup calibration enabled 1 _B ... startup calibration disabled | 0 _B |
| LVGAIN | 12 | RW | Sample configuration for LV channels: 0 _B ... Gain = 1.0 1 _B ... Gain = 0.75 | 0 _B |
| SESP | 11 | RW | Spreaded early sampling point enable: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| OVERS_CFG | 10:9 | RW | Oversampling configuration: 0 _D ... No oversampling → 8 bits resolution 1 _D ... Oversampling by 2 2 _D ... Oversampling by 4 → 9 bits resolution 3 _D ... Oversampling by 32 → 10 bits resolution | 0 _D |
| SD_EN | 8 | RW | Sigma delta loop enable: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| RSVD | 7:5 | RW | RSVD | 0 _D |
| SADC_START | 4 | W | SADC trigger: 1 _B ... Trigger the SADC to start a measurement 0 _B ... Default value or value after the trigger is captured; internally the value is set back to SADC_START= 0 _B . | 0 _B |
| SADC_CHSEL | 3:0 | RW | Analog multiplexer input for channel selection into the SADC: 0 _D ... Temperature Sensor 1 _D ... RSVD | 0 _D |

BGT60TR13C Registers

Table 28 SADC_CTRL: Register Description

| Symbol | Bits | Type | Description | RST |
|--------|------|------|---|-----|
| | | | 2 _D ... Temperature Sensor reference 3 _D ... pd_outx 4 _D ... pd_out 5 _D ... ifx_mix3 6 _D ... if_mix3 7 _D ... ifx_mix2 8 _D ... if_mix2 9 _D ... ifx_mix1 10 _D ... if_mix1 11-15 _D ... RSVD | |

4.10 CSx: Channel Set Registers

The channel set registers together with the channel set control registers defines the RF and baseband behavior during the shapes. CSUx= Channel Set Upchirp, CSDx= Channel Set Downchirp, CSI= Channel Set Idle, CSDS= Channel Set Deep Sleep.

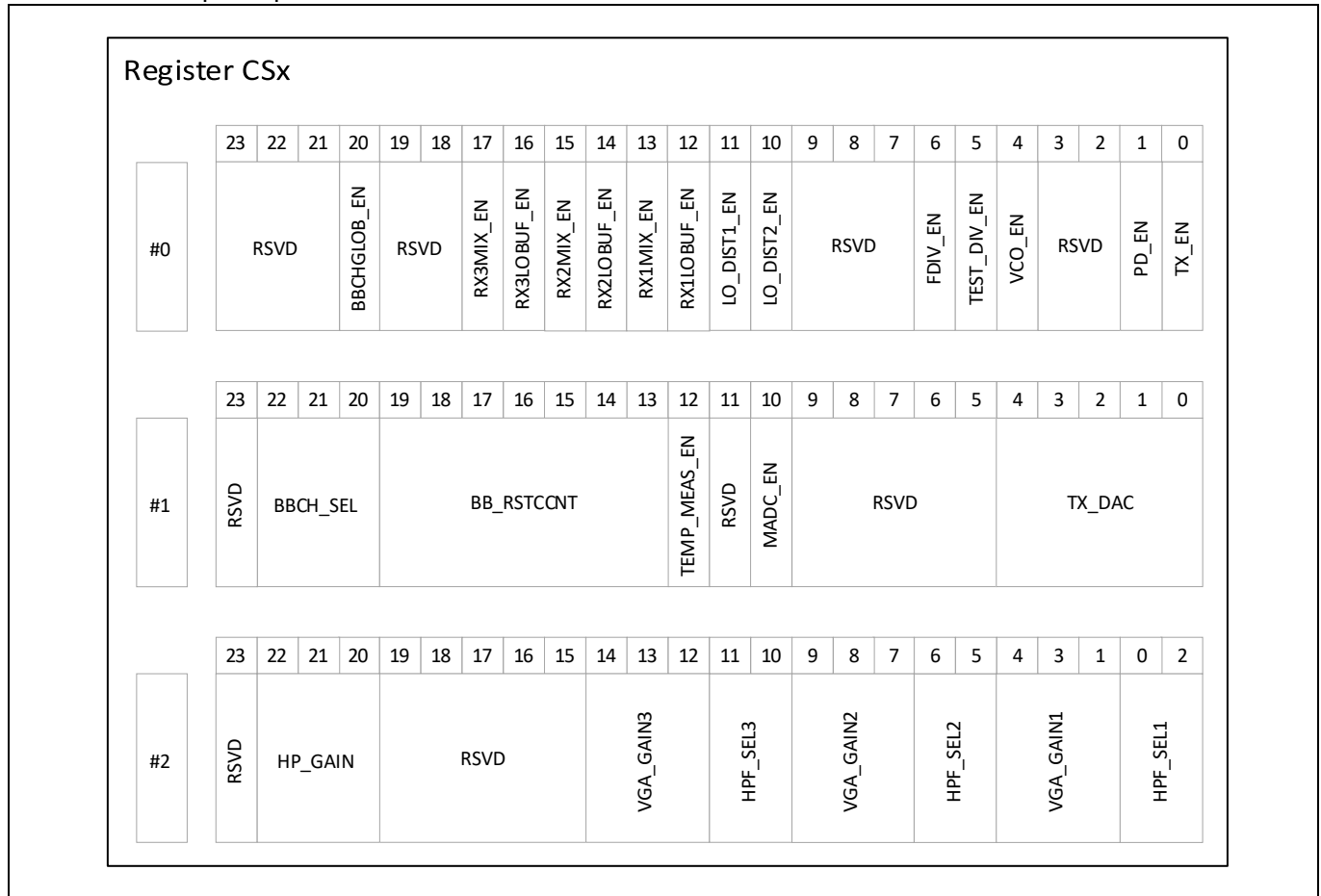


Figure 27 Channel Set Registers

BGT60TR13C Registers

Table 29 CSx#0: Register Description

| Symbol | Bits | Type | Description | RST |
|--|-------|------|---|----------------|
| RSVD | 23:21 | RW | RSVD | 0 _D |
| BBCHGLOB_EN | 20 | RW | Enables the baseband chain together with the bit BBCH_SEL: 0 _B ... Baseband channels are disabled 1 _B ... Baseband channels are enabled | 0 _B |
| RSVD | 19:18 | RW | RSVD | 0 _D |
| RX3MIX_EN | 17 | RW | Enable the mixer on ch3: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| RX3LOBUF_EN | 16 | RW | Enable the local oscillator buffer to the mixer on ch3: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| RX2MIX_EN | 15 | RW | Enable the mixer on ch2: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| RX2LOBUF_EN | 14 | RW | Enable the local oscillator buffer to the mixer on ch2: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| RX1MIX_EN | 13 | RW | Enable the mixer on ch1: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| RX1LOBUF_EN | 12 | RW | Enable the local oscillator buffer to the mixer on ch1: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| LO_DIST1_EN (formerly LO_DISTRIB_EN) | 11 | RW | Enable the local oscillator distribution buffer to the RX2 and TX channels: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| LO_DIST2_EN (formerly LO_MOD1_EN) | 10 | RW | Enable the local oscillator distribution buffer to the RX1 and RX3 channels: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| RSVD | 9:7 | RW | RSVD | 0 _D |
| FDIV_EN | 6 | RW | Enable the VCO frequency divider: 0 _B ... Disable the DIV output 1 _B ... Enable the DIV output | 0 _B |
| TEST_DIV_EN | 5 | RW | Frequency divider test control bit: 0 _B ... Disable the divider 1 _B ... Enable the divider | 0 _B |
| VCO_EN | 4 | RW | Enable the VCO: 0 _B ... Disabled | 0 _B |

BGT60TR13C Registers

Table 29 CSx#0: Register Description

| Symbol | Bits | Type | Description | RST |
|--------|------|------|---|----------------|
| | | | 1 _B ... Enabled | |
| RSVD | 3:2 | RW | RSVD | 0 _D |
| PD_EN | 1 | RW | Enable the power detector from TX: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| TX_EN | 0 | RW | Enable the DAC and power amplifier of TX 0 _B ... Disabled 1 _B ... Enabled | 0 _B |

Table 30 CSx#1: Register Description

| Symbol | Bits | Type | Description | RST |
|--------------|-------|------|---|----------------|
| RSVD | 23 | RW | RSVD | 0 _B |
| BBCH_SEL | 22:20 | RW | Enable the baseband filters, baseband amplifiers and ADCs on channel BBCHx, where x can be 1...3: BBCHx = 0 _D ... channel disabled BBCHx = 1 _D ... channel enabled CSx#1[22] ... BBCH3 CSx#1[21] ... BBCH2 CSx#1[20] ... BBCH1 | 0 _D |
| BB_RSTCNT | 19:13 | RW | Baseband reset timer counter value for the analog baseband amplifiers. The reset counter will start together with the PAON signal after the T_PAEN timer. $BB_RSTCNT = T_{BBRST} * f_{SYS_CLK}$ 0 _D ... No analog baseband reset 1 _D ... Min. reset time is $T_{BBRST} = 12.5 \text{ ns}$ 127 _D ... Max. reset counter, $T_{BBRST} = 1.5875 \mu\text{s}$ | 0 _D |
| TEMP_MEAS_EN | 12 | RW | Enables the temperature sensor: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| RSVD | 11 | RW | RSVD | 0 _B |
| MADC_EN | 10 | RW | Enable the three channel ADC module at once: 0 _B ... ADC module powered down 1 _B ... ADC module powered up | 0 _B |
| RSVD | 9:5 | RW | RSVD | 0 _D |
| TX_DAC | 4:0 | RW | TX power setting: 0 _D ... Min. TX output power 31 _D ... Max. TX output power | 0 _D |

Table 31 CSx#2: Register Description

| Symbol | Bits | Type | Description | RST |
|--------|------|------|-------------|----------------|
| RSVD | 23 | RW | RSVD | 0 _B |

BGT60TR13C Registers

Table 30 CSx#1: Register Description

| Symbol | Bits | Type | Description | RST |
|-----------|-------|------|--|----------------|
| HP_GAIN | 22:20 | RW | Set the gain of the first stage: HPF GAIN[x]= 1 _D ... 18dB Gain HPF GAIN[x]= 0 _D ... 30dB gain bit20→ch1, bit21→ch2, bit22→ch3 | 0 _D |
| RSVD | 19:15 | RW | RSVD | 0 _D |
| VGA_GAIN3 | 14:12 | RW | VGA gain setting channel 3: 0 _D ... 0dB gain 1 _D ... 5dB gain 2 _D ... 10dB gain 3 _D ... 15dB gain 4 _D ... 20dB gain 5 _D ... 25dB gain 6 _D ... 30dB gain 7 _D ... RSVD | 0 _D |
| HPF_SEL3 | 11:10 | RW | High pass filter channel 3 cutoff setting: 0 _D ... 20kHz 1 _D ... 45kHz 2 _D ... 70kHz 3 _D ... 80kHz | 0 _D |
| VGA_GAIN2 | 9:7 | RW | VGA gain setting channel 2: 0 _D ... 0dB gain 1 _D ... 5dB gain 2 _D ... 10dB gain 3 _D ... 15dB gain 4 _D ... 20dB gain 5 _D ... 25dB gain 6 _D ... 30dB gain 7 _D ... RSVD | 0 _D |
| HPF_SEL2 | 6:5 | RW | High pass filter channel 2 cutoff setting: 0 _D ... 20kHz 1 _D ... 45kHz 2 _D ... 70kHz 3 _D ... 80kHz | 0 _D |
| VGA_GAIN1 | 4:2 | RW | VGA gain setting channel 1: 0 _D ... 0dB gain 1 _D ... 5dB gain 2 _D ... 10dB gain 3 _D ... 15dB gain 4 _D ... 20dB gain 5 _D ... 25dB gain 6 _D ... 30dB gain 7 _D ... RSVD | 0 _D |

BGT60TR13C Registers

Table 30 CSx#1: Register Description

| Symbol | Bits | Type | Description | RST |
|----------|------|------|--|----------------|
| HPF_SEL1 | 1:0 | RW | High pass filter channel 1 cutoff setting: 0 _D ... 20kHz 1 _D ... 45kHz 2 _D ... 70kHz 3 _D ... 80kHz | 0 _D |

4.11 CSCx - Channel Set Control Register

The channel set control register CSCx is related to the channel set register CSUx and CSDx as well as to CSI and CSDS, see description in section 4.10.

Besides REPC, all other bits are used to define a specific power mode.

“_ISOPD” represents a logical isolation layer used to disable one main block (MADC e.g.) preserving its configuration (no change in the ADC0 register configuration e.g.).

REPC is one parameter used to define the modulation sequence, see also 3.2.

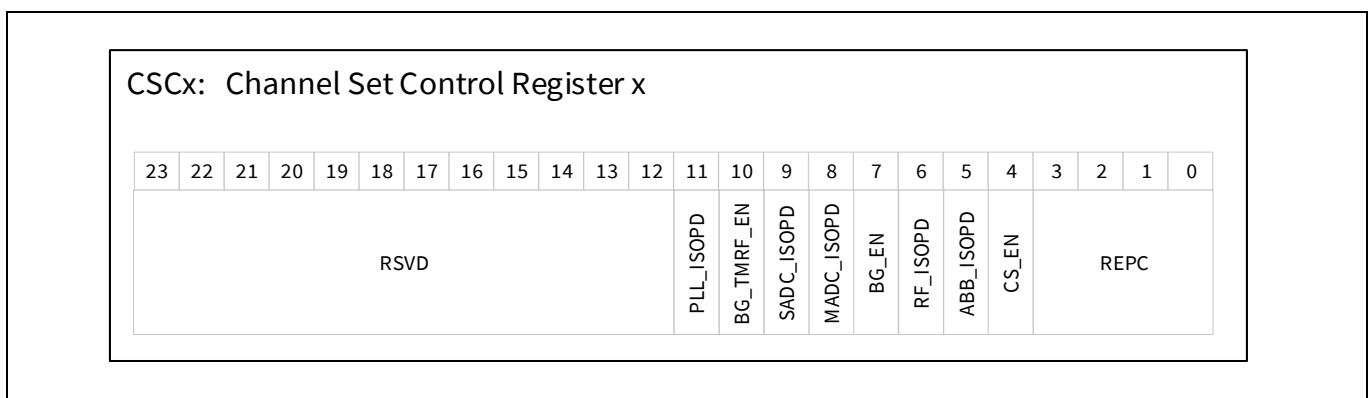


Figure 28 Channel Set Control Register

Table 32 CSCx: Register Description

| Symbol | Bits | Type | Description | RST |
|------------|-------|------|--|----------------|
| RSVD | 23:12 | RW | RSVD | 0 _D |
| PLL_ISOPD | 11 | RW | Isolation pin to disable the PLL: 0 _B ... PLL is connected 1 _B ... PLL is isolated | 1 _B |
| BG_TMRF_EN | 10 | RW | Required for temperature sensor readout: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| SADC_ISOPD | 9 | RW | Enable the isolation of all control signals towards the sensor ADC: 0 _B ... SADC connected 1 _B ... SADC isolated | 1 _B |
| MADC_ISOPD | 8 | RW | Enable the isolation of all control signals towards the MADC: | 1 _B |

BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|-----------|------|------|--|----------------|
| | | | 0 _B ... MADC connected 1 _B ... MADC isolated | |
| BG_EN | 7 | RW | Enable bandgap in MADC: 0 _B ... Disabled 1 _B ... Enabled | 0 _B |
| RF_ISOPD | 6 | RW | Enable the isolation of all control signals towards the RF block: 0 _B ... RF connected 1 _B ... RF isolated | 1 _B |
| ABB_ISOPD | 5 | RW | Enable the isolation of all control signals towards the analog baseband (BB) block: 0 _B ... BB connected 1 _B ... BB isolated | 1 _B |
| CS_EN | 4 | RW | Enable channel set (CS): 0 _B ... CS is not used 1 _B ... CS is used In case of CSCI or CSCDS this bit is ignored. In the application at least the first channel set should be used by the host (CSC1:CS_EN= 1 _B). | 0 _B |
| REPC | 3:0 | RW | Repetition factor for Channel set: RC= 2 ^{REPC} : 0 _D ... RC= 1 repetition 1 _D ... RC= 2 repetitions 2 _D ... RC= 4 repetitions ... 10 _D ... RC= 1024 repetitions 15 _D ... RC= 32768 repetitions In case of CSCI or CSCDS this bit is ignored. | 0 _D |

4.12 CCR0 - Chirp Control Registers 0

Registers CCRx are used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counter to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

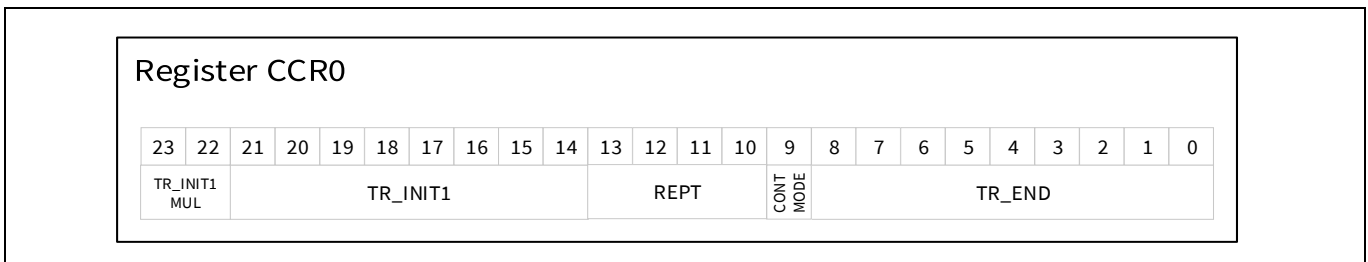


Figure 29 Chirp Control Register 0

Table 33 CCR0: Register Description

BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|--------------|-------|------|--|----------------|
| TR_INIT1_MUL | 23:22 | RW | Timer multiplier factor for T_INIT1. Precise timing provided under CCR0:TR_INIT1. | 0 _D |
| TR_INIT1 | 21:14 | RW | Coefficient to calculate T_INIT1: 0 _D ... T _{SYS_CLK} From 1 _D to 255 _D the time delay for T_INIT1 is calculated as follows: $T_INIT1 = (TR_INIT1 \times 2^{TR_INIT1_MUL} \times 8 + TR_INIT1_MUL + 3) \times T_{SYS_CLK}$. See Note below. | 0 _D |
| REPT | 13:10 | RW | Repetition factor for shape sets in a frame: RT= 2 ^{REPT} : 0 _D ... 1 repetition 1 _D ... 2 repetitions 2 _D ... 4 repetitions ... 15 _D ... 32768 repetitions The host should program as default value 15_D. | 0 _D |
| CONT_MODE | 9 | RW | After last repetition of RT, the CONT_MODE is enabled. 0 _B ... only in case if deep sleep power mode is enabled (CCR1: PD_MODE= 2 _D). The system clock is disabled internally. 1 _B ... goes to specified power mode (CCR1:PD_MODE) and after T_FED next shapes will run. | 0 _B |
| TR_END | 8:0 | RW | Coefficient to calculate T_END. T_END Ramp End Delay defines the waiting time after generation of the ramp. $T_END = (TR_END \times 8 + 5) \times T_{SYS_CLK}$. 0 _D ... 5 * T _{SYS_CLK} 511 _D ... Max. delay | 0 _D |

Note:

These values are used for every up and every down-ramp.

4.13 CCR1 - Chirp Control Registers 1

Registers CCRx are used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counter to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

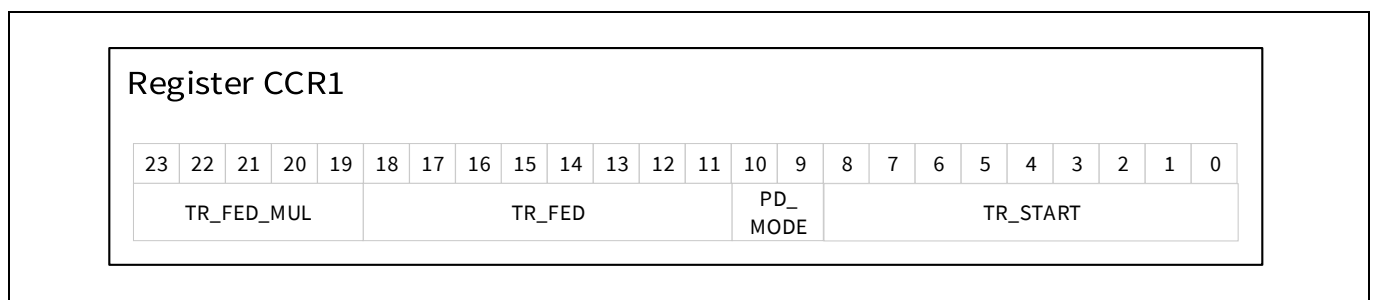


Figure 30 Chirp Control Register 1

BGT60TR13C Registers

Table 34 CCR1: Register Description

| Symbol | Bits | Type | Description | RST |
|------------|-------|------|--|----------------|
| TR_FED_MUL | 23:19 | RW | Timer multiplier factor for frame end delay T_FED. Precise timing provided under CCR1:TR_FED. Note: only values TR_FED_MUL ≤ 10 _D are verified. | 0 _D |
| TR_FED | 18:11 | RW | Coefficient to calculate T_FED: 0 _D ... T _{SYS_CLK} From 1 _D to 255 _D the time delay T_FED is calculated as follows: $T_FED = (TR_FED \times 2^{TR_FED_MUL \times 8 + TR_FED_MUL + 3}) \times T_{SYS_CLK}$. | 0 _D |
| PD_MODE | 10:9 | RW | After last RT repetition the chip enters this power mode for the time T_FED: 0 _D ... Keep power mode same (CSx, CSCx) 1 _D ... Idle Mode (CSI + CSCI) 2 _D ... Deep Sleep Mode (CSDS + CSCDS) 3 _D ... RSVD | 0 _D |
| TR_START | 8:0 | RW | Coefficient to calculate T_START. T_START Ramp Start Delay defines the waiting time before generation of the ramp. $T_START = (TR_START \times 8 + 10) \times T_{SYS_CLK}$: 0 _D ... 10 * T _{SYS_CLK} 511 _D ... Max. delay | 0 _D |

4.14 CCR2 - Chirp Control Registers 2

Registers CCRx are used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counter to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

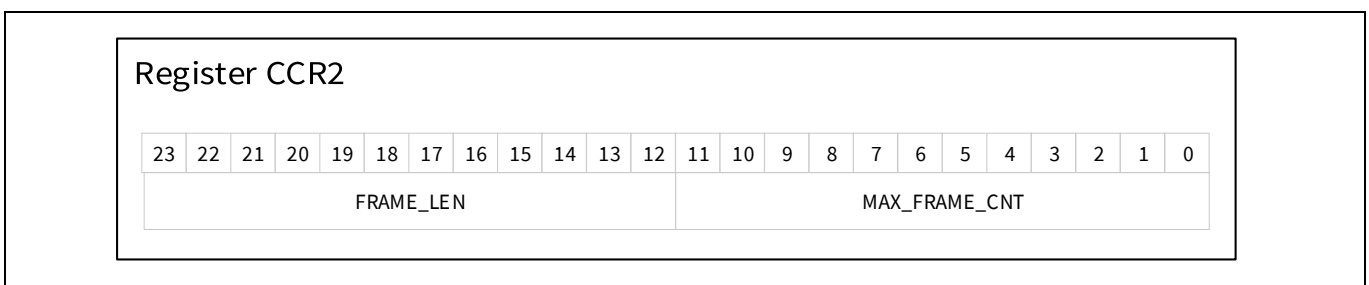


Figure 31 Chirp Control Register 2

Table 35 CCR2: Register Description

| Symbol | Bits | Type | Description | RST |
|-----------|-------|------|--|----------------|
| FRAME_LEN | 23:12 | RW | Frame Length specifies the number of shape groups in a frame. When specified frame length is reached frame counter will be incremented and shape group counter reset: 0 _D ... 1 shape group 1 _D ... 2 shape group 4095 _D ... Max. value (=4096). | 0 _D |

BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|---------------|------|------|--|----------------|
| MAX_FRAME_CNT | 11:0 | RW | Maximum number of frames to be executed. When MAX_FRAME_CNT is reached, shape generation will stop and the chip will go into deep sleep power mode. The next frame can be triggered only after a reset (eg. FSM_RESET). The frame generation can be stopped any time by the FSM reset (see MAIN: FSM_RESET). 0 _D ... Endless generation 1 _D ... 1 frame will be generated 4095 _D ... Max. number of frames generated (=4095). | 0 _D |

4.15 CCR3 - Chirp Control Registers 3

Registers CCRx are used to program the parameters for the modulation sequence. The main FSM will use those parameters to set internal timers and counter to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

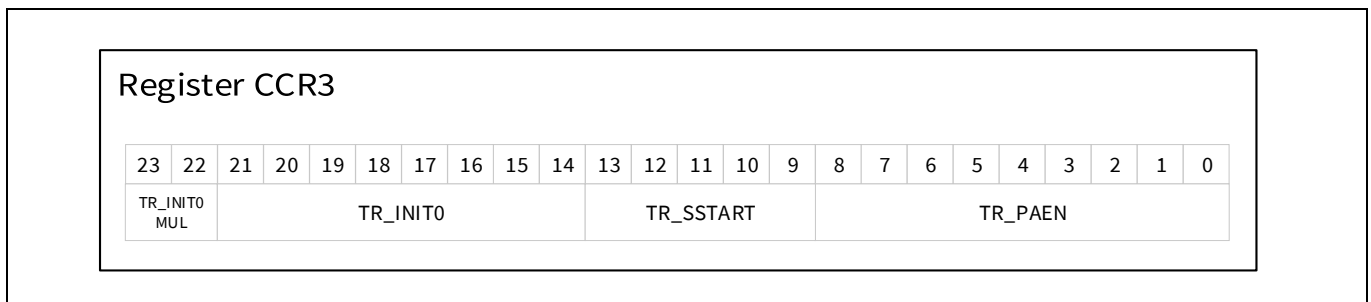


Figure 32 Chirp Control Register 3

Table 36 CCR3: Register Description

| Symbol | Bits | Type | Description | RST |
|--------------|-------|------|---|----------------|
| TR_INIT0_MUL | 23:22 | RW | Timer multiplier for delay T_INIT0. Precise timing provided under CCR3:TR_INIT0. | 0 _D |
| TR_INIT0 | 21:14 | RW | Coefficient to calculate T_INIT0: 0 _D ... T _{sys_clk} From 1 _D to 255 _D the time delay for T_INIT0 is calculated as follows: $T_INIT0 = (TR_INIT0 \times 2^{TR_INIT0_MUL} \times 8 + TR_INIT0_MUL + 3) \times T_{sys_clk}$. See Note 3. | 0 _D |
| TR_SSTART | 13:9 | RW | Coefficient to calculate T_SSTART. T_SSTART Sampling Start Delay Time after PA enable until 1 st trigger to MADC. $T_SSTART = (TR_SSTART \times 8 + 1) \times T_{sys_clk}$ 0 _D ... T _{sys_clk} 31 _D ... Max. delay | 0 _D |
| TR_PAEN | 8:0 | RW | Coefficient to calculate T_PAEN. T_PAEN Delay Time after PLL Start to PA enable. $T_PAEN = TR_PAEN \times 8 \times T_{sys_clk}$ 0 _D ... RSVD 1 _D ... Min. delay | 0 _D |

BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|--------|------|------|---------------------------------|-----|
| | | | 511 _D ... Max. delay | |

Note:

1. One single step is equal to $8 \times T_{SYS_CLK}$ system clock cycles (= 100 ns)
2. The delay values are used for every up and every down-ramp
3. T_INIT0 and T_INIT1 should be programmed to a minimum value according to the ADC calibration time. See also Table 15 and Table 60.

4.16 PLLx[0..6] - Chirp Shape Registers

Registers PLLx, where x can be 1 to 4, are used to program the parameters for the modulation sequence inside the PLL local FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

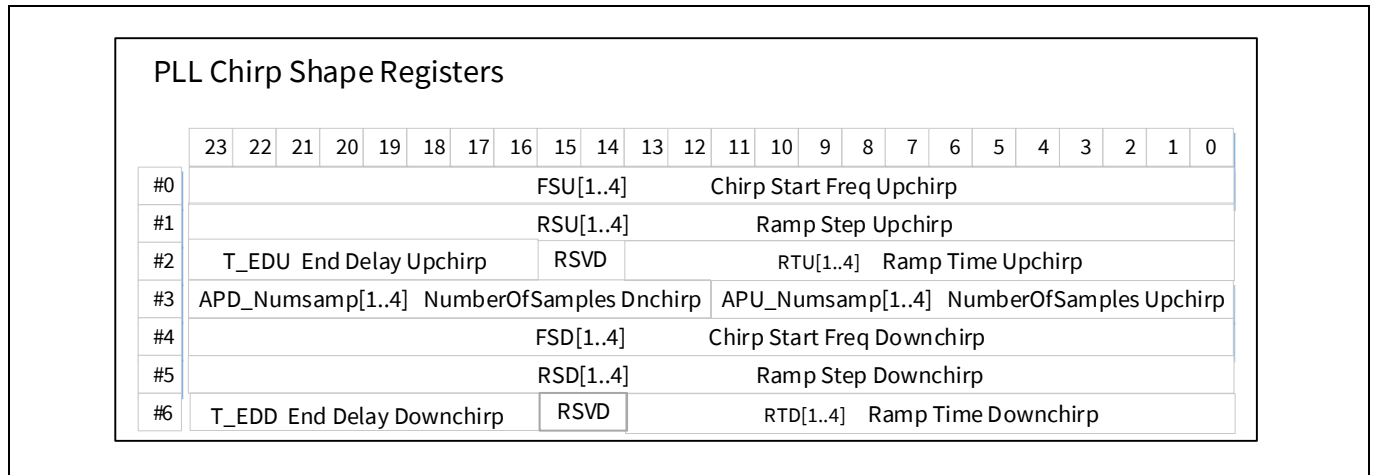


Figure 33 PLL Chirp Shape Registers 1-6

Table 37 PLLx#0 ... PLLx#6 Chirp Shape: Register Description

| Symbol | Bits | Type | Description | RST |
|------------------------|------|------|--|----------------|
| FSU[1..4] FSD[1..4] | 23:0 | RW | Chirp Start Freq Upchirp / Downchirp. SDM start frequency for the ramp generator: FSD = 0 _D for saw-tooth shape In case FSD=0, RSD=0, and RTD=0, then the fast saw-tooth shape is enabled. In all other cases the triangular shape is enabled. | 0 _D |
| RSU[1..4] RSD[1..4] | 23:0 | RW | Ramp Step Upchirp / Downchirp. A ramp step is the RF frequency difference added to the actual frequency during single clock cycle time of $T_{SYS_CLK} = 12.5$ ns. In case the value is zero the RF frequency will be almost constant during the RTU/RTD time. Bit(23) represents the sign for the ramp: 0 _D ... Upchirp 1 _D ... Downchirp | 0 _D |

BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|------------------------------|---------------|------|--|----------------|
| TR_EDU[1..4] TR_EDD[1..4] | 23:16 | RW | Coefficients to calculate T_EDU and T_EDD, respectively. T_EDU and T_EDD are End of Chirp Delay applied after every Upchirp and Downchirp. If TR_EDU/D = 0: T_EDU/D = 2 x T _{sys_clk} . If TR_EDU/D > 0: T_EDU/D = (8 x TR_EDU/D + 5) x T _{sys_clk} . 255D ... Max. delay | 0 _D |
| RSVD | 15:14 | | Reserved on register #2 and #6. | 0 _D |
| RTU[1..4] RTD[1..4] | 13:0 | RW | Ramp Time Upchirp / Downchirp. RTU/D defines the number of clock cycles for the Upchirp (RTU) or Downchirp (RTD). The actual ramp time is T_RAMP[U D] = [RTU RTD] * 8 x T _{sys_clk} : 0 _D ... Timer disabled. Disabling the timer is useful when doing Downchirp operation with fast down chirp enabled. 1 _D ... T_RAMP = 100 ns 16383 _D ... T_RAMP = 2 ¹⁴ x 100 ns = 1.6383 ms | 0 _D |
| APD[1..4] APU[1..4] | 23:12 11:0 | RW | Number of samples for Upchirp (APU) or Downchirp (APD) for the results of a single ADC: 0 _D ... No sampling during chirp 1 _D ... Number of samples = 1 4095 _D ... Max. number of samples is 4095 | 0 _D |

Note:

IRQ FIFO interrupt is generated based on FIFO words. One FIFO word of 24 bit captures two ADC samples of 12 bit. For dual and quad ADC operation all samples result in 1 or more FIFO words. In single ADC mode, if an odd number of samples are selected, the FIFO interrupt will be generated after the following (even) sample. For single channel mode an even number of samples is recommended.

4.17 PLLx[7] – SCR Shape Control Register

Registers PPLx[7], where x can be 1 to 4, are used to program the parameters for the modulation sequence inside the PLL local FSM. The main FSM will control the local PLL FSM to run the expected modulation sequence in standalone mode (no external trigger required except the first one).

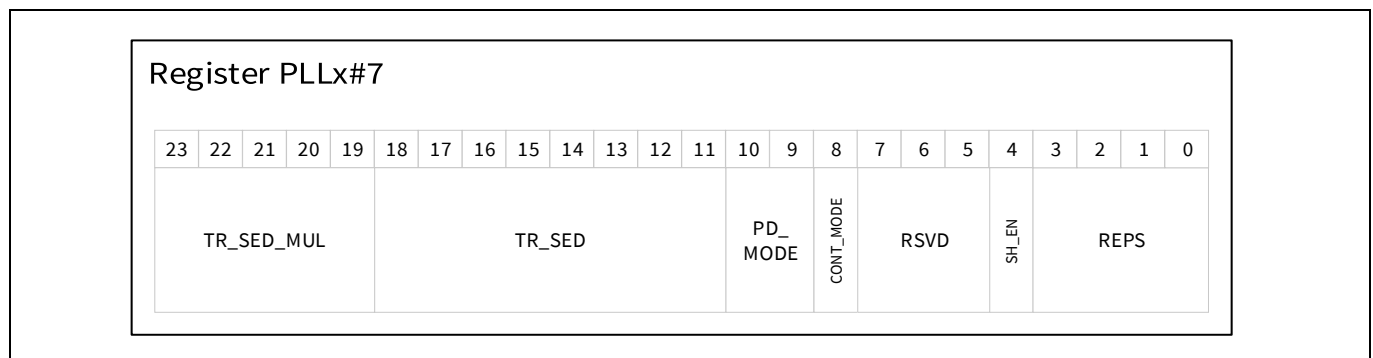


Figure 34 PLLx#7 SCR shape control register

Table 38 PLLx#7 SCR Shape Control: Register Description

BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|------------|-------|------|--|----------------|
| TR_SED_MUL | 23:19 | RW | Timer multiplier factor for shape end delay T_SED. Precise timing provided under PLLx#7:TR_SED. Note: only values TR_SED_MUL ≤ 10 _D are verified. | 0 _D |
| TR_SED | 18:11 | RW | Coefficient to calculate T_SED: 0 _D ... T _{SYS_CLK} From 1 _D to 255 _D the time delay T_SED is calculated as follows: $T_SED = (TR_SED \times 2^{TR_SED_MUL \times 8 + TR_SED_MUL + 3}) \times T_{SYS_CLK}$ | 0 _D |
| PD_MODE | 10:9 | RW | After last shape repetition, FSM goes to a specified Power Down Mode (run this mode during T_SED): 0 _D ... Keep power mode same (CSx, CSCx) 1 _D ... Idle Mode (CSI + CSCI) 2 _D ... Deep Sleep Mode (CSDS + CSCDS) 3 _D ... RSVD | 0 _D |
| CONT_MODE | 8 | RW | After last shape repetition REPS, FSM: 0 _B ... goes to a specified Power Down Mode and stop immediately 1 _B ... goes to a specified Power Down Mode and after T_SED it runs the next shapes | 0 _B |
| RSVD | 7:5 | RW | RSVD | 0 _D |
| SH_EN | 4 | RW | Enables the specific shape x (see Note 3): 0 _B ... shape is not used regardless of shape parameters PLLx[1..7] are programmed with values different from default value. 1 _B ... shape is used | 0 _B |
| REPS | 3:0 | RW | Repetition factor for a single shape x: RSx = 2 ^{REPSx} : 0 _D ... RSx = 1 repetition 1 _D ... RSx = 2 repetitions 2 _D ... RSx = 4 repetitions ... 15 _D ... RSx = 32768 repetitions | 0 _D |

Note:

1. When chirp shapes are not used FSU/RSU/RTU register fields must be programmed to 0_D (see also Table 37).
2. A "saw-tooth" chirp can be defined by setting field FSD = 0_D, and programming the fields for Upchirp (see also Table 37).
3. At least the first shape needs to be enabled (PLL1[7]:SH_EN = 1_B)

4.18 PLL DFT0 Register

The setting in this register should be used when the CW mode is enabled (see also 10.2).

BGT60TR13C Registers

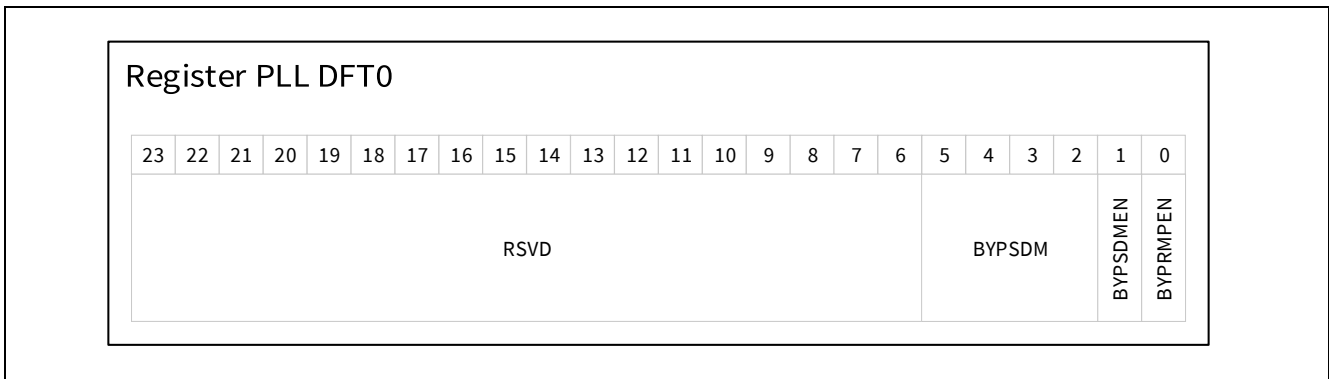


Figure 35 PLL DFT0 register

Table 39 PLL DFT0: Register Description

| Symbol | Bits | Type | Description | RST |
|----------|------|------|---|----------------|
| RSVD | 23:6 | RW | RSVD | 0 _D |
| BYPSDM | 5:2 | RW | SDM output data when SDM is bypassed | 0 _D |
| BYPSDMEN | 1 | RW | The PLL core shall overwrite SDM output value with value driven on PDCR2.BYPSDM when this register changes from '0 _B ' to '1 _B '. A transition from '1 _B ' to '0 _B ' disables this feature and returns the control to SDM: 0 _B ... SDM module drives the ANA (functional mode) 1 _B ... BYPSDM(3:0) drives the ANA | 0 _B |
| BYPRMPEN | 0 | RW | The PLL core shall overwrite SDM input value with value driven on PDCR1.SDMSTRT when this register changes from '0' to '1'. A transition from '1' to '0' disables this feature and returns the control to ramp generator: 0 _B ... Ramp generator drives SDM input 1 _B ... PDCR1.SDMSTRT drives SDM input | 0 _B |

4.19 RFT0 – RF Test Register 0

Register contains several bits used to enable dedicated paths for self-test.

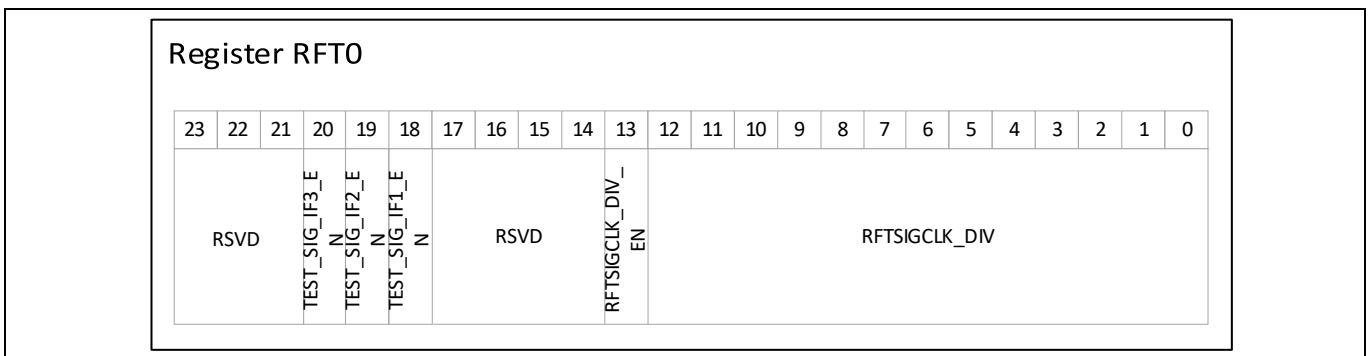


Figure 36 RFT0 RF test register 0

Table 40 RFT0: Register Description

BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|------------------|-------|------|---|-------------------|
| RSVD | 23:21 | RW | RSVD | 0 _D |
| TEST_SIG_IF3_EN | 20 | RW | Enable the test signal output for IF channel 3 | 0 _B |
| TEST_SIG_IF2_EN | 19 | RW | Enable the test signal output for IF channel 2 | 0 _B |
| TEST_SIG_IF1_EN | 18 | RW | Enable the test signal output for IF channel 1 | 0 _B |
| RSVD | 17:14 | RW | RSVD | 0 _D |
| RFTSIGCLK_DIV_EN | 13 | RW | Enable the RF test tone signal output to the baseband module: 0 _B ... Disable the divider output 1 _B ... Enable the divider output | 0 _B |
| RFTSIGCLK_DIV | 12:0 | RW | RF test tone signal divider value: $f_{RFTST} = f_{SYS_CLK} / RFTSIGCLK_DIV$. 2 _D ... Min. divider value 8191 _D ... Max. divider value | 8000 _D |

4.20 RFT1 – RSVD

Reserved Register.

4.21 STAT0 - Status Register 0

The status register STAT0 provides the actual value of some specific internal states. However, it should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after eg. 100 μs.

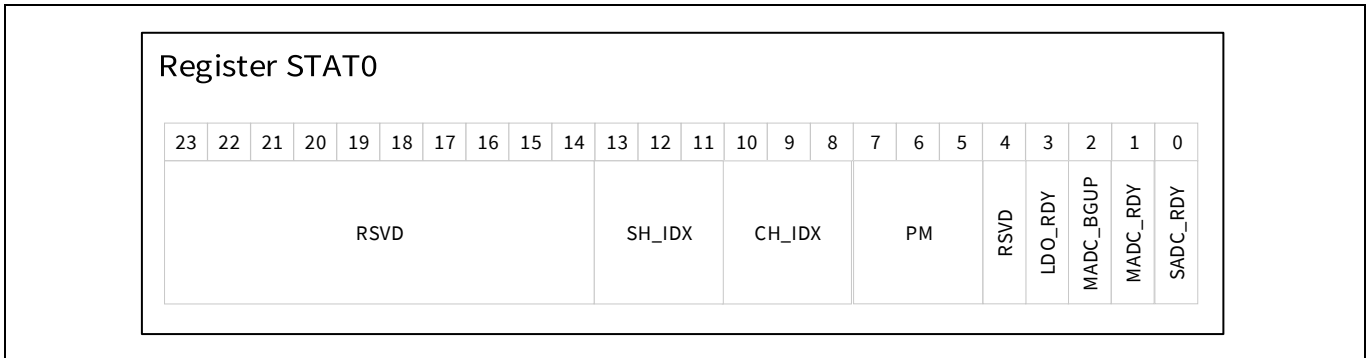


Figure 37 STAT0: Control FSM Status Register

Table 41 STAT0: Register Description

| Symbol | Bits | Type | Description | RST |
|--------|-------|------|--|----------------|
| RSVD | 23:14 | R | RSVD | 0 _D |
| SH_IDX | 13:11 | R | Actual chirp shape enabled by the FSM: 0 _D ... PLLU1 1 _D ... PLLD1 2 _D ... PLLU2 3 _D ... PLLD2 4 _D ... PLLU3 | 0 _D |

BGT60TR13C Registers

Table 41 STAT0: Register Description

| Symbol | Bits | Type | Description | RST |
|-----------|------|------|--|----------------|
| | | | 5 _D ... PLLD3 6 _D ... PLLU4 7 _D ... PLLD4 | |
| CH_IDX | 10:8 | R | Actual channel set enabled by the FSM: 0 _D ... CSU1 1 _D ... CSD1 2 _D ... CSU2 3 _D ... CSD2 4 _D ... CSU3 5 _D ... CSD3 6 _D ... CSU4 7 _D ... CSD4 | 0 _D |
| PM | 5:7 | R | Power Mode is the current power mode status of FSM: 1 _D ... Active Mode 2 _D ... Interchirp Mode 3 _D ... Idle Mode 5 _D ... Deep Sleep Mode 0 _D ,4 _D ,6 _D ,7 _D ... RSVD | 5 _D |
| RSVD | 4 | R | RSVD | 0 _B |
| LDO_RDY | 3 | R | LDO output level, i.e., VDDC above the threshold: 0 _B ... LDO output level below threshold 1 _B ... LDO output level above threshold, ready | 0 _B |
| MADC_BGUP | 2 | R | MADC bandgap reference power up status: 0 _B ... Status down 1 _B ... Up and running | 0 _B |
| MADC_RDY | 1 | R | MADC status: 0 _B ... Status down 1 _B ... Up and running | 0 _B |
| SADC_RDY | 0 | R | SADC startup / calibration status: 0 _B ... Status down 1 _B ... Up and running | 0 _B |

4.22 SADC_RESULT Sensor ADC Result Register

The sensor ADC register SADC_RESULT is used to monitor the SADC as well as to read out the output from the conversion.

BGT60TR13C Registers

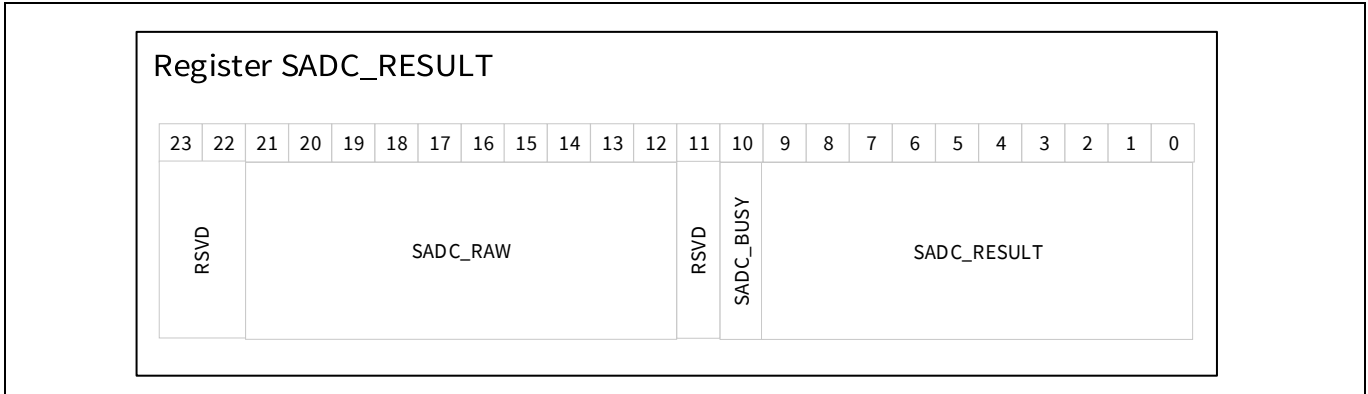


Figure 38 SADC_RESULT registers

Table 42 SADC: Register Description

| Symbol | Bits | Type | Description | RST |
|-------------|-------|------|---|----------------|
| RSVD | 23:22 | R | RSVD | 0 _D |
| SADC_RAW | 21:12 | R | SADC Raw data (for test only) | 0 _D |
| RSVD | 11 | R | RSVD | 0 _B |
| SADC_BUSY | 10 | R | Shows if SADC is busy: 0 _B ... SADC not busy 1 _B ... SADC busy | 0 _B |
| SADC_RESULT | 9:0 | R | 10 bits measurement result. In case just 8 bits are converted, the 8 bits value is left-shifted by two (multiplied by 4). In case 9 bit are converted, the 9 bits result is left-shifted by 1 (multiplied by 2). | 0 _B |

4.23 FSTAT - FIFO Status Register

The FIFO status register FSTAT is used to monitor the FIFO. It should be mentioned that for all status registers, STAT0, STAT1, and FSTAT, with the exception of the FIFO status and error flags, updates to each status register field can happen on different timing events relative to FSM states and the field content should be treated independently from one-another. In CW mode the status bits can be read properly after eg. 100 μs.

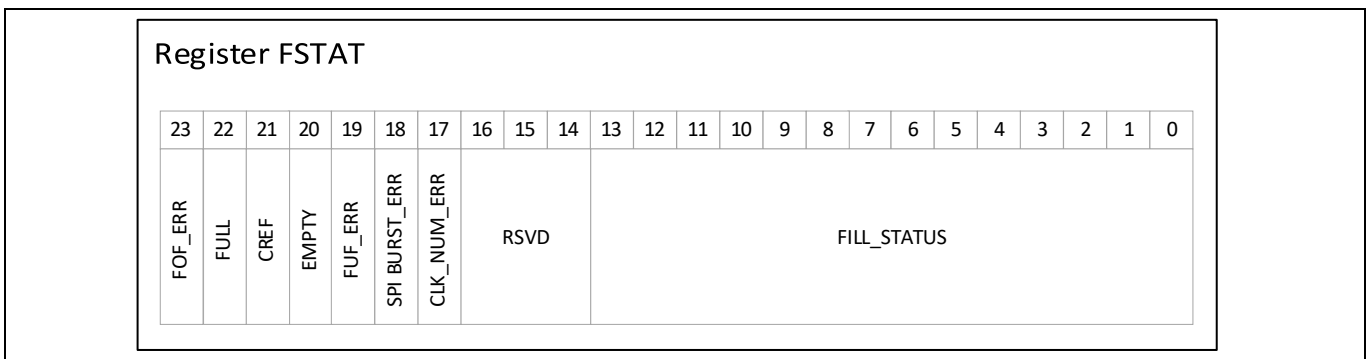


Figure 39 FSTAT Register

Table 43 FSTAT: Register Description

BGT60TR13C Registers

| Symbol | Bits | Type | Description | RST |
|---------------|-------|------|--|----------------|
| FOF_ERR | 23 | R | FIFO overflow error bit shows if more sample data are transferred to the FIFO than FIFO memory locations are available to store the data. The flag will be shown also in GSR0 as a part of FIFO over or underflow error bit FOU_ERR: 0 _B ... No FIFO overflow 1 _B ... FIFO had an overflow condition | 0 _B |
| FULL | 22 | R | The FULL bit shows if the FIFO has fully filled up: 0 _B ... FIFO is not full 1 _B ... FIFO is full | 0 _B |
| CREP | 21 | R | 0 _B ... FIFO filling status below CREP 1 _B ... FIFO filling status is > CREP | 0 _B |
| EMPTY | 20 | R | The FIFO empty bit EMPTY signals if the FIFO is empty: 0 _B ... FIFO stores at least one sample 1 _B ... FIFO is empty | 1 _B |
| FUF_ERR | 19 | R | FIFO under flow error signals if the host was reading more sampling data from the FIFO than available. The flag will be shown also in GSR0 as a part of FIFO over or underflow error bit FOU_ERR: 0 _B ... No error 1 _B ... FIFO underflow occurred | 0 _B |
| SPI BURST_ERR | 18 | R | In case of burst error this bit is set. Further details in the Note below and in 5.8: 0 _B ... No error 1 _B ... Burst error occurred. Bit will be reset after HW or SW reset condition. See also section 5.8. | 0 _B |
| CLK_NUM_ERR | 17 | R | Clock number error bit is set when SPI clocks do not fit the expected clock cycles. Further details in the Note below and in 5.8: 0 _B ... No error 1 _B ... Burst error occurred. Bit will be reset after HW or SW reset condition. See also section 5.8. | 0 _B |
| RSVD | 16:14 | R | Not used | 0 _B |
| FILL_STATUS | 13:0 | R | FIFO filling status: 0x0 ... FIFO empty 0x1000 ... FIFO 50% filled 0x2000 ... FIFO full This bit field is for de-bugging only. It should not be evaluated while the MADDC sampling and filing up the FIFO. It can be evaluated when the FSM status is held, for example, after an FSM reset or in a specific power mode e.g., Deep Sleep. | 0 _B |

BGT60TR13C Registers

Note:

FOF/FUF will be cleared after these resets:

- FIFO reset
- SW reset
- HW reset

4.24 GSR0 - Global Status Register

The global status register GSR0 is related to SPI read/write monitoring.

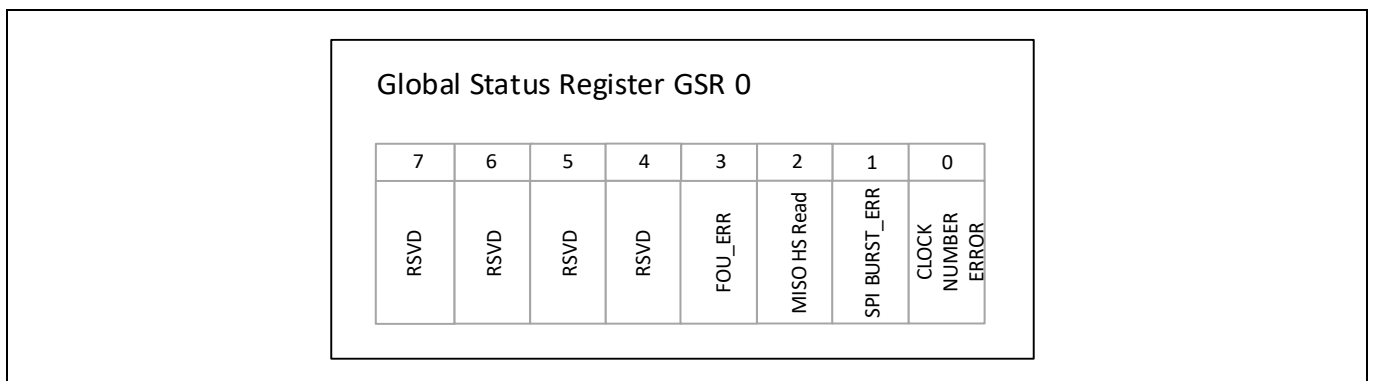


Figure 40 GSR0 Register

Table 44 GSR0: Register Description

| Symbol | Bits | Type | Description | RST |
|--------------------|------|------|---|----------------|
| RSVD | 7 | R | Reserved | |
| RSVD | 6 | R | Reserved | |
| RSVD | 5 | R | Reserved | |
| RSVD | 4 | R | Reserved | |
| FOU_ERR | 3 | R | Shows if FIFO overflow or underflow condition occurred. The error will be cleared after the following resets: FIFO reset or SW reset or HW reset: 1 _B ... Error condition occurred 0 _B ... No error | 0 _B |
| MISO HS Read | 2 | R | SPI: MISO high speed mode activated | 1 _B |
| SPI BURST_ERR | 1 | R | SPI burst error, defined within the SPI spec (see section 5.8): 0 _B ... No burst read/write error 1 _B ... Burst error | 0 _B |
| CLOCK NUMBER ERROR | 0 | R | Defined within the SPI Spec: 0 _B ... No clock number error 1 _B ... Error condition occurred | 0 _B |

Data Organization and SPI Interface

5 Data Organization and SPI Interface

5.1 Data Header

The main FSM is capable of generating a data header to be attached to the actual radar raw data. The structure of the header is shown in Figure 41 and in Table 45. The data header can be disabled by controlling the bit SFCTL:PREFIX_EN (see section 4.8).

A sync-word is sent at the beginning of each acquisition to make the radar raw-data from each shape unique. This can be useful in case of broken communication with the application processor or in case of errors. Supposing the FIFO will generate a “FIFO overflow flag” the sync-word 0x000000 can be evaluated by the host controller and used to resync with the BGT60TR13C and discard the data received before this sync word (if header or sync-word not used then the controller should reset the FIFO, discarding the actual FIFO data). On “FIFO underflow flag”, the received data bits from the host are 111111111111_B.

Following, the header includes also the frame counter and shape group counter, as well as the actual APU/APD value (see section 4.16) and temperature value.

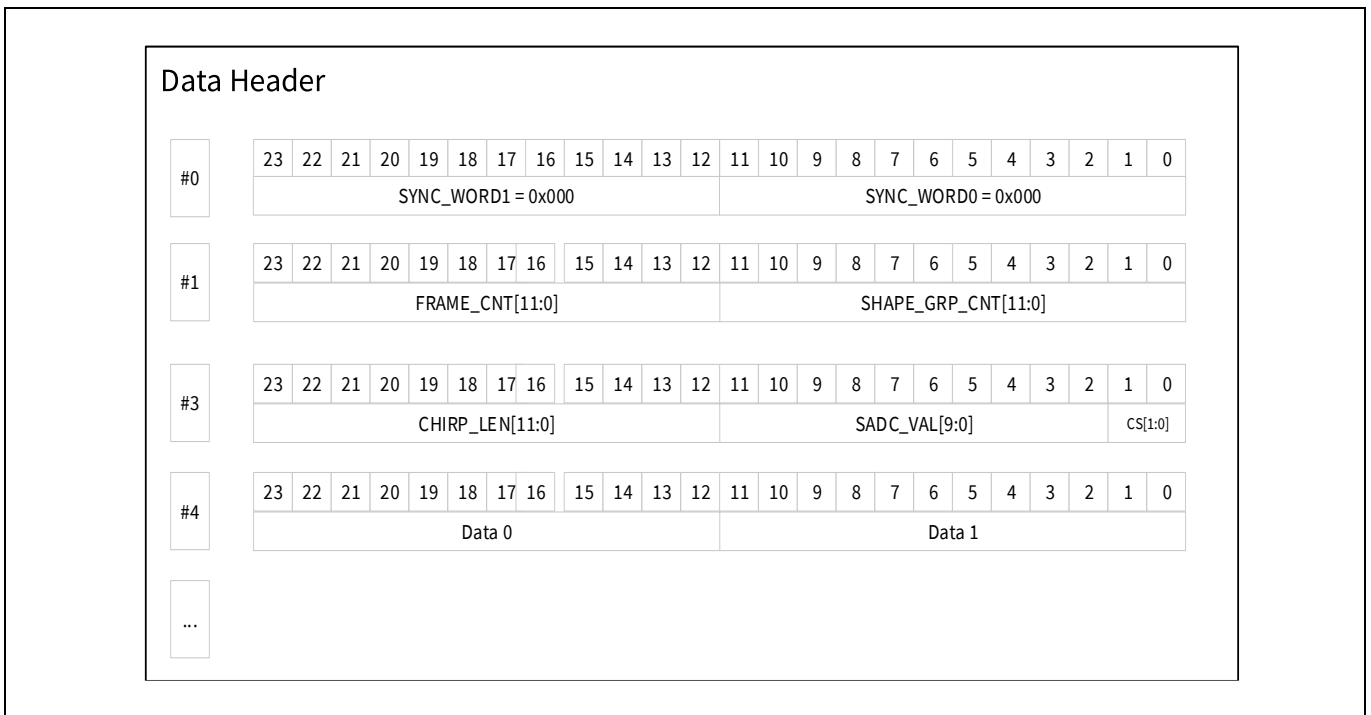


Figure 41 Data header

Data Organization and SPI Interface

Table 45 Data Header Description

| Symbol | Reg | Bits | Description | RST |
|---------------|-----|-------|---|----------------|
| SYNC_WORD1 | #0 | 23:12 | The sync-word can be used to identify the start of a new chirp. In case the MADC will output also a sequence of 0x000000, to make the sync-word unique, the data from the MADC will be automatically changed to 0x001 before transferring it to the FIFO. | 0 _D |
| SYNC_WORD0 | #0 | 11:0 | See SYNC_WORD1. | 0 _D |
| FRAME_CNT | #1 | 23:12 | Same as STAT1:FRAME_CNT (see section 4.5). Note: FRAME_CNT info should not be used by the host when endless mode is enabled (please check CCR2:MAX_FRAME_CNT). | 0 _D |
| SHAPE_GRP_CNT | #1 | 11:0 | Same as STAT1:SHAPE_GRP_CNT (see section 4.5). | 0 _D |
| CHIRP_LEN | #2 | 23:12 | Number of MADC samples inside the chirp (APU/APD value of related chirp). | 0 _D |
| SADC_VAL | #2 | 11:2 | 10 bits of sensor ADC output data (eg. temperature). | 0 _D |
| CS | #2 | 1:0 | Indicates the channel shape number to which the following sampling data belongs to. | |
| Data 0 | #3 | 23:12 | MSB data (see section 5.2). | |
| Data 1 | #3 | 11:0 | LSB data (see section 5.2). | |

5.2 FIFO and Dataflow

The memory in the BGT60TR13C is based on a FIFO. The FIFO consists of a circular shift register organized in 8192 words of 24 bits each. Three dataflow modes from MADC to the FIFO are supported by the FSM (see Figure 42):

- Mode 1: Only one ADC active (can be any ADC from 1 to 3)
 - Data from 1st sample, 12 bits, are temporarily stored in a buffer
 - When the 2nd sample, 12 bits, are available, both, 1st and 2nd, 24 bits, are stored into one data word
- Mode 2: Two ADCs active (can be any ADC from 1 to 3)
 - Data from active ADCs, 12+12 bits, are occupying one data word in the FIFO
- Mode 3: Three ADCs active
 - Data from first two channels are stored into a data word while data from third channel is buffered. On the consecutive trigger the buffered data and the one from first channel are stored in a data word while the data of the second channel is buffered. On the next trigger the buffered data plus the data from the third channel are stored in a third data word, etc.

Data Organization and SPI Interface

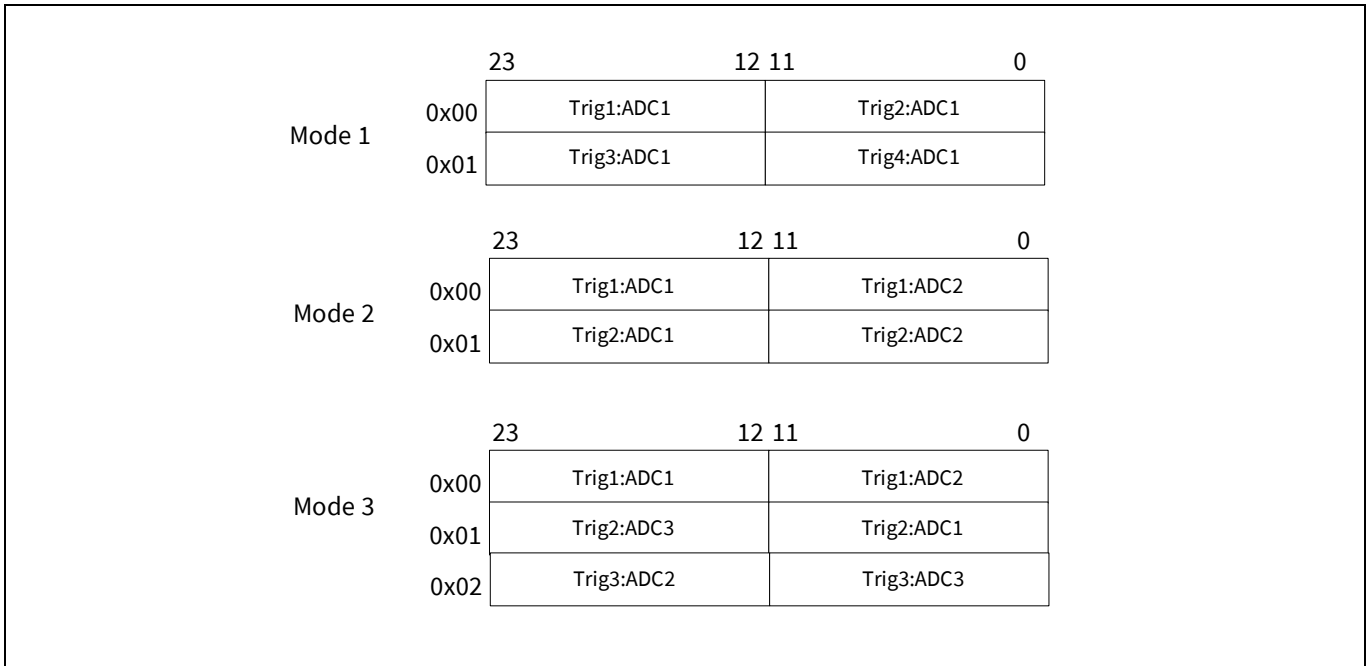


Figure 42 FIFO organization

Readout from the FIFO is done from the SPI block. Due to max frequency of SPI clock, 50 MHz, the readout rate from the FIFO is:

- $50 \text{ MHz} / \text{SPI Mode} / 24 \text{ bit} = 480 \text{ ns} = 40 \text{ cycles}$ (in the 80 MHz domain)

Readout from the FIFO should be executed from the host controller using memory address with correct data length. Data length can be derived from the data header or based on the “sync-word”.

Note:

An illegal write to memory address space will lead to lost FIFO data!

5.3 SPI – Serial Peripheral Interface Module

The SPI is the communication interface between the host and the BGT60TR13C. It enables the host to read from, or write to (program) the registers as well as reading from the FIFO.

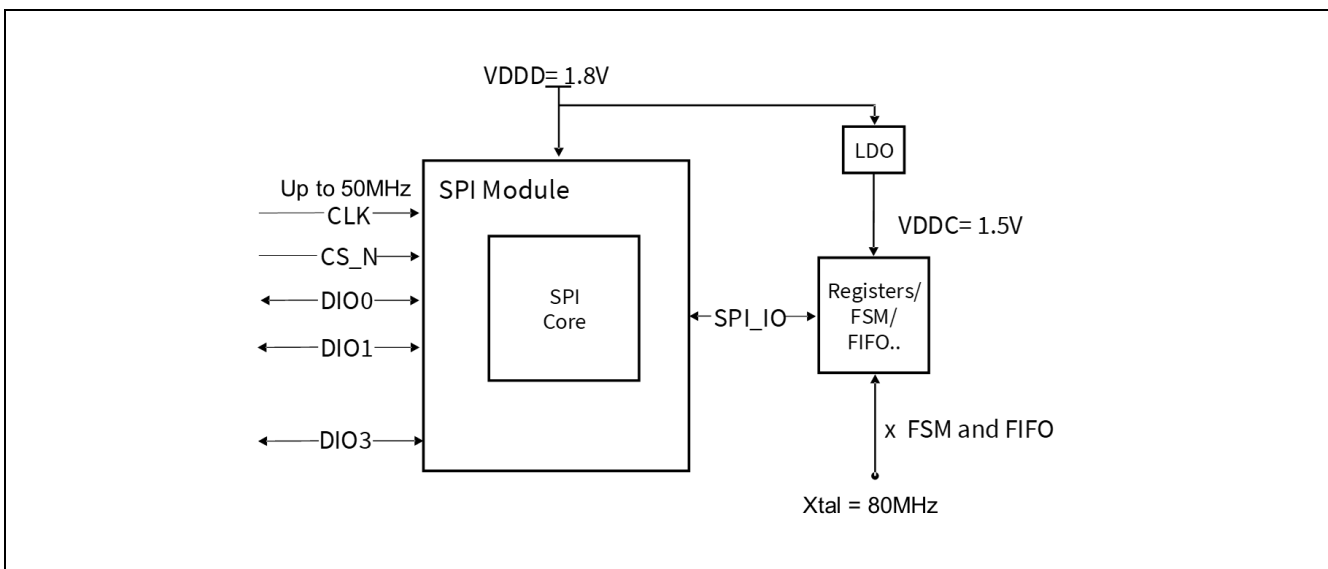


Figure 43 SPI module

Data Organization and SPI Interface

BGT60TR13C device features four I/O pins for SPI communication and one for chip reset. DIO[x] pins are pulled up to logic high inside the pad.

- CS_N to be connected to SS of the SPI master
- CLK to be connected to CLK of the SPI master
- DIO0, DI to be connected to MOSI of the SPI master
- DIO1, DO to be connected to MISO of the SPI master
- DIO2 not available on BGT60TR13C
- DIO3 to be connected to reset

Table 46 SPI Pins

| Pin Name | Standard SPI Mode Function | Remarks |
|----------|----------------------------|-----------------------------|
| CS_N | CS_N | Chip select |
| CLK | CLK | SPI clock |
| DIO0 | DI | HiZ, bidirectional |
| DIO1 | DO | HiZ, bidirectional |
| DIO2 | N.A. | Not available on BGT60TR13C |
| DIO3 | RESET | HiZ, bidirectional |

The SPI interface can be clocked up to 50 MHz. To meet the timing requirements for higher SPI clock frequencies (e.g., > 25 MHz) the BGT60TR13C device offers an additional high-speed mode (SFCTL:MISO_HS_RD) which increase the timing budget on SPI master side by sending out data via DO with the rising edge instead of the falling edge of the CLK.

5.3.1 Standard SPI Timing

The timing diagram for normal SPI mode (SFCTL:MISO_HS_RD =0) is presented in Figure 44. A SPI transfer is started with a falling edge of chip select signal CS_N generated by the SPI master. At the same time, the SPI master shall drive the level of the data input signal DI (master output, slave input) according to the first bit. Also, with the falling edge of the chip select signal CS_N the SPI slave applies the level of the data output signal DO (master input, slave output) according to the first bit which shall be transferred to the SPI master, the level becomes stable after the period $t(ds)$. The SPI master has to wait for the time $t(L)$ before the clock signal CLK can be generated.

With the rising edge of CLK the SPI slave captures the level of DI. The SPI master must keep the DI level stable for $t(mos)$ before and for $t(moh)$ after the rising edge of CLK to ensure valid setup and hold time of the SPI slave. With the falling edge of CLK the SPI master shall set the level of DI according to the next bit the master wants to send.

The SPI master is supposed to read the level of DO with the rising edge of CLK. The SPI slave keeps the DO level stable for $t(mis)$ before and for $t(mih)$ after the rising edge of CLK. With the falling edge of CLK the SPI slave drives the level of DO according to the next bit, DO becomes stable after $t(mih)$.

After the last bit has been transferred and CLK has gone to low level, the SPI master must set CS_N to high level to stop the transfer. The master must take care that the period between the last rising edge of CLK and the rising edge of CS_N is not shorter than $t(T)$. Within the period $t(dh)$ after the rising edge of CS_N the SPI slave drives DO to high impedance state again.

Data Organization and SPI Interface

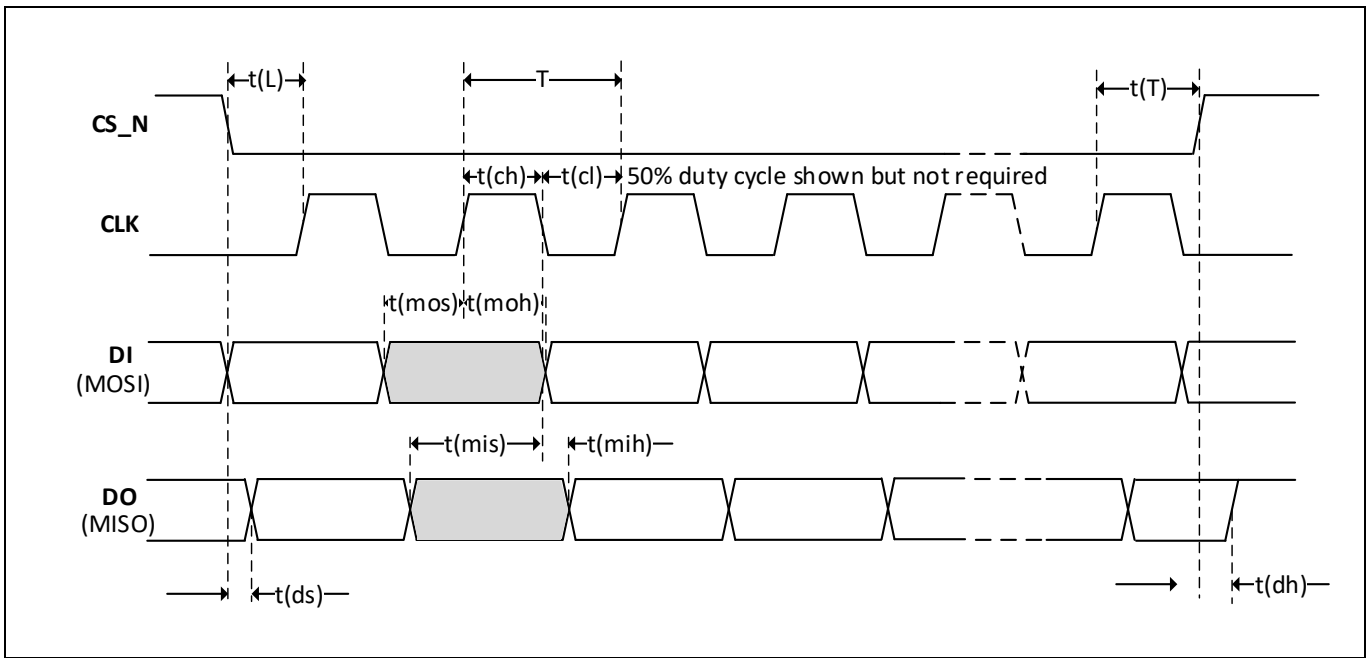


Figure 44 SPI interface timing diagram for SFCTL:MISO_HS_RD = 0_b

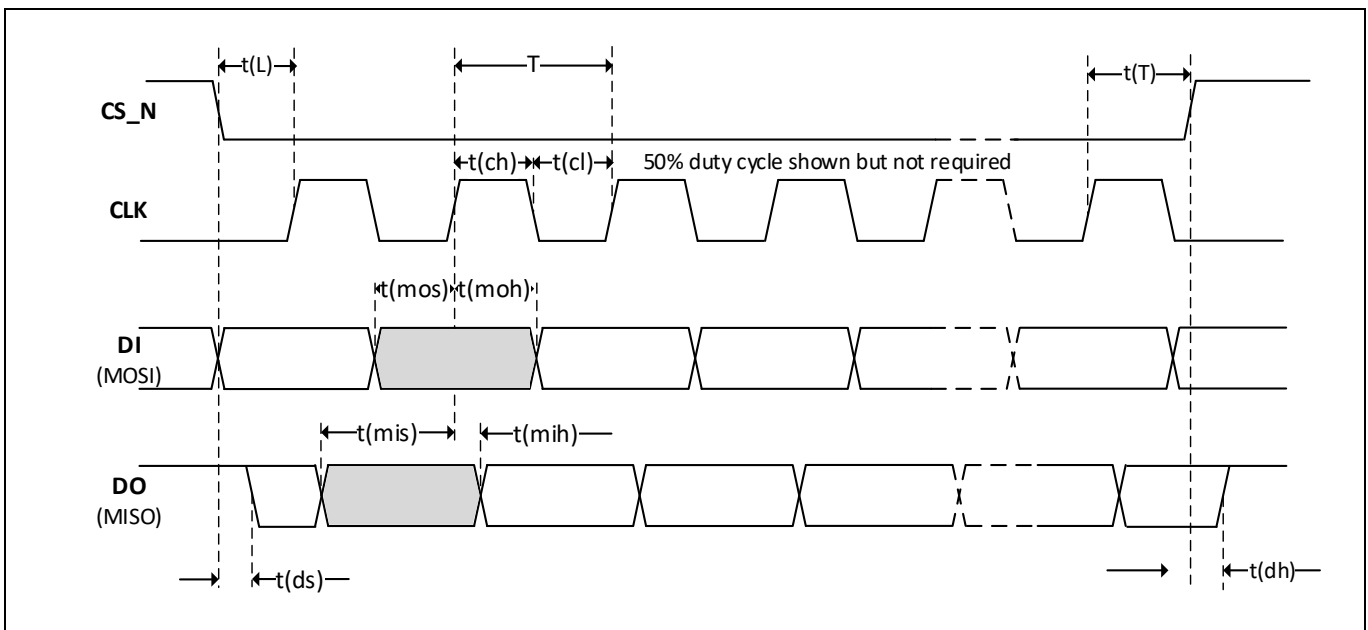


Figure 45 SPI interface timing diagram for SFCTL:MISO_HS_RD = 1_b

BGT60TR13C can operate at SPI clock frequencies up to 50MHz, but the maximum achievable SPI clock frequency is limited by DI related setup and hold times of SPI master and SPI slave. If for example the SPI master requires a longer MISO setup time than $t(mis)$, the SPI clock speed in normal SPI mode must be reduced. Alternatively, BGT60TR13C can be switched to SPI high-speed mode by setting SFCTL:MISO_HS_RD = 1_b.

The timing diagram for high speed SPI mode is presented in Figure 45. In this mode the SPI master is still supposed to capture the level of DO with the rising edge of CLK. The SPI slave keeps the level of DO stable for $t(mis)$ before the rising edge of CLK. The SPI slave keeps the level of DO stable for $t(mih)$ after the rising edge of CLK, and then sets the level of DO according to the next bit which is send out.

Data Organization and SPI Interface

Table 47 SPI Timing Requirements, VDDD = 1.71 to 1.89 V, Tb = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|--|--------|------|-------|-----|-----|----------------------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| SPI clock period: 50MHz, with 1% clock jitter | T | ns | 20 | | | |
| Clock high | t(ch) | ns | 9.0 | | | |
| Clock low | t(cl) | ns | 9.0 | | | |
| Master output setup | t(mos) | ns | 5.0 | | | |
| Master output hold | t(moh) | ns | 5.0 | | | |
| Master input setup | t(mis) | ns | 5.0 | | | T=20ns (see Note 2) |
| Master input hold | t(mih) | ns | 1.0 | | | |
| Lead time before the first working clock edge occurs | t(L) | ns | 9.0 | | | |
| Tailing time after the last working clock edge | t(T) | ns | 1 | | | |
| Data setup time after the DO goes in low impedance state | t(ds) | ns | | | 5 | Guaranteed by design |
| Data hold time before the DO goes in hi impedance state. | t(dh) | ns | | | 5 | Guaranteed by design |

Note:

1. If SFCTL:MISO_HS_RD is not set properly then data read on MISO may not be correct.
2. $t(mis)$ is specified for a maximum SPI clock frequency of 50 MHz. This results in a maximum delay (time output valid) of $T-t(mis) = 15\text{ ns}$ between falling edge of CLK (for MISO_HS_RD=0) and DO level becoming valid. For MISO_HS_RD=1 it's the rising edge of CLK. The timing is guaranteed for worst case condition: VDDD = 1.71 V, Tb = +70 °C, output load of Cload = 50 pF.

5.3.2 Logic Levels

The digital inputs and outputs are fully CMOS compatible (reported in Table 48). All IO input / output timings are based on 50% voltage reference levels (see Figure 46). I/O interfaces are shown in Figure 49, input pins, and Figure 50, output pins, which include internal pull-ups.

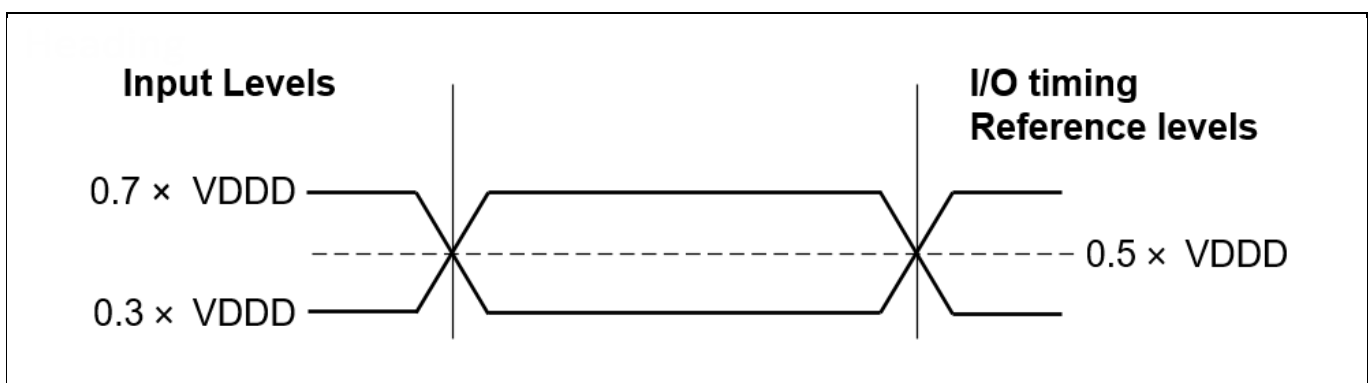


Figure 46 AC timing input/output reference levels

The input logic hysteresis prevents input buffers from oscillation. The minimum hysteresis range V_{HYST} is in between the lower ($0.3 \times V_{DDD}$) and upper logic level ($0.7 \times V_{DDD}$) boundaries (see Figure 47). Above $0.7 \times V_{DDD}$

Data Organization and SPI Interface

the input signal is a logical '1' while below $0.3 \times V_{DD}$ it is a logical '0' regardless of hysteresis. Due to temperature drifts and device variation the hysteresis range V_{HYST} can be up to $0.7 \times V_{DD}$ or down to $0.3 \times V_{DD}$ but typically around $0.5 \times V_{DD}$. Parameters reported in Table 48 and Table 49.

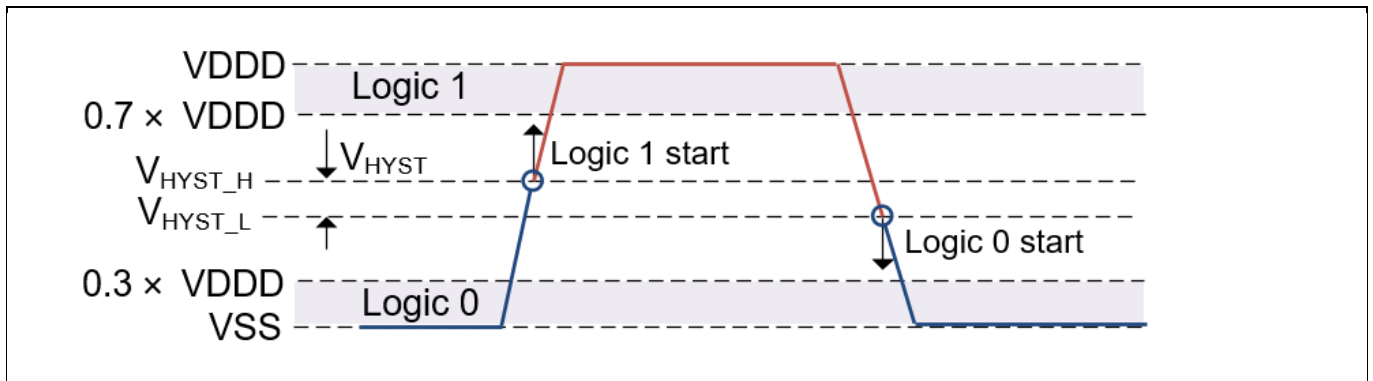


Figure 47 Logic input levels and hysteresis

The digital output pads have a fixed output pad strength that gives a specific slew-rate for rising signals, dV_{TR} , and falling signals, dV_{TF} (see Figure 48). Minimum slew rates were simulated considering a total capacitive load of 15pF. Results reported in Table 48 and Table 49.

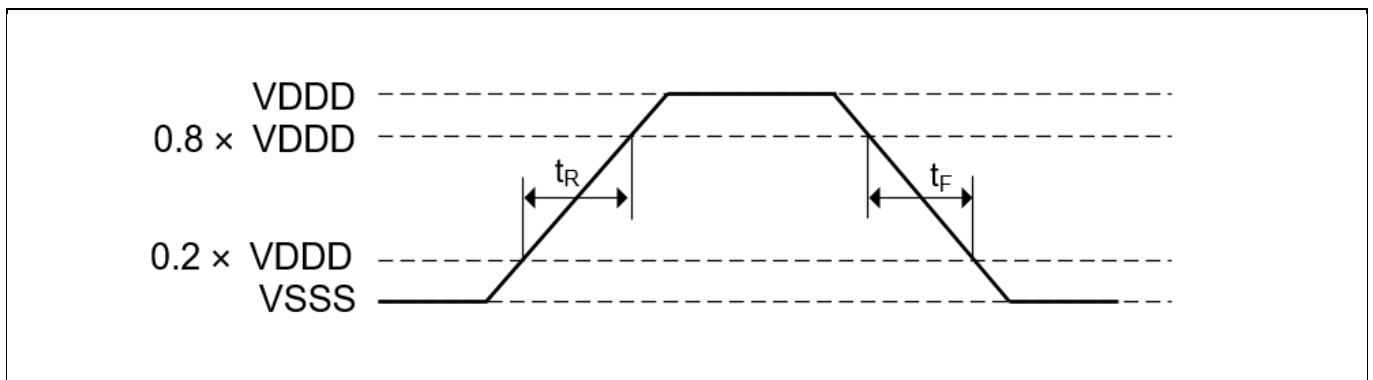


Figure 48 Rise/Fall Time, Slew Rate specified between $0.2 \times V_{DD}$ and $0.8 \times V_{DD}$

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Table 48 Logical Levels for input pins VDDD = 1.71 to 1.89 V, Tb = -20 to +70 °C, ambient temperature not below -40 °C; all voltages with respect to VSSD digital ground, positive current flowing into pin (unless otherwise specified)

| Spec | Symbol | Unit | Value | | | Condition |
|--|---------------|---------|----------------------|---|----------------------|-----------------------------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| LOW level | $V_{IN(L)}$ | V | 0 | | $0.3 \times V_{DDD}$ | |
| HIGH level | $V_{IN(H)}$ | V | $0.7 \times V_{DDD}$ | | VDDD | |
| Input current ($0V < V_{IN} < V_{DDD}$) | I_{IN} | μA | -150 | | 150 | |
| Input capacitance CLK/CS_N | C_{IN} | pF | | 2.0 | | |
| Input capacitance DI/DIO3 | C_{IN} | pF | | 3.15 | | |
| Minimum hysteresis voltage range between $0.3 \times V_{DDD}$ and $0.7 \times V_{DDD}$ | V_{HYST} | V | 0.175 | | | $V_{HYST_H} - V_{HYST_L}$ |
| Upper hysteresis signal level | V_{HYST_H} | V | | $0.5 \times V_{DDD} + \frac{V_{HYST}}{2}$ | $0.7 \times V_{DDD}$ | |
| Lower hysteresis signal level | V_{HYST_L} | V | $0.3 \times V_{DDD}$ | $0.5 \times V_{DDD} - \frac{V_{HYST}}{2}$ | | |

Data Organization and SPI Interface

Table 49 Logic Levels for output pins VDDD = 1.71 to 1.89 V, Tb = -20 to +70 °C, ambient temperature not below -40 °C; all voltages with respect to VSSD digital ground, positive current flowing into pin (unless otherwise specified)

| Spec | Symbol | Unit | Value | | | Condition |
|--|---------------|------|----------------------|---|----------------------|--|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| LOW level | $V_{OUT(L)}$ | V | 0 | | $0.3 \times V_{DDD}$ | |
| HIGH level | $V_{OUT(H)}$ | V | $0.7 \times V_{DDD}$ | | VDDD | |
| Output current (LOW) | $I_{OUT(L)}$ | mA | -5 | | | |
| Output current (HIGH) | $I_{OUT(H)}$ | mA | | | 5 | |
| Allowed load capacitance to provide maximum signal frequency on DO | C_{LOAD} | pF | | | 15 | |
| Minimum hysteresis voltage range between $0.3 \times V_{DDD}$ and $0.7 \times V_{DDD}$ | V_{HYST} | V | 0.175 | | | $V_{HYST_H} - V_{HYST_L}$ |
| Upper hysteresis signal level | V_{HYST_H} | V | | $0.5 \times V_{DDD} + \frac{V_{HYST}}{2}$ | $0.7 \times V_{DDD}$ | |
| Lower hysteresis signal level | V_{HYST_L} | V | $0.3 \times V_{DDD}$ | $0.5 \times V_{DDD} - \frac{V_{HYST}}{2}$ | | |
| Output pad slew rate for rising wave form | dV_{TR} | V/ns | 0.32 | | | $0.2 \times V_{DDD}$ to $0.8 \times V_{DDD}$ |
| Output pad slew rate for falling wave form | dV_{TF} | V/ns | 0.33 | | | $0.2 \times V_{DDD}$ to $0.8 \times V_{DDD}$ |

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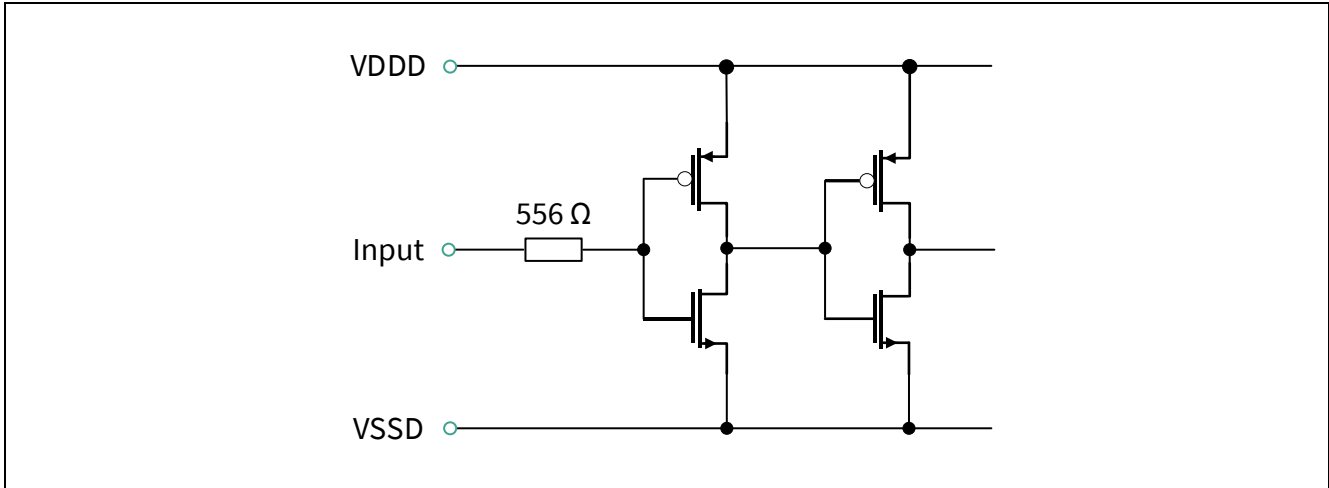


Figure 49 Interface for input pins CLK, CS_N, DI, DIO3

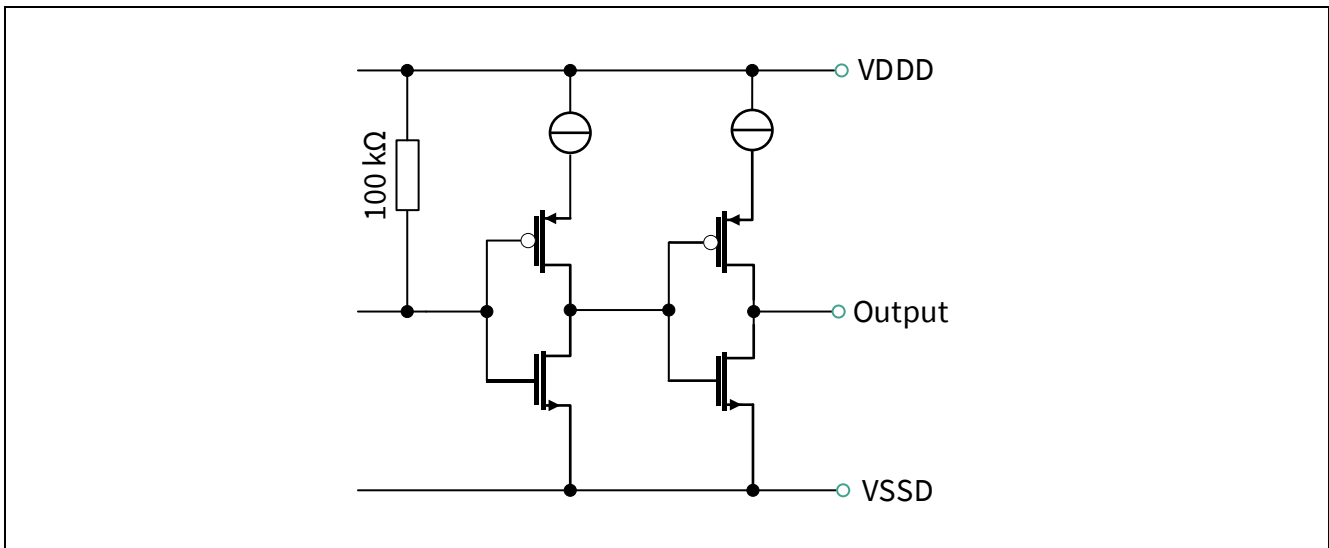


Figure 50 Interface for output pins IRQ, DO, DIO3

5.4 Overshoot and Undershoot Waveform Definition

During operation, the applied signals and supply levels should not exceed absolute maximum DC levels specified in datasheet. Digital signals can have positive or negative overshoots due to inductive and/or capacitive loads. The following Table 50 reports the allowed overshoot timings and signal levels for all logic signals.

Table 50 Overshoot and Undershoot Signal Levels

| Spec | Symbol | Unit | Value | | | Condition |
|---|--------|------|-------|-----|--------------|-----------|
| | | | Min | Typ | Max | |
| Maximum absolute overshoot voltage level | Vos | V | | | VDDD + 0.5 V | see Note: |
| Maximum absolute undershoot voltage level | Vus | V | | | VSS - 0.5 V | see Note: |

Note:

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Maximum pad current not exceeding ± 5 mA (see also Table 49). No slew rate limitation existing on digital signals for overshoots / undershoots.

5.5 IBIS Model

A BGT60TR13C IBIS Model is available under NDA upon request. It is based on timing simulations. In order to better reflect the real timing behavior, different pad models for input/output signals are used and summarized in Table 51. The driver strength for all pads are fix (PRG0=0).

Table 51 IBIS Pad Types and Models (see Ibis model)

| Pin | Ibis PAD Model |
|--------------|---|
| CSN | IN: MODEL_654_7345_110 |
| CLK | IN: MODEL_654_7345_110 |
| DIO0 / DI | IN: MODEL_8138_4982_52 OUT: MODEL_8138_4982_59 |
| DIO1 / DO | IN: MODEL_8138_4982_52 OUT: MODEL_8138_4982_59 |
| DIO2 | Not available on BGT60TR13C |
| DIO3 / Reset | IN: MODEL_8138_4982_52 OUT: MODEL_8138_4982_59 |
| IRQ | OUT: MODEL_8138_4982_55 |

5.6 SPI Functionality

Each word transferred over the SPI bus has a length of 1 command byte + 3 data Bytes. The communication is done bitwise. First the address is transferred with MSB first. The address is followed by the R/W-bit and then followed by the data which is sent MSB first, too. At the same time, while command byte is received, a freely from system level configurative global status register (8 bits, GSR0) is serial shifted out on DO (MSB first). On the following 24 clock cycles the selected register content is shifted out on DO, MSB first.

Depending on sent R/W-bit there are two different operation modes available, the write mode and the read mode. Every write mode is a read mode too.

Write-Mode

After the start condition the desired address is sent. The address is 7 bits long followed by a bit that is a data direction bit (read/write). A one indicates a write operation (see Figure 51).

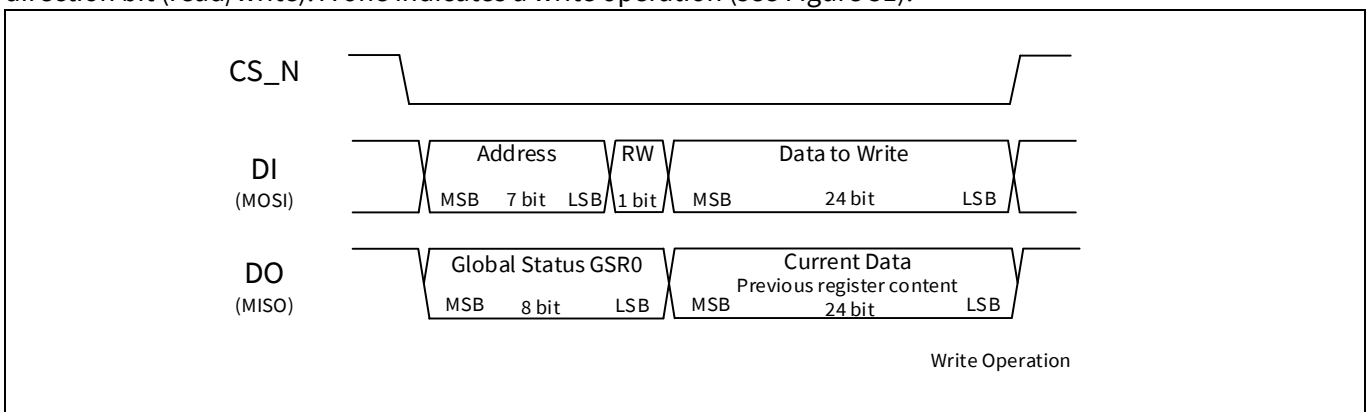


Figure 51 SPI timing write mode

Data Organization and SPI Interface

Read-Mode

After the start condition, the desired address is sent like in the write operation. A zero of the R/W-bit indicates a read access. The data on DI after the command byte may contain any value. The DO behavior is the same as in write mode.

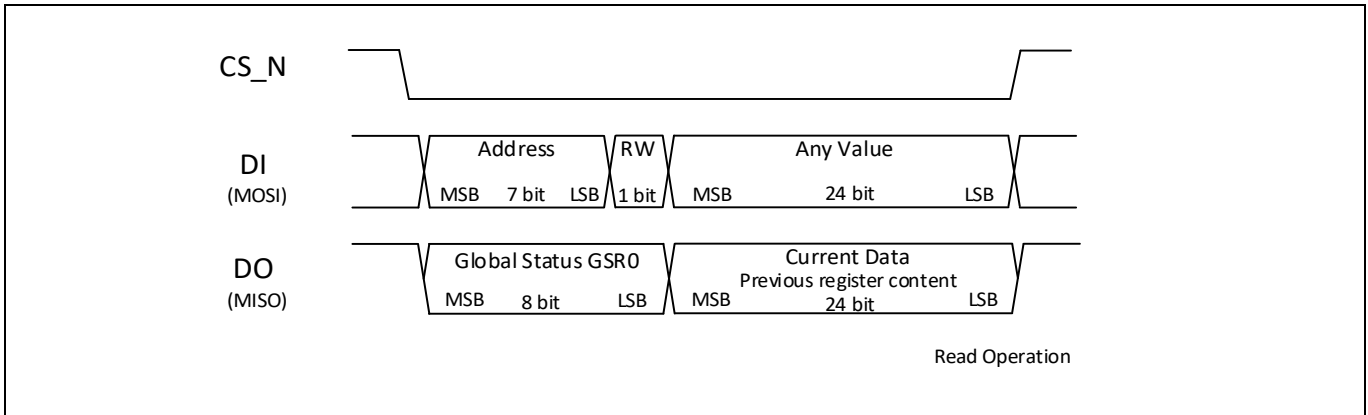


Figure 52 SPI timing read mode

5.7 SPI Burst Mode

The burst mode can be used to read or write out several registers or some data from the FIFO instead of reading just single registers or data. The burst mode command is sent by the host. The burst mode command consists of several bit fields and is shown in Figure 53.

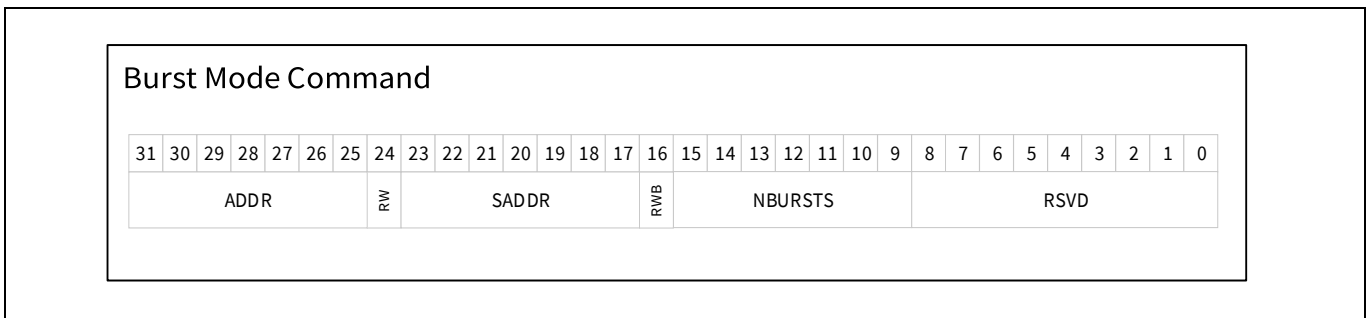


Figure 53 Burst mode command

The following Table 52 shows a detailed description on the burst mode command bit fields.

Table 52 Burst Mode Command Bit Field Description

| Bit field | Bit | Description | RST |
|-----------|-------|---|-----|
| ADDR | 31:25 | To enter the burst mode the following address is used: 0x7F ... request the burst read/write. | |
| RW | 24 | Read/Write register access: Fixed to 1 _B ... write to address 0x7F | |
| SADDR | 23:17 | Starting address where the burst starts processing: < 0x60 Register access == 0x60 FIFO access > 0x60 Reserved - Address is incremented automatically inside a burst. | |
| RWB | 16 | Burst read or write: 0 _B ... Perform a read burst | |

Data Organization and SPI Interface

| Bit field | Bit | Description | RST |
|-----------|------|--|-----|
| | | 1 _B ... Perform a write burst, (writes to FIFO not supported) | |
| NBURSTS | 15:9 | Number of processed data blocks: 0x00... “unbounded” burst accesses 0x01 to 0x7E ... number of words to transfer | |

Note:

A single data block is 24 bits width for both, the sampling memory and the registers.

Burst Mode Operation

After the start condition the 32 bits burst mode command is sent from the SPI master on DI. At the same time, the status register GSR0 (four 1_B bits + four status bits) followed by 24 padding bits set to 0_B is shifted out on DO. After the command sequence is done, the register/FIFO data is shifted out to the SPI master on DO. In burst write mode, the register data to be written is shifted in from the SPI master (application processor e.g.).

Burst Mode Read Sequence:

In the read sequence, the SPI master reads from the device.

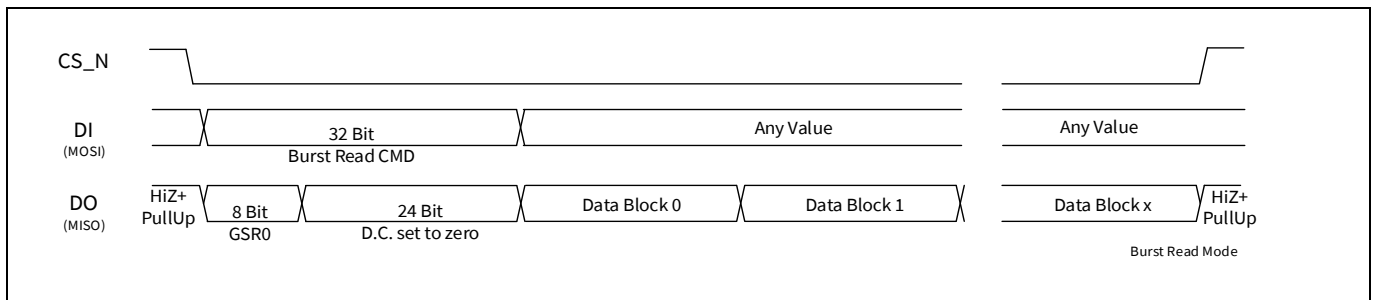


Figure 54 Burst mode read sequence

Burst Mode Write Sequence:

In the burst write mode, the SPI master writes to the device.

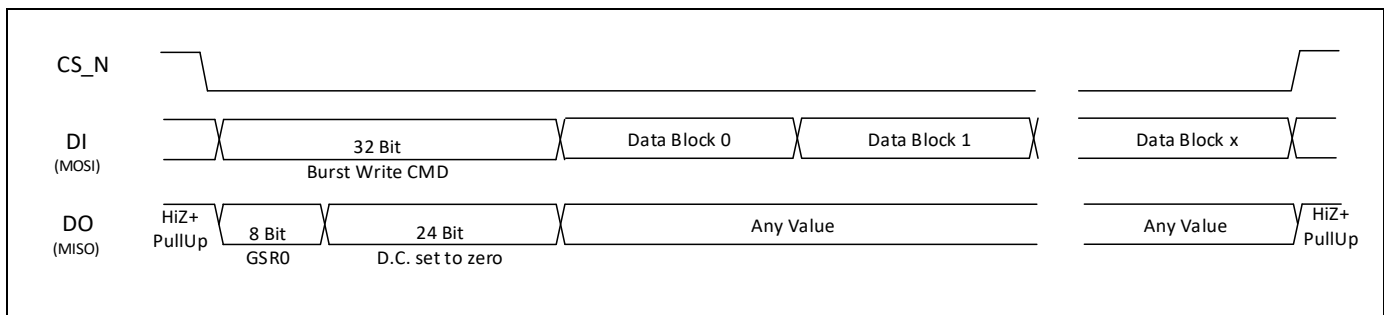


Figure 55 Burst mode write sequence

Sampling Data Arrangements in Data Blocks

The data from the FIFO are streamed out during the burst read request, starting from the FIFO address zero. The 1st ADC is the ADC channel with the lowest channel number. As far as the sampling memory is organized in 24 bits

Data Organization and SPI Interface

and up to three ADC channels are selectable through the ADC channel selection bits (CSx:BBCH_SEL, see section 4.10) the data blocks are arranged as follows.

In case a single ADC is selected, the data structure is shown in Figure 56.

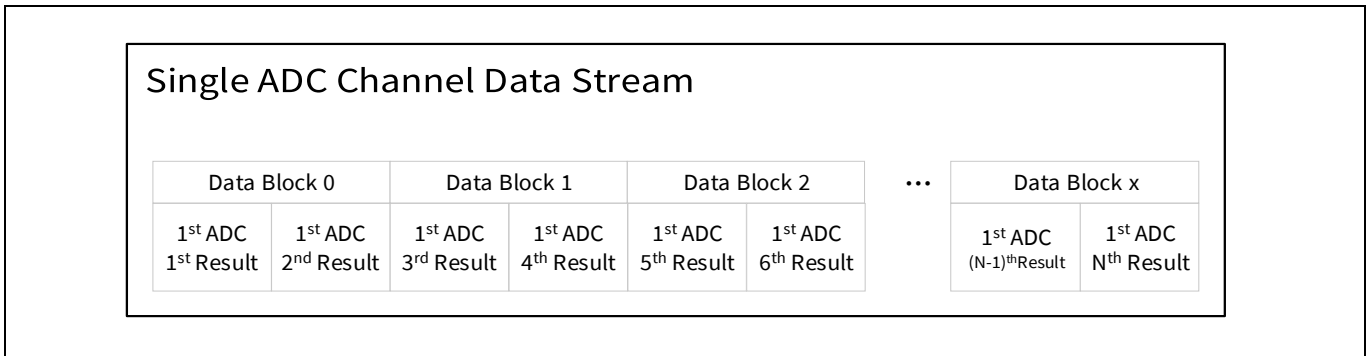


Figure 56 Single ADC channel selected

In case two ADCs are selected, the data structure is shown in Figure 57.

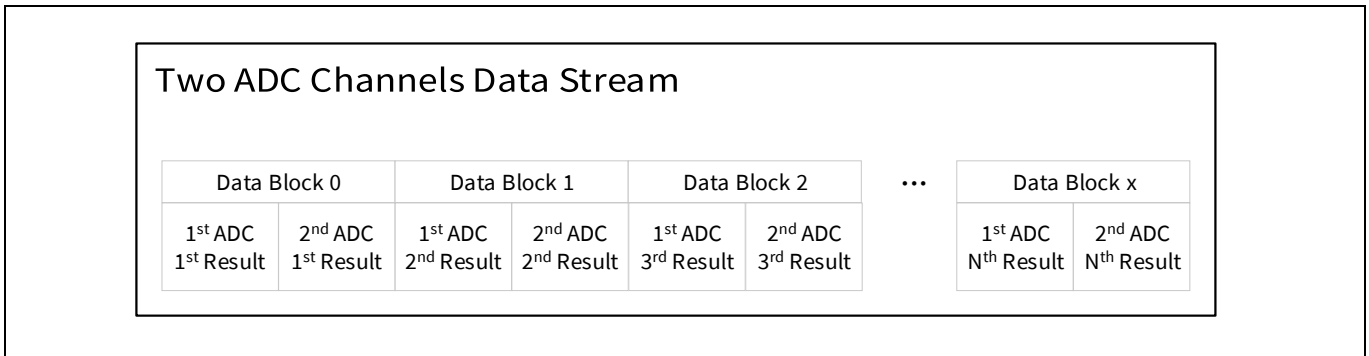


Figure 57 Two ADC channels selected

In case three ADCs are selected, the data structure is shown in Figure 58.

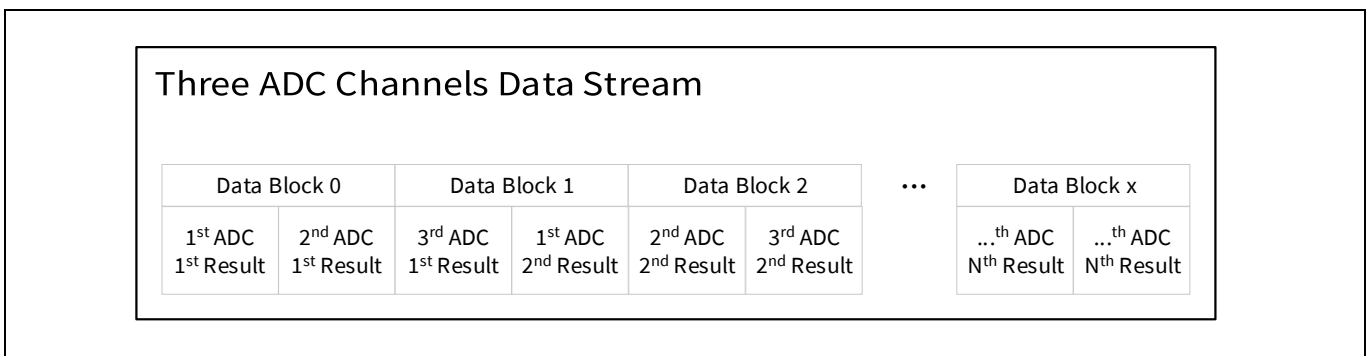


Figure 58 Three ADC channels selected

Example: Burst Mode Read Sampling Memory Sequence

The following burst mode command is sent from the host to initialize the burst mode to read from the FIFO an undefined number of sampling data:

```
BMCMD_RS = (ADDR = 0x7F, RW = 0x01, SADDR = 0x60, RWB = 0x0, NBURSTS = 0)
```

REMARK:

Data Organization and SPI Interface

For each burst read request to the sampling memory, the sampling-memory address pointer is reset to the initial value. So that memory can be read out from the beginning until the application processor stops burst reading.

Example: Burst Mode Read Registers Sequence

The following burst mode command is sent from the host to initialize the burst mode to read out 10 registers starting from register address 3:

```
BMCMD_RR10 = (ADDR = 0x7F, RW = 0x01, SADDR = 0x3, RWB = 0x0, NBURSTS = 10)
```

5.8 SPI Error Detection

SPI BURST_ERR and CLK_NUM_ERR (see also Table 43) will be cleared after these resets:

- SW reset
- HW reset

SPI BURST_ERR and CLK_NUM_ERR are reported in the global status bits of the next SPI transaction and latched as sticky bits in the FSTAT register.

In order to understand if the captured sample data are corrupted, the host can evaluate the bit field CLK_NUM_ERR and SPI BURST_ERR as reported in Table 53.

Table 53 SPI BURST_ERR and CLK_NUM_ERR Definitions

| Length Range | Transaction | SPI BURST_ERR | CLK_NUM_ERR | Behavior on read/write |
|--------------|--|----------------|----------------|------------------------------------|
| 0 | Null command | 0 _B | 0 _B | Ignored |
| 1-31 | Short length error in single | 0 _B | 1 _B | Command ignored |
| >32 | Long length error in single | 0 _B | 1 _B | Extra bits ignored |
| 1-31 | Short length error in SPI burst header | 0 _B | 1 _B | Command ignored |
| <24xN | Missing whole data word in bounded burst | 1 _B | 0 _B | Available data words used |
| >24xN | Extra whole data word in bounded burst | 1 _B | 0 | Extra data word(s) ignored |
| %24>0 | Misaligned bit-count for bounded burst | 1 _B | 1 _B | Extra bits ignored |
| %24>0 | Misaligned bit-count for infinite burst | 0 _B | 1 _B | Partial data word may be discarded |

Note:

- Ignored write transaction means that no register (or memory) content is affected by the partial write command, or incomplete data word.
- Ignored read transaction means that the returned data is invalid, and for the FIFO no words are removed by the partial read command, or incomplete data word.
- Discarded read transaction means that the data is already read from the FIFO but only partially transferred; subsequent read pops next word from FIFO.

Data Organization and SPI Interface

- Data from the FIFO may be discarded after a length error in the infinite burst (NBURST=0) occurs. The FIFO read has to happen, since at that stage the data is required to be shifted out, but if not all bits are shifted out the FIFO is already read and the partial data word may be discarded.

5.9 Hardware Reset Sequence

The chip should not be in reset state after any reset condition (SW, HW, FIFO, and FSM- reset) especially when no external clock OSC_CLK is applied (see Table 2). For a proper device reset a special reset sequence is required:

While CS_N is '1_B' DIO3 must perform a 1_B → 0_B → 1_B transition

The behavior is presented in Figure 59 with:

T_CS_BRES = 100 ns

T_RES = 100 ns

T_CS_ARES = 100 ns

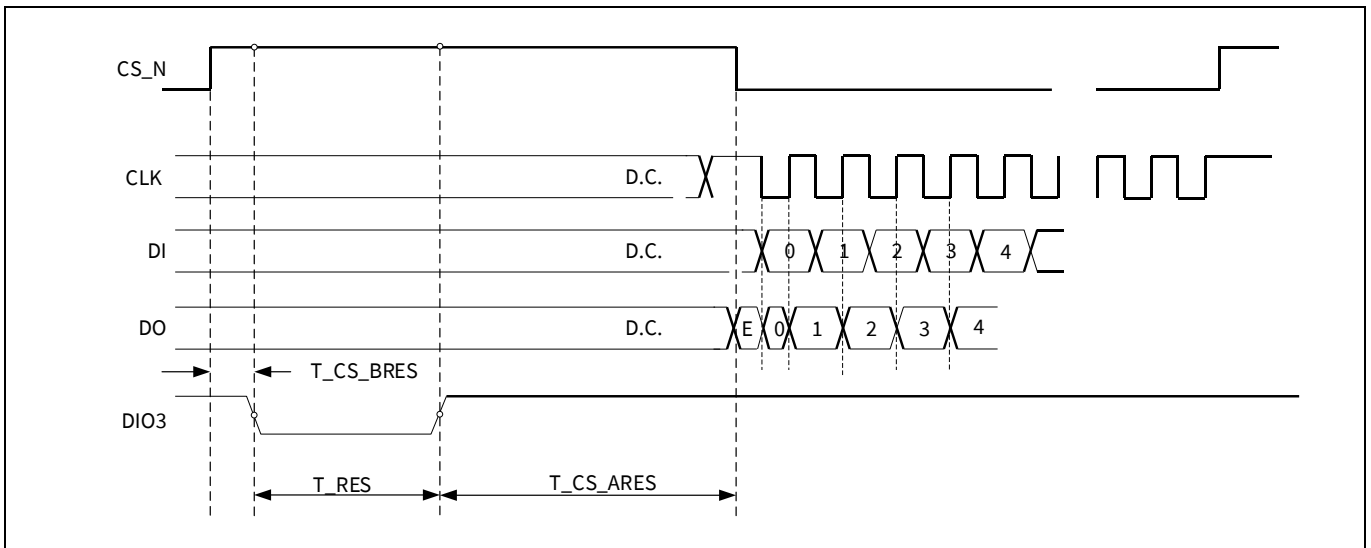


Figure 59 Hardware reset Sequence

5.10 Software Triggered Resets

Besides the hard reset, three reset sequences are supported and can be triggered in the ISO register (see also 4.2). They are defined according to the following hierarchy:

Soft reset → FIFO reset → FSM reset

* **Software Reset**

- Resets all registers to default state
- Resets all internal counters (e.g. shape, frame)
- Perform FIFO reset
- Performs FSM reset
- A delay of 100 ns after the SW_RESET is needed before the next SPI command is sent

* **FIFO Reset**

Data Organization and SPI Interface

- Reset the read and write pointers of the FIFO
- Array content will not be reset, but cannot be read out
- FIFO empty is signaled, filling status = 0
- Resets register FSTAT
- Performs an implicit FSM reset

*** FSM Reset**

- Resets FSM to deep sleep mode
- Resets FSM internal counters for channel/shape set and timers
- Resets STAT0 and STAT1 register
- Reset PLL ramp start signal
- Reset PA_ON
- Terminates frame (shape and frame counters incremented although maybe not complete)

PLL Domain Functional Specification

6 PLL Domain Functional Specification

The PLL is designed to generate high performance frequency chirps in the range of 58 GHz to 63.5 GHz. The modulation is performed inside the PLL bandwidth (in-band-modulation) with an analog charge pump based fractional-N RF-PLL architecture. It furthermore features a shape generator with high flexibility to allow different ramp shapes and duration times. The loop requires a low noise reference clock with a nominal frequency of 80 MHz.

6.1 PLL Interfaces and Clock Distribution:

Figure 60 shows the interfaces to the PLL and the distribution of the 80 MHz reference clock.

6.2 Reference Clock Distribution

The external 80 MHz reference clock signal is provided via a short, low jitter path directly to the input of the PLL analog part. From there the clock is distributed to the reference clock buffer of the PLL and also via another path to the STS, which is the defined interface between the PLL analog and the digital part. These paths are independent from each other since the clock provided through the STS to the output of the PLL macro (“osc_clk2dig”) serves as the clock for the main FSM. It must be available even when the PLL is put into power down. Therefore, the usage of internally generated supplies of the PLL is avoided. The main FSM clock can be gated via a dedicated register bit called PACR1:OSCCLKEN (see section 4.6) which quiets the clock path already at its beginning.

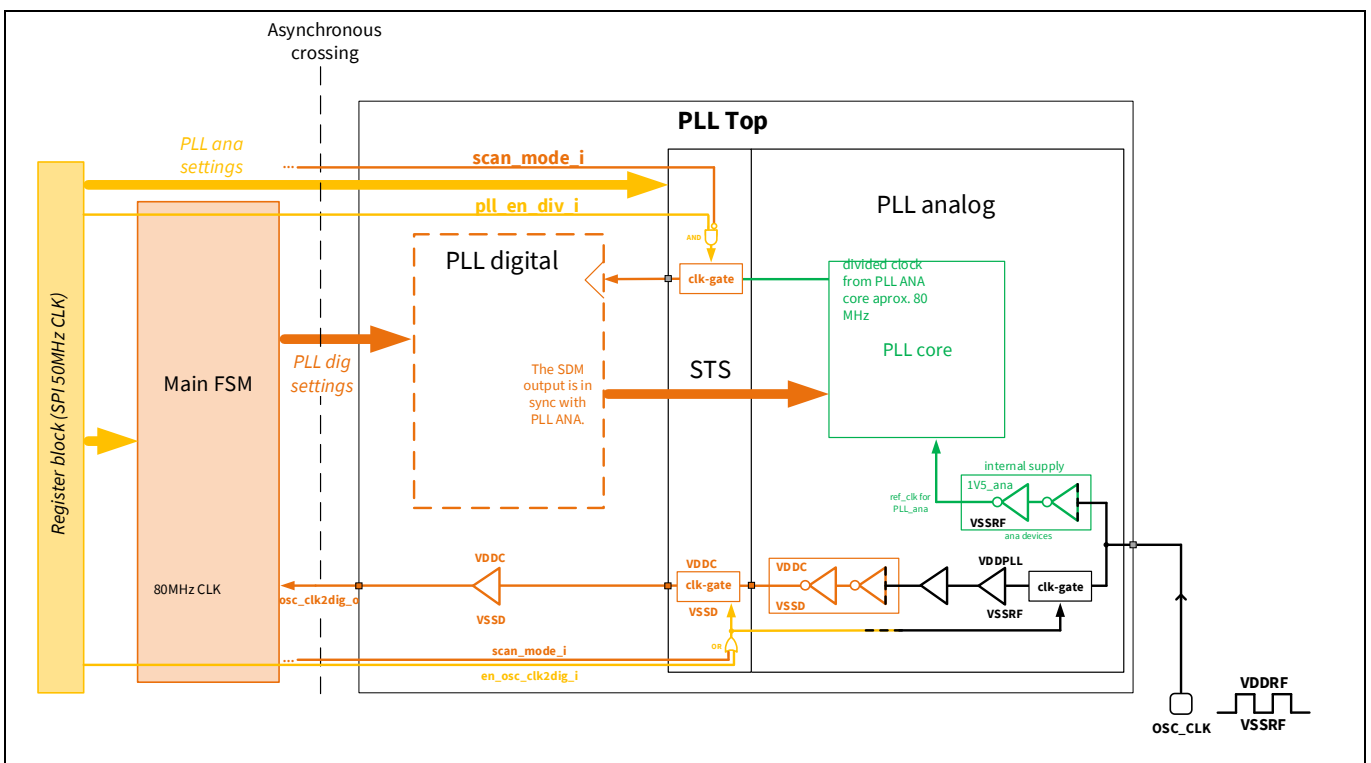


Figure 60 PLL and 80 MHz clock interface to the main FSM

PLL Domain Functional Specification

6.2.1 Interfaces to the PLL

Most static settings and control signals dedicated to the analog part of the PLL are treated as asynchronous signals and are passed from the register bank to the STS of the PLL. This applies to digital signals that are not timing critical. Ramp generation parameters provided from the main FSM to the digital part of the PLL are registered inside the PLL digital. The start signal of the ramp also acts as a synchronization signal of the ramp parameters. This is required since the PLL digital runs on the divided clock of the PLL which ensures a known and synchronous timing relation between the sigma-delta bit stream and the analog part of the PLL that realizes the ramping behavior. The divided clock is only available if the PLL macro and the VCO are activated. Other control signals from PLL digital to the analog part are kept asynchronous. In order to close the PLL loop the analog part of the PLL core has interfaces to the RF-macro where the VCO and a part of the divider chain are located.

6.3 PLL Parameters and Specification

Table 54 summarizes the target parameters of the PLL-based frequency generator.

Table 54 PLL Specifications, VDDPLL = 1.71 to 1.89 V, VDDLDF = 2.5 to 3.63 V, Tb = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition/Note |
|--|-------------------|--------------|-------|-----|------|---|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Reference Clock | | | | | | |
| Reference Frequency | f_{ref} | MHz | 75 | 80 | 85 | $f_{ref} = f_{SYS_CLK}$ See 2.2 78 MHz not allowed |
| Rise and Fall Time of Reference Clock | $t_{rs,fs,clk}$ | ns | | | 2 | 1.8 V CMOS clock |
| PLL Chirp Parameters | | | | | | |
| Output Frequency Range | f_{RF} | GHz | 58.0 | | 63.5 | Range depends on the VDDLDF value |
| Continuous FM-Chirp Bandwidth | BW | GHz | 0 | | 5.5 | PLL tuning range |
| VDDLDF Range | VDDLDF | V | 2.5 | | 3.63 | 5.5 GHz modulation BW requires at least VDDLDF= 3.3V |
| Chirp slope | Slope | MHz/ μ s | | | 400 | |
| Frequency Ramp Linearity Error | Error | % | | | 1 | For 2 GHz BW minimum See 6.3.1, Figure 12, Table 15 |
| Frequency Ramp Settling Time (fast chirp feature active) | $t_{PLL,settle}$ | μ s | | 5 | | See 6.3.2, section 3.3.5 |
| PLL Phase Noise Single Sideband | $PN_{PLL,100kHz}$ | dBc/Hz | | -80 | -75 | @100kHz offset |

PLL Domain Functional Specification

6.3.1 Frequency Ramp Linearity Definition:

Frequency ramp linearity error is defined to be <1% of the FM-chirp bandwidth. The linearity error is calculated as the deviation from an “ideal” frequency ramp. The specification needs to be fulfilled after the frequency ramp settling time (see also section 3.3). The assumed worst-case FM-chirp bandwidth for linearity evaluations is 2 GHz.

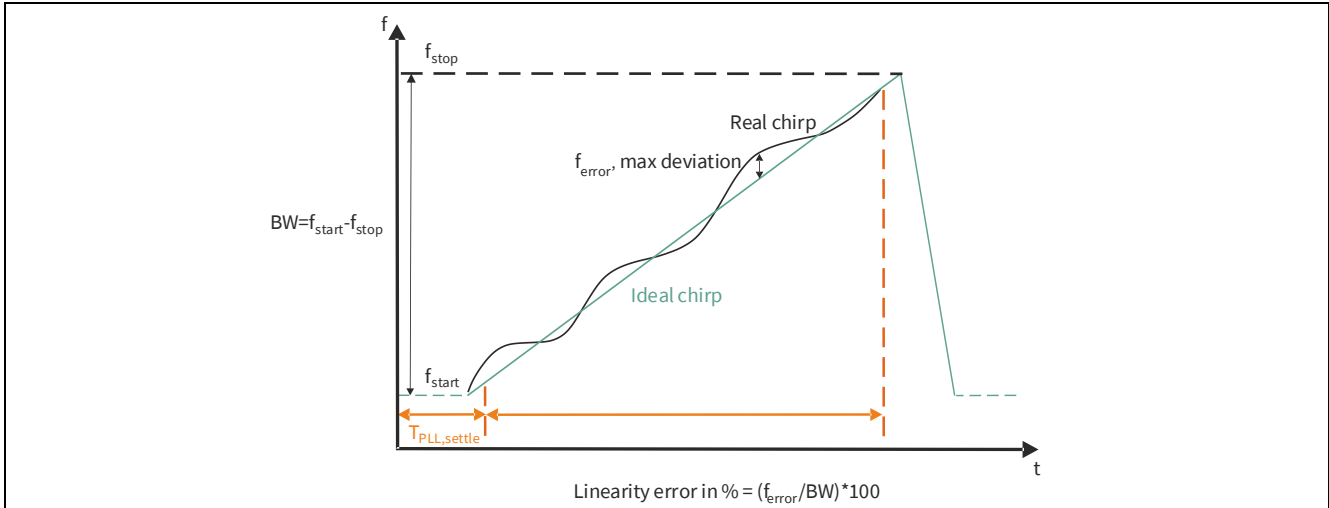


Figure 61 Frequency linearity definition

The max frequency error expected, assuming 2 GHz minimum BW and a max deviation of 1%, will be 20 MHz.

6.3.2 Frequency Ramp Settling Time

It is the time required by the PLL to damp undershoot and overshoot in case of saw-tooth shapes. A qualitative view is shown in Figure 62. See section 3.3 for a more detailed definition of the timings.

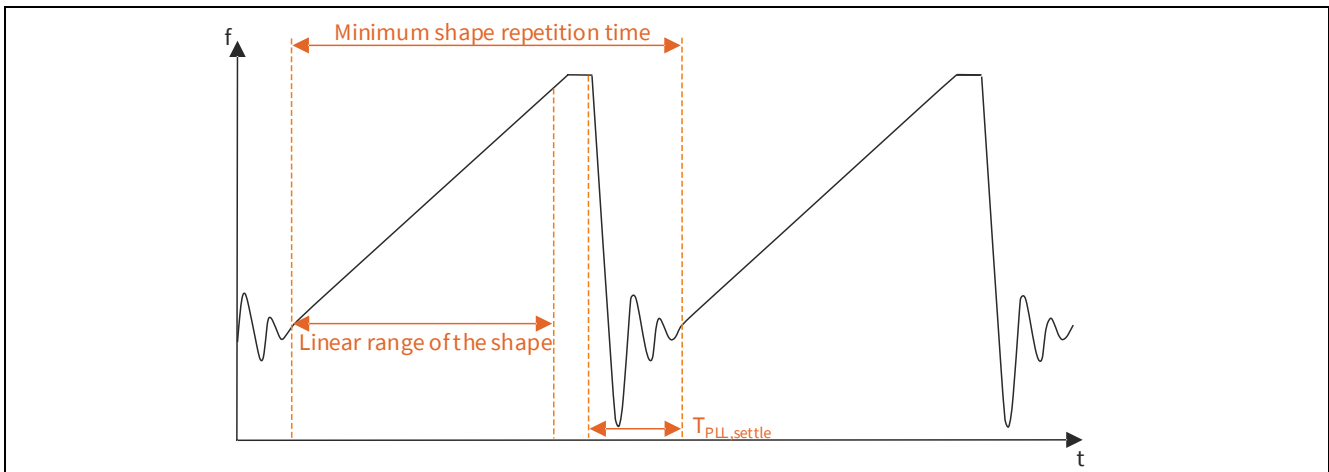


Figure 62 Chirp settling time

Analog-RF Domain Functional Specification

7 Analog-RF Domain Functional Specification

In the analog functional specification all analog components like RF frontend (RF FE), baseband amplifiers, and filters are described in more details.

The register definitions for the components are in section 4.10.

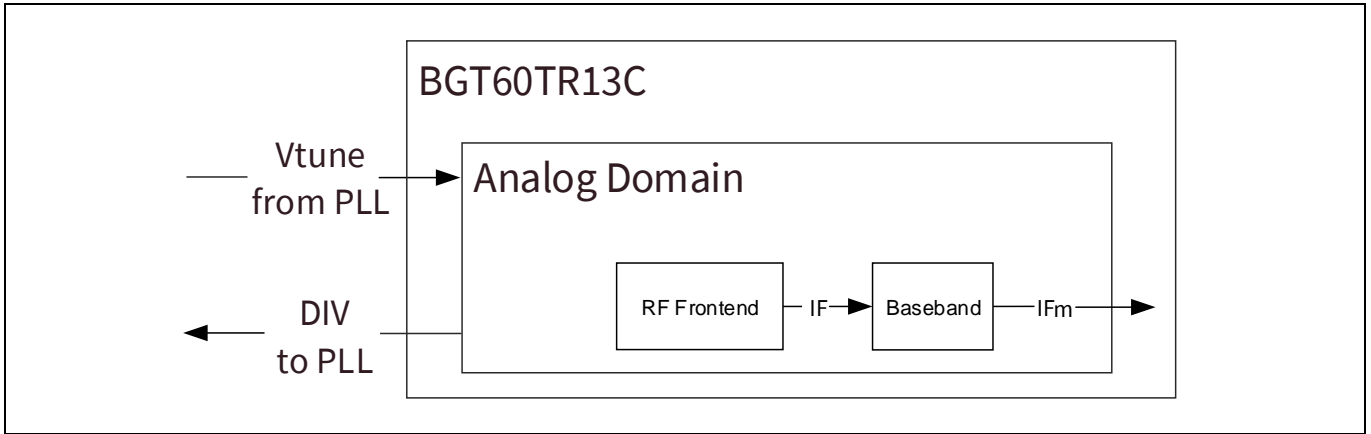


Figure 63 Analog domain simplified block diagram

7.1 RF Frontend (RF FE)

In the RF frontend, all features to enable the radar functionality are implemented.

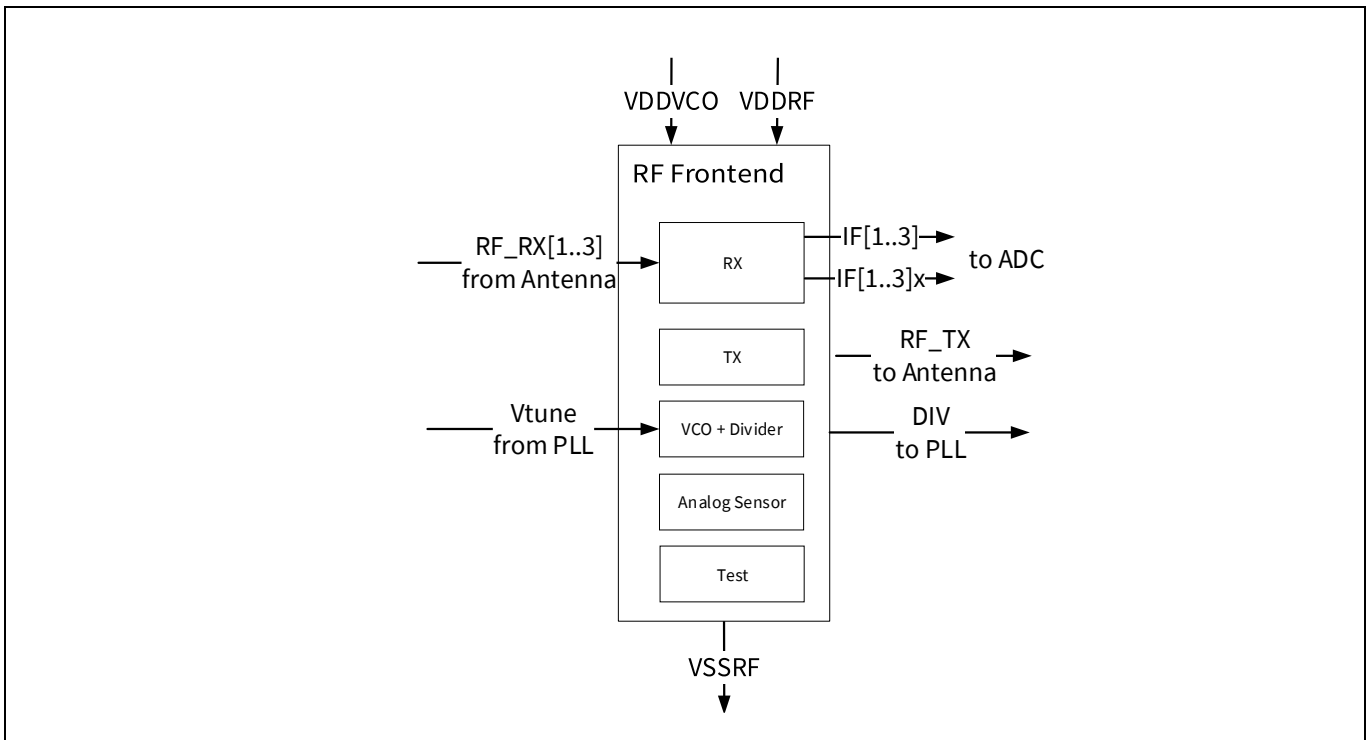


Figure 64 Simplified block diagram of BGT60TR13C transceiver frontend

7.1.1 On-Chip Analog Sensor Output

The analog sensor outputs are connected to the SADC. See section 4.9 for the SADC input configuration. See also section 4.10 for enable pins definition.

Analog-RF Domain Functional Specification

7.1.2 RF FE Specifications

In the table below the target specifications for the RF frontend measured at die PAD interface.

Table 55 RF FE Specifications, min and max values cover the specified frequency range, $f_{RF} = 58.0$ to 63.5 GHz. Temperature range, $T_b = -20$ to $+70$ °C, and voltage supply range, $V_{DDRF} = 1.71$ to 1.89 V (unless otherwise specified)

| Spec | Symbol | Unit | Value | | | Condition |
|--|----------------------------------|--------------|--|---------|---------|---------------------------------------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Frequency Range | f_{RF} | GHz | 58.0 | | 63.5 | |
| Transmitter | | | | | | |
| Transmit Output Power ¹⁾ | P_{TX} | dBm | 1.0 | 4.0 | 8.0 | Conductive Power |
| Output Power Variation over Temperature | P_{TX_Temp} | dB | -2.0 | | +2.0 | For Tx DAC set to #31 |
| Transmitter Power Control Dynamic Range | P_{TXD} | dB | | 15 | | |
| DAC Resolution Transmitter Power Control | P_{TXC} | Bits | | 5 | | By design |
| Receiver (for all three RX channels) | | | | | | |
| Receiver Conversion Gain ²⁾ | CG_{RX} | dB | 12 | 14 | 16 | |
| Conversion Gain Variation Over Temperature | CG_{RX_Temp} | dB | -3 | | +3 | Including the complete baseband chain |
| Receiver Single Sideband Noise Figure | $NF_{SSB_{RX}}$ | dB | | 12 | 14 | @100kHz offset |
| Receiver 1-dB Compression Point | $P-1dB_{RX}$ | dBm | -10 | -5 | | |
| Channel-to-Channel RX Isolation ³⁾ | ISO_{RX} | dB | | 40 | | |
| LO feedthrough at the RX port ³⁾ | $LO_{feed_{RX}}$ | dBm | | -30 | | |
| TX-to-RX Isolation ³⁾ | ISO_{TXRX} | dB | | 50 | | |
| Sensors | | | | | | |
| Temperature Sensor Range | T_b | °C | -40 | | 105 | |
| Chip Backside Temperature (Temp) Vs Temperature Sensor Readout (Tsense) Relation | Temp Tsense | °C V | $Temp = \frac{Tsense - a}{b}$ | | | |
| Temperature Sensor Offset (a) | a | V | 0.77384 | 0.78984 | 0.80584 | |
| Temperature Sensor Slope (b) | b | V/K | | 0.00286 | | |
| Output Power at Chip Pad Vs TX Peak Detector Readout Relation | Pout PPD_PA ⁴⁾ | dBm V | $P_{out} = t_1 * \ln\left(\frac{PPD_PA + y_0}{A_1}\right)$ $y_0 = 0.00836$ V $A_1 = 0.09972$ V $t_1 = 8.82773$ dBm | | | PPD_PA selected at SADC input |
| TX Peak Detector Accuracy | PPD_PAacc | dB | -2 | | +2 | Over f_{RF} |
| TX Peak Detector Dynamic Range | PPD_PA _{DR} | dBm | -10 | | +10 | Min. 8 bits SADC |

¹⁾: at die pad

²⁾: power to voltage gain;

Analog-RF Domain Functional Specification

³⁾: not including the package

⁴⁾: output power can be evaluated by sampling the level of the peak detector level at the output of the TX power amplifier. This signal has to be compared to a reference to de-embed thermal drift of the sensor. Therefore, both signals on channel SADC:CH3 (pd_out) and SADC:CH4 (pd_outx) are sampled by the SADC in two consecutive steps. PPD_PA= pd_out - pd_outx. See section 4.9.

Note: The 80 MHz spur clock signal could affect the SADC the readout (+/- 10mW). In order to have a more stable read out for the sensors, 16 avg for each sensor measurement are recommended.

7.2 Analog Baseband: Amplifiers and Filters

The baseband amplifiers and filters adjust the IF signals to fulfill the system requirements. They set the signal levels to drive full scale the ADC inputs without clipping.

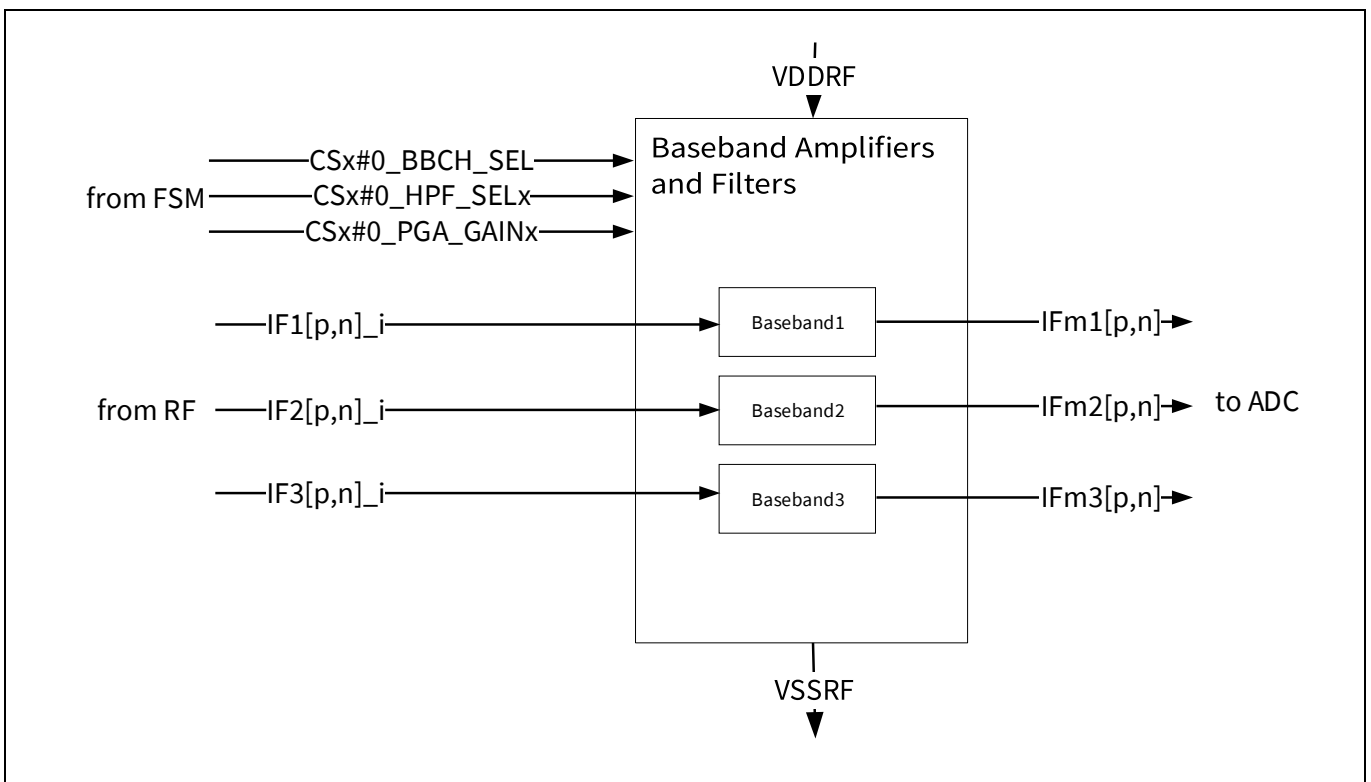


Figure 65 Baseband amplifiers and filters block diagram

Analog-RF Domain Functional Specification

7.2.1 Baseband Characteristics

The baseband block consists of three channels. Each channel consists of a high pass filter (HPF), a variable gain amplifier (VGA), and anti-aliasing filter (AAF) plus a driver for the ADC (see Figure 67).

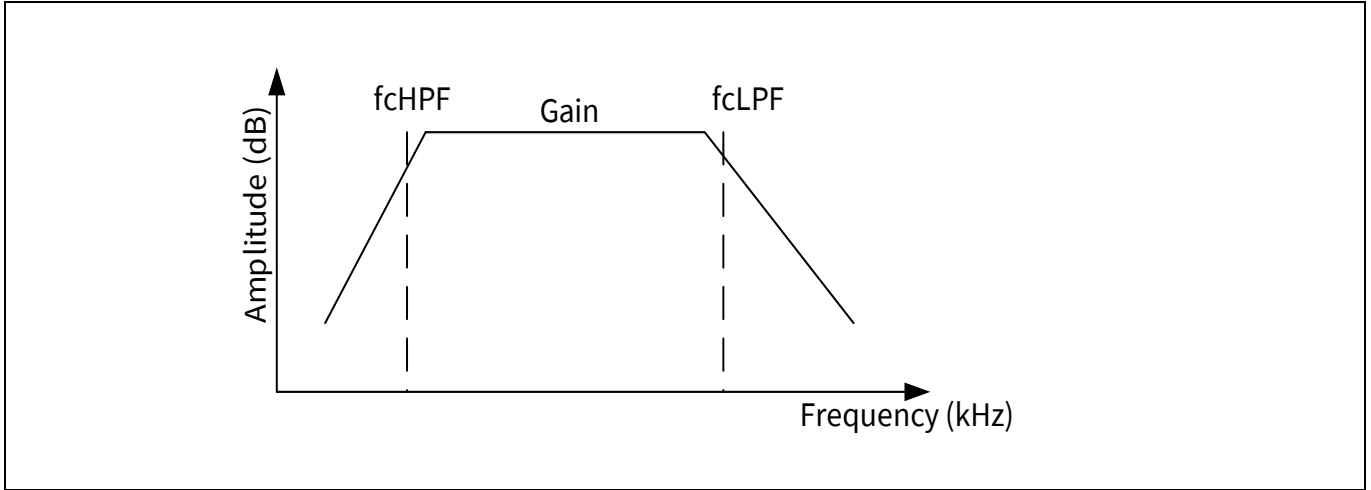


Figure 66 Baseband characteristic

The high pass filter is used in order to remove the DC-offset at the output of the RX mixer and also suppress the reflected signal from close in unwanted targets (e.g., radome).

7.2.2 Baseband Requirements

The high pass filter can be tuned to accommodate different f_{cHPF} according to different modulation parameters. As presented in Table 56 four different settings are possible.

Given the expected power levels the radar system will deal with, the HPF should not degrade the linearity of the system.

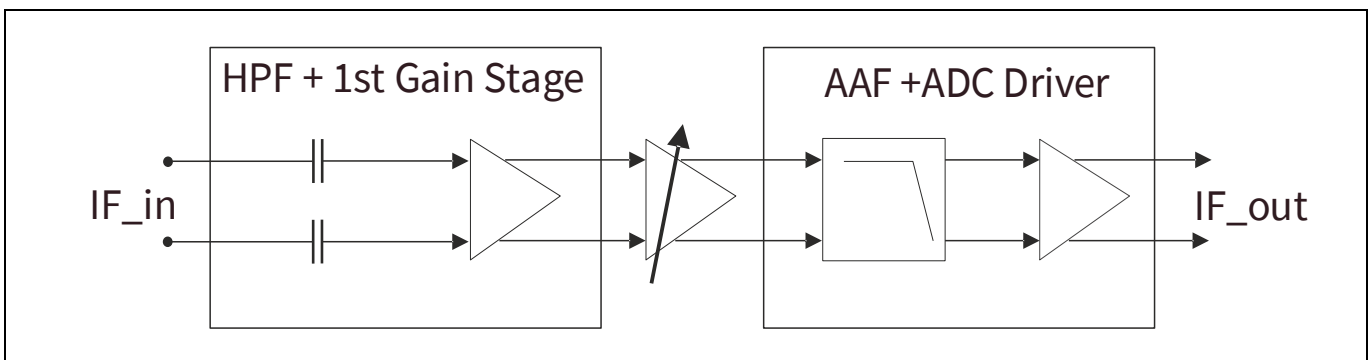


Figure 67 Baseband simplified block diagram, one for each channel

After the AC-coupling, the IF signals are amplified by the first amplifier stage. The first stage shows a selectable voltage gain of 18 or 30 dB. The gain can be adjusted in the VGA in 6 steps of 5 dB each up to a maximum gain of 30 dB. The VGA is followed by a two-stages, four-poles antialiasing filter. The signal is then applied to an ADC driver amplifier, which has a gain of 1. Overall, the baseband chain can be set to a maximum gain of 60 dB.

The specific parameters of the baseband chain are summarized in Table 56, Table 56, and Table 57

Analog-RF Domain Functional Specification

Table 56 High Pass Filter Selection. VDDRF = 1.71 to 1.89 V, Tb = -20 to +70 °C

| Spec | Unit | Value | | | Description |
|-----------|------|-------|-----|-----|---------------------------|
| | | Min | Typ | Max | |
| Parameter | | | | | |
| Fc_HPF_0 | kHz | 12 | 20 | 28 | HPF 3 dB cutoff frequency |
| Fc_HPF_1 | kHz | 32 | 40 | 48 | HPF 3 dB cutoff frequency |
| Fc_HPF_2 | kHz | 63 | 70 | 93 | HPF 3 dB cutoff frequency |
| Fc_HPF_3 | kHz | 65 | 80 | 95 | HPF 3 dB cutoff frequency |

Table 57 Baseband Gain Stages, VDDRF = 1.71 to 1.89 V, Tb = -20 to +70 °C

| Spec | Unit | Value | | | Description |
|----------------------------|------|-------|-------|-----|-----------------------|
| | | Min | Typ | Max | |
| Parameter | | | | | |
| 1 st Gain Stage | dB | | 18/30 | | Selectable, by design |
| VGA | dB | | 30 | | 6 steps |
| VGA Step Size | dB | 4 | 5 | 6 | |

Table 58 Antialiasing Filter Specification, VDDRF = 1.71 to 1.89 V, Tb = -20 to +70 °C

| Spec | Unit | Value | | | Description |
|--------------|------|-------|-----------------|-----|--|
| | | Min | Typ | Max | |
| Parameter | | | | | |
| fcLPF | kHz | 450 | 500 | 650 | 3 dB cutoff frequency |
| LPF_Order | | | 2 nd | | Four poles, by design |
| LPF_Flatness | dB | | 1 | | In band flatness, guaranteed by design |

MADC Domain Functional Specification

8 MADC Domain Functional Specification

The multichannel ADC (MADC) block consists of three differential SAR ADCs. The three ADCs are capturing the three differentials IF output signals from the baseband and convert them into a digital representation of the same. The one 1.5 V supply (VDDC) is internally generated by a dedicated LDO (see Figure 4). This block is enabled by bit MADC_EN in Table 30, parameters are set in 4.3. Each channel of the MADC can be enable/disable together with the respective baseband channel by the bits BBCH_SEL in Table 30. To simplify the dataflow to the memory either one single ADC channel, two single ADC channels or three single ADC channels can be selected via the BBCH_SEL in Table 30. See also APU and APD in Table 37 and paragraph 5.2.

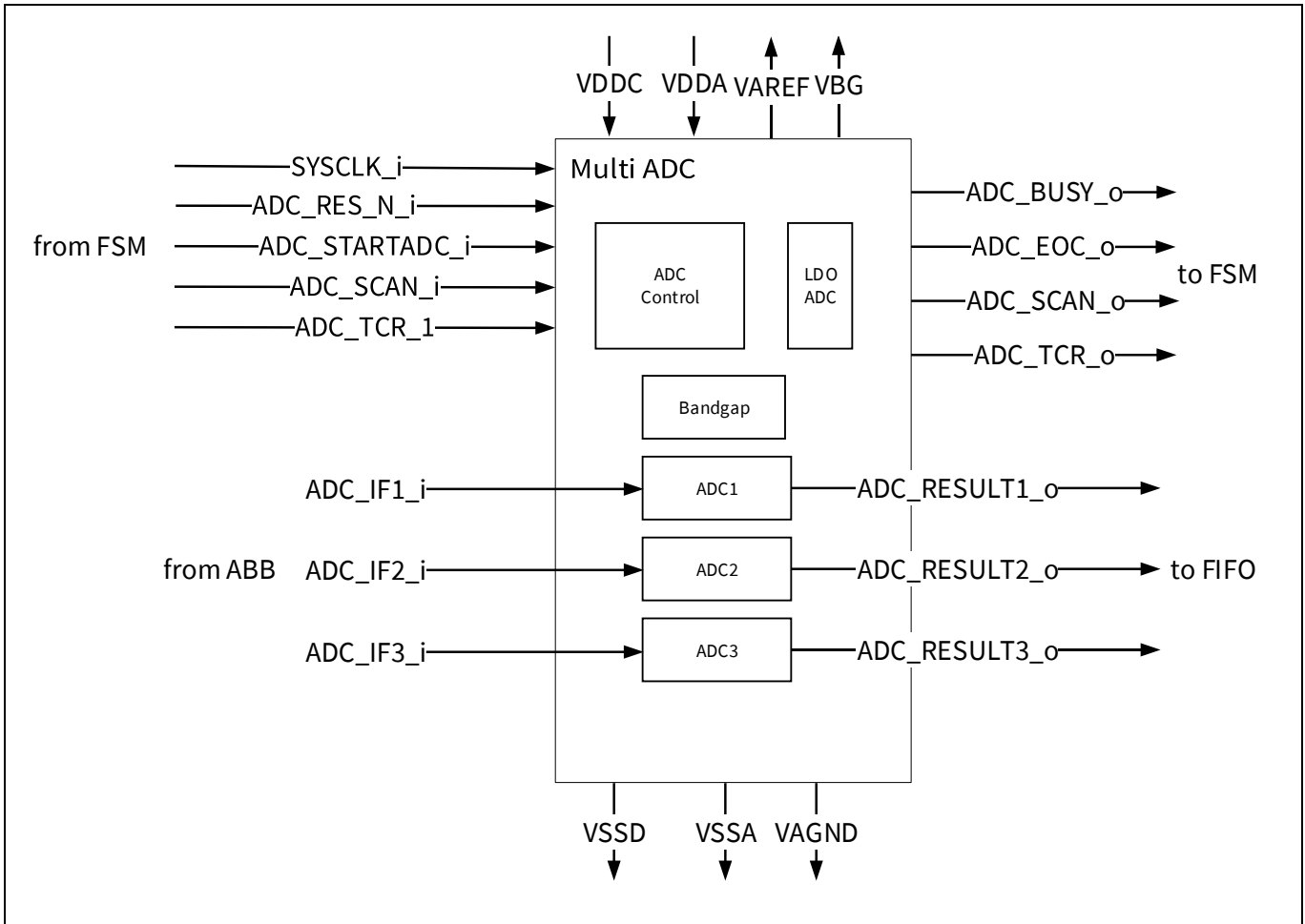


Figure 68 MADC block diagram

8.1 MADC Supply Voltage Requirements

The voltage supply to the ADC domain is provided on pin VDDA and the output of the internal ADC reference voltage is provided on pinVAREF. In order to filter out the voltage ripples due to switching effects a low ESR bypass capacitor of $C_{b2} = 470 \text{ nF}$ should be used on the PCB.

MADC Domain Functional Specification

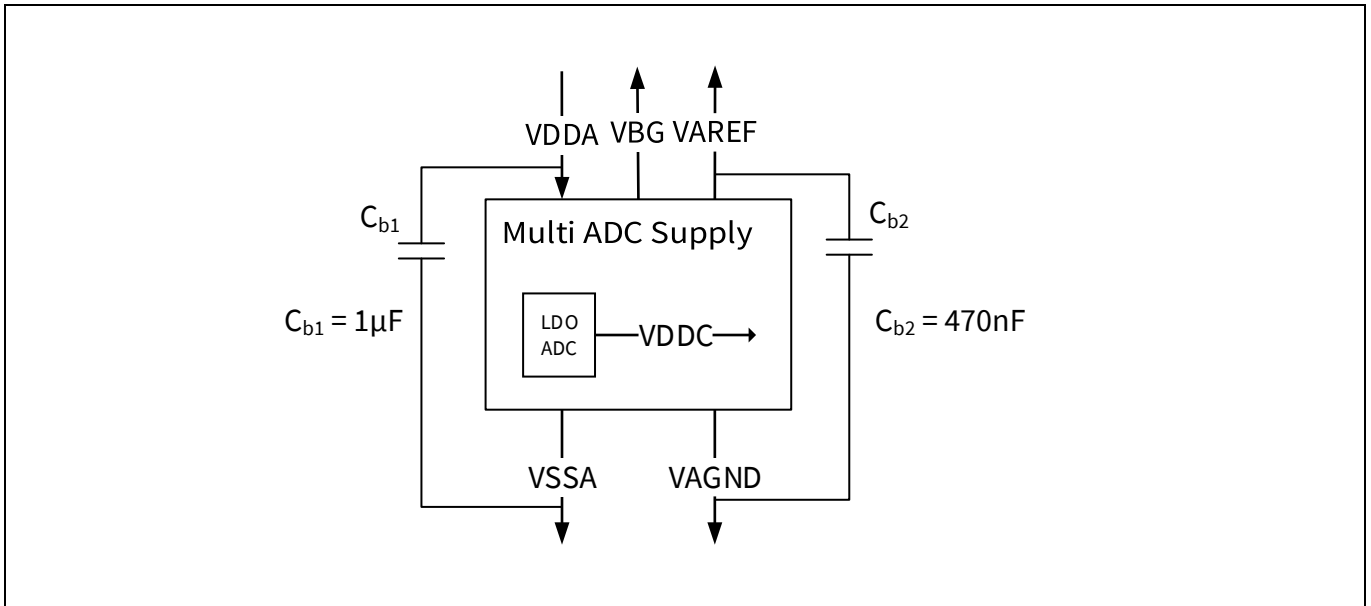


Figure 69 MADC input pin requirements

Both ground connection pins VSSA and VAGND share the same analog ground connection on PCB. The bypass capacitors should be mounted as close as possible to those pins.

Table 59 MADC Voltage Reference, VDDA = 1.71 to 1.89 V, T_b = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|--|--------|------|-------|-----|------|-------------------------------------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Positive reference voltage with respect to VAGND, generated internally | VREFP | V | 1.14 | 1.2 | 1.26 | |
| Negative analog reference voltage | VAGND | V | 0 | | 0.1 | Refers to board design ground plane |

8.2 MADC Specifications

Table 60 below specifies the ADC parameters. The numbers include one over-conversion. All parameters are only valid with executed startup calibration. No parameter is targeted for production test.

Note:

$$f_{ADC_CLK} = f_{SYS_CLK}$$

REMARK:

If the ADC starts sampling before the bandgap is powered up (BG_EN in Table 32), the results will show some gain errors. To avoid this, follow the bandgap power up timing presented in section 8.4.

Table 60 MADC Specifications, VDDA = 1.71 to 1.89 V, T_b = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|------------|--------|------|-------|-----|-----|---------------------------|
| | | | Min | Typ | Max | |
| Parameter | | | Min | Typ | Max | |
| Resolution | | | | 12 | | With default settings and |

MADC Domain Functional Specification

Table 60 MADC Specifications, VDDA = 1.71 to 1.89 V, Tb = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|--|----------------------|---------------|-------|------|-------|---|
| | | | | | | |
| | | | | | | tracking conversion Table 63 |
| Analog input voltage | V _A | V | 0.145 | | 1.455 | |
| ADC Clock Frequency | f _{ADC_CLK} | MHz | 75 | 80 | 85 | f _{ADC_CLK} = f _{SYS_CLK} See 2.2 78 MHz not allowed |
| Signal to noise ratio | SNR | dB | 55 | 64 | | @ -6dB FS |
| Spurious free dynamic range | SFDR | dB | 58 | 69 | | @ -6dB FS @ 600kHz |
| Inter modulation product | IM3 | dB | 62 | 69 | | @ -12dB FS each input tone @ 600kHz max f @ 50KHz Δf |
| Bandwidth input buffer | BW | kHz | 600 | | | 1 st order Filter in input Buffer |
| Conversion time – excluding sample time | Nconv | Counts of clk | | 24 | | Including one tracking conversion, sampling time not included |
| Sampling time | T _s | Counts of clk | 4 | 8 | | @ 80 MHz clk |
| Wake up time – bandgap and BG reference Buffer | T _{WUBGB} | us | 300 | 600 | 1000 | |
| Wake up time – ADC | T _{WUADC} | Counts of clk | | 660 | | without startup calibration |
| Startup calibration time ¹⁾ | T _{SUCAL} | Counts of clk | 3361 | 6049 | 16801 | ADC0:DSCAL= 0 _B Typical conditions: ADC0:STC=1 _B ADC0:MSB_CTRL= 1 _B |
| Setup time common mode input voltage | T _{VCM} | μs | | | 1 | |
| Power supply Rejection Ration on VDD5 | PSRR | dB | 20 | | | |

* Parameters guaranteed by design

$$1) T_{SUCAL} = (1792 * 2^{(ADC0:STC)} + 896 * ADC0:MSB_CTRL + 1569) * 1/f_{SYS_CLK}$$

$$2) Overall\ wake\ up\ time\ when\ calibration\ time\ is\ enabled = T_{WUADC} + T_{SUCAL}$$

MADC Domain Functional Specification

8.3 MADC Timing Diagrams

The interface is fully synchronized to the main clock. Figure 70 shows the 12 bits conversion timing in case of one tracking and no oversampling. Thus, the maximum speed of the ADC is set to 2.5 MSps at 80 MHz clock input. Figure 70 shows the SAR ADC timing.

Important: all configuration signals must be stable during a running conversion (between start_adc and one cycle before eoc).

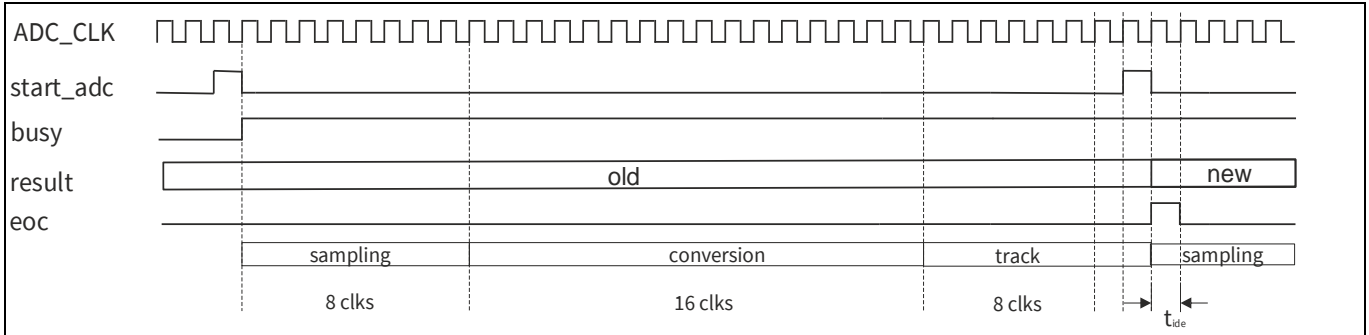


Figure 70 SAR ADC conversion timing diagram, 12 bits

8.4 MADC Startup Sequence

The following figure shows the startup sequence for the complete ADC.

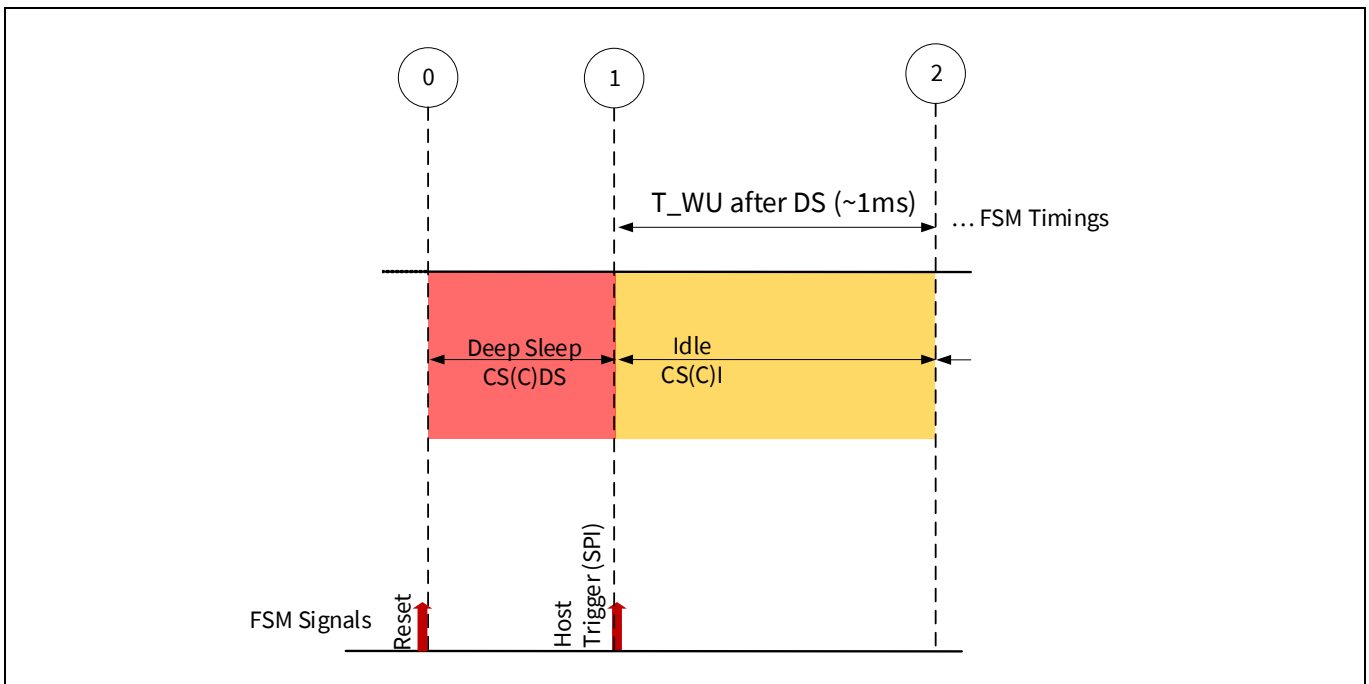


Figure 71 MADC start-up timing constraints

After a reset and trigger from the host, the FSM will move from the deep sleep mode into the idle mode. Here T_{WKUP} represents the overall time required by the bandgap to settle and it is the longest time required in the settling of the ADC.

The following Table 61 shows the start-up timing constraints:

MADC Domain Functional Specification

Table 61 MADC Timing Constraints, VDDA = 1.71 to 1.89 V, T_b = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|---|--------------------|------|-------|------|------|-----------|
| | | | Min | Typ | Max | |
| Parameter | | | | | | |
| Wake up time | T _{WUADC} | μs | | 8.25 | | @80 MHz |
| Setup time common mode input voltage | T _{VCM} | μs | | | 1 | |
| Wake-up time for bandgap and bandgap reference buffer | T _{WU} | μs | 300 | | 1000 | |

8.5 MADC Conversion Rate

The ADC clock input is $f_{\text{ADC_CLK}} = f_{\text{SYS_CLK}} = 80$ MHz and is derived from the system clock.

A conversion can include three different phases:

- Sampling
- Conversion
- Tracking

8.5.1 Sampling

During the first phase, the analog input voltage is sampled onto the input capacitor. The duration is controlled using the ADC0:STC bits. The following Table 62 shows the link between the register value ADC0:STC the clock periods STC_NUM and the sampling time.

Table 62 ADC0:STC Value Table (see section 4.3)

| | Sampling clock periods | Sampling time in ns ($f_{\text{ADC_CLK}} = 80$ MHz) |
|--------------------------|------------------------|--|
| ADC0:STC | STC_NUM | t _{sample} |
| 0 _D | 4 | 50 |
| 1 _D (default) | 8 | 100 |
| 2 _D | 16 | 200 |
| 3 _D | 32 | 400 |

The sampling time is calculated as: $N_{\text{sample}} = \text{STC_NUM}$

8.5.2 Conversion

The charge from the sampling capacitor is redistributed to 13 + 2 capacitors. To identify the LSB bits of the result, 13 clock cycles are needed.

To identify the MSB bit of the result, one or two clock cycles are used, depending on register setting ADC0:MSB_CTRL:

- In case of MSB_CTRL is set to 0_B, just a single (1) clock cycle is used
- In case of MSB_CTRL is set to 1_B, two (2) clock cycles are used

The redistribution time is calculated as:

$$N_{\text{conv}} = (13 + 2 + \text{ADC0:MSB_CTRL})$$

MADC Domain Functional Specification

8.5.3 Tracking

In this mode, the ADC performs a single sample conversion followed by several tracking conversions, depending on the setting of bits ADC0:TRACK_CFG:

Table 63 ADC0:TRACK_CFG Value Table

| ADC0:TRACK_CFG | Additional conversions TRACK_CFG_NUM | Remarks |
|----------------|---|---------|
| 0 _D | 0 | |
| 1 _D | 1 | Default |
| 2 _D | 3 | |
| 3 _D | 7 | |

The duration of one tracking conversion is:

$$N_{\text{track}} = 8$$

The duration of all tracking conversions for a single result is then:

$$N_{\text{track_all}} = 8 \times \text{TRACK_CFG_NUM}$$

8.5.4 ADC Conversion Rate

Based on what defined in 8.5.1, 8.5.2, and 8.5.3 the following cycles are defined for a single conversion:

$$N_{\text{ADC_CONV}} = N_{\text{samp}} + N_{\text{conv}} + N_{\text{track_all}}$$

with N_{samp} the number of sampling, N_{conv} conversion and N_{track} tracking cycles, respectively.

All ADCs are synchronized to $f_{\text{SYS_CLK}}$.

8.5.5 ADC Sampling Rate

The ADC sampling rate is controlled by the ADC0:ADC_DIV value (see Table 22). The sampling rate of the ADC is given then by $f_{\text{ADC_SAMP}} = f_{\text{ADC_CLK}} / \text{ADC_DIV}$. ADC0:ADC_DIV value needs to be greater than the number of clock cycles needed by a single ADC conversion as described in 8.5.4.

The sampling rate of the ADC is:

$$f_{\text{ADC_SAMP}} = f_{\text{ADC_CLK}} / \text{ADC_DIV}$$

$$\text{with } \text{ADC_DIV} > N_{\text{ADC_CONV}}$$

Table 64 ADC Sampling Rate, VDDA = 1.71 to 1.89 V, T_b = -20 to +70 °C

| Spec | Symbol | Unit | Value | | | Condition |
|-------------------------------------|------------------------|------|-------|------|-----|-----------|
| | | | Min | Typ | Max | |
| Parameter | | | | | | |
| ADC sampling rate | $f_{\text{ADC_SAMP}}$ | MHZ | | 2 | 4 | |
| Effective number of bits resolution | ENOB | 1 | | 10.5 | | |

SADC Domain Functional Specification

9 SADC Domain Functional Specification

The Sensor ADC (SADC) is a single channel single-ended 8 bits SAR ADC.

The sensor ADC can be used to monitor the temperature output as well as the power detector outputs from the transmitter channels. Conversion data can be read out through the SADC register (see also section 4.22). The data can be added also to the header of MADC data frame in the FIFO (see also section 5.1). By default, the SADC is set to read out the temperature sensor out (SADC_CTRL:SADC_CHSEL=0 in section 4.9). For additional settings, please check section 4.9. See also Figure 72. The SADC can achieve a better resolution of 10 bits by means of oversampling (see section 9.2).

Due to the required conversion time, ADC data are not available during a shape, but they would be available during next shape (there is a delay of one shape for these data).

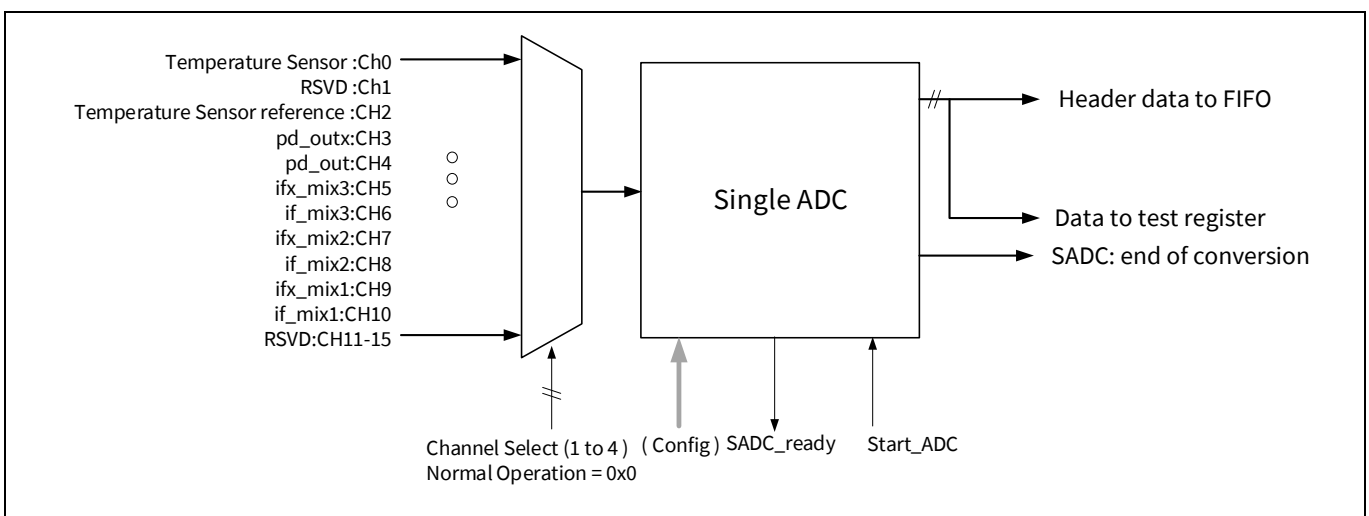


Figure 72 SADC Integration

9.1 SADC Functionality

Four main tasks are performed by the FSM to control the SADC:

- Enabling:
 - The SADC module is enabled through the CSCx register in any phase of the FSM state (see also 4.11)
- Initialization:
 - The host selects the channel in the channel register from SADC_CTRL control register (see also section 4.9)
- Triggering:
 - Each chirp-start during the active phase of shapes will trigger the SADC sampling/conversion
 - or by sending a SADC_START to SADC_CTRL register (see section 4.9)
- Results:
 - The conversion results are stored in the result register SADC_RESULTS register (see section 4.22) after the sampling and conversion is completed

SADC Domain Functional Specification

9.2 SADC Conversion Formula

The SADC clock signal is running at 20 MHz and is derived from $f_{ADC_CLK} = f_{SYS_CLK} = 80$ MHz. The SADC startup time is 101 clock cycles without startup-calibration and 422 clock cycles with startup-calibration. If temperature or power supply conditions did not change dramatically, the startup-calibration can be avoided during frames.

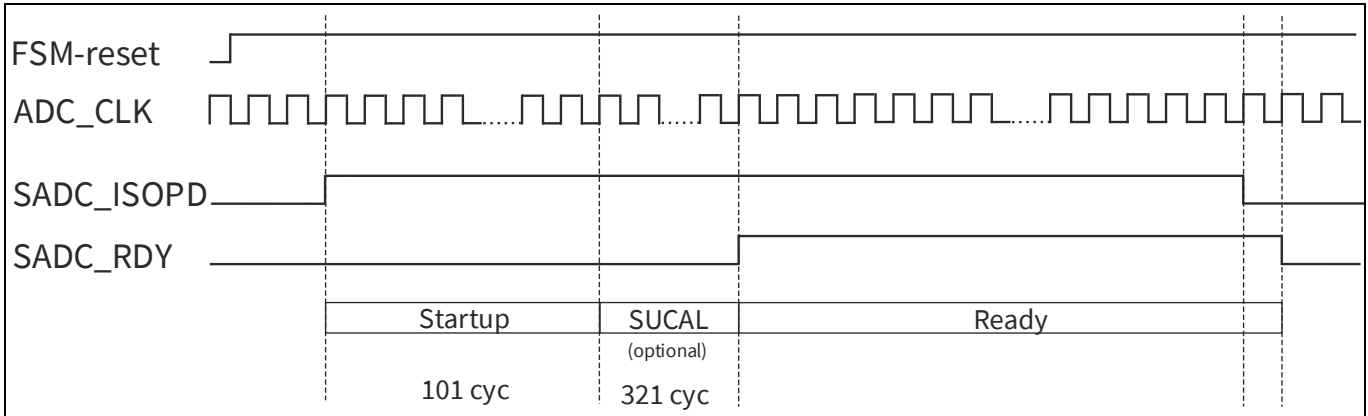


Figure 73 SADC startup timing

The conversion time N_{CONV_LEN} for a single analog to digital conversion into the result register SADC_RESULT (see section 4.22) is defined by the following relation:

$$N_{CONV_LEN} = (N_{conv} + N_{sample_dflt} + SESP \times N_{spread_early_sample}) \times OVS$$

Where:

$N_{conv} = 13$ clock cycles

$N_{sample_dflt} = 16$ clock cycles

$N_{spread_early_sample} = 16$ clock cycles

OVS ... see SADC_CTRL:OVERS_CFG (see section 4.9)

SESP ... see SADC_CTRL:SESP (see section 4.9).

The SADC conversion formula for 8 bits resolution is:

$$Dout_{8b} = ((2^8 \times V_{Ain}) / VREFP) \times G_{Ain} \text{ with an error of } \pm 0.1\%$$

Where:

V_{Ain} is the analog input to the SADC

G_{Ain} is the gain of the ADC module and can be set either to 1 or 0.75 (see section 4.9)

$VREFP = 1.21V$.

In order to achieve 10 bits resolution, the oversampling should be set to 32 (see section 4.9).

In order to measure correctly the power sensor output, see sections 7.1.2 and 4.9.

Note: Disabling the SADC

To disable the SADC simply set in register CSCx (see section 4.11) SADC_ISOPD= '0b' (f_{SYS_CLK} has to be still provided for at least one additional cycle for the command to take effect).

Enhanced Functions

10 Enhanced Functions

10.1 Data Test Mode

A linear feedback shift register (LFSR) is built-in on chip. It will generate a pseudo random bit M-sequence that can be used to fill up the FIFO. This can be used to develop and test the complete pipeline from the FIFO on the BGT60TR13C up to the Application Processor (AP) memory, including firmware and drivers, with a defined bit sequence.

The implemented LFSR is described by the following polynomial: $x^{12}+x^{11}+x^{10}+x^4+1$.

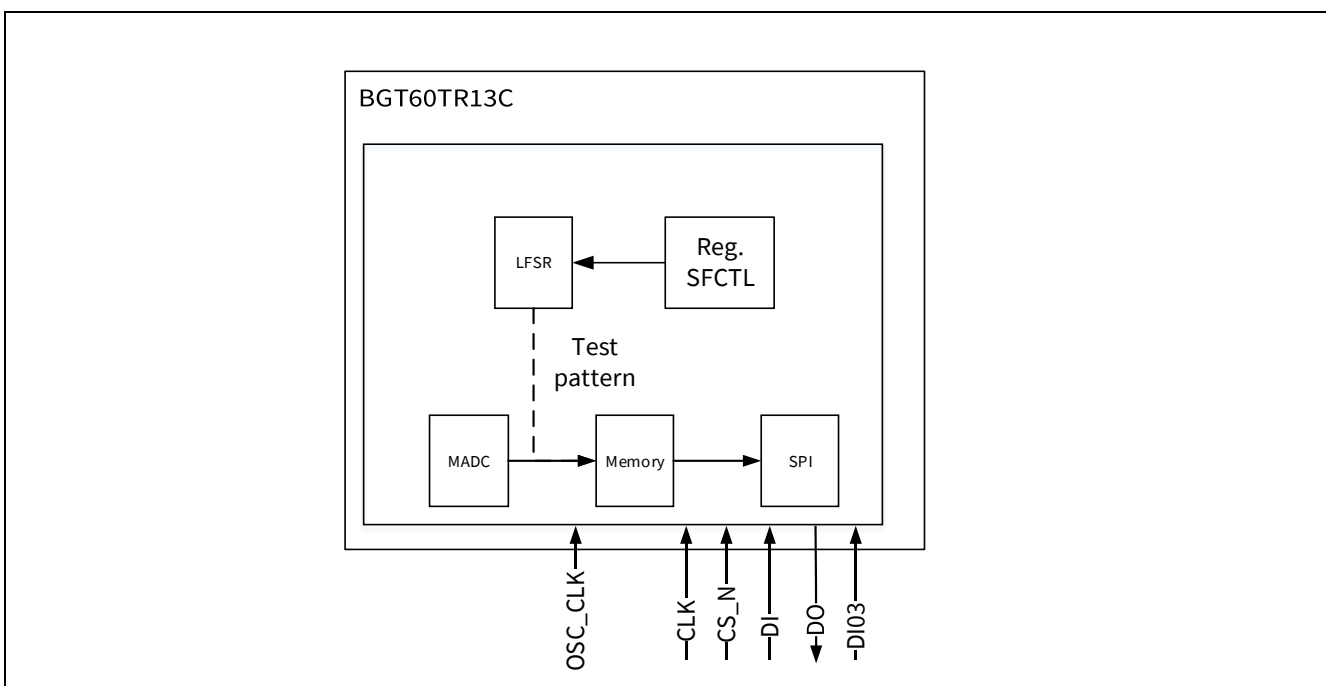


Figure 74 Digital pipeline simplified block diagram

The first ADC channel ADC_CH1 output data stream is bypassed by the data sequence coming from the LFSR generator.

The other channels can be disabled or used in normal operation.

- This test mode can be started with bit SFCTL:LFSR_EN= 1_B (see also 4.8):
- Activate test data instead of ADC data
- Initialization with MAIN:FSM_RESET= 1_B

10.2 CW Mode

In the continuous wave (CW) mode the device will be set to provide a constant output frequency. During CW mode no shapes are executed.

During the execution of this mode:

- Freq/timing parameters defined in shape registers are ignored
- PLL / RF / ADC runs with values programmed in PLL DFT0 (4.18) and CSU1 (0).
- All other CSx / shape settings are not handed over to functional blocks

Enhanced Functions

- The values for REPS/REPC/REPT and frame relevant timings are used to shape a “virtual frame”
- Data from the FIFO can be read out following the structure of that “virtual frame”

Note:

For test purposes the “virtual frame” definition should be kept simple: 1 shape, 1 CS, e.g.

10.2.1 Enabling the CW mode

The CW mode should be preceded by either an HW or SW reset.

After this in order to enable the CW mode, the steps below should be followed:

- Enable the MAIN: CW_MODE = 1_B (see 4.2)
- Initialize the chip registers according to defined “virtual frame” (settings in 4.10 and 4.16)
- Enable the clock: PACR1: OSCCLKEN (see 4.6)
- Set frequency via PLLx: FSU setting from shape 1
- Set channel set for CSD/CSI/CSU1 (see 4.11)
- set PLL DFT0: BYPRMPEN = 1_B (see 4.18)

By using the FRAME_START as trigger, the chip can be set in the different states of a shape as shown in Figure 75:

- TRIG#1: jump to 1 (DS -> IDLE)
- TRIG#2: jump to 2 (IDLE -> INIT0)
- TRIG#3: jump to 3 (INIT0 -> INIT1)
- TRIG#4: jump to 4
- TRIG#5: jump to 6

Frequency update: at this stage the output frequency can be updated/programed (FSU) to any value and the current frequency will be updated immediately after PLL transition of DFT0: BYPRMPEN = 0_B -> 1_B.

- TRIG#6: jump to 7

At this stage, the APU number of samples is generated by the ADC according to the ADC0 settings. In case if APU=0 no triggers are generated, manual triggering of MADC can be done via ADC0: TRIG_MADC. Once the APU number of samples is generated another automatic generation of samples can be done after FSM reset.

-
- TRIG7: jump to 8
- TRIG8: jump to 10
- TRIG9: jump to 11
- TRIGx

Enhanced Functions

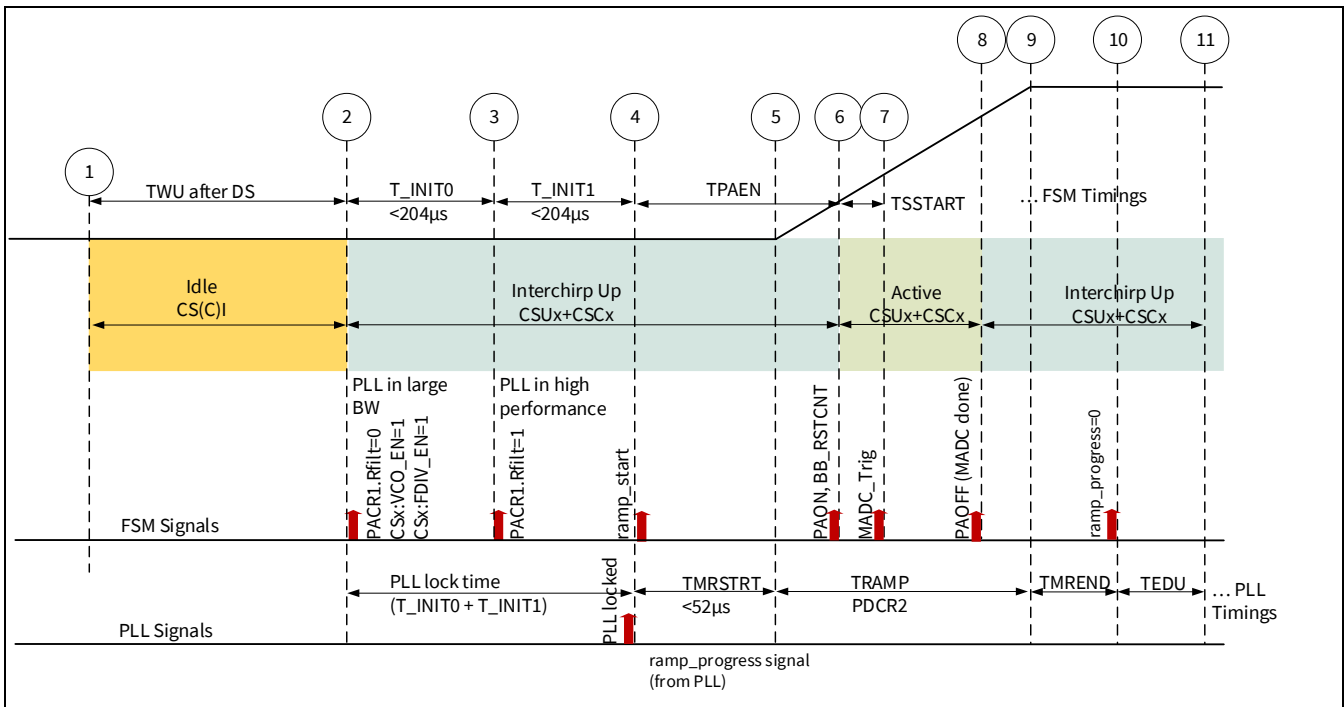


Figure 75 Steps that can be followed during a “virtual frame”

The FSM-reset will set back the FSM to initial state to start again with TRIG1.

This specific mode is intended also to test the power consumption of the chip during a specific sequence. It will offer the opportunity to break the expected shape that should be run during the radar (active) mode in static steps where the current consumption can be measured.

10.2.2 Baseband and ADC Test Mode

A test-tone generator can be used together with the CW mode. A test signal source derived from the OSC_CLK input at 80 MHz can be activated in the analog receiver chain; the same in each Rx chain. This test signal can be programmed in the register RFT0 (see section 4.19). The test tone can propagate through to each baseband chain by enabling a dedicated path. The MADC is triggered by the TRIG7 in Figure 75 and will sample the number of samples specified in the APU1 (see section 4.16). To run a new measurement an FSM-Reset is required.

Enhanced Functions

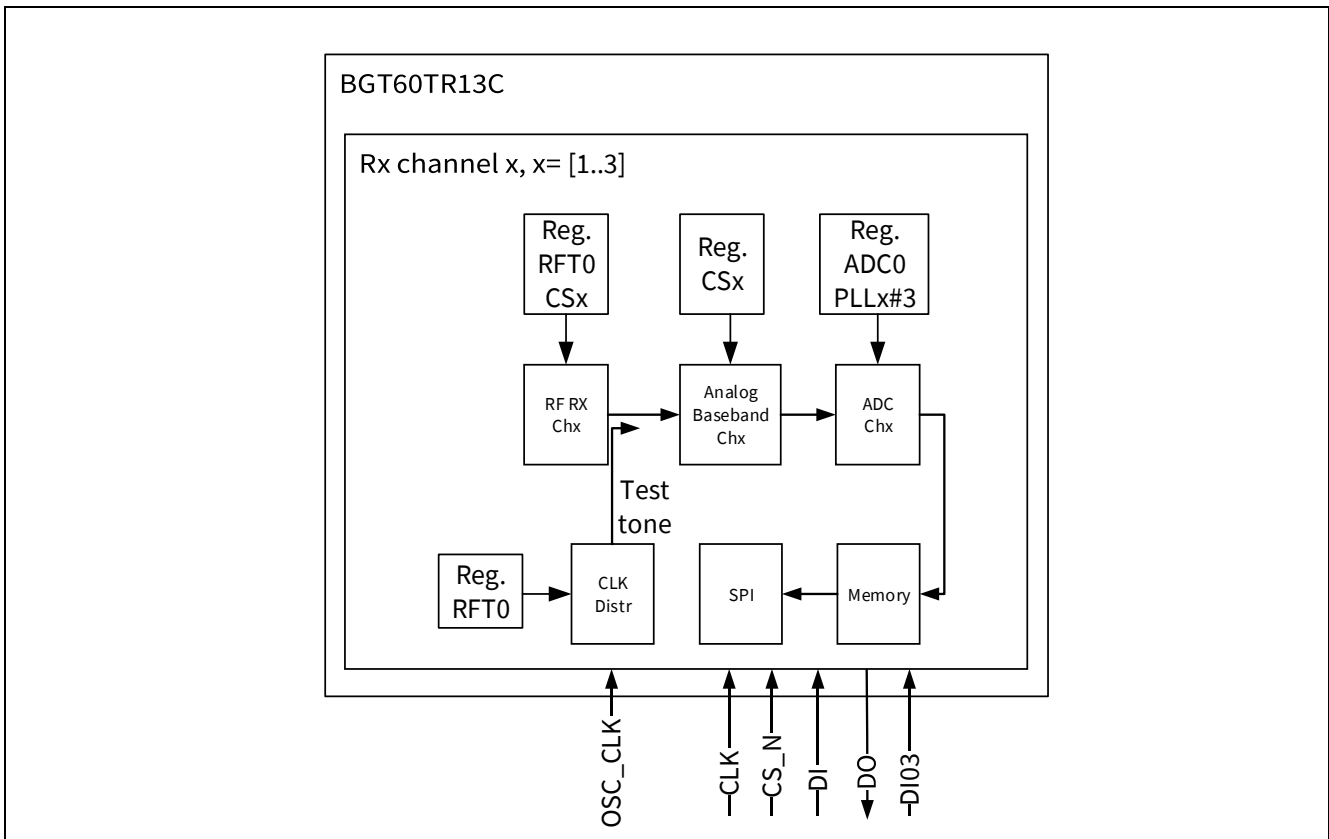


Figure 76 Baseband/ADC test block diagram

This feature represents a very convenient way to test and debug a complete system. The customer can program a dedicated frequency, set the baseband gain and cutoff filter of the HPF (0), set the ADC (see 4.3), and readout via SPI the sampled data into the application processor or microcontroller unit to verify if the complete baseband chain is working as expected.

In Figure 77 is reported one example of ADC readout when the baseband is fed with a test tone at 400kHz internally derived from the OSC_CLK input. Different readouts from different VGA settings are reported.

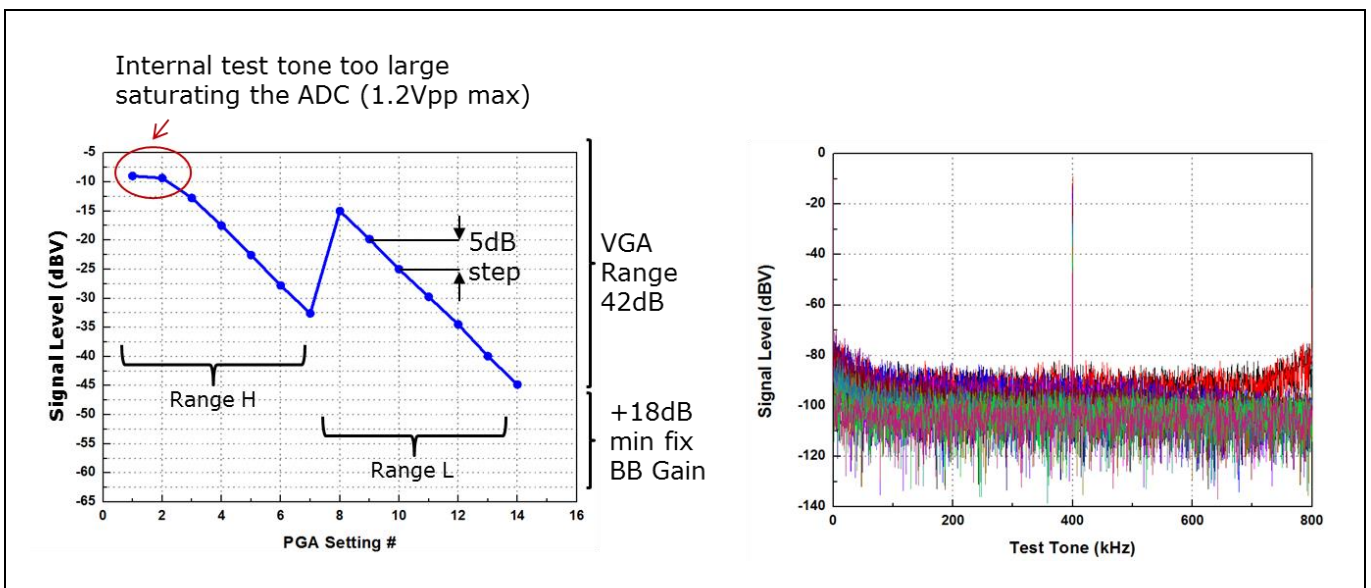


Figure 77 Example: ADC readout after FFT

Enhanced Functions

10.3 IRQ Output

BGT60TR13C provides one interrupt pin output (IRQ). In default mode, the IRQ signal is used to monitor the filling level of the FIFO as described below.

IRQ status definition:

- IRQ is high after:
 - CS_N goes high and FSTAT:FILL_STATUS >= SFCTL:FIFO_CREF (see also 4.8 and 4.23).
- IRQ is low (as a consequence of):
 - CS_N goes high and FSTAT:FILL_STATUS < SFCTL:FIFO_CREF (see also 4.8 and 4.23).
 - or CS_N is active low

The following figure shows the IRQ signal in case of FIFO-burst reads.

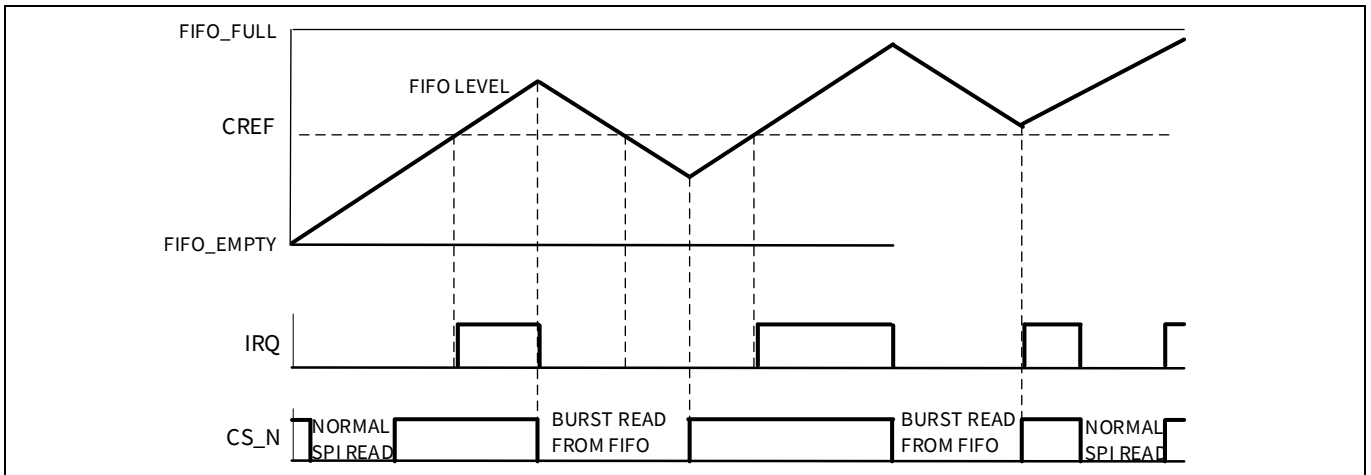


Figure 78 IRQ status behavior during radar mode with FSM capturing data

Example of Typical Configurations

11 Example of Typical Configurations

11.1 Case #1

A specific use case targeting two alternating operation modes, for long range and short range, is presented. In short range mode, the sensor is expected to achieve a large resolution and transmit low power while in long range a large transmitted power associated to a lower resolution is expected. The parameters are selected also to avoid overflow as well as underflow error in the FIFO. In Figure 79 is reported an overview of the proposed case #1.

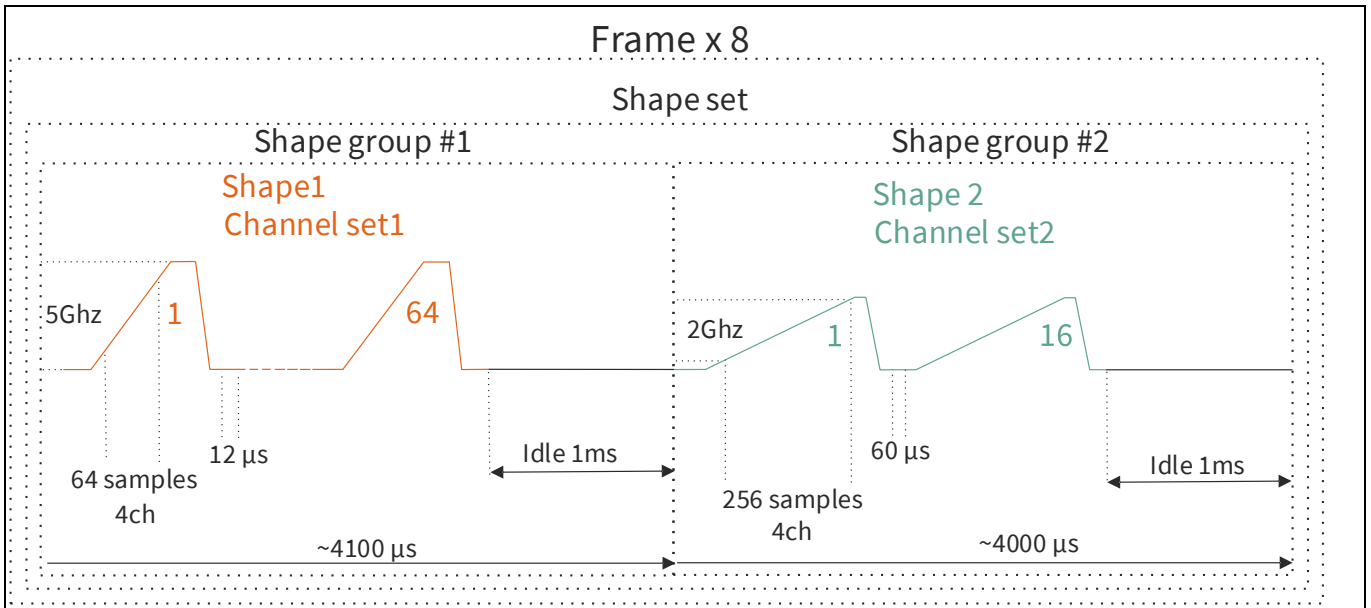


Figure 79 Case #1 definition

General Settings:

- T_WU = 1000 µs (see section 4.2)
- T_INIT0 = 70 µs (see section 4.15)
- T_INIT1 = 15 µs (see section 4.12)

ADC Settings in ADC0 register:

- ADC_DIV = 40_D → f_{ADC_SAMP} = 2 MSps
- TRIG_MADC = 0_B
- MSB_CTRL = 1_B
- TRACK_CFG = 1_D
- DSCAL = 0_B
- STC = 1_B
- BG_CHOP_EN = 0_B
- BG_TC_TRIM = 0_D
- ADC_OVERS_CFG = 00

Frame Definition (see section 3):

Example of Typical Configurations

| | | |
|-------------------------|------------------------------------|------------------|
| Frames to be run | = 8 | |
| Shape set | = 1 (shape set=frame in this case) | → RT=1 → REPT=0 |
| N_SHAPE_EN | = 2 | |
| FRAME_LEN | = 2*1 | |
| Shape group | = 2 | |
| Shape1 | = enabled and repeated 64 times | → RS=64 → REPS=6 |
| Shape2 | = enabled and repeated 16 times | → RS=16 → REPS=4 |
| Channel set 1 | = enabled | → RC=64 → REPC=6 |
| Channel set 2 | = enabled | → RC=16 → REPC=4 |
| T_SED | = 1000 μs (see section 4.17) | |
| T_EDU | = 0 μs (see section 4.16) | |
| T_EDD shape1 | = 12 μs (see section 4.16) | |
| T_EDD shape2 | = 60 μs (see section 4.16) | |

Frequency Parameter Definition:

Shape 1

| | |
|--|---|
| Saw-tooth shape | → PACR2: FSTDNEN set to 1 to 3 _D (see section 4.7) |
| | → PLL4:FSD set 0 _B |
| | → PLL5:RSD set 0 _B |
| | → PLL6:RTD set 0 _B |
| Start first frequency, FSU | → 58 GHz → mapped in 24 bits: 101010100000000000000000 _b |
| Expected Bandwidth | → 5 GHz |
| Nr. of samples, APU | → 64 |
| ADC sample rate, f_{ADC_SAMP} | → 2 MSps |
| Then: | |
| Acquisition time, T_{ACQUx} | → (APU)/ f _{ADC_SAMP} = 31.5 μs |
| Ramp time, T_{RAMP} | → T_PAEN + T_SSTART + T_ACQUx + T_ECM – T_START= 37.5 μs |
| with: | |
| T_SSTART | → 1 μs |
| T_PAEN | → 10 μs |
| T_ECM | → 3 μs |
| T_START | → 8 μs |

Then:

Example of Typical Configurations

| | |
|-----------------------------|---|
| Number of steps, RTU | → 37.5 μ s/100 ns= 375 |
| Step size, RSU | → ~1.667 MHz → mapped in 24 bits: 101010101010 _b |
| Calculated Bandwidth | → RTU*8*RSU= 4.998779297 GHz |

Shape 2

| | |
|--|--|
| Saw-tooth shape | → PACR2: FSTDNEN: 1 to 3 _D (see section 4.7) → PLL4:FSD set 0 _B → PLL5:RSD set 0 _B → PLL6:RTD set 0 _B |
| Start first frequency, FSU | → 60 GHz → mapped in 24 bits: 110111000000000000000000 _b |
| Expected Bandwidth | → 2 GHz |
| Nr. of samples, APU | → 256 |
| ADC sample rate, f_{ADC_SAMP} | → 2 MSps |
| Then: | |
| Acquisition time, T_{ACQUx} | → (APU)/ f_{ADC_SAMP} = 127.5 μ s |
| Ramp time, T_{RAMP} | → T_PAEN + T_SSTART + T_ACQUx + T_ECM – T_START= 133.5 μ s |
| with: | |
| T_{SSTART} | → 1 μ s |
| T_PAEN | → 10 μ s |
| T_ECM | → 3 μ s |
| T_START | → 8 μ s |
| Then: | |
| Number of steps, RTU | → 133.5 μ s/100 ns= 1335 |
| Step size, RSU | → ~0.187 MHz → mapped in 24 bits: 100110010 _b |
| Calculated Bandwidth | → RTU*8*RSU= 1.994677734 GHz |

Example of Typical Configurations

Channel Set Parameter Definition:

Channel Set 1

Table 65 CSU1_0 Register Settings

| Symbol | Bits | SET | Comment |
|--------------|------|----------------|---------|
| TEMP_MEAS_EN | 21 | 1 _B | |
| BBCHGLOB_EN | 20 | 1 _B | |
| RX3MIX_EN | 17 | 1 _B | |
| RX3LOBUF_EN | 16 | 1 _B | |
| RX2MIX_EN | 15 | 1 _B | |
| RX2LOBUF_EN | 14 | 1 _B | |
| RX1MIX_EN | 13 | 1 _B | |
| RX1LOBUF_EN | 12 | 1 _B | |
| LO_DIST1_EN | 11 | 1 _B | |
| LO_DIST2_EN | 10 | 1 _B | |
| FDIV_EN | 6 | 1 _B | |
| TEST_DIV_EN | 5 | 0 _B | |
| VCO_EN | 4 | 1 _B | |
| PD1_EN | 1 | 1 _B | |
| TX1_EN | 0 | 1 _B | |

Table 66 CSU1_1 Register Settings

| Symbol | Bits | SET | Comment |
|--------------|-------|---------------------|--------------------|
| BBCH_SEL | 23:20 | 0111 _B | 3ch ADC mode |
| BB_RSTCNT | 19:13 | 101000 _D | |
| TEMP_MEAS_EN | 12 | 0 _B | It will be removed |
| MADC_EN | 10 | 1 _B | |
| TX_DAC | 4:0 | 00111 _B | Low Tx power |

Table 67 CSU1_2 Register Settings

| Symbol | Bits | SET | Low gain settings |
|-----------|-------|-------------------|-------------------|
| HP_GAIN | 23:20 | 0111 _B | |
| VGA_GAIN3 | 14:12 | 0 _B | |
| HPF_SEL3 | 11:10 | 11 _B | |
| VGA_GAIN2 | 9:7 | 0 _B | |
| HPF_SEL2 | 6:5 | 11 _B | |
| VGA_GAIN1 | 4:2 | 0 _B | |
| HPF_SEL1 | 1:0 | 11 _B | |

Example of Typical Configurations

Channel set2

Table 68 CSU2_0 Register Settings

| Symbol | Bits | SET | Comment |
|--------------|------|----------------|---------|
| TEMP_MEAS_EN | 21 | 1 _B | |
| BBCHGLOB_EN | 20 | 1 _B | |
| RX3MIX_EN | 17 | 1 _B | |
| RX3LOBUF_EN | 16 | 1 _B | |
| RX2MIX_EN | 15 | 1 _B | |
| RX2LOBUF_EN | 14 | 1 _B | |
| RX1MIX_EN | 13 | 1 _B | |
| RX1LOBUF_EN | 12 | 1 _B | |
| LO_DIST1_EN | 11 | 1 _B | |
| LO_DIST2_EN | 10 | 1 _B | |
| FDIV_EN | 6 | 1 _B | |
| TEST_DIV_EN | 5 | 0 _B | |
| VCO_EN | 4 | 1 _B | |
| PD_EN | 1 | 1 _B | |
| TX_EN | 0 | 1 _B | |

Table 69 CSU2_1 Register Settings

| Symbol | #Bits | SET | Comment |
|--------------|-------|---------------------|--------------------|
| BBCH_SEL | 23:20 | 1111 _B | 4ch ADC mode |
| BB_RSTCNT | 19:13 | 101000 _D | |
| TEMP_MEAS_EN | 11 | 1 _B | It will be removed |
| MADC_EN | 10 | 1 _B | |
| TX_DAC | 4:0 | 11111 _B | Highest Tx power |

Table 70 CSU2_2 Register Settings

| Symbol | Bits | SET | Comment |
|-----------|-------|-------------------|---|
| HP_GAIN | 23:20 | 0111 _B | Highest gain settings for longest range detection |
| VGA_GAIN3 | 14:12 | 111 _B | |
| HPF_SEL3 | 11:10 | 11 _B | |
| VGA_GAIN2 | 9:7 | 111 _B | |
| HPF_SEL2 | 6:5 | 11 _B | |
| VGA_GAIN1 | 4:2 | 111 _B | |
| HPF_SEL1 | 1:0 | 11 _B | |

Example of Typical Configurations

CSCx Register Settings:

Table 71 CSCx Register Settings

| CSCx Register | RST | CSC1 | CSC2 | CSC3 | CSC4 | CSCI | CSCDS |
|---------------|-----|------|------|------|------|------|-------|
| PLL_ISOPD | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| BG_TMRF_EN | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| SADC_ISOPD | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| MADC_ISOPD | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| BG_EN | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| RF_ISOPD | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| ABB_ISOPD | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| CS_EN | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| REPC | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Package

12 Package

The BGT60TR13C chipset is housed in a laminate package with solder balls of 300 µm diameter and a standoff of 240 µm. According to IPC/JEDEC’s J-STD0, the moisture sensitivity level (MSL) is 3. Figure 80 shows the top view of BGT60TR13C package and its physical dimension. The bottom view is presented in Figure 81. The package size is 6.5 x 5 x 0.9 mm³ with ball pitch of 500 µm. Package outline is reported on Figure 82. Package name: PG-VF2BGA40-1.

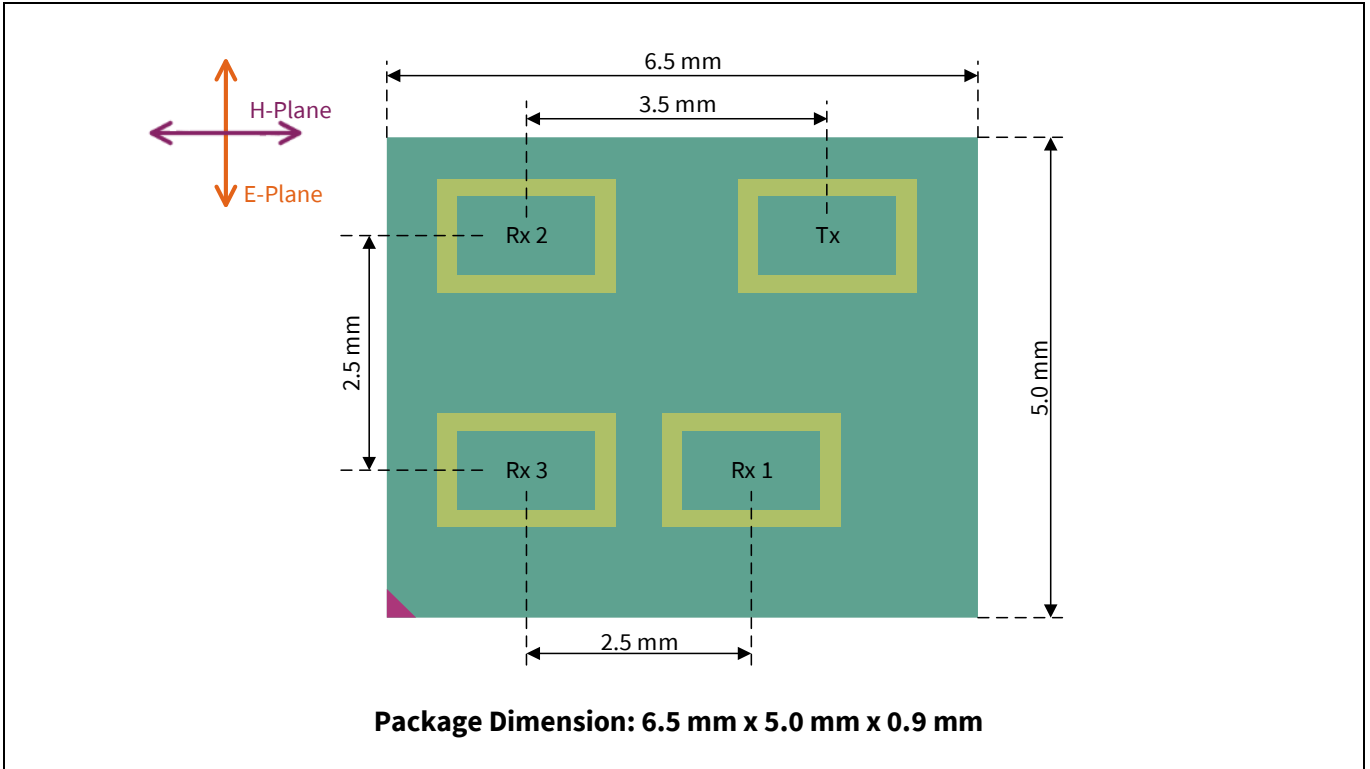


Figure 80 Top view of BGT60TR13C

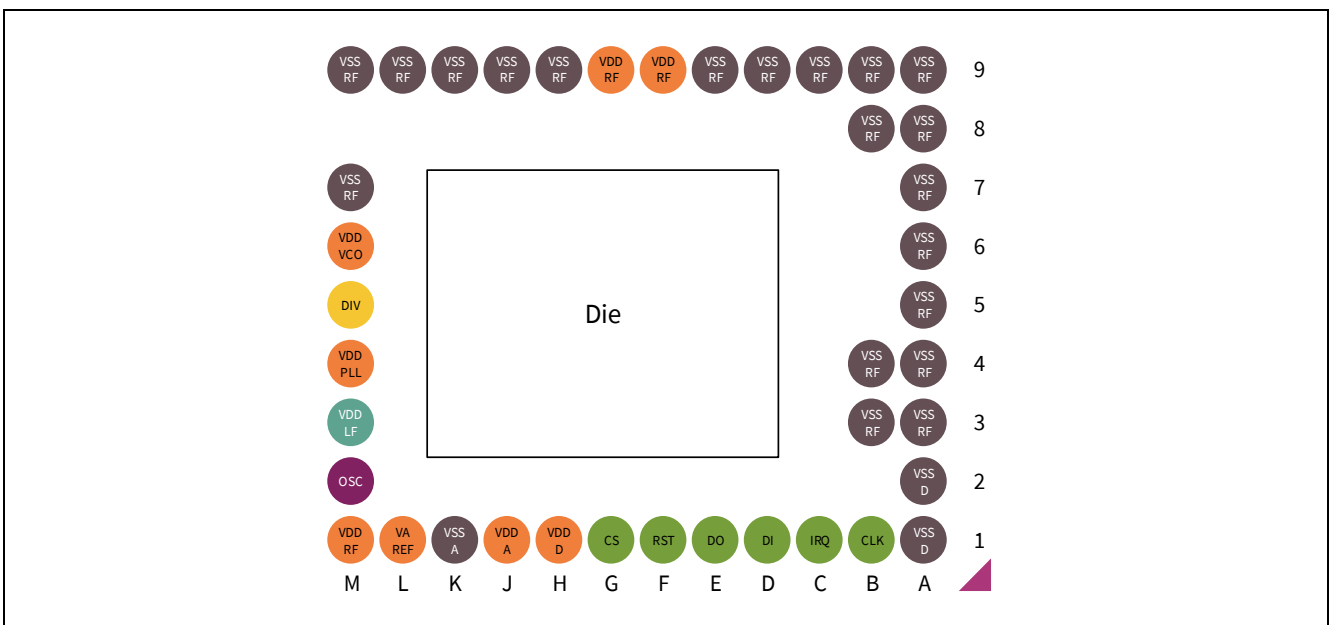


Figure 81 Bottom view of BGT60TR13C

Package

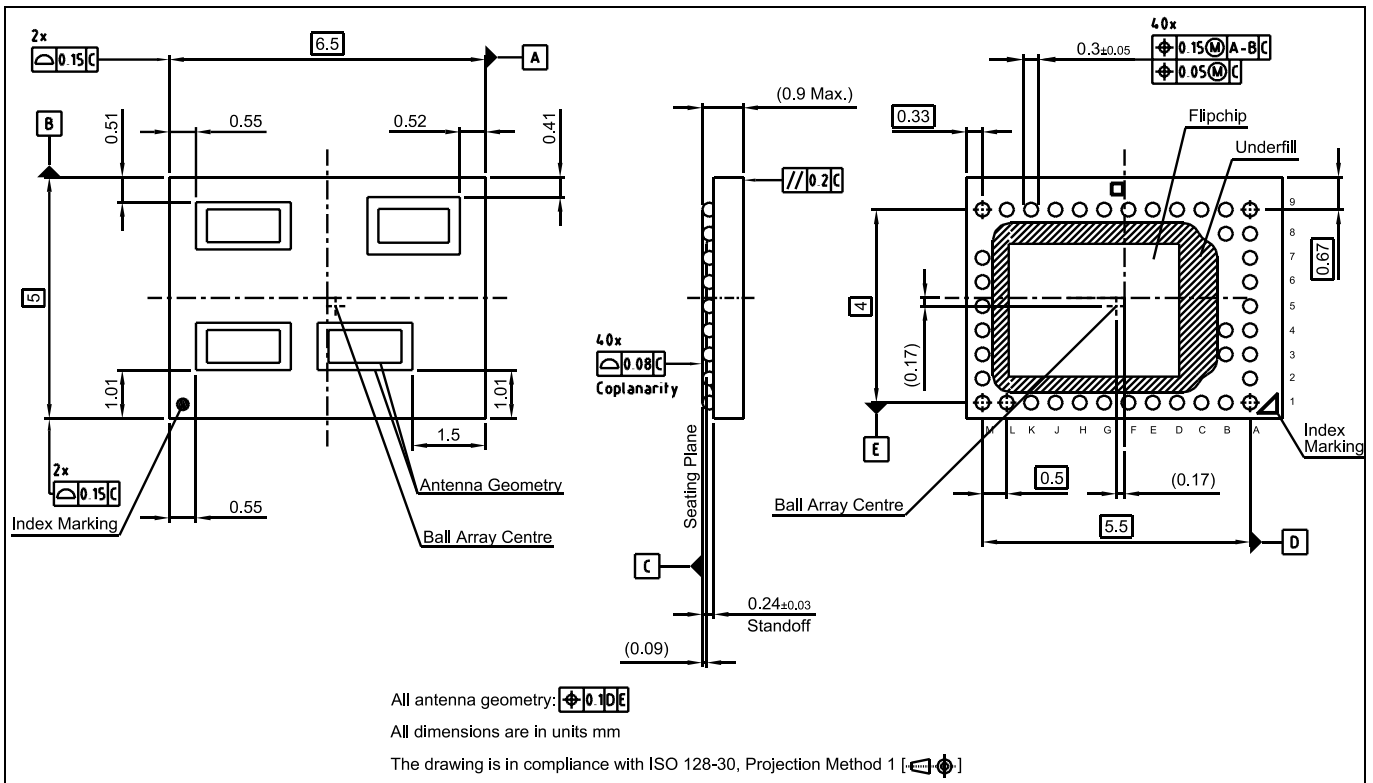


Figure 82 Package outline PG-VF2BGA-40-1

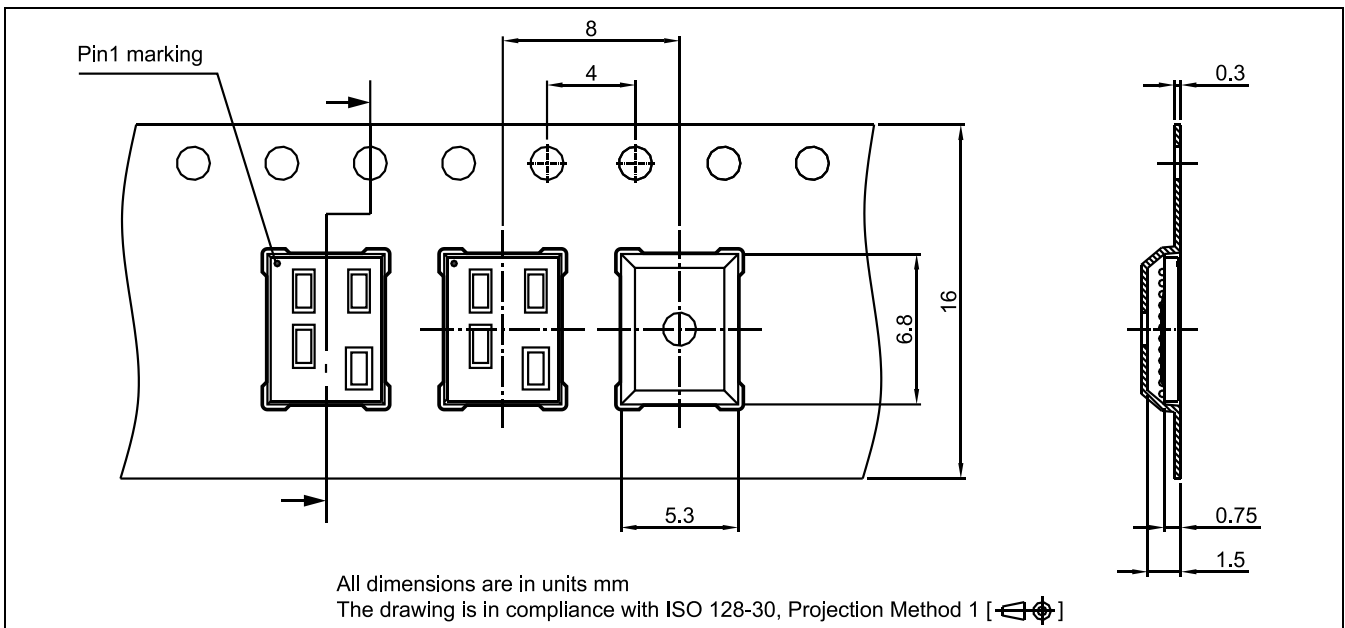


Figure 83 Tape of PG-VF2BGA-40-1

Package

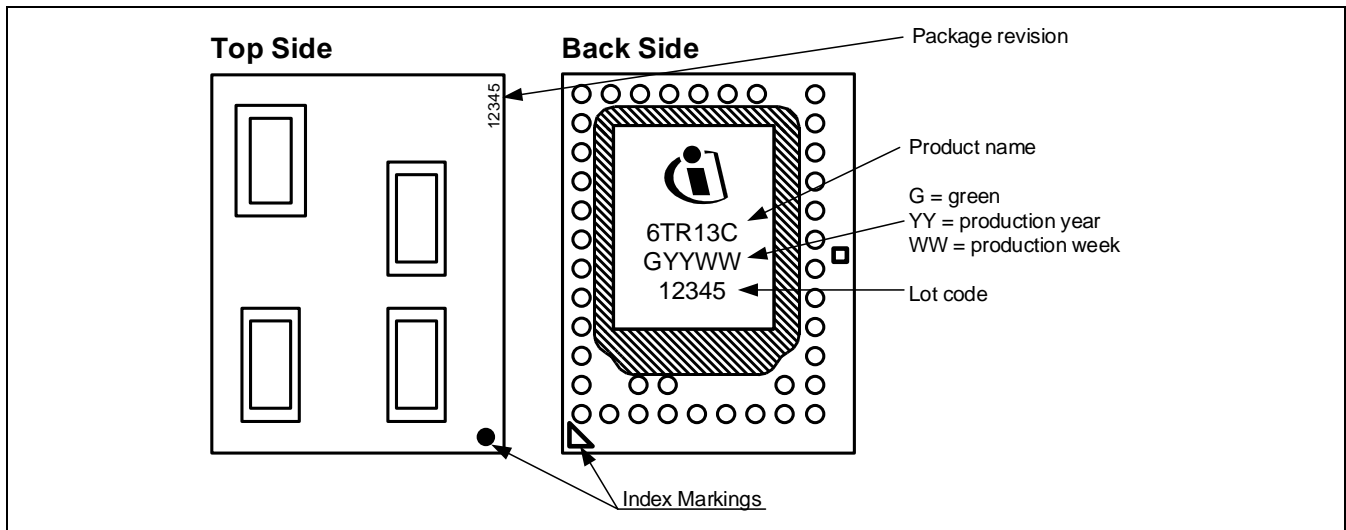


Figure 84 Marking layout of PG-VF2BGA-40-1 (example)

12.1 Built-in Antenna Specifications

Antenna performance reported in Table 72 are guaranteed by design. Typical antenna behavior is measured on Infineon reference board. Typical antenna beam plots are available in a specific application note and upon specific request.

Table 72 Antennas In Package Specifications

| Spec | Unit | Value | | | Condition |
|--------------|------|-------|-----|------|--|
| | | Min | Typ | Max | |
| Parameter | | | | | |
| RX_BW, TX_BW | GHz | 58.0 | | 63.5 | Antenna bandwidth |
| GTX | dBi | 2.0 | 3.5 | 5.0 | Antenna gain of a single TX antenna |
| GRX | dBi | 2.0 | 3.5 | 5.0 | Antenna gain of a single RX antenna |
| HPBW_RX_E | Deg | 50 | 65 | 80 | Half-power beam width of a single RX antenna in the E-plane direction |
| HPBW_RX_H | Deg | 20 | 35 | 50 | Half-power beam width of a single RX antenna in the H-plane direction. |
| HPBW_TX_E | Deg | 50 | 65 | 80 | Half-power beam width of a single TX antenna in the E-plane direction |
| HPBW_TX_H | Deg | 25 | 40 | 55 | Half-power beam width of a single TX antenna in the H-plane direction |
| D_RX_RX | mm | | 2.5 | | Center-to-center distance between RX antennas in X and Y direction |

Abbreviations

13 Abbreviations

Table 73 Abbreviations

| Symbol | Description |
|---------------|--------------------------------------|
| AAF | Anti-aliasing filter |
| ADC | Analog to digital converter |
| AP | Application Processor |
| DAC | Digital to analog converter |
| ESD | Electrostatic discharge |
| FMCW | Frequency modulated continuous wave |
| HBM | Human body model (related to ESD) |
| CDM | Charge device model (related to ESD) |
| HPF | High pass filter |
| IC | Integrated circuit |
| LPF | Low pass filter |
| MCU | Microcontroller Unit |
| PLL | Phase locked loop integrated circuit |
| RF | Radio Frequency |
| RSVD | Reserved |
| RX | Receiver |
| SPI | Serial peripheral interface |
| TX | Transmitter |
| LDO | Low dropout voltage regulator |
| RST | Reset or Default setting |
| MSB | Most significant bit |
| LSB | Least significant bit |

Revision History

14 Revision History

| Document version | Date of release | Description of changes |
|------------------|-----------------|--|
| 2.4.2 | 2020-02-21 | Updated description for FRAME_CNT in Table 24 and Table 45. Updated Figure 49 and Figure 50. Remove typo in Chapters 5.3 and 8. Changed text in Chapters 4.6 and 4.7. Changed Table 60. |
| 2.4.3 | 2020-03-25 | Added line for DFT0 in Table 20. Typo in package name in Chapter 12. Added Figure 83 and Figure 84 in Chapter 12. Removed remaining QSPI statements in chapters 4.8 and 5.8. |
| 2.4.4 | 2020-05-04 | Updated Min values for Table 6. |
| 2.4.5 | 2020-06-23 | Updated description for: <ul style="list-style-type: none"> - TR_WKUP and TR_WKUP_MUL in Table 21 - TR_INIT1 and TR_INIT1_MUL in Table 33 - TR_END in Table 33 - TR_FED and TR_FED_MUL in Table 34 - TR_START in Table 34 - TR_INIT0 and TR_INIT0_MUL in Table 36 - TR_SSTART in Table 36 - FSU and FSD in Table 37 - TR_EDD in Table 37 - TR_SED and TR_SED_MUL in Table 38 |
| 2.4.6 | 2021-01-08 | Update paragraph 4.2 and 5.3. Added paragraphs 5.4 and 5.5. Updated Table 26, 27, 30, 32, 40, 41 and corresponding Figures. |
| 2.4.7 | 2023-01-08 | Updated T_INIT0 and T_INIT1 in Table 15. Updated Note 3 of CCR3 register. Updated T _{WUADC} in Table 61. Updated input capacitance. Added Typ. and removed Min. values Table 48. |
| 2.4.8 | 2023-06-06 | Updated “CW Mode” trigger5 and trigger6. |
| 2.4.9 | 2023-11-21 | Removed output slewrates from input pad timing Table 48. Fixed several typos. |

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