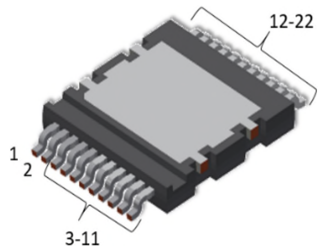
Final datasheet

CoolSiC™ Automotive MOSFET 1200 V in HDSOP-22-3 package

Features



- V_{DSS} = 1200 V at T_{vj} = -55...175°C
- I_{DDC} = 34 A at T_C = 25°C
- $R_{DS(on)}$ = 80 mΩ at V_{GS} = 20 V, T_{vj} = 25°C
- New performance-optimized chip technology (Gen1p) with improved R_{DSon}* A
- Best in class switching energy for lower switching losses and reduced cooling efforts
- Lowest device capacitances for higher switching speeds and higher power density
- A combination of low C_{rss}/C_{iss} ratio and high $V_{GS(th)}$ to avoid parasitic turn-on and enable unipolar gate driving
- Reduced total gate charge Q_G for lower driving power and losses
- Increased recommended turn-on voltage ($V_{GS(on)}$ = 20 V) for lower $R_{DS(on)}$
- .XT die attach technology for best in class thermal performance
- Low package stray inductance for faster and cleaner switching
- Drive (Kelvin) Source pin for better gate control and reduced switching losses
- Creepage distance > 4.75 mm fitting $V_{rms(max)}$ > 950 V based on IEC60664 for material group I, pollution degree 2
- SMT package for automated assembly and reduced system costs
- Low R_{th} Top-Side Cooled package for best thermal performance and power density

Halogen-free
AEC Qualified
Lead-free
RoHS

Potential applications

- On-board charger
- DC/DC converter
- Auxiliary drives

Product validation

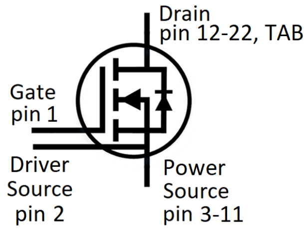
- Qualified for Automotive Applications. Product Validation according to AEC-Q100/101

Description

Pin definition:

- Pin 1 - Gate
- Pin 2 - Drive Source
- Pin 3...11 - Power Source
- Pin 12...22, TAB - Drain

Note: the drive source and power source pins are not exchangeable, their exchange might lead to malfunction



Type	Package	Marking
AIMCQ120R080M1T	PG-HDSOP-22-3	12A080M1

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1 Package

Table 1 Characteristic values

Parameter	Symbol	Note or test condition	Values			Unit
			Min.	Typ.	Max.	
Storage temperature	T_{stg}		-55		150	°C
Soldering temperature	T_{sold}				260	°C
MOSFET/body diode thermal resistance, junction-case[1)]	$R_{th(j-c)}$			0.54	0.71	K/W

1) not subject to production test - verified by design/characterization

2 MOSFET

Table 2 Maximum rated values

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage[1)]	V_{DSS}	T_{vj} = -55...175 °C		1200	V
Continuous DC drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$ [2)]	I_{DDC}	V_{GS} = 20 V	T_c = 25 °C	34	A
			T_c = 100 °C	24	
Peak drain current, t_p limited by $T_{vj(max)}$ [2)]	I_{DM}	V_{GS} = 20 V		86	A
Gate-source voltage, max. transient voltage[3)]	V_{GS}	$t_p \leq 0.5$ µs, $D < 0.01$		-10/25	V
Gate-source voltage, max. static voltage[3)]	V_{GS}			-5/23	V
Avalanche energy, single pulse	E_{AS}	I_D = 7.6 A, V_{DD} = 50 V, L = 4.76 mH		136	mJ
Power dissipation, limited by $T_{vj(max)}$ [2)]	P_{tot}		T_c = 25 °C	211	W
			T_c = 100 °C	106	

1) tested at Tvj=25°C, verified by design/characterization over full temperature range
2) not subject to production test - verified by design/characterization
3) **Important note:** The selection of positive and negative gate-source voltages impacts the long-term behavior of the device. The design guidelines described in Application Note AN2018-09 must be considered to ensure sound operation of the device over the planned lifetime.

Table 3 Recommended values

Parameter	Symbol	Note or test condition	Values	Unit
Recommended turn-on gate voltage	$V_{GS(on)}$		20	V
Recommended turn-off gate voltage	$V_{GS(off)}$		0	V

Table 4 **Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source on-state resistance	$R_{DS(on)}$	$I_D = 10$ A	$T_{vj} = 25$ °C, $V_{GS(on)} = 20$ V		80	100	mΩ
			$T_{vj} = 100$ °C, $V_{GS(on)} = 20$ V		112		
			$T_{vj} = 175$ °C, $V_{GS(on)} = 20$ V		159		
			$T_{vj} = 25$ °C, $V_{GS(on)} = 18$ V		84		
Gate-source threshold voltage	$V_{GS(th)}$	$I_D = 3.3$ mA, $V_{DS} = V_{GS}$ (tested after 1 ms pulse at $V_{GS} = 20$ V)	$T_{vj} = 25$ °C	3.7	4.4	5.1	V
			$T_{vj} = 175$ °C		3.6		
Zero gate-voltage drain current	I_{DSS}	$V_{DS} = 1200$ V, $V_{GS} = 0$ V	$T_{vj} = 25$ °C		0.3	10	µA
			$T_{vj} = 175$ °C		10		
Gate leakage current	I_{GSS}	$V_{DS} = 0$ V	$V_{GS} = 25$ V			100	nA
			$V_{GS} = -10$ V			-100	
Forward transconductance	g_{fs}	$I_D = 10$ A, $V_{DS} = 20$ V			6.2		S
Short-circuit withstand time[1)]	t_{SC}	$V_{DD} \leq 800$ V, $V_{DS,peak} < 1200$ V, $T_{vj(start)} = 25$ °C, $R_{G,ext} = 2$ Ω	$V_{GS(on)} = 20$ V		1.5		µs
			$V_{GS(on)} = 18$ V		2		
			$V_{GS(on)} = 15$ V		2.5		
Internal gate resistance	$R_{G,int}$	$f = 1$ MHz, $V_{AC} = 25$ mV			3.8		Ω
Input capacitance	C_{iss}	$V_{DD} = 800$ V, $V_{GS} = 0$ V, $f = 100$ kHz, $V_{AC} = 25$ mV			671		pF
Output capacitance	C_{oss}	$V_{DD} = 800$ V, $V_{GS} = 0$ V, $f = 100$ kHz, $V_{AC} = 25$ mV			35		pF
Reverse transfer capacitance	C_{rss}	$V_{DD} = 800$ V, $V_{GS} = 0$ V, $f = 100$ kHz, $V_{AC} = 25$ mV			2		pF
C_{oss} stored energy	E_{oss}	$V_{DD} = 800$ V, $V_{GS} = 0$ V, $f = 100$ kHz, $V_{AC} = 25$ mV			14		µJ
Total gate charge	Q_G	$V_{DD} = 800$ V, $I_D = 10$ A, $V_{GS} = 0/20$ V, turn-on pulse			24		nC
Plateau gate charge	$Q_{GS(pl)}$	$V_{DD} = 800$ V, $I_D = 10$ A, $V_{GS} = 0/20$ V, turn-on pulse			7		nC
Gate-to-drain charge	Q_{GD}	$V_{DD} = 800$ V, $I_D = 10$ A, $V_{GS} = 0/20$ V, turn-on pulse			4		nC
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 800$ V, $I_D = 10$ A, $V_{GS} = 0/20$ V, $R_{G,ext} = 2$ Ω, $L_\sigma = 13$ nH, diode: body diode at $V_{GS} = 0$ V	$T_{vj} = 25$ °C		6.6		ns
			$T_{vj} = 175$ °C		6.4		

(table continues...)

Table 4 **(continued) Characteristic values**

Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Rise time	t_r	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{G,ext}$ = 2 Ω, L_σ = 13 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		4		ns
			T_{vj} = 175 °C		4.7		
Turn-off delay time	$t_{d(off)}$	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{G,ext}$ = 2 Ω, L_σ = 13 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		11.8		ns
			T_{vj} = 175 °C		12.5		
Fall time	t_f	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{G,ext}$ = 2 Ω, L_σ = 13 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		11.1		ns
			T_{vj} = 175 °C		12		
Turn-on energy	E_{on}	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{G,ext}$ = 2 Ω, L_σ = 13 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		71		µJ
			T_{vj} = 175 °C		91		
Turn-off energy	E_{off}	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{G,ext}$ = 2 Ω, L_σ = 13 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		30		µJ
			T_{vj} = 175 °C		30		
Total switching energy	E_{tot}	V_{DD} = 800 V, I_D = 10 A, V_{GS} = 0/20 V, $R_{G,ext}$ = 2 Ω, L_σ = 13 nH, diode: body diode at V_{GS} = 0 V	T_{vj} = 25 °C		101		µJ
			T_{vj} = 175 °C		121		
Virtual junction temperature	T_{vj}			-55		175	°C

1) not subject to production test - verified by design/characterization

***Note**: Characteristics at T_{vj} = 25°C, unless otherwise specified.*

3 Body diode (MOSFET)

Table 5 **Maximum rated values**

Parameter	Symbol	Note or test condition		Values	Unit
Drain-source voltage[1)]	V_{DSS}	T_{vj} = -55...175 °C		1200	V
Continuous reverse drain current for $R_{th(j-c,max)}$, limited by $T_{vj(max)}$ [2)]	I_{SDC}	V_{GS} = 0 V	T_c = 25 °C	22.7	A
			T_c = 100 °C	20.5	
Peak reverse drain current, t_p limited by $T_{vj(max)}$ [2)]	I_{SM}	V_{GS} = 0 V		22.7	A

1) tested at Tvj=25°C, verified by design/characterization over full temperature range

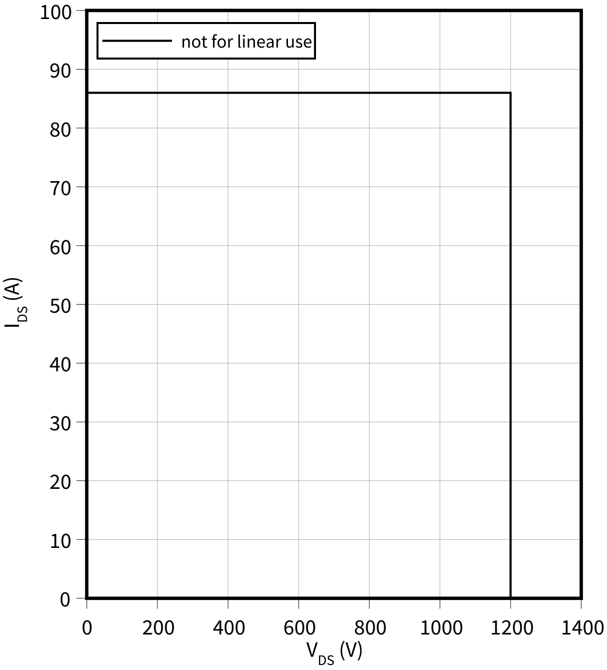
2) not subject to production test - verified by design/characterization

Table 6 **Characteristic values**

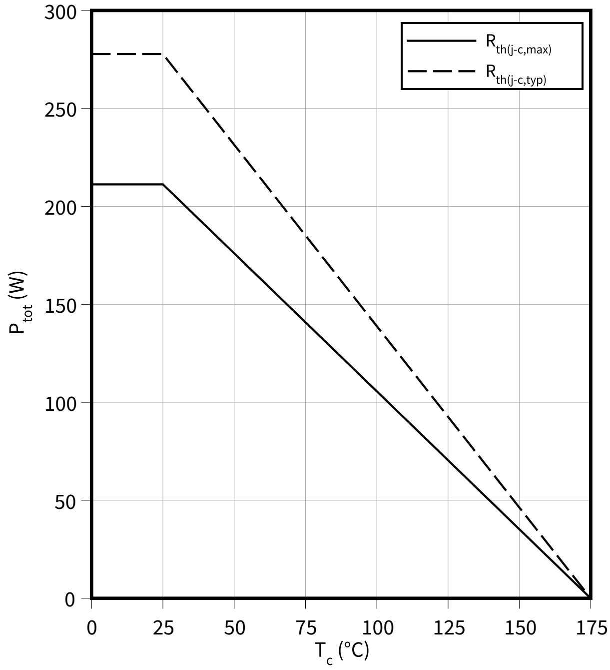
Parameter	Symbol	Note or test condition		Values			Unit
				Min.	Typ.	Max.	
Drain-source reverse voltage	V_{SD}	I_{SD} = 10 A, V_{GS} = 0 V	T_{vj} = 25 °C		3.9	5	V
			T_{vj} = 100 °C		3.8		
			T_{vj} = 175 °C		3.7		
MOSFET forward recovery charge	Q_{fr}	V_{DD} = 800 V, I_{SD} = 10 A, V_{GS} = 0 V, $-di_{SD}/dt$ = 1000 A/µs, Q_{fr} includes also Q_C	T_{vj} = 25 °C		134		nC
			T_{vj} = 175 °C		190		
MOSFET peak forward recovery current	I_{frm}	V_{DD} = 800 V, I_{SD} = 10 A, V_{GS} = 0 V, $-di_{SD}/dt$ = 1000 A/µs, Q_{fr} includes also Q_C	T_{vj} = 25 °C		8.1		A
			T_{vj} = 175 °C		8.6		
Virtual junction temperature	T_{vj}			-55		175	°C

4 Characteristics diagrams

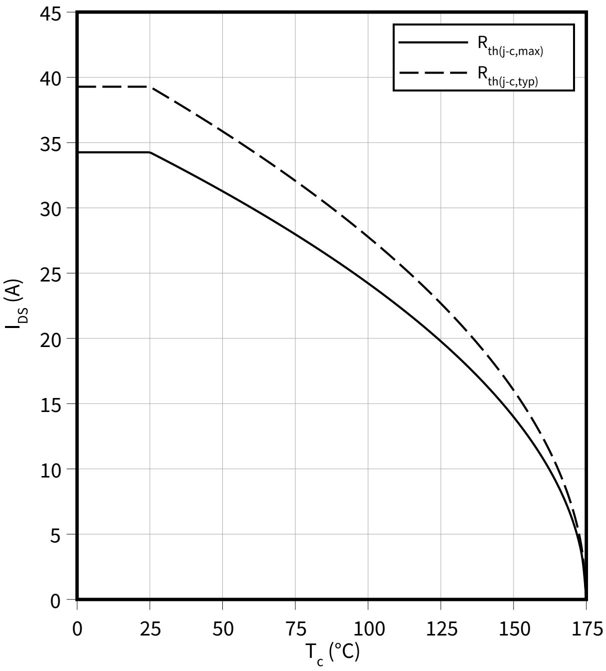
Reverse bias safe operating area (RBSOA)
$I_{DS} = f(V_{DS})$
$T_{vj} \leq 175$ °C, $V_{GS} = 0/20$ V, $T_c = 25$ °C



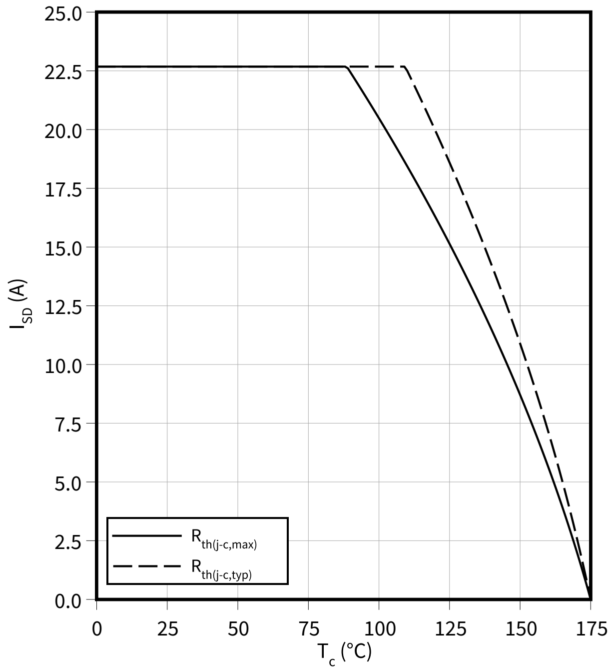
Power dissipation as a function of case temperature
$P_{tot} = f(T_c)$
$T_{vj} \leq 175$ °C



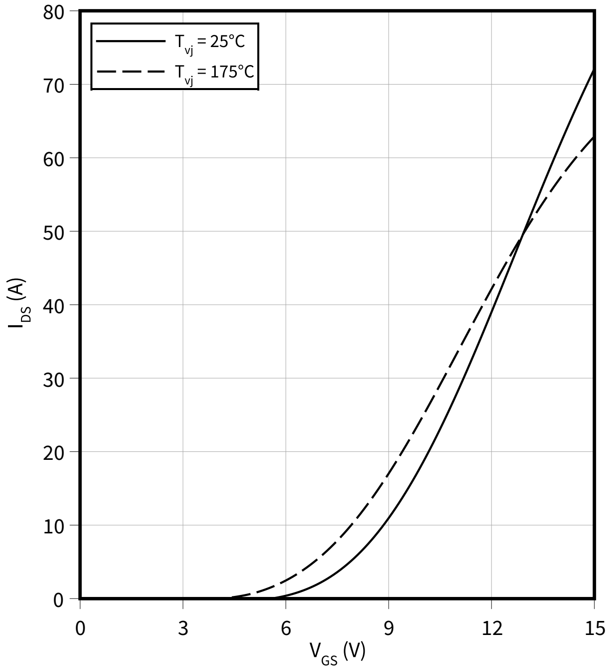
Maximum DC drain to source current as a function of case temperature
$I_{DS} = f(T_c)$



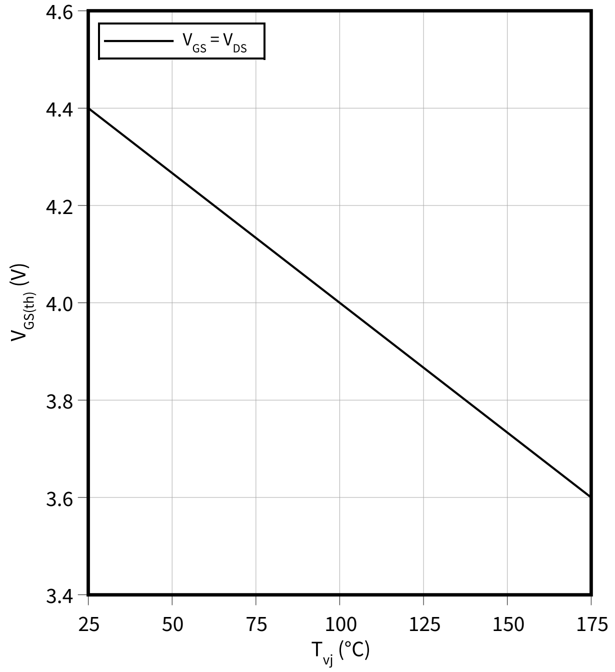
Maximum source to drain current as a function of case temperature
$I_{SD} = f(T_c)$
$V_{GS} = 0$ V



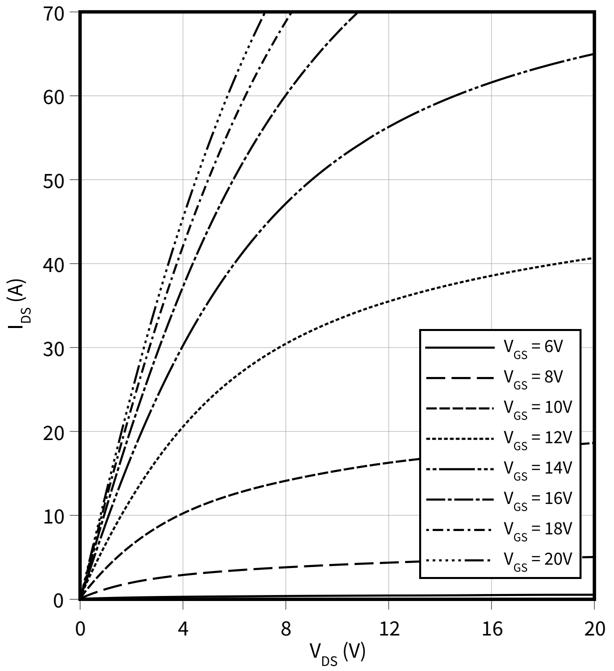
Typical transfer characteristic
$I_{DS} = f(V_{GS})$
$V_{DS} = 20$ V, $t_p = 20$ µs



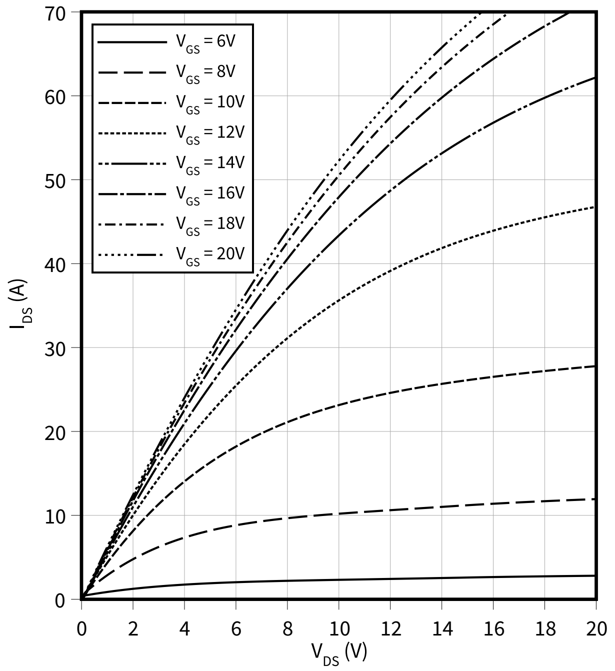
Typical gate-source threshold voltage as a function of junction temperature
$V_{GS(th)} = f(T_{vj})$
$I_D = 3.3$ mA



Typical output characteristic, V_{GS} as parameter
$I_{DS} = f(V_{DS})$
$T_{vj} = 25$ °C, $t_p = 20$ µs



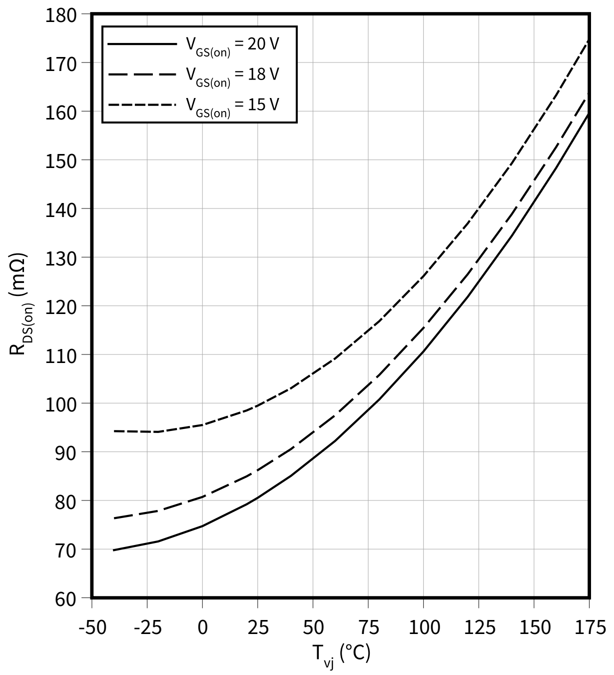
Typical output characteristic, V_{GS} as parameter
$I_{DS} = f(V_{DS})$
$T_{vj} = 175$ °C, $t_p = 20$ µs



Typical on-state resistance as a function of junction temperature

$R_{DS(on)} = f(T_{vj})$

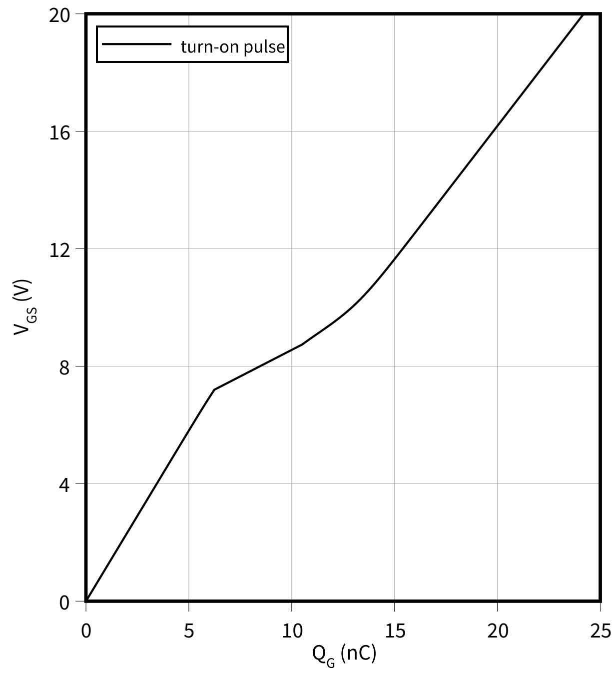
$I_D = 10$ A



Typical gate charge

$V_{GS} = f(Q_G)$

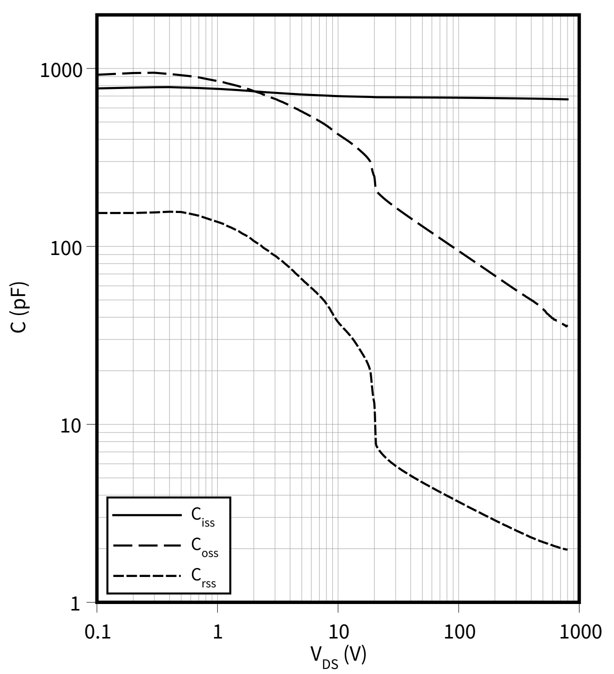
$I_D = 10$ A, $V_{DS} = 800$ V



Typical capacitance as a function of drain-source voltage

$C = f(V_{DS})$

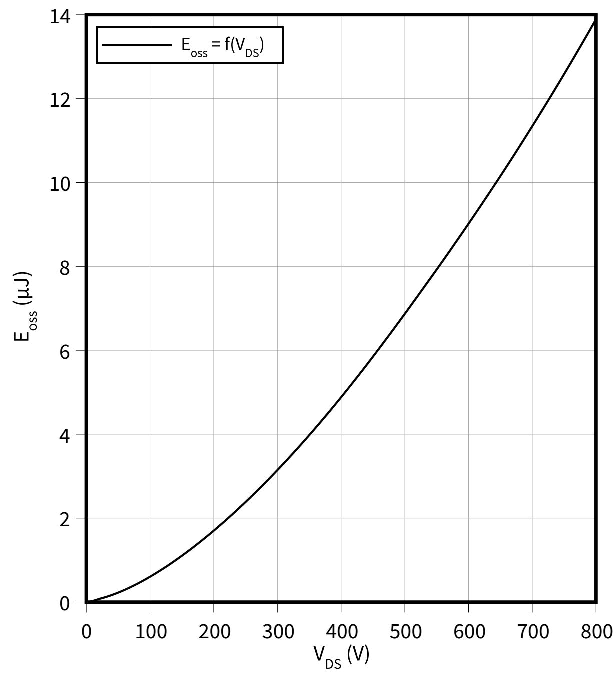
f = 100 kHz, $V_{GS} = 0$ V



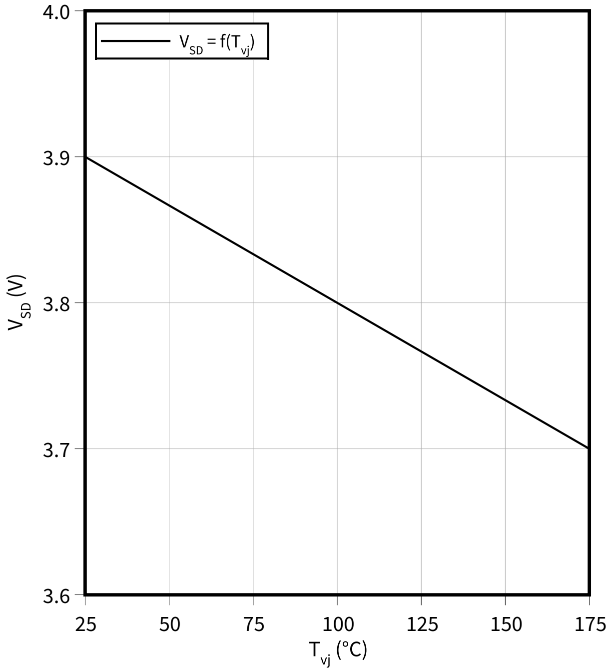
Typical C_{oss} stored energy

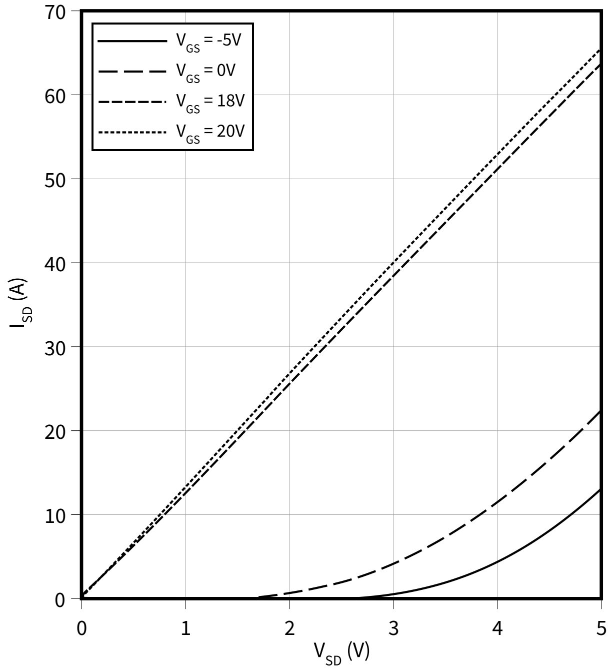
$E_{oss} = f(V_{DS})$

f = 100 kHz, $V_{GS} = 0$ V

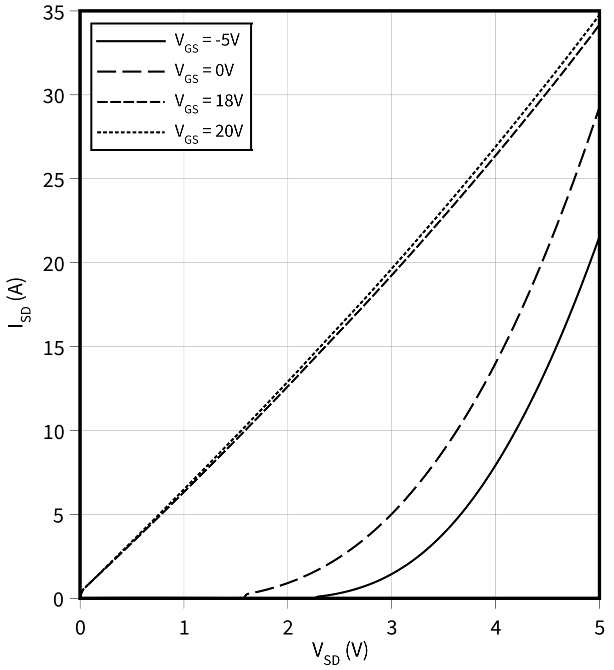


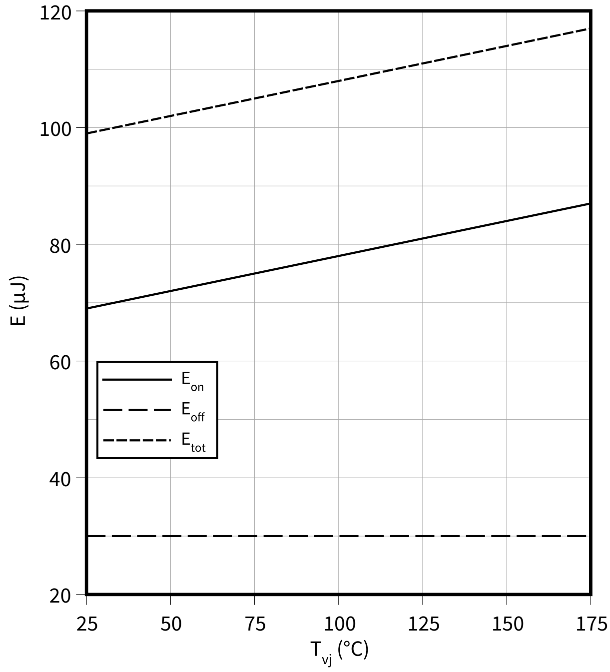
Typical reverse drain voltage as function of junction temperature $V_{SD} = f(T_{vj})$ $I_{SD} = 10$ A, $V_{GS} = 0$ V	**Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter** $I_{SD} = f(V_{SD})$ $T_{vj} = 25$ °C, $t_p = 20$ µs





Typical reverse drain current as function of reverse drain voltage, V_{GS} as parameter $I_{SD} = f(V_{SD})$ $T_{vj} = 175$ °C, $t_p = 20$ µs	**Typical switching energy as a function of junction temperature, test circuit in Fig. F, 2nd device own body diode: $V_{GS} = 0$ V** $E = f(T_{vj})$ $V_{GS} = 0/20$ V, $I_D = 10$ A, $R_{G,ext} = 2\ \Omega$, $V_{DD} = 800$ V

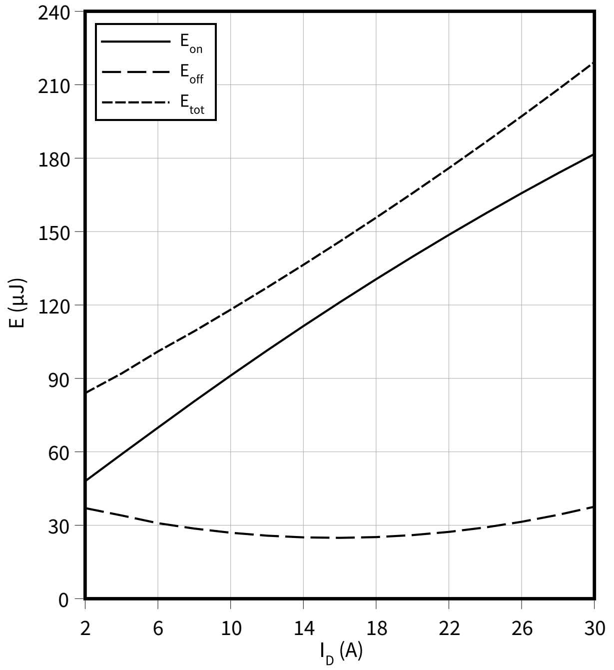




Typical switching energy as a function of drain current, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(I_D)$

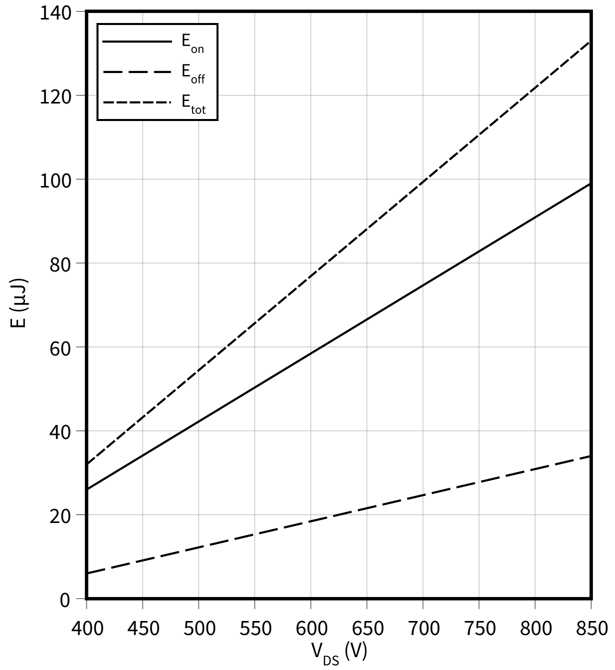
V_{GS} = 0/20 V, T_{vj} = 175 °C, $R_{G,ext}$ = 2 Ω, V_{DD} = 800 V



Typical switching energy as a function of drain voltage, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(V_{DS})$

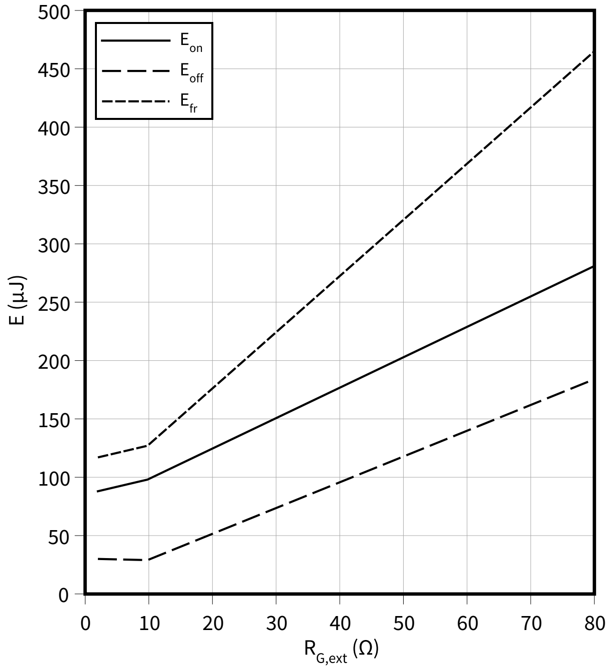
V_{GS} = 0/20 V, I_D = 10 A, T_{vj} = 175 °C, $R_{G,ext}$ = 2 Ω



Typical switching energy as a function of gate resistance, test circuit in Fig. F, 2nd device own body diode: V_{GS} = 0 V

$E = f(R_{G,ext})$

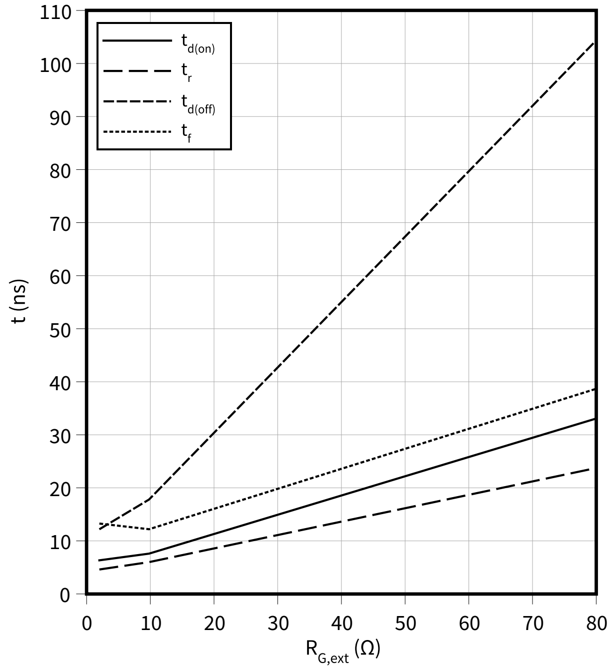
V_{GS} = 0/20 V, I_D = 10 A, T_{vj} = 175 °C, V_{DD} = 800 V



Typical switching times as a function of gate resistance

$t = f(R_{G,ext})$

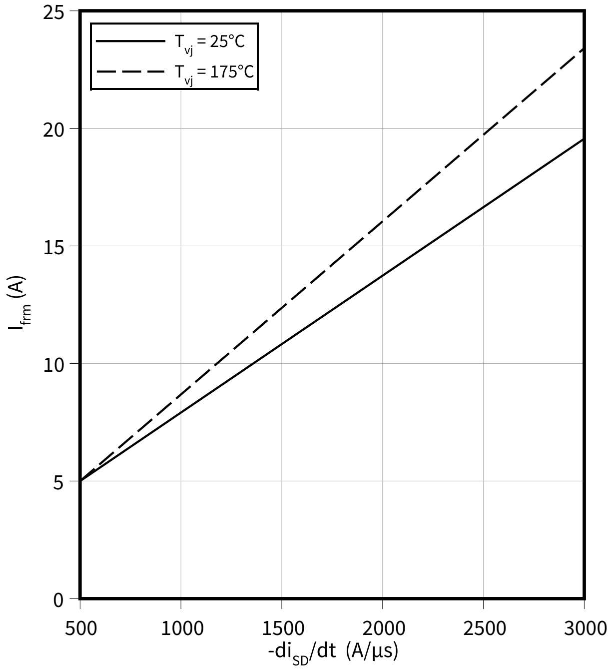
I_D = 10 A, V_{GS} = 0/20 V, T_{vj} = 175 °C, V_{DD} = 800 V



Typical MOSFET peak forward recovery current as a function of reverse drain current slope

$I_{frm} = f(-di_{SD}/dt)$

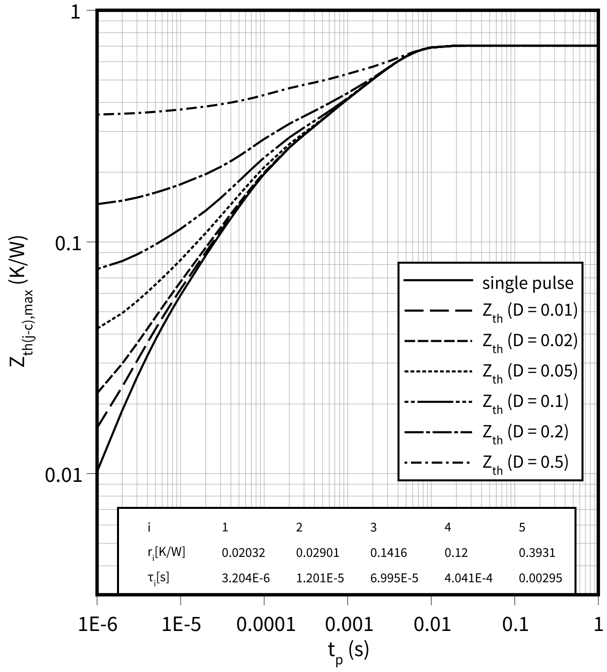
$V_{GS} = 0/20$ V, $I_{SD} = 10$ A, $V_{DD} = 800$ V



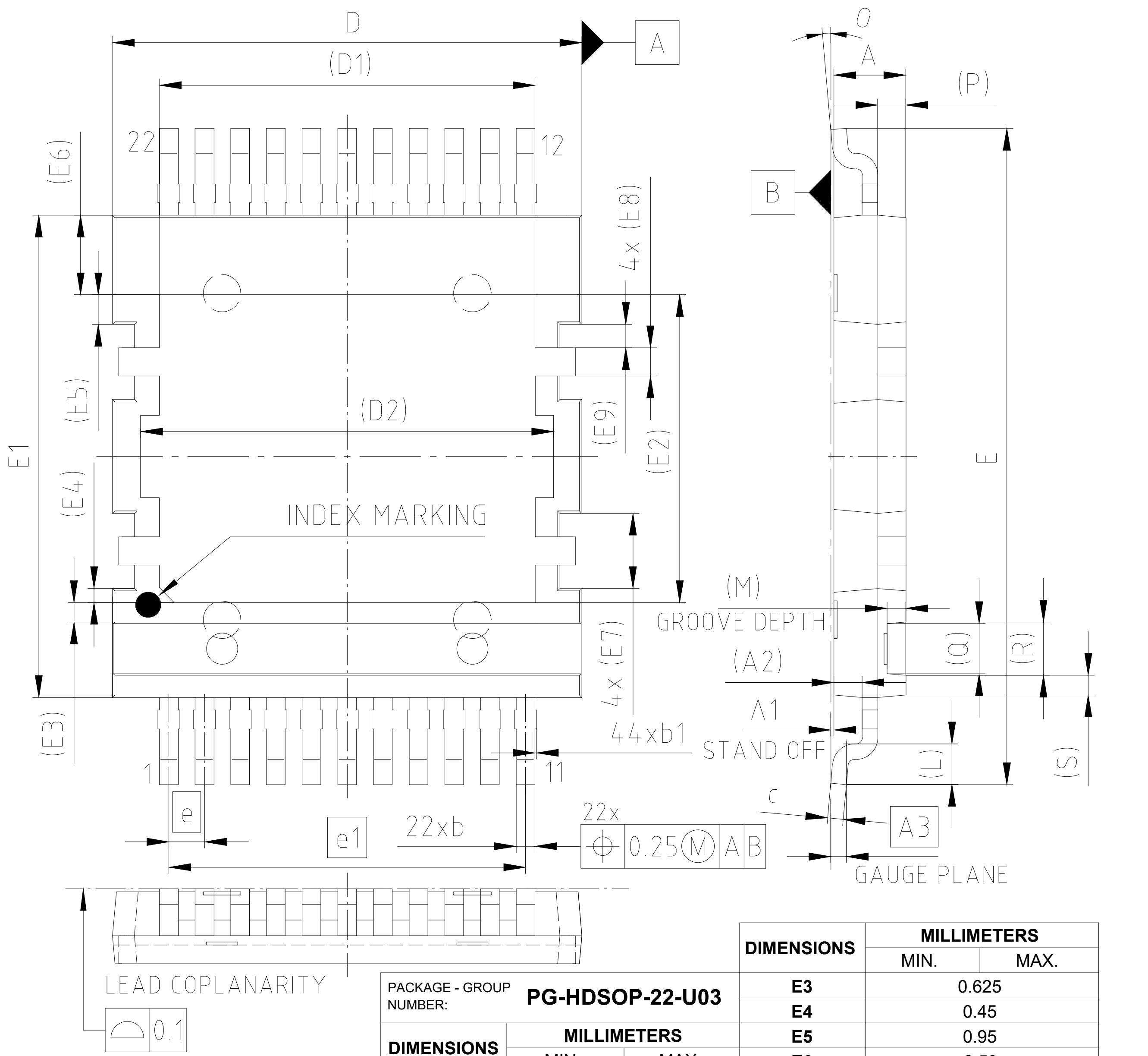
Max. transient thermal impedance (MOSFET/diode)

$Z_{th(j\text{-}c),max} = f(t_p)$

$D = t_p/T$



5 Package outlines



NOTES:

ALL METAL SURFACES TIN PLATED EXCEPT AREA OF CUT

DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS

PACKAGE - GROUP NUMBER: **PG-HDSOP-22-U03**

DIMENSIONS	MILLIMETERS MIN.	MILLIMETERS MAX.
A	2.25	2.35
A1	0.00	0.15
A2	0.90	
A3	0.50	
b	0.50	0.70
b1	---	0.15
c	0.46	0.58
D	14.90	15.10
D1	12.00	
D2	13.20	
E	20.81	21.11
E1	15.30	15.50
E2	9.83	

DIMENSIONS	MILLIMETERS MIN.	MILLIMETERS MAX.
E3	0.625	
E4	0.45	
E5	0.95	
E6	2.53	
E7	2.40	
E8	0.90	
E9	0.75	
e	1.14	
e1	11.4	
L	1.30	
M	0.60	
N	22	
O	0°	8°
P	0.90	
Q	1.60	
R	1.70	
S	0.631	

Figure 1

6 Testing conditions

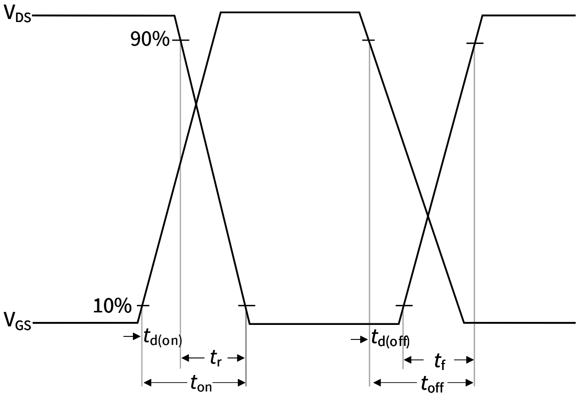


Figure A. **Definition of switching times**

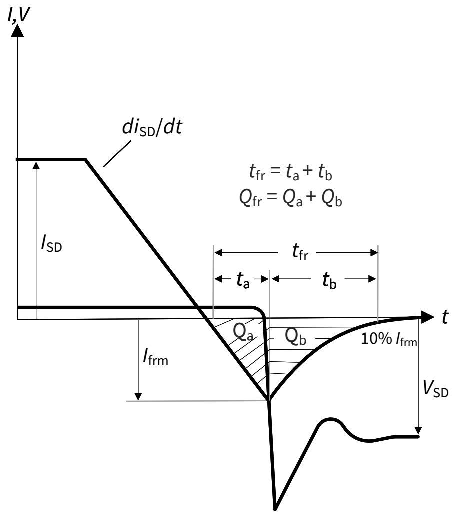


Figure B. **Definition of body diode switching characteristics**

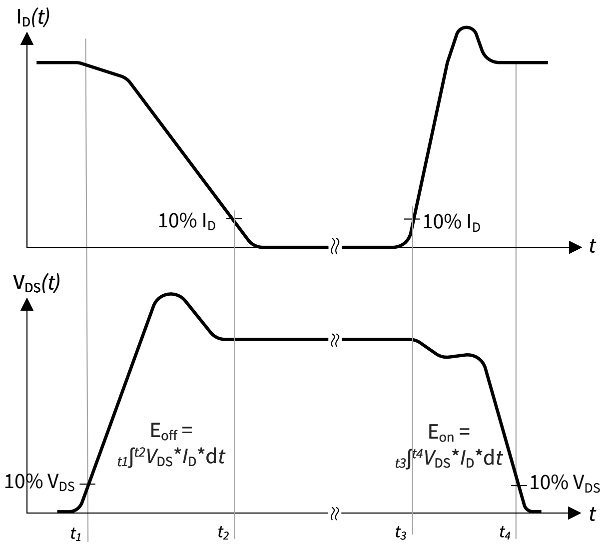


Figure C. **Definition of switching losses**

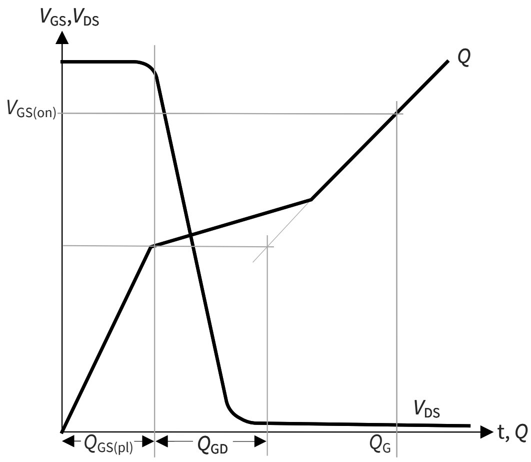


Figure D. **Definition of QGD**

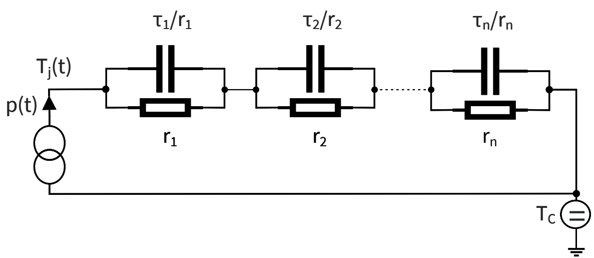


Figure E. **Thermal equivalent circuit**

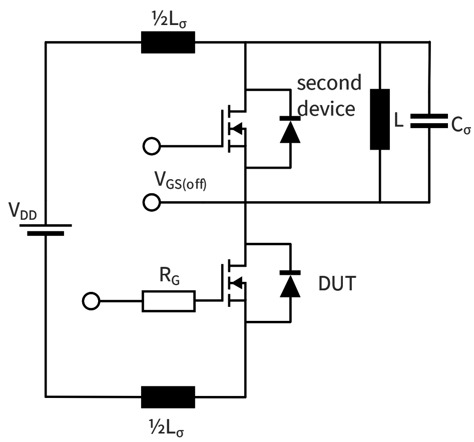


Figure F. **Dynamic test circuit**
Parasitic inductance L_σ,
Parasitic capacitor C_σ,

Figure 2

Revision history

Document revision	Date of release	Description of changes
0.10	2023-01-17	Target datasheet
0.20	2024-07-01	Preliminary datasheet
1.00	2024-07-22	Final datasheet

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