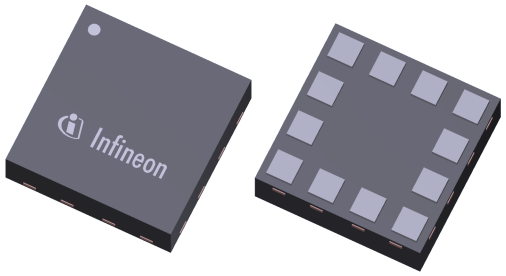
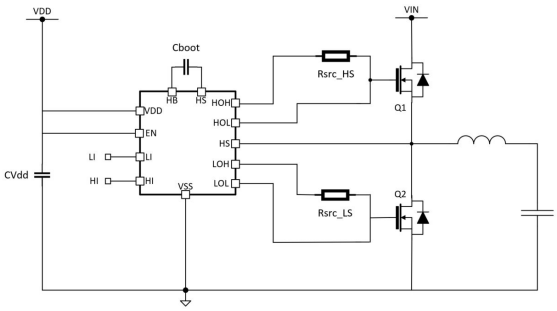
Features

- Independent high- and low-side TTL logic inputs
- UVLO for both high- and low-side drivers
- Integrated bootstrap switch
- Active bootstrap clamp to avoid bootstrap capacitor overcharging during deadtime (2EDL5013U2D)
- Absolute maximum bootstrap voltage of 120 V
- Split outputs for adjustable turn-on / turn-off driving strength
- 2 A to 3 A peak source, 5 A peak sink current capability
- Built-in active miller clamp
- 1.5 Ω pull-up, 0.5 Ω pull-down resistance for low-side
- 0.9 Ω pull-up, 0.5 Ω pull-down resistance for high-side
- Fast propagation delay (20 ns typical)
- 1 ns typical propagation delay matching
- 4.5 V to 5.5 V supply voltage operating range
- Offered in TSNP-12 2x2 package





Potential applications

- Telecom/Datacom half- and full-bridge power converters
- Buck converters
- Two switch forward converters
- Active clamp forward converters
- Class D amplifiers
- Class D wireless charging

Product validation

Qualified for industrial applications according to the relevant tests of JEDEC47/20/22.

Description

The 2EDL50X3U2D is a half-bridge gate driver designed to drive both the high-side and the low-side MOSFETs in a synchronous buck or half-bridge configuration. The floating high-side driver is capable of driving a high-side MOSFET operating up to 120 V bootstrap voltage. The high-side bias voltage is generated using a bootstrap technique via the internal bootstrap switch which is controlled by the low-side PWM. An active bootstrap clamp mechanism is implemented in 2EDL5013U2D to avoid overcharging the bootstrap capacitor during deadtime. The inputs of the driver are TTL logic compatible and can withstand input voltage of up to 5.9 V. The gate outputs are split to provide flexibility in adjusting the turn on and turn off strength independently and an active miller clamp is implemented on both outputs to avoid induced turn-on phenomenon. The 2EDL50X3U2D is available in TSNP-12 pins 2 mm x 2 mm package.

Table 1 Device information

Part number	Active bootstrap clamp feature	Package	Body size
2EDL5013U2D	Yes	PG-TSNP-12-5	2 mm x 2 mm
2EDL5023U2D	No	PG-TSNP-12-5	2 mm x 2 mm

Table of contents

1 Package information

1.1 Ordering information

Base part number	Package type	Standard pack		Orderable part number	Marking code
		Form	Quantity		
2EDL5013U2D	PG-TSNP-12-5	Tape and reel	5000	2EDL5013U2DXTMA1	2EDL5013
2EDL5023U2D	PG-TSNP-12-5	Tape and reel	5000	2EDL5023U2DXTMA1	2EDL5023

1.2 Pin configuration

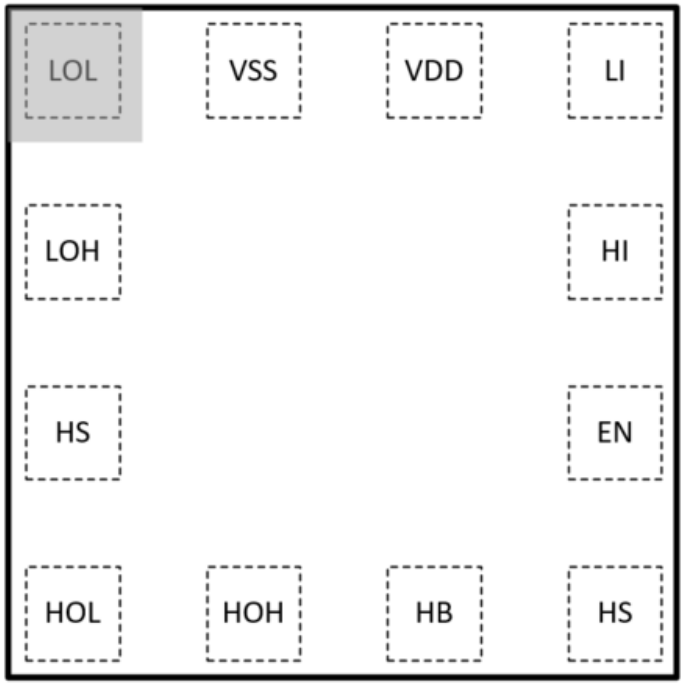


Figure 1 Top view

1.3 Pin description

Pin #	Symbol	Function
1	LOL	Low-side gate driver sink current output
2	LOH	Low-side gate driver source current output
3	HS	High-side source connection
4	HOL	High-side gate driver sink current output
5	HOH	High-side gate driver source current output
6	HB	High-side gate driver bootstrap rail
7	HS	High-side source connection

8	EN	Enable input. When this pin is high or left-open, it enables the driver. If pulled low, it disables the driver.
9	HI	High-side PWM input
10	LI	Low-side PWM input
11	VDD	5V gate drive supply
12	VSS	Ground return

2 General product characteristics

2.1 Absolute maximum ratings

Table 3

Stresses above the values listed under "Absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability. All voltage parameters are referenced to V_{SS} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply input voltage	V_{DD}	-0.3	–	5.9	V	
High-side supply voltage	V_{HB-HS}	-0.3	–	5.9	V	Referenced to V_{HS}
High-side bootstrap voltage	V_{HB}	-0.3	–	120	V	1)
Phase voltage	V_{HS}	-5.9	–	V_{HB} + 0.3	V	1)
HI and LI input voltage	V_{HI}, V_{LI}	-0.3	–	V_{DD} + 0.3	V	
Enable input voltage	V_{EN}	-0.3	–	V_{DD} + 0.3	V	
Output voltage on LOL, LOH	V_{LOL}, V_{LOH}	-0.3	–	V_{DD} + 0.3	V	
Output voltage on HOL, HOH	V_{HOL}, V_{HOH}	V_{HS} - 0.3	–	V_{HB} + 0.3	V	
Operating junction temperature	T_J	-40	–	150	°C	
Storage temperature	T_S	-55	–	150	°C	

1) Not subject to production test. Verified by design/characterization.

2.2 ESD Ratings

Description	Symbol	Value	Unit
Human body model sensitivity as per ANSI/ESDA/JEDEC JS-001	ESD_{HBM}	±1000	V
Charged device model sensitivity as per ANSI/ESDA/JEDEC JS-002	ESD_{CDM}	±1000	V

2.3 Recommended operating conditions

Table 4

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to V_{SS} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply input voltage	V_{DD}	4.5	5	5.5	V	
High-side supply voltage	V_{HB-HS}	4	5	5.5	V	Referenced to V_{HS}

(table continues...)

Table 4 (continued)

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the device. All voltage parameters are referenced to V_{SS} unless otherwise specified.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
High-side bootstrap voltage	V_{HB}	-0.3	–	110	V	
Phase voltage	V_{HS}	-2	–	V_{HB} - V_{DD}	V	V_{HB-HS} = 4.5 V
HI and LI input voltage	V_{HI}, V_{LI}	0	–	VDD	V	
Enable input voltage	V_{EN}	0	–	VDD	V	
Low-side output voltage	V_{LOL}, V_{LOH}	0	–	VDD	V	
High-side output voltage	V_{HOL}, V_{HOH}	V_{HS}	–	V_{HB}	V	
HS Slew rate	$HS_{dV/dT}$	–	–	100	V/ns	
Junction temperature range	T_J	-40	–	125	°C	

2.4 Thermal mechanical characteristics

Table 5

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Junction-to-ambient thermal resistance	Θ_{JA}	–	65	–	°C/W	1)
Junction-to-case thermal resistance - bottom	θ_{JC}	–	21	–	°C/W	
Junction-to-case thermal resistance - top	θ_{JC}	–	69	–	°C/W	

1) Device on 76.2 mm x 76.2 mm x 1.5 mm epoxy PCB FR4 (JEDEC 2s2p). PCB vertical in still air.

2.5 Electrical characteristics

Table 6

Unless otherwise specified: $V_{DD} = V_{HB} = 5$ V, $V_{HS} = V_{SS} = 0$ V. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Supply current						
VDD quiescent current	I_{QVDD}	–	90	150	uA	V_{LI} and $V_{HI} = 0$ V
VDD operating current	I_{OVDD}	–	3.2	4.2	mA	$F_{sw} = 500$ kHz, $C_{load} = 1$ nF
HB quiescent current	I_{QHB}	–	145	230	uA	V_{LI} and $V_{HI} = 0$ V
HB operating current	I_{OHB}	–	3.1	4	mA	$F_{sw} = 500$ kHz, $C_{load} = 1$ nF
HB to VSS leakage current	I_{QHBS}	–	0.1	2	uA	$V_{HS} = V_{HB} = 110$ V, V_{LI} and $V_{HI} = 0$ V
Input						
Input voltage rising threshold	V_H	–	2.4	2.6	V	
Input voltage falling threshold	V_L	1.25	1.6	–	V	
Input voltage hysteresis	V_{HYS}	–	0.8	–	V	
Input pull down resistance	R_{IN}	100	200	300	kΩ	
Enable						
Enable input rising threshold	V_{EN}	–	2.3	–	V	
Enable input falling threshold	V_{DIS}	–	1.1	–	V	
Enable voltage hysteresis	V_{ENHYS}	–	1.2	–	V	
Enable pull up resistance	R_{EN}	80	100	120	kΩ	
Time to enable the driver	T_{EN}	–	13	20	ns	
Time to disable the driver	T_{DIS}	–	13	20	ns	
Undervoltage lockout						
VDD UVLO Rising threshold	V_{DDR}	3.2	3.8	4.5	V	
VDD UVLO Falling threshold	V_{DDF}	3	3.6	4.3	V	
VDD UVLO Threshold hysteresis	V_{DDH}	–	0.20	–	V	
VHB UVLO Rising threshold	V_{HBR}	2.5	3.2	3.9	V	
VHB UVLO Falling threshold	V_{HBF}	2.3	3	3.7	V	

(table continues...)

Table 6 (continued)

Unless otherwise specified: $V_{DD} = V_{HB} = 5$ V, $V_{HS} = V_{SS} = 0$ V. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
VHB UVLO Threshold hysteresis	V_{HBH}	–	0.20	–	V	
Bootstrap switch						
Bootstrap switch high current forward voltage	V_{DH}	–	1.4	1.6	V	I_{VDD-HB} = 100 mA, 2EDL5013U2D
Bootstrap switch high current forward voltage	V_{DH}	–	1.1	1.3	V	I_{VDD-HB} = 100 mA, 2EDL5023U2D
Bootstrap switch low current forward voltage	V_{DL}	–	0.01	0.10	V	I_{VDD-HB} = 100 uA, 2EDL5013U2D
Bootstrap switch low current forward voltage	V_{DL}	–	0.01	0.10	V	I_{VDD-HB} = 100 uA, 2EDL5023U2D
Bootstrap switch resistance	R_{BS}	–	14	16	Ω	I_{VDD_HB} = 100 mA, 2EDL5013U2D
Bootstrap switch resistance	R_{BS}	–	11	13	Ω	I_{VDD-HB} = 100 mA, 2EDL5023U2D
Low-side gate driver						
Peak source current	I_{LSRC}	–	2.0	–	A	V_{LOH} = 0 V[1)]
Peak sink current	I_{LSNK}	–	5.0	–	A	V_{LOL} = 5 V[1)]
Pull up resistance	R_{LPU}	–	1.40	1.90	Ω	I_{LOH} = -100 mA
Pull down resistance	R_{LPD}	–	0.50	0.70	Ω	I_{LOL} = 100 mA[2)]
High-side gate driver						
Peak source current	I_{HSRC}	–	3.0	–	A	V_{HOH} = 0 V[1)]
Peak sink current	I_{HSNK}	–	5.0	–	A	V_{HOL} = 5 V[1)]
Pull up resistance	R_{HPU}	–	0.90	1.20	Ω	I_{HOH} = -100 mA
Pull down resistance	R_{HPD}	–	0.50	0.70	Ω	I_{HOL} = 100 mA[2)]
Output miller clamp (LOL and HOL)						
Miller clamp activation threshold	V_{MILLER}	–	0.5	–	V	[1)]
Miller clamp activation delay	T_{MILLER}	–	5	10	ns	[1)]
Peak sink current during miller clamp activation	I_{SNK_OFF}	–	7	–	A	V_{LOL} , V_{HOL} = 5 V[1)]

(table continues...)

Table 6 (continued)

Unless otherwise specified: $V_{DD} = V_{HB} = 5$ V, $V_{HS} = V_{SS} = 0$ V. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Pull down resistance during miller clamp activation	R_{PD_OFF}	–	0.40	0.60	Ω	I_{LOL}, I_{HOL} = 100 mA

1) Not subject to production test. Verified by design/characterization.
2) Verified by design.

2.6 Switching characteristics

Table 7

Unless otherwise specified: $V_{DD} = V_{HB} = 5$ V, $V_{HS} = V_{SS} = 0$ V. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
Propagation delay						
LO Rising propagation delay	T_{LLH}	–	20	30	ns	C_{load} = 0 , LI rising to LOH rising
LO Falling propagation delay	T_{LHL}	–	20	30	ns	C_{load} = 0 , LI falling to LOL falling
HO Rising propagation delay	T_{HLH}	–	20	30	ns	C_{load} = 0 , HI rising to HOH rising
HO Falling propagation delay	T_{HHL}	–	20	30	ns	C_{load} = 0 , HI falling to HOL falling
Delay matching						
Delay matching LO on and HO off	T_{DMON}	–	1	3.5	ns	Between LO rising and HO falling
Delay matching LO off and HO on	T_{DMOFF}	–	1	3.5	ns	Between LO falling and HO rising
Output rise and fall time						
HO Rise time	T_{HRC}	–	4.4	–	ns	C_{load} = 1 nF, 10 % to 90 %[1)]
LO Rise time	T_{LRC}	–	4.2	–	ns	C_{Load} = 1 nF, 10 % to 90 %[1)]
HO Fall time	T_{HFC}	–	3.5	–	ns	C_{Load} = 1 nF, 90 % to 10 %[1)]

(table continues...)

Table 7 (continued)

Unless otherwise specified: $V_{DD} = V_{HB} = 5$ V, $V_{HS} = V_{SS} = 0$ V. The minimum and maximum limits are valid over the full operating temperature range and are ensured by characterization and statistical correlation. Typical values are tested at $T_C = 25$°C.

Parameter	Symbol	Values			Unit	Note or condition
		Min.	Typ.	Max.		
LO Fall time	T_{LFC}	–	2.7	–	ns	C_{Load} = 1 nF, 90 % to 10 %[1)]
Miscellaneous						
Shortest input pulse width transferred to the output	T_{PW}	–	5	10	ns	

1) Not subject to production test. Verified by design/characterization.

3 Timing diagrams

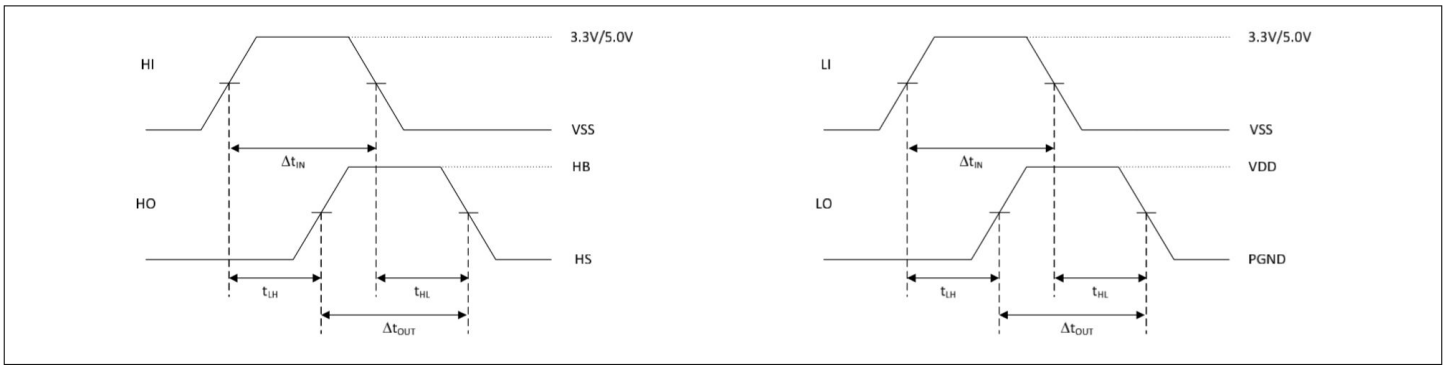


Figure 2 Propagation delay

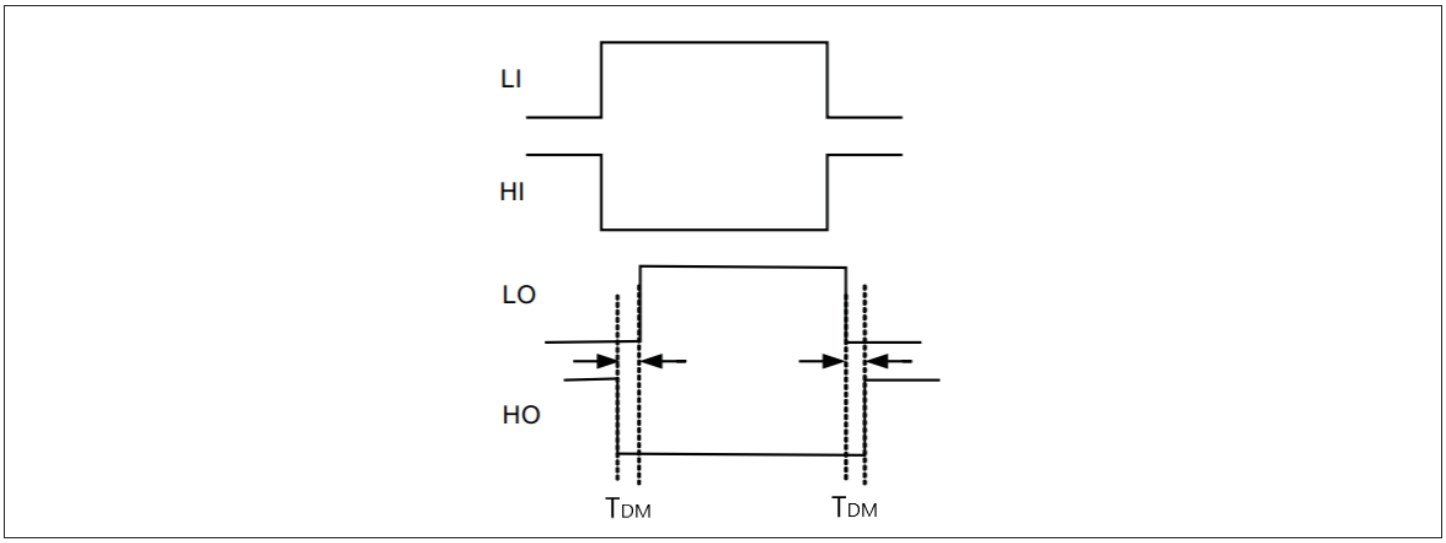


Figure 3 Delay matching

4 Typical characteristics

Unless otherwise specified: $V_{DD} = V_{HB} = 5$ V, $V_{HS} = V_{SS} = 0$ V, $T_C = 25$°C and no load on the outputs.

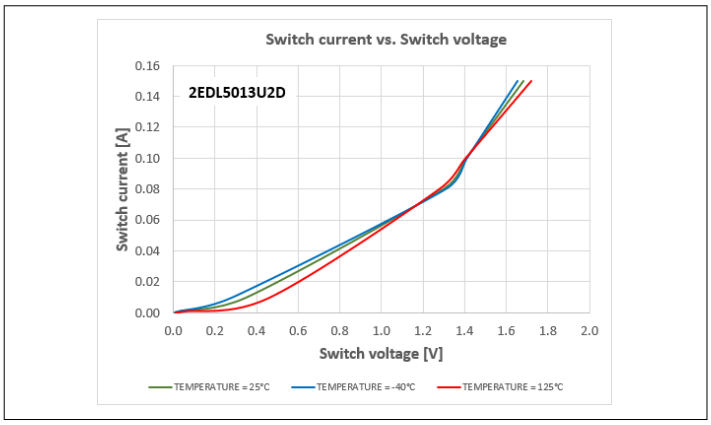


Figure 4 Bootstrap switch current vs. voltage

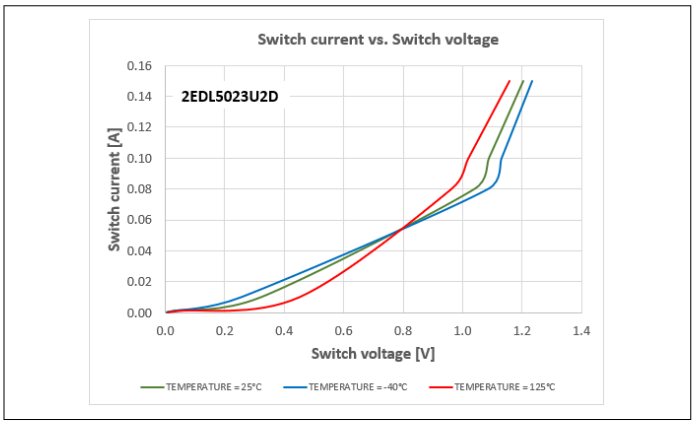


Figure 5 Bootstrap switch current vs. voltage

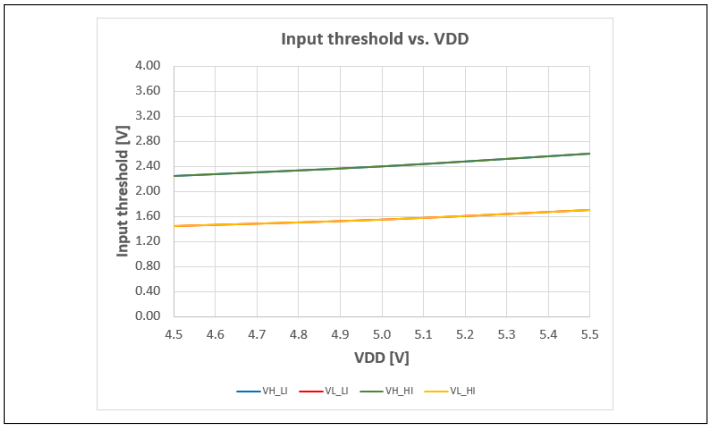


Figure 6 Input threshold vs. VDD

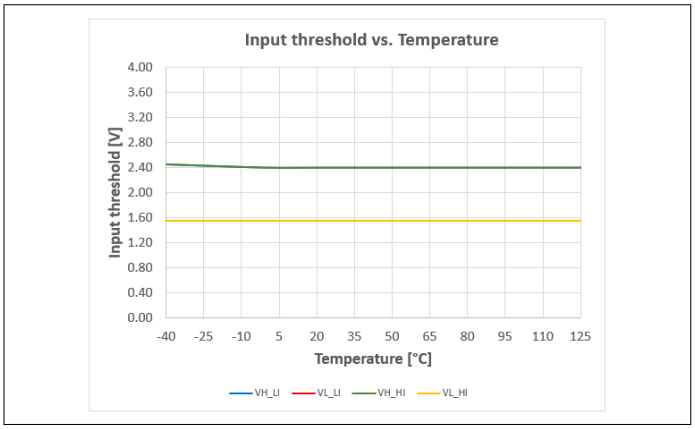


Figure 7 Input threshold vs. Temperature

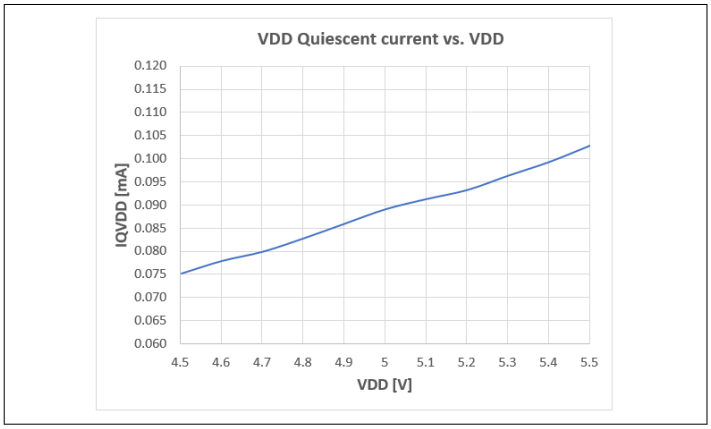


Figure 8 VDD Quiescent current vs. VDD

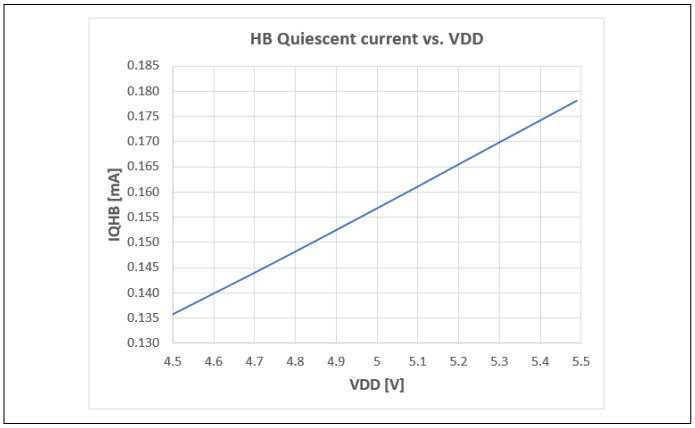


Figure 9 HB Quiescent current vs. VDD

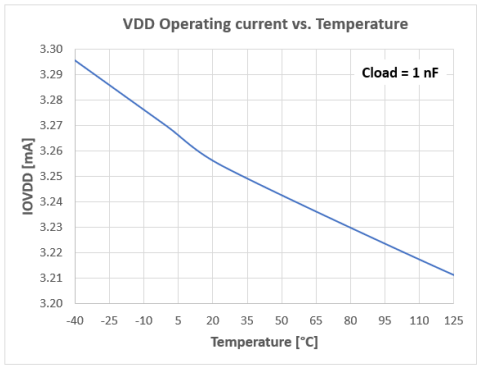


Figure 10 VDD Operating current vs. Temperature

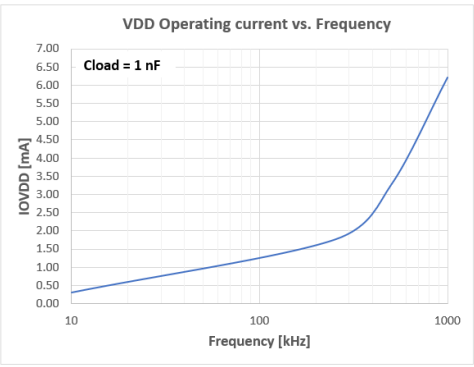


Figure 11 VDD Operating current vs. Frequency

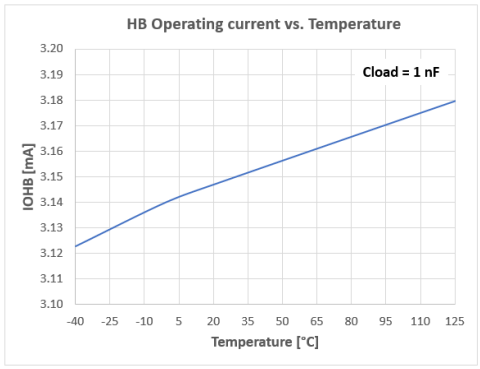


Figure 12 HB Operating current vs. Temperature

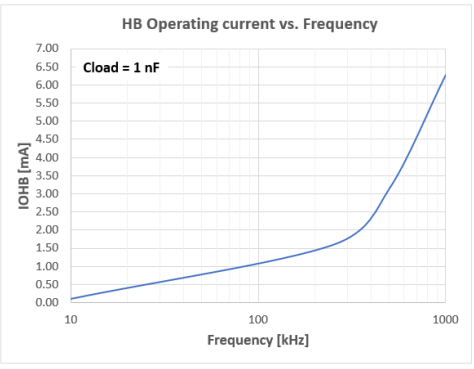


Figure 13 HB Operating current vs. Frequency

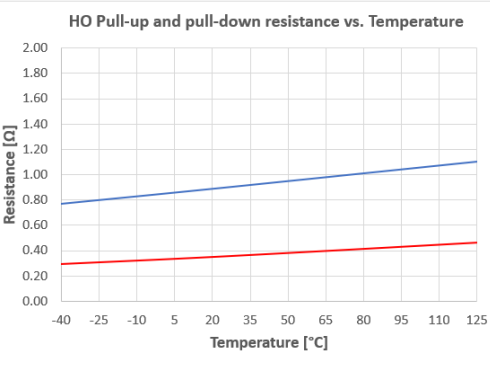


Figure 14 HO Pull-up and pull-down resistance vs. Temperature

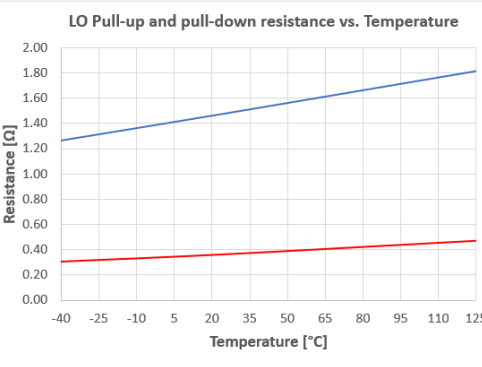


Figure 15 LO Pull-up and pull-down resistance vs. Temperature

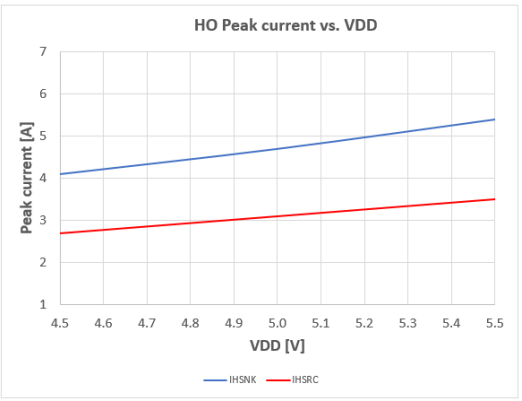


Figure 16 HO Peak current vs. VDD

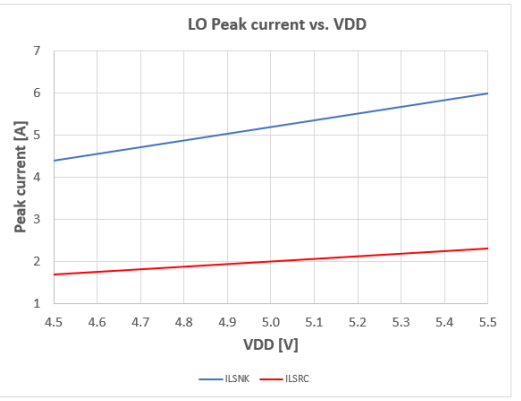


Figure 17 LO Peak current vs. VDD

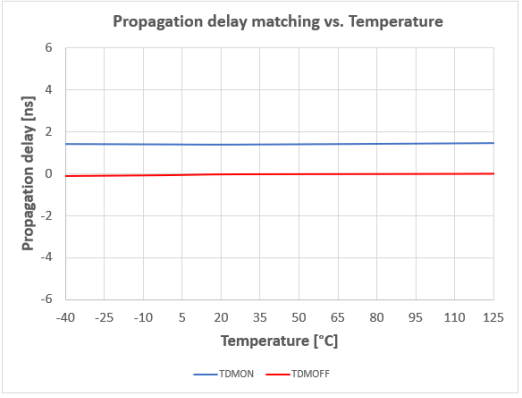


Figure 18 Propagation delay matching vs. Temperature

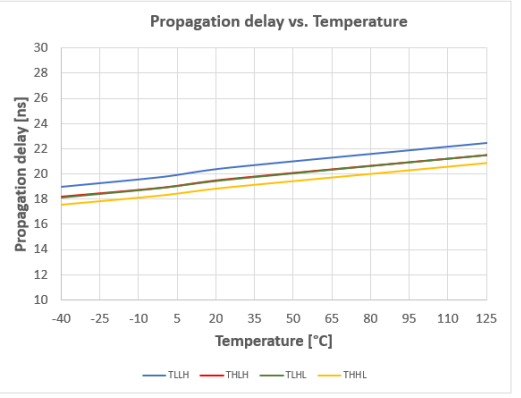


Figure 19 Propagation delay vs. Temperature

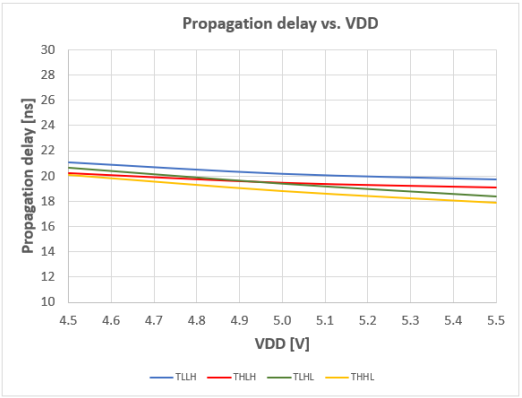


Figure 20 Propagation delay vs. VDD

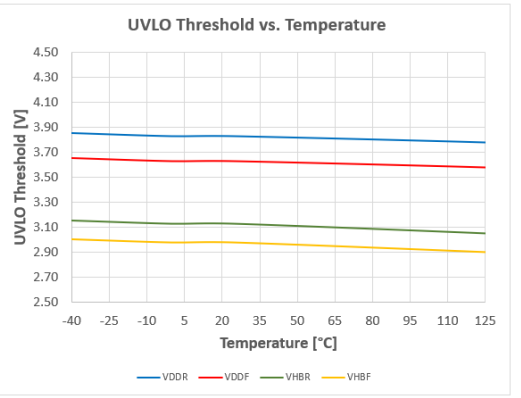


Figure 21 UVLO Threshold vs. Temperature

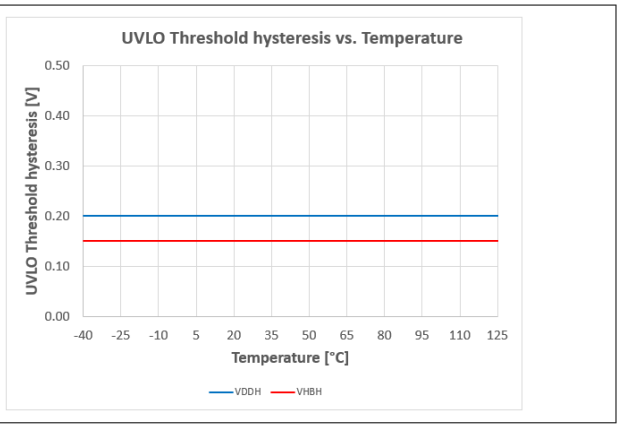


Figure 22 **UVLO Threshold hysteresis vs. Temperature**

5 Product information

5.1 Block diagram

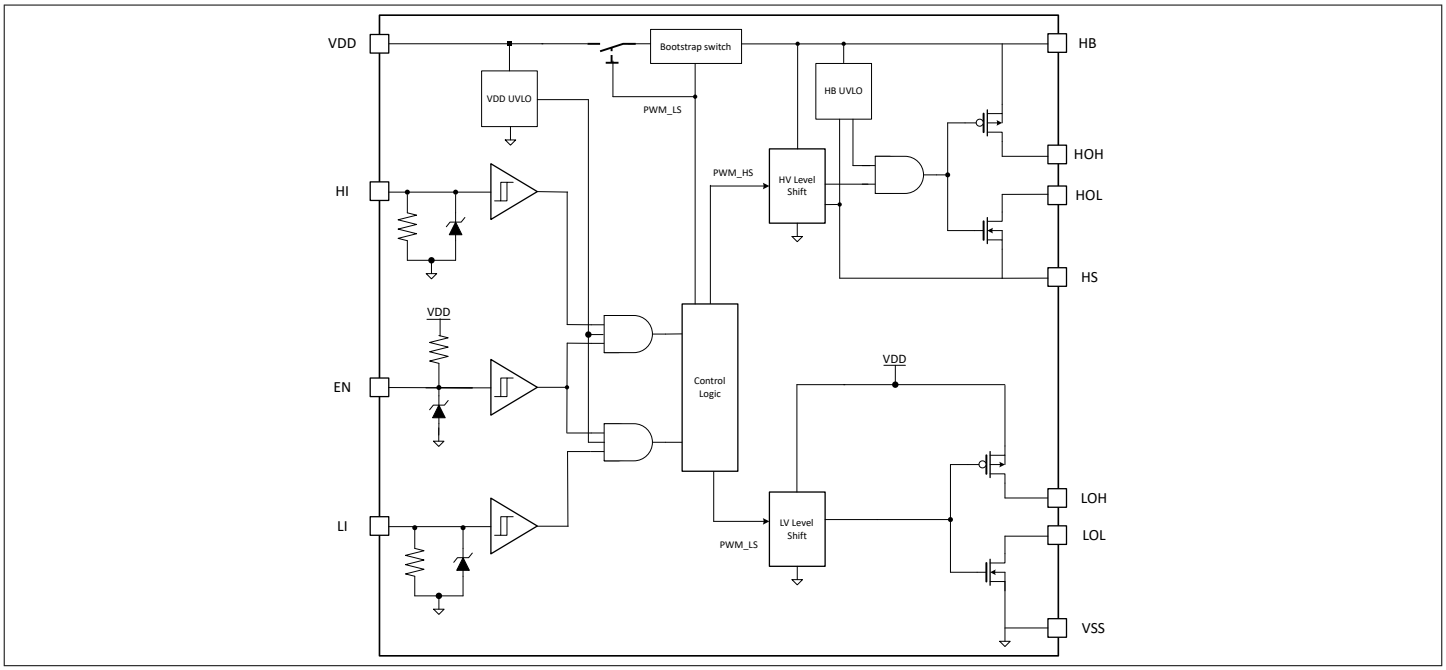


Figure 23 2EDL5013U2D Block diagram

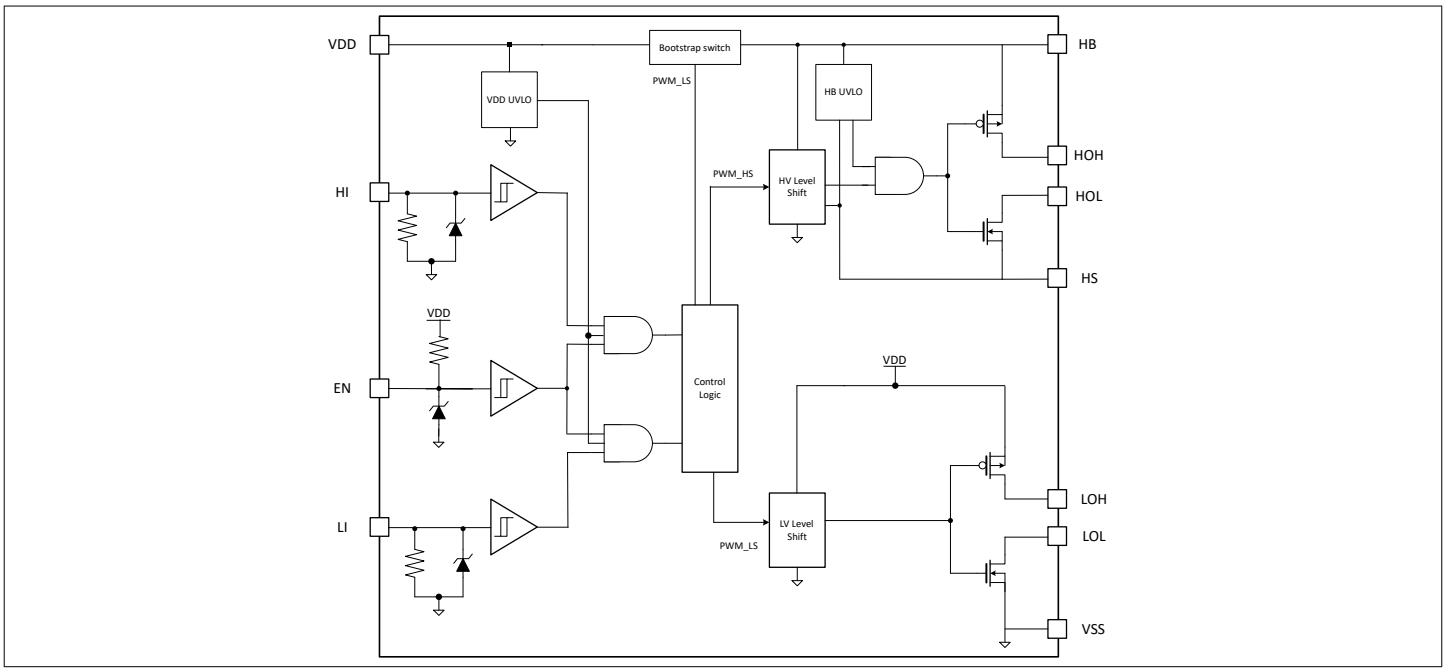


Figure 24 2EDL5023U2D Block diagram

5.2 Functional description

The 2EDL50X3U2D is a fast half-bridge driver for both high-side and low-side MOSFETs in a synchronous buck or half-bridge configuration. The output stages with very low output impedance and high current capability are chosen to ensure highest flexibility and cover a wide range of applications. The focus on robustness at the input and output side

additionally gives this device a safety margin in critical abnormal situations. All outputs are robust against reverse current. The interaction with the power switch, even reverse reflected power will be handled by the strong internal output stage. All inputs are compatible with LV_TTL signal levels. Since the 2EDL50X3U2D aims at fast-switching applications, signal delays and rise/fall times have been minimized. Special effort has been made towards minimizing delay differences between the high-side and low-side to values of typically 1 ns.

5.2.1 Supply voltage and undervoltage lockout (UVLO)

The absolute maximum supply voltage is 5.9 V for both VDD and HB-HS and the minimum operating supply voltage is set by the under voltage lockout function. The under voltage lockout function ensures that the output can be switched to its high level only if the supply voltage exceeds the UVLO rising threshold voltage. Thus, it can be guaranteed that the switch transistor is not switched on if the driving voltage is too low to completely switch it on, thereby avoiding excessive power dissipation. Leaving the VDD floating while supplying the PWM inputs leaves the output stage in an undefined state. The UVLO level is set to a typical value of 3.8 V for VDD and 3.2 V for HB-HS. The maximum value of the rising edge is the value that ensures all the device among the production will be turned on during startup; that means designers have to provide a voltage higher than 4.5 V for VDD and 3.9 V for HB-HS to turn on all the devices in the production of their equipment within the specified temperature range. On the opposite side, the minimum voltage necessary to switch off all the devices is the minimum of the falling edge. Therefore to be sure that all the devices in production will be turned off, in the specified temperature range, a voltage lower than 3.2 V for VDD and 2.5 V for HB-HS has to be provided. A 200 mV hysteresis is implemented on both supplies to ensure some margin on noise effect like false turn off. For instance, a negative glitch smaller than the hysteresis will not have an effect on the device preventing an unwanted turn off.

5.2.2 Input stage

The inputs LI and HI control two PWM channels. The input signal is transferred to the corresponding gate driver outputs HO and LO. All inputs are compatible with LV-TTL threshold levels and provide a hysteresis of typically 0.8 V. The hysteresis is independent of the supply voltage VDD. The PWM inputs are internally pulled down to a logic low voltage level (VSS). In case the PWM controller signals have an undefined state during the power-up sequence, the gate driver outputs are forced to the "off" state (low). Table 8 shows the truth table of the device once the two UVLOs are turned on. In case the VDD-VSS voltage or HB-HS voltage is below the UVLO threshold, the corresponding output will be low.

Table 8 Truth table

EN	LI	HI	LO	HO
L	L	L	L	L
	H	L	L	L
	L	H	L	L
	H	H	L	L
H	L	L	L	L
	H	L	H	L
	L	H	L	H
	H	H	H	H

5.2.3 Enable

The EN pin enables or disables the outputs of the driver. The outputs are active when the voltage at the EN pin is above the rising threshold and will be disabled when the EN pin voltage falls below the falling threshold. An internal 100 kΩ pull-up resistor connects EN pin to VDD thus leaving the EN pin floating enables the outputs. Externally pulling the EN pin to ground will disable the outputs. The EN input stage has built-in hysteresis for enhanced noise immunity.

5.2.4 Bootstrap switch and active bootstrap clamp

Generating the high-side supply voltage can be done via the internal bootstrap switch which is controlled by the low-side PWM. If the low-side PWM is high, the bootstrap switch is actively driven and if the low-side PWM is low, the bootstrap switch is not driven. In 2EDL5013U2D, an active bootstrap clamp feature is implemented where an internal switch disconnects the bootstrap switch from the VDD rail when the low-side PWM is low. This prevents the bootstrap capacitance from being overcharged during the deadtime.

5.2.5 Driver outputs

The strong peak current capability of 2 A source and 5 A sink for low-side output and 3 A source and 5 A sink for high-side output allows for faster switching of the power device thus leading to lower switching losses. The output impedance is very low with a typical value of 0.9 Ω (high-side) and 1.5 Ω (low-side) for the sourcing p-channel MOS and 0.5 Ω (high-side and low-side) for the sinking n-channel MOS transistor. The output is split to provide flexibility in adjusting the turn-on and turn-off strength independently. Gate drive outputs are held active low in case of floating inputs V_{HI}, V_{LI} or during startup or power down once UVLO is not exceeded. Under any situation, startup, UVLO or shutdown, outputs are held under defined conditions.

5.2.6 Active miller clamp

Active miller clamp feature is added on both the low-side and high-side output to provide immunity against induced turn-on caused by high dv/dt or high di/dt event. When the gate to source voltage falls below the miller clamp activation threshold of 0.5 V typical, the peak sink current increases to 7 A with an equivalent pull-down resistance of 0.40 Ω after a 5 ns activation delay time.

5.2.7 High voltage level shifter

The interface between the low voltage domain (e.g. high-side input signal which is referenced to VSS) to the high voltage domain, which is referenced to the HS node, is the level shifter. It allows control of the high-side output (HO) which is referenced to the switching node (HS). Having a low propagation delay while consuming less bias current are the desired characteristics of a level shifter especially for applications operating at very high switching frequency. In applications where the switch node (HS) goes negative (e.g. soft-switching), the turn-on propagation delay of the high-side output (HO) increases as the HS node becomes more negative. Figure 25 shows the variation of the high-side rising propagation delay against a static negative HS voltage at different bootstrap capacitor voltage and operating temperature. The minimum recommended negative HS voltage is -2 V. If this voltage is exceeded, the high-side output may not respond until the HS pin voltage returns within the recommended range. Refer to "Driving transistors with high reverse voltage drop (VSD)" under the application information section for additional information.

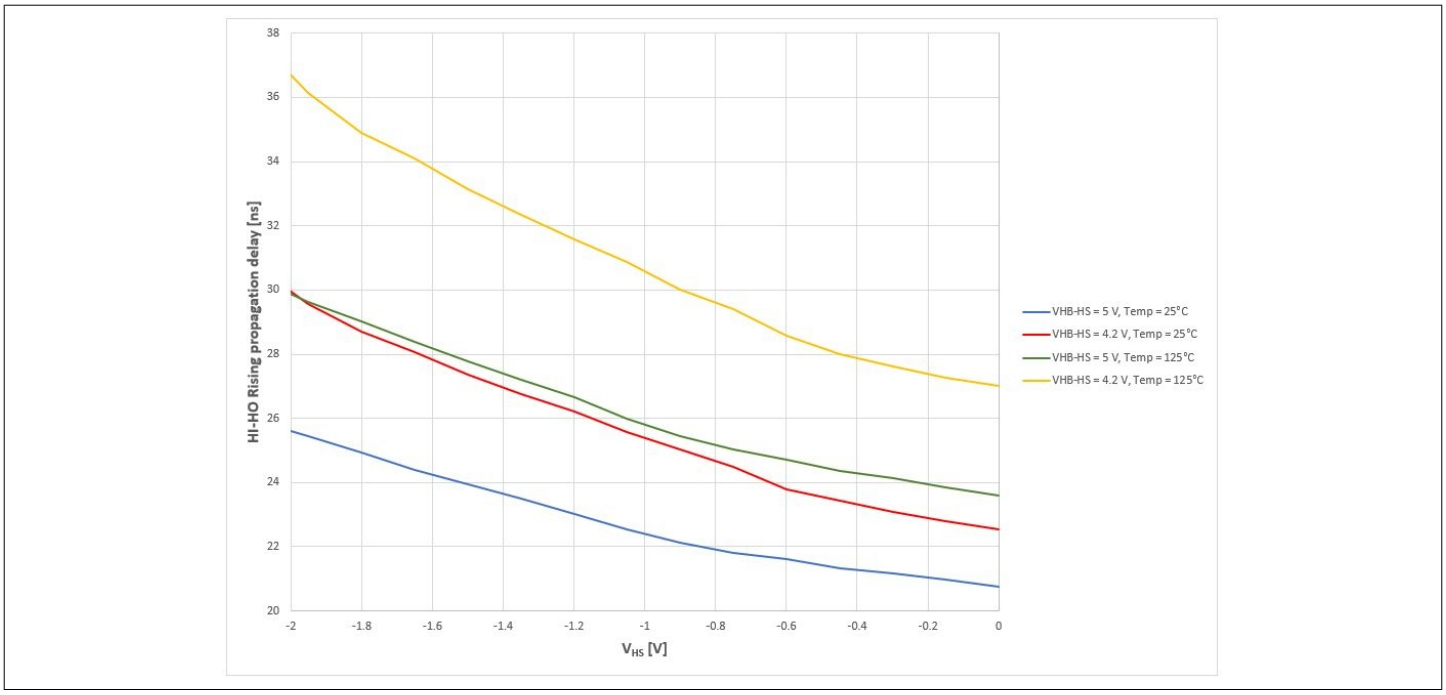


Figure 25 High-side rising propagation delay vs. negative HS voltage

5.2.8 Minimum ON time

The device responds to input level according to the truth table in the input stage section as long as the logic signal complies with the minimum pulse width requirement. Signal pulse longer than the minimum allowable input pulse yields valid output. Any output in response to shorter pulses or glitches should be disregarded and filtered out by the user. Under all allowable operation above the shortest input pulse width of 10 ns, the output behaves one to one to the input with minimal pulse width distortion.

6 Application information

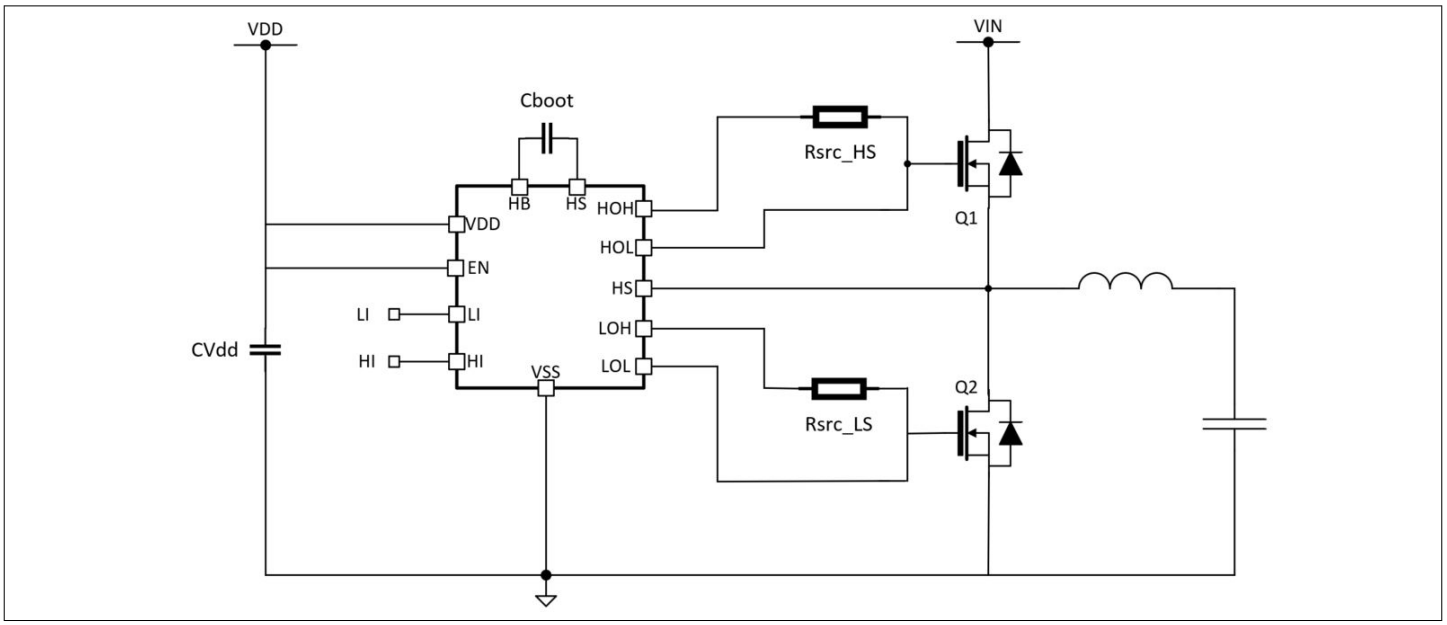


Figure 26 Typical application

6.1 Design guidelines

In a half-bridge configurations, a high-side bias which is referenced to the switch node is needed in order to drive the gate of the high-side transistor. One of the most common solutions due to its simplicity and low cost is the usage of a bootstrap circuit consisting of a bootstrap switch (internal to the driver) and a capacitor as seen in Figure 27. However, this method imposes limitation on the power converter's duty cycle due to the requirement of recharging the bootstrap capacitor. This limitation can be mitigated through the proper selection of the bootstrap components.

The bootstrap circuit operation is defined by two main periods:

Charging period: When the low-side transistor (Q2) is ON and the high-side transistor (Q1) is OFF, the switch node/HS pin is pulled to ground creating a charging path for the bootstrap capacitor (Cboot) through the *V*dd bypass capacitor (*C*Vdd) and the bootstrap switch (internal to the driver). For high dV/dt application, it is recommended to use an external bootstrap diode.

Discharging period: When the low-side transistor (Q2) is OFF and the high-side transistor (Q1) is ON, the switch node/HS pin is pulled to the high voltage *V*in thus for 2EDL5023U2D, since the bootstrap switch is not actively driven when the low-side PWM is low, the body diode of this bootstrap switch is reverse biased. While for 2EDL5013U2D, the bootstrap switch is disconnected from the V_{DD} rail. The bootstrap capacitor (*C*boot) will then discharge some of its stored charges to the gate of the high-side transistor as well as to other contributing factors such as the transistor's gate-source leakage current, floating section quiescent current, floating section leakage current and the bootstrap diode reverse bias leakage current.

Typical waveform for the voltage across *C*boot as a function of time is shown in Figure 28 where the various contributions have been distinguished. The voltage across *C*boot increases during the charging period and then it drops with a high negative dV/dt as it charges the gate of the high-side transistor (Q1). After which, the *C*boot voltage continues to drop but with a much lower slope because only the high-side bias current and some leakage current is discharing the *C*boot during this phase.

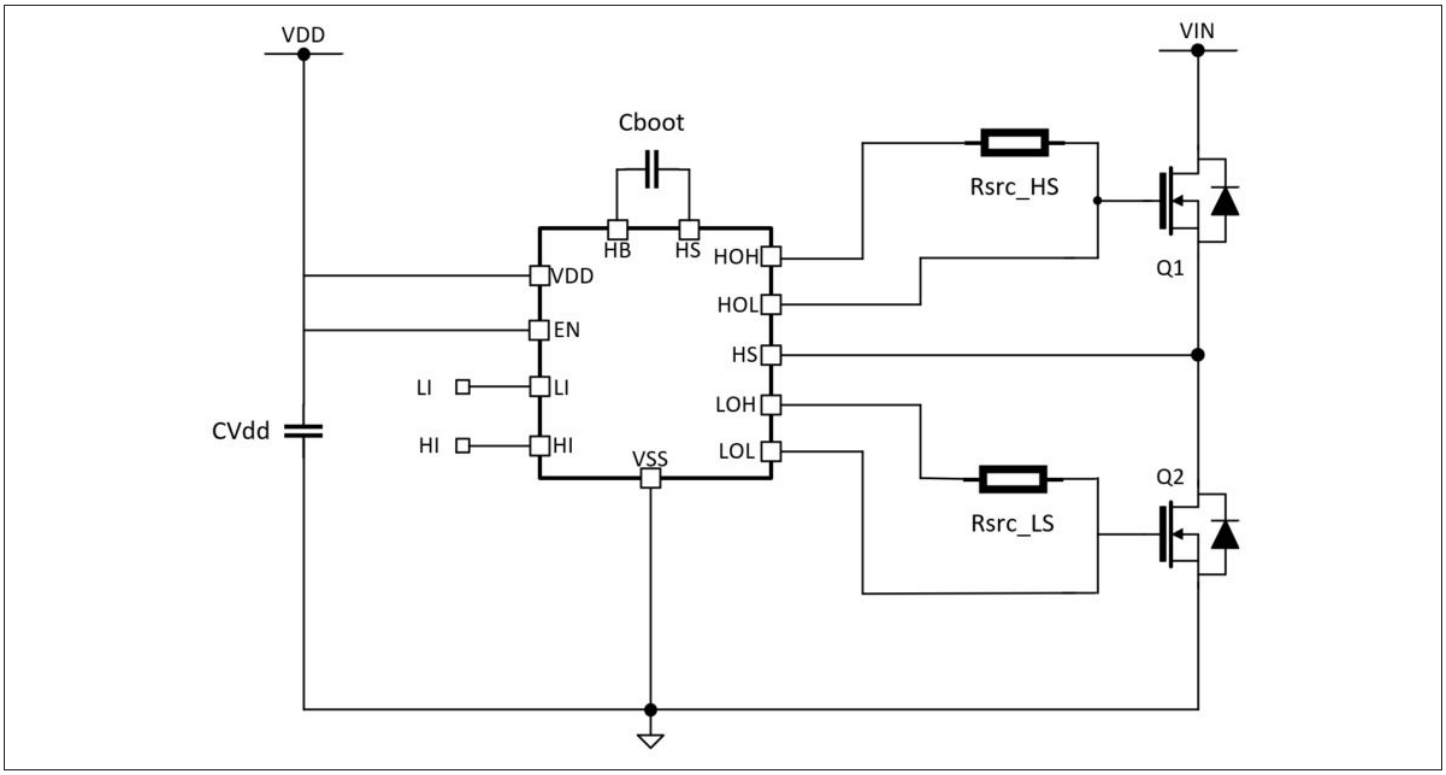


Figure 27 Gate drive circuitry to drive MOSFETs in a half-bridge configuration

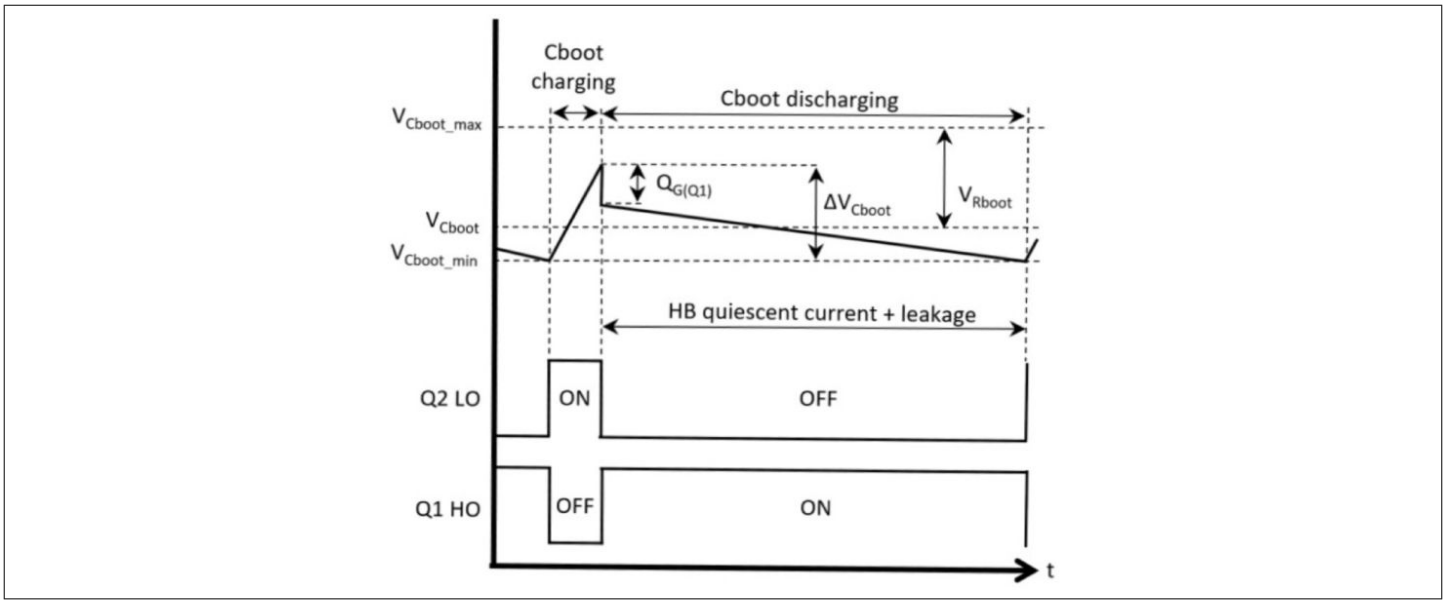


Figure 28 Typical C_{boot} waveform

6.1.1 Selection of bootstrap capacitor

The bootstrap capacitor provides the necessary charge to drive the high-side transistor and thus it needs to be sized in such a way that the maximum voltage drop across this capacitor will not fall below the high-side UVLO threshold during transient and normal operations. First, determine the maximum allowable voltage drop (ΔV_{Cboot_max}) when the high-side transistor (Q1) is on which is given by the following formula:

$$\Delta V_{Cboot\_max} = V_{dd} - V_F - V_{HBR} - V_{HBH} \quad (1)$$

Where:

V_{dd} = Gate driver supply voltage
V_F = Bootstrap switch forward voltage drop
V_{HBR} = HB UVLO rising threshold
V_{HBH} = HB UVLO threshold hysteresis

Next, determine the total charge (Q_{BOOT}) that must be delivered by the bootstrap capacitor at maximum duty cycle. As mentioned, there are several factors that contribute to the discharge of the bootstrap capacitor such as the Q1's total gate charge, Q1's gate-source leakage current, HB quiescent current, HB leakage current, bootstrap diode reverse bias leakage current and bootstrap capacitor leakage current (if using an electrolytic capacitor). For sake of simplicity, only Q1's total gate charge and HB quiescent and leakage current are considered as the other sources of leakage are negligible in comparison.

$$Q_{BOOT} = Q_G + \left(\frac{I_{HB}}{F_{sw}} + I_{HBS}\right) \times \frac{D_{max}}{F_{sw}} \quad (2)$$

Where:

Q_G = high-side transistor (Q1) total gate charge
I_{HB} = HB maximum quiescent current
I_{HBS} = HB to VSS leakage current
D_{max} = maximum duty cycle
F_{sw} = switching frequency

The minimum bootstrap capacitor value can then be calculated using the formula:

$$C_{boot\_min} \geq \frac{Q_{BOOT}}{\Delta V_{Cboot\_max}} \quad (3)$$

6.1.2 Selection of VDD bypass capacitor

The V_{dd} bypass capacitor provides the gate charge (Q_G) to drive the transistors, as well as additional power consumption by the driver itself. It should be placed as close as possible to the VDD and VSS pins of the gate driver. The minimum value for this bypass capacitor can be calculated based on the maximum allowable voltage ripple (ΔV_{dd_max}) in the design. This ripple should be minimized such that the lowest possible V_{dd} is above the UVLO limit of the gate driver as well as above the safe driving voltage of the transistor. In a half-bridge configuration, the V_{dd} bypass capacitor also provides the charge (Q_{BOOT}) for the bootstrap capacitor during the charging period. Therefore, it should be sized to be much larger than the bootstrap capacitor. The minimum value can be calculated as

$$C_{Vdd} \gg \frac{Q_G + Q_{BOOT}}{\Delta V_{dd\_max}} \quad (4)$$

In practice, this capacitance value should be increased somewhat to account for dc bias effects in the capacitor and other non-idealities in the circuit.

6.1.3 Selection of bootstrap resistor

The bootstrap resistor limits the current in the bootstrap switch during start-up when the bootstrap capacitor is initially completely discharged. The peak current through this resistor is given by:

$$I_{Pk\_Rboot} = \frac{V_{dd} - V_F}{R_{boot}} \quad (5)$$

The bootstrap resistor together with the bootstrap capacitor introduces a time constant and should be sized appropriately to achieve the desired start-up time. For this calculation, it is assumed that the bootstrap capacitor is fully charged after 4 time constant. With this, R_{boot} can be calculated using the following formula:

$$R_{boot} \leq \frac{t_{min}}{4 \times C_{boot}} \quad (6)$$

Where:

t_{min} = minimum on time of the low-side transistor (Q2)

6.1.4 Selection of external bootstrap diode

The 2EDL50X3U2D has an integrated bootstrap switch for charging the bootstrap capacitor. The 2EDL5013U2D has an active bootstrap clamp feature to avoid overcharging the bootstrap capacitor. Therefore, it is not recommended to use an external bootstrap diode if this feature is needed unless there is an external circuit that can regulate the bootstrap capacitor voltage. If an external bootstrap diode is needed in the application such as when operating at very high switching frequency or with large high-side gate charge requirement, a fast recovery or Schottky diode with low forward voltage drop is recommended in order to minimize the losses and leakage current. It should be chosen such that it can handle the peak transient current from Equation (5) during start-up conditions and the blocking voltage rating should be higher than the maximum input voltage (V_{in}) with enough derating. Figure 29 shows the variation of the bootstrap capacitor voltage against the switching frequency with 1 nF load at different V_{DD} voltage.

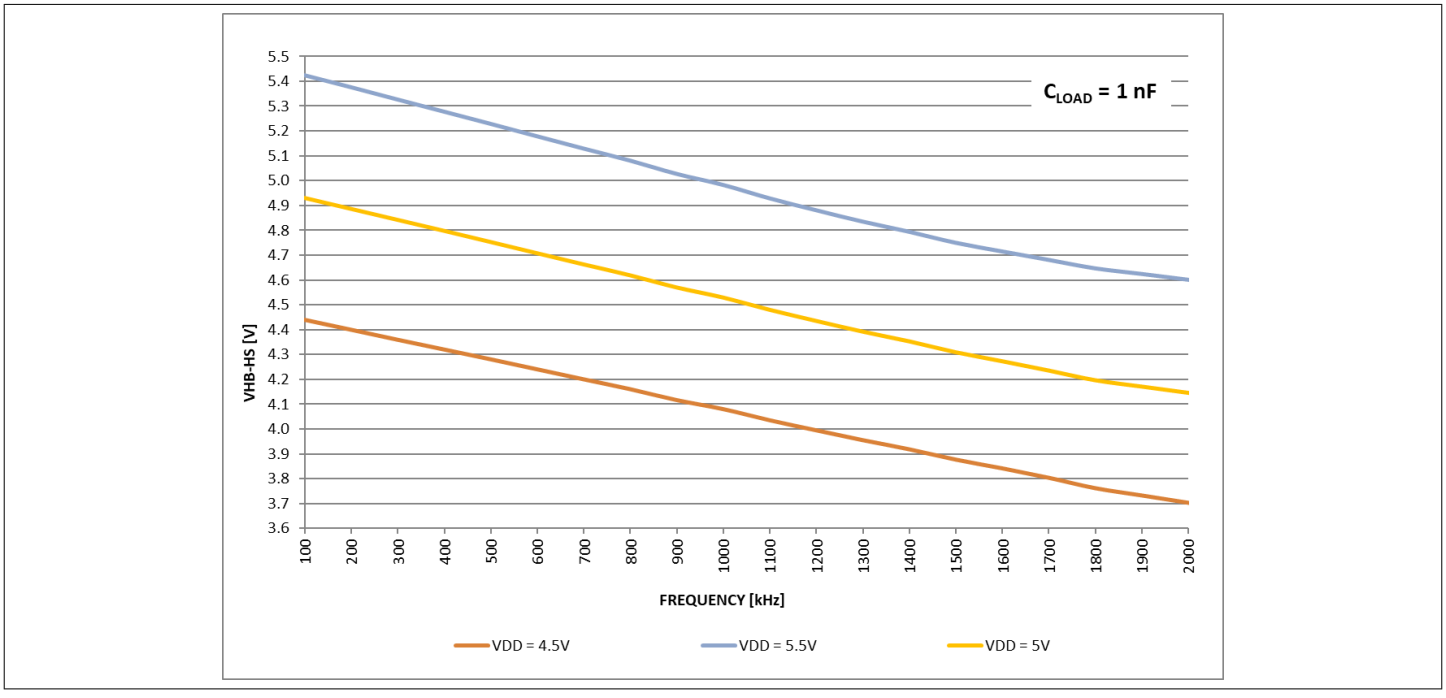


Figure 29 Bootstrap capacitor voltage (V_{HB-HS}) vs. switching frequency (F_{SW})

6.1.5 Selection of gate resistor

The turn-on and turn-off external gate resistors control the turn-on and turn-off current of the gate driver providing an external way to control the switching speed of the transistor for purposes such as voltage overshoot control, ringing reduction, EMI mitigation, spurious turn-on protection, shoot –through protection etc. The following formulas show the effect of the external gate resistor to the output current capability of the gate driver.

$$I_{HSRC} = \frac{V_{dd} - V_F}{R_{PUH} + R_{G\_HS} + R_{G\_int}} \quad (7)$$

$$I_{HSNK} = \frac{V_{dd} - V_F}{R_{PDH} + R_{G\_HS} + R_{G\_int}} \quad (8)$$

$$I_{LSRC} = \frac{V_{dd}}{R_{PUL} + R_{G\_LS} + R_{G\_int}} \quad (9)$$

$$I_{LSNK} = \frac{V_{dd}}{R_{PDL} + R_{G\_LS} + R_{G\_int}} \quad (10)$$

Where:

I_{HSRC} = High-side peak source current
I_{HSNK} = High-side peak sink current
I_{LSRC} = Low-side peak source current
I_{LSNK} = Low-side peak sink current
R_{PUH} = High-side pull-up resistance
R_{PDH} = High-side pull-down resistance
R_{PUL} = Low-side pull-up resistance
R_{PDL} = Low-side pull-down resistance
V_{dd} = Gate driver supply voltage
V_F = Bootstrap switch forward voltage drop
R_{G_HS} = High-side external gate resistance
R_{G_LS} = Low-side external gate resistance
R_{G_int} = MOSFET internal gate resistance

It is important to consider that the peak current may not reach this level during a fast switching transition. It is also worth noting that this peak current cannot exceed the specified peak source/sink current of the gate driver, as the pull-up and pull-down transistors within the driver saturate at that current. The use of an external gate resistor in the sink path is not recommended for most designs as this will limit the effectiveness of the active miller clamp feature.

6.1.6 Driving transistors with high reverse voltage drop (VSD)

When using 2EDL50X3U2D, care must be taken to limit the negative voltage applied on the HS pin especially during deadtime. As discussed in the product information section under "High voltage level shifter", the high-side output turn-on propagation delay increases with a more negative HS voltage. When the HS pin voltage exceeds the minimum recommended -2 V, the high-side output may not respond until the HS pin returns to a voltage within the recommended range. It is therefore not recommended to use this driver to drive devices with a reverse voltage exceeding 2 V (e.g. GaN HEMTs), unless an external Schottky diode is placed antiparallel to the low-side device to clamp the HS pin within the recommended range. When used with a GaN HEMT on the low-side, the reverse voltage (V_{SD}) observed in "body diode" operation during deadtime may vary due to part-to-part tolerance, as well as changes in current (I_{SD}) and temperature. This variation may cause jitter in high-side switching or loss of functionality when V_{SD} exceeds 2 V. Refer to "High voltage level shifter" under the product information section for additional information.

6.1.7 Driving HI and LI with the same PWM state

The 2EDL50X3U2D has two independent inputs but due to the way that the bootstrap switch is controlled, driving the two inputs with the same PWM state is not recommended when used in a full-bridge or similar topology with diagonal driving configuration. Consider the full-bridge circuit in Figure 30, if both HI and LI are driven low at the same time, for 2EDL5013U2D there is no charging path for the bootstrap capacitor since the bootstrap switch will be disconnected from the V_{DD} rail when LI is low. For 2EDL5023U2D, charging of the bootstrap capacitor is through the body diode of the bootstrap switch since it is not actively driven when LI is low. If both HI and LI are driven high at the same time, reverse current will flow from HB pin to VDD pin for both variants since the bootstrap switch is turned ON when LI is high.

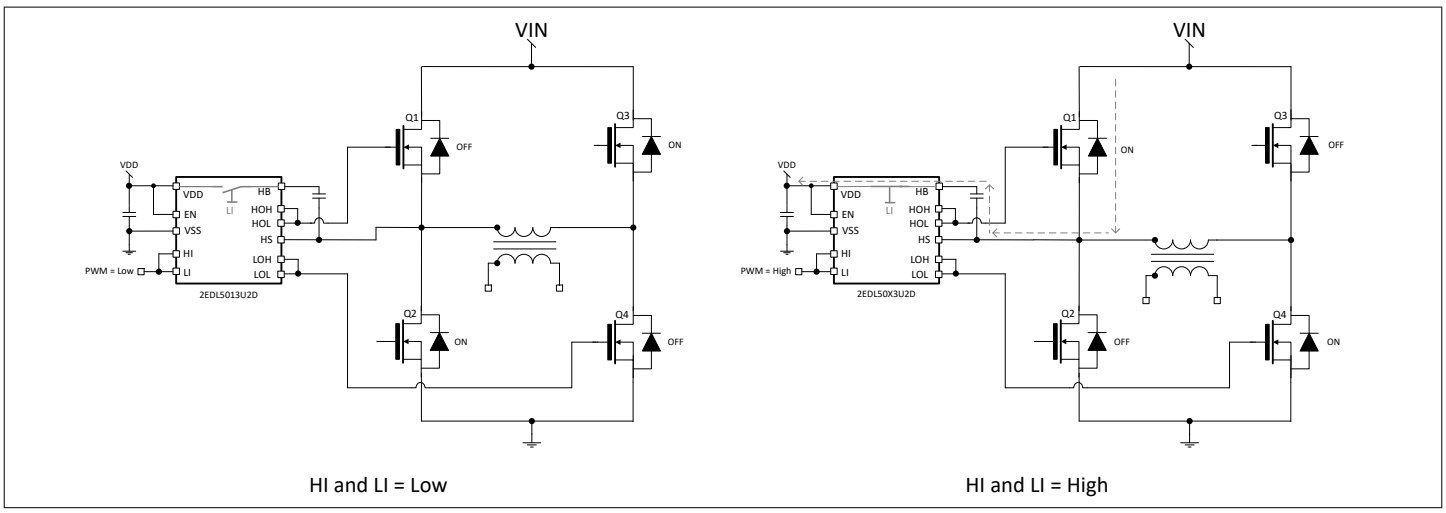


Figure 30 Full-bridge circuit with diagonal driving configuration

6.2 PCB Layout guidelines

The EiceDRIVER™ 2EDL50X3U2D is offered in a low inductance TSNP package which is beneficial for fast switching applications, as it reduces the parasitic inductance on the gate drive loop. In order to fully maximize the performance of 2EDL50X3U2D, below are some recommendations on how to optimize the PCB layout:

- Minimize the gate loop inductance by placing the driver as close as possible to the switching transistors.
- Use a low-ESR decoupling capacitors on VDD-GND and HB-HS and placed it as close as possible to the VDD-GND and HB-HS pins of the driver. If possible, place the decoupling capacitors on the same side of the PCB as the driver.
- All high current traces (LOL, LOH, HOL, HOH, VDD, HB, HS and VSS) should be as short and wide as possible and copper pours are recommended over traces when the design allows.
- Connection to the HS pin of the driver from the high-side transistor source and low-side transistor drain should be as short and wide as possible to reduce the parasitic inductance which can cause excessive negative transient voltage on the driver. Also, avoid connecting the HS pin directly through the high-side transistor switching current path. Same rules will apply when connecting the VSS pin of the driver to the source of the low-side transistor.

- To optimize heat spreading, electrical shielding and magnetic field cancellation, a VSS-connected copper plane should be placed directly underneath the IC (PCB layer directly below the IC) as well as all components encompassed by the gate driving loop (e.g. bypass capacitors, gate and source pads of the transistors).
- To avoid interference between the power loop and gate loops, separate shielding layers should be used for each loop, even if they are both connected to the same net.
- It is not recommended to put an external gate resistor in the sink path (LOL and HOL) as this will limit the effectiveness of the active miller clamp feature.

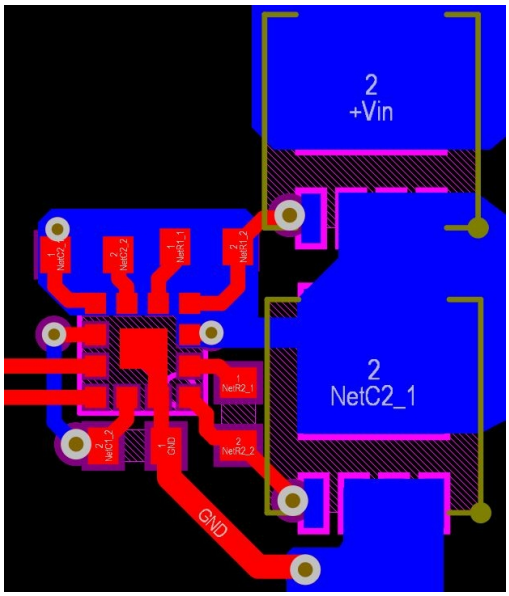


Figure 31 2EDL50X3U2D Layout example in a half-bridge configuration

7 Outline dimensions

For further information on package types, recommendation for board assembly, please go to: www.infineon.com\packages

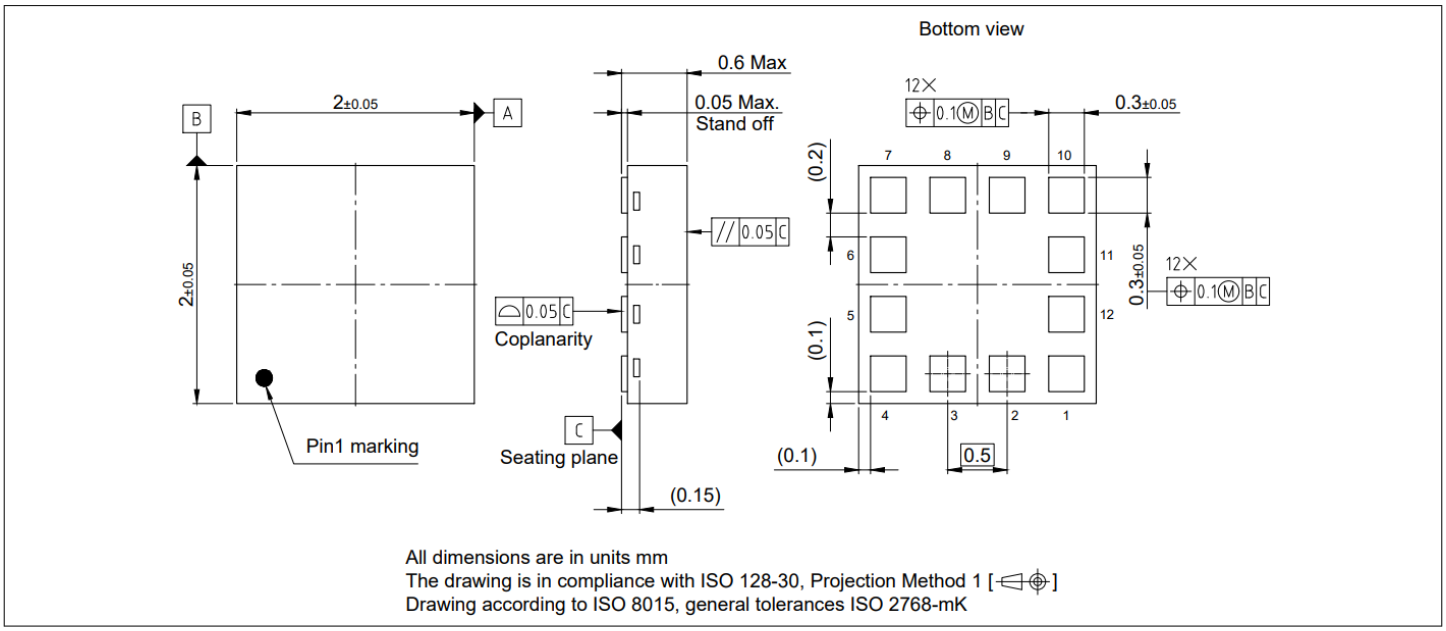


Figure 32 PG-TSNP-12-5 Outline dimensions

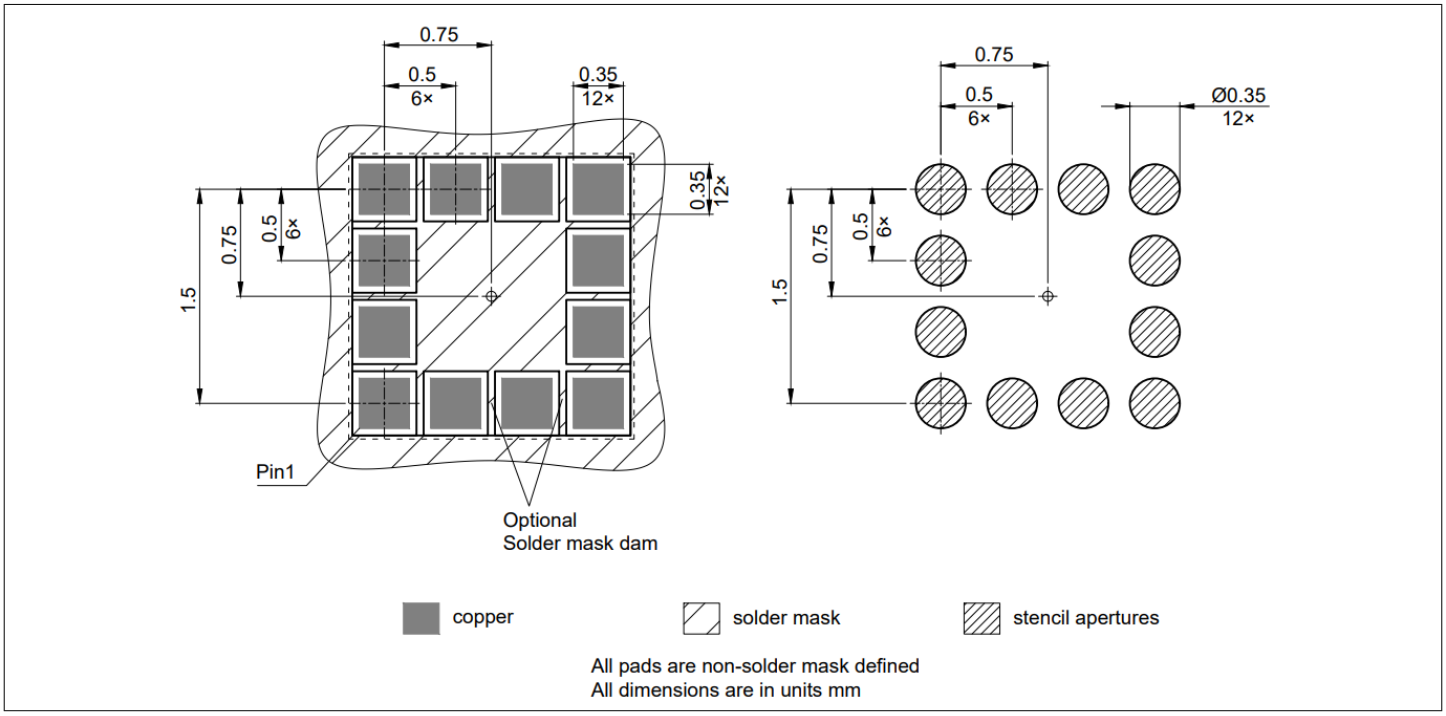


Figure 33 PG-TSNP-12-5 Footprint dimensions

8 Tape and reel

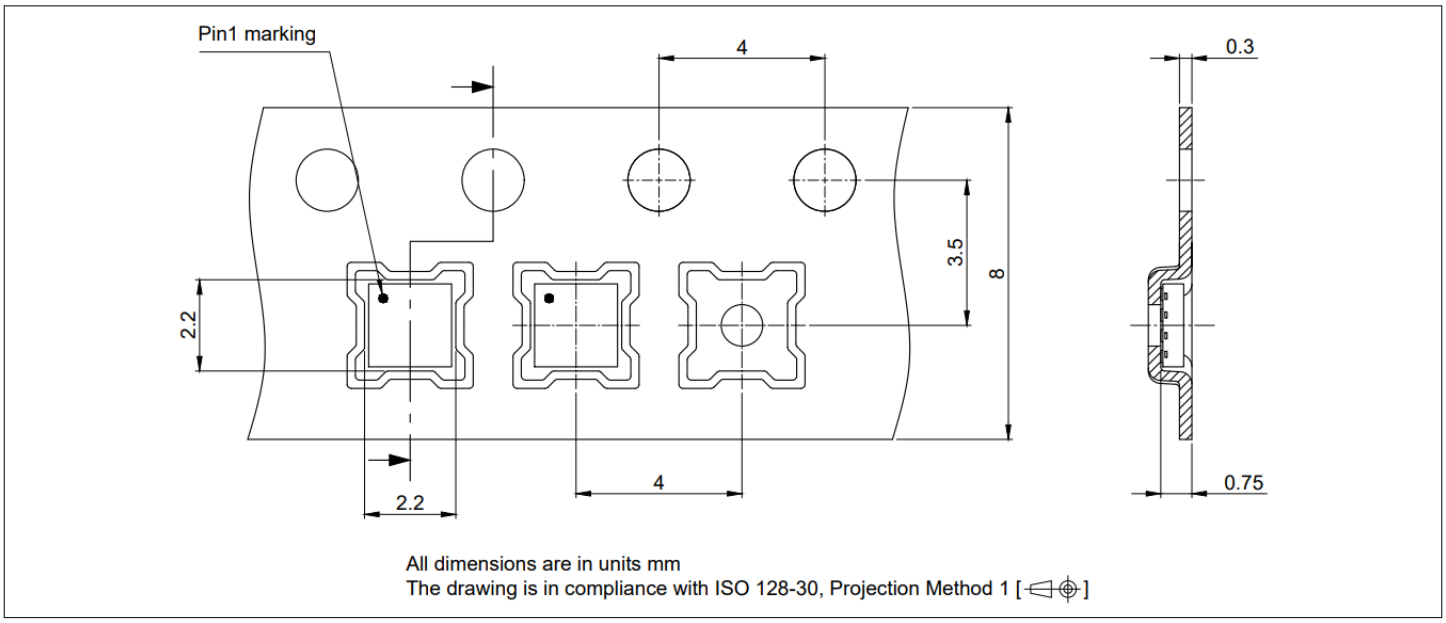


Figure 34 PG-TSNP-12-5 Tape and reel

Revision History

2EDL50x3U2D

Revision 2024-10-07, Rev. 2.2

Previous Revision

Revision	Date	Subjects (major changes since last revision)
2.0	2023-08-08	Release of final version
2.1	2023-12-19	Update ESD_HBM ratings, LO and HO typical rise and fall time, and remove max limit. Modify list of potential applications.
2.2	2024-10-07	Update feature list and description in cover page, description related to bootstrap switch, block diagram and application information section.

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