

Low Noise, Precision Voltage Operational Amplifier

Features

- Low Offset Voltage: 50 μ V Maximum
- Low Drift: 0.5 μ V/ $^{\circ}$ C Maximum
- 8MHz gain bandwidth
- Excellent CMRR and PSRR
- Wide Supply Range: $\pm 2.25\text{V} \sim \pm 18\text{V}$
- Low Quiescent Current: 1.7mA
- Input Over-Voltage Protection
- Available as SOP8, MSOP8, DIP8 package

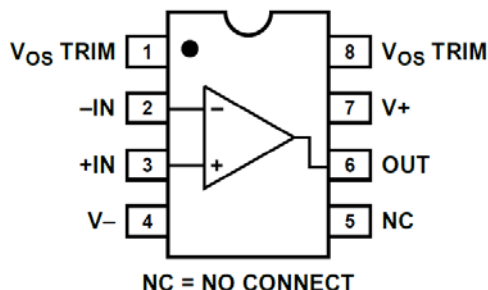
Applications

- Sensors and controls
 - Thermocouples
 - Resistor thermal detectors (RTDs)
 - Strain bridges
 - Shunt current measurements
- Precision filters
- Data acquisition
- Medical instrumentation
- Optical network control circuits
- Wireless base station control circuits

General Description

The OP27 has very low input offset voltage (50 μ V) maximum that is obtained by trimming at the wafer stage. These low offset voltages generally eliminate any need for external nulling. The OP27 also features low input bias current and high open-loop gain. The low offset and high open-loop gain make the OP27 particularly useful for high gain instrumentation applications. The wide input voltage range combined with a high CMRR of 106 dB and high input impedance provide high accuracy in the noninverting circuit configuration. Excellent linearity and gain accuracy can be maintained even at high closed-loop gains. Stability of offsets and gain with time or variations in temperature is excellent. The accuracy and stability of the OP27, even at high gain, combined with the freedom from external nulling have made the OP27 an ideal choice for instrumentation applications. The OP27 is available in epoxy 8-lead PDIP and 8-lead narrow SOP and MSOP packages.

1.0 Pin Configuration and Functions



Pin	Name	Description
1,8	Vos TRIM	Optional, place a offset nulling resistor (e.g. 20kΩ) between pin1 & 8
2	-IN	Negative input
3	+IN	Positive input
4	V-	Negative supply
5	NC	No connection
6	OUT	Output
7	V+	Positive supply

2.0 Product Specification

2.1 Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Parameter	Min	Max	Unit
DC supply voltage Vs		±18	V
Operating junction temperature	-40	85	°C
Storage temperature	-55	125	°C
Maximum input voltage		±18	V
Differential Input voltage		±18	V

2.2 Thermal Data

Parameter	Rating	Unit
Package Thermal Resistance	155(SOP8) 206(MSOP) 125(DIP8)	°C/W

2.3 Recommended Operating Conditions

Parameter	Rating	Unit
DC Supply Voltage	$\pm 2.25\text{V} \sim \pm 18\text{V}$	V
Input common-mode voltage range	$(V_-)+2 \sim (V_+)-2$	V
Operating ambient temperature	-40 to +85	°C

2.4 Electrical Characteristics

(Typical values are tested at $T_A=25^\circ\text{C}$, $V_S=\pm 15\text{V}$)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input Offset Voltage	V_{IO}		-	± 15	± 50	μV
Input Offset Voltage Drift	TC			0.1	0.6	$\mu\text{V}/^\circ\text{C}$
Input Offset Current	I_{IO}		-	± 7	± 35	nA
Input Bias Current	I_{BIAS}		-	± 10	± 40	nA
Operating Current	I_{CC}		-	2.0	2.5	mA
Common Mode Input Voltage Range	V_{ICM}		± 13	± 14	-	V
Common Mode Rejection Range	CMRR		70	115	-	dB
Power Supply Rejection Ratio	PSRR		80	120	-	dB
Output Voltage Swing	$V_{O(P-P)}$	$R_L \geq 10\text{k}\Omega$	± 12	± 13.8	-	V
Short Circuit Current	I_{SC}		-	± 28	-	mA
Gain Bandwidth Product	GBW	$C_L = 100\text{pF}$, $R_L = 10\text{k}\Omega$	-	8.0	-	MHz
Slew Rate	SR	$C_L = 100\text{pF}$, $R_L = 10\text{k}\Omega$, $A_v = 1$	-	3.0	-	V/ μs
Input Noise Voltage	e_N	$f = 1\text{kHz}$	-	3.0	-	nV/ $\sqrt{\text{Hz}}$

3.0 Typical Test Circuits

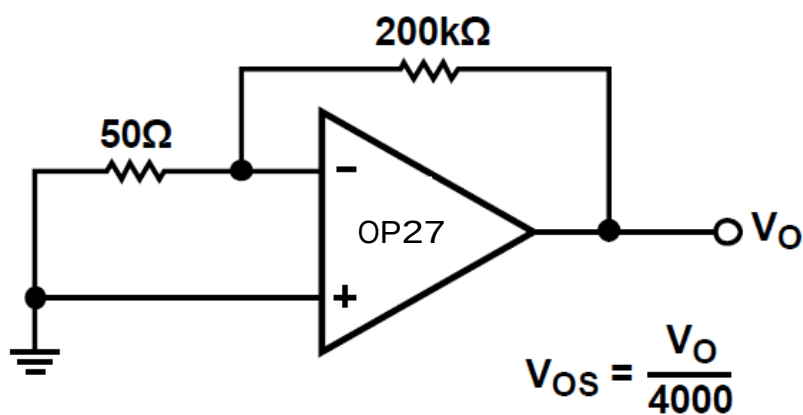


Figure 3.1 Typical Offset Voltage Test Circuit

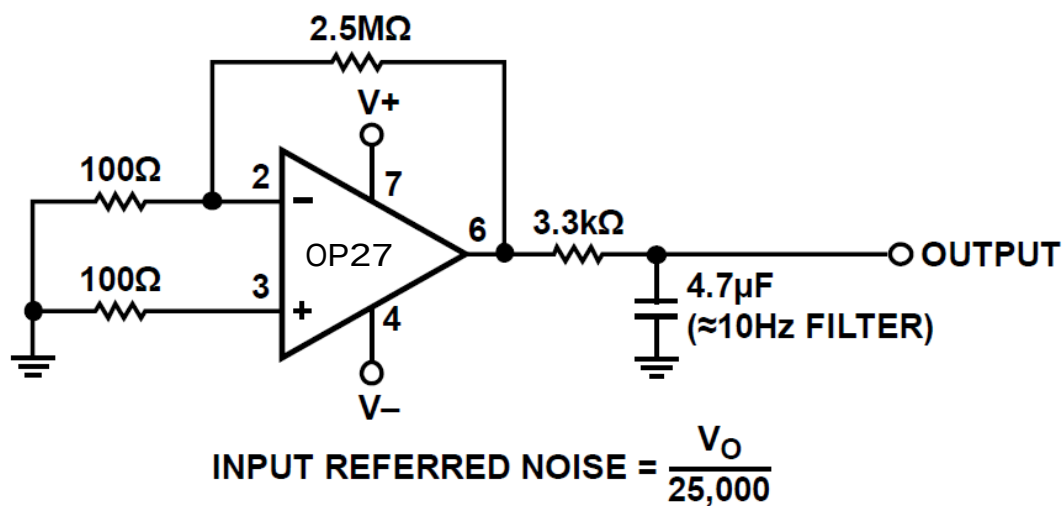


Figure 3.2 Typical Low Frequency Noise Test Circuit

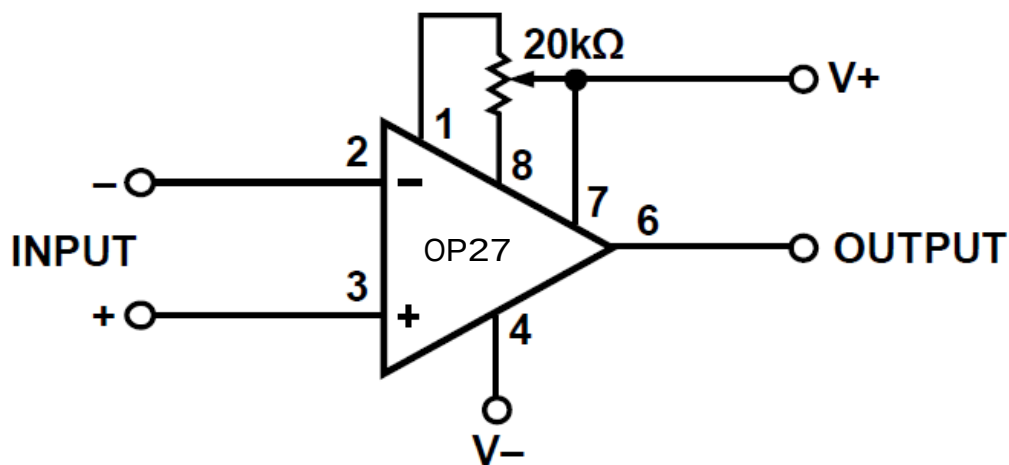


Figure 3.3 Optional Offset Nulling Circuit

4.0 Basic Application Circuits

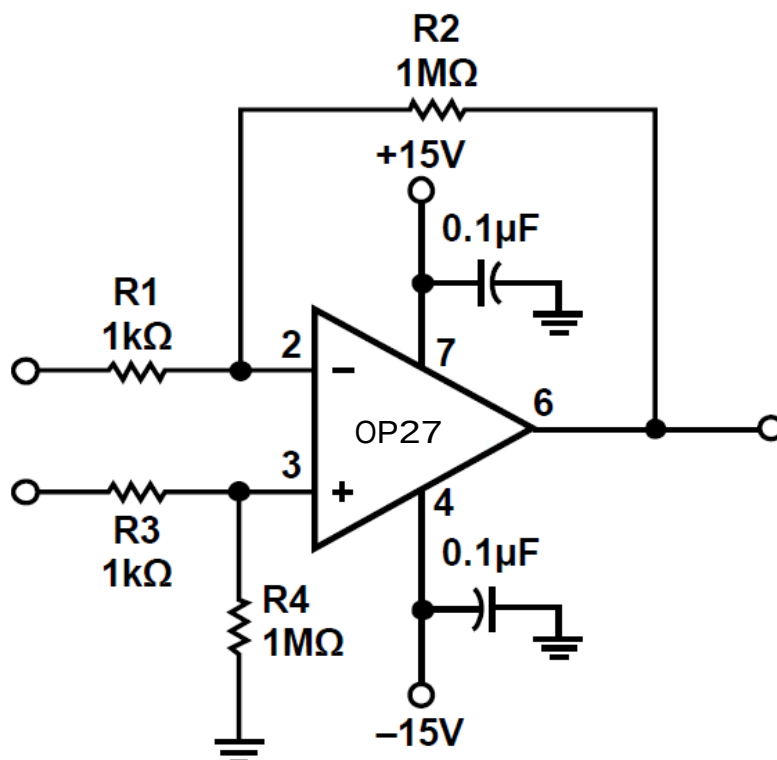


Figure 4.1 Precision High Gain Differential Circuit

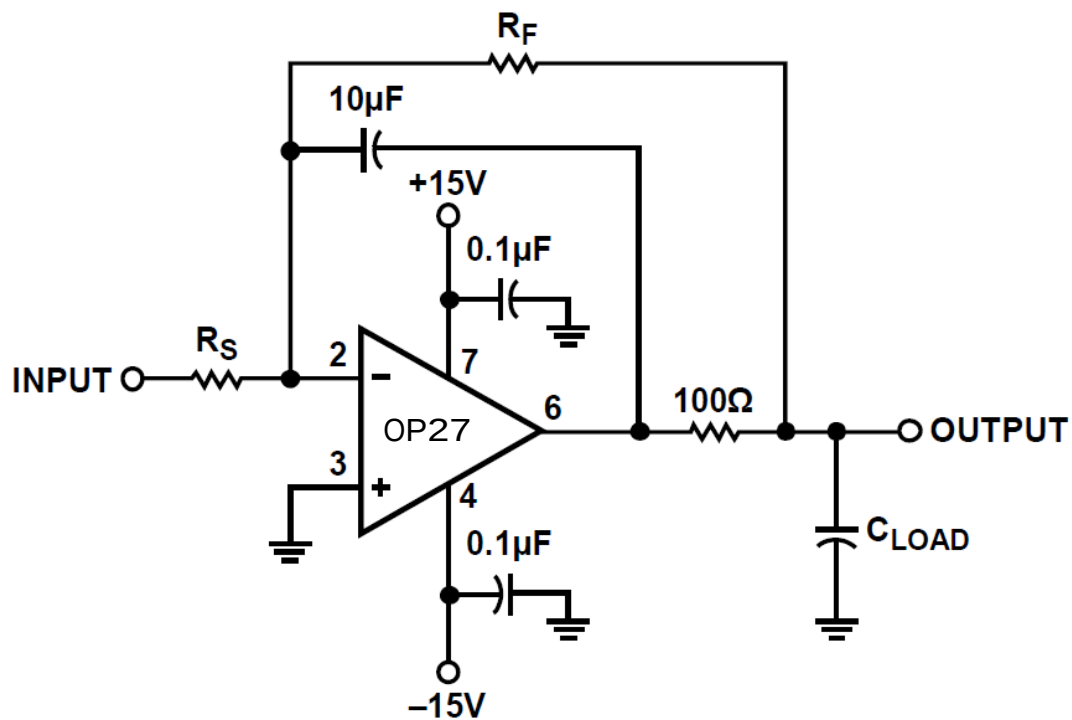


Figure 4.2 Isolating Large Capacitive Loads

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