DATA SHEET

# GRF2583

## LNA with Selectable Gain 5.8 to 6 GHz

PRELIMINARY DATA SHEET

### FEATURES

- Two Selectable Gain Modes: 27.2 & 15 dB
- 2.7 to 6 V Supply Voltage
- Flexible Biasing Provides Latitude for Linearity Optimization
- 52 mA Native Mode Quiescent Current Consumption
- 50 Ω Single-Ended Input and Output Impedances
- RoHS Compliant

**Reference: High Gain Mode 5 V / 52 mA / 5.9 GHz**

- Gain: 27.2 dB
- OP1dB: 16 dB
- OIP3: 33 dBm
- Evaluation Board NF: 1.2 dB

**Reference: Low Gain Mode 5 V / 15 mA / 5.9 GHz**

- Gain: 15 dB
- OP1dB: 10 dBm
- OIP3: 21.2 dBm
- Evaluation Board NF: 1.25 dB

### APPLICATIONS

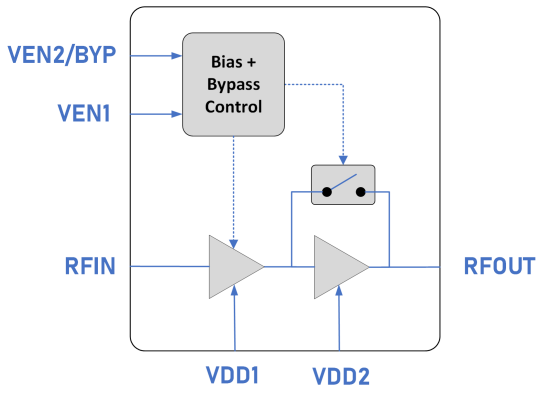
- Automotive V2X Band
- n47 Front Ends and Compensators
- High-Performance RF Infrastructure

### DESCRIPTION

The GRF2583 is a two-stage GaAs pHEMT low noise amplifier targeting high-performance wireless infrastructure applications. The second stage can be bypassed with an independent control pin, thus allowing the device to support high and low gain modes of 27.2 and 15.2 dB, respectively.

For optimal efficiency and linearity, the amplifier was designed to operate with a single 5 V supply voltage while using only 52 mA of quiescent current. Supply voltages ranging from 2.7 to 6 volts are also supported. Similarly, quiescent current can be increased beyond the native biasing point for enhanced linearity performance.

### BLOCK DIAGRAM







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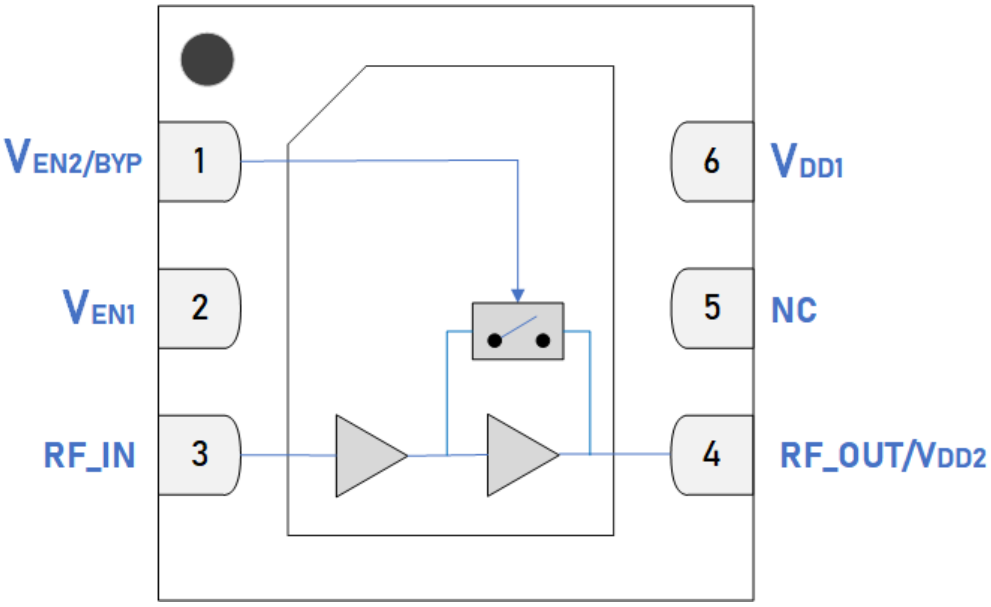



**Pin Out (Top View)**

## Pin Assignments

| Pin | Name | Description | Note |
|---|---|---|---|
| 1 | $V_{EN2/BYP}$ | 2nd Stage Enable/Bypass | $V_{EN2/BYP} \leq 0.2$ volts sets Bypass Mode. $V_{EN2/BYP}$ and external series resistor controls the second stage $I_{DDQ}$ when $V_{EN2/BYP}$ is high. |
| 2 | $V_{EN1}$ | 1st Stage Enable | $V_{EN1} \leq 0.2$ disables the first stage. $V_{EN1}$ and external series resistor control the first stage $I_{DDQ}$ when $V_{EN1}$ is high. |
| 3 | RF_IN | RF Input | Internally matched 50 Ω. An external DC blocking cap must be used. |
| 4 | RF_OUT/$V_{DD2}$ | RF Output/2nd Stage Bias | Internally matched 50 Ω. $V_{DD}$ must be applied through a choke to this pin. |
| 5 | NC | No Connect | No internal connection. This pin can be left unconnected, or be connected to the ground (recommended). Use a via as close to the pin as possible if grounded. |
| 6 | $V_{DD1}$ | 1st Stage Bias | Pull up to $V_{DD}$ through the inductor and use bypass capacitors as close to the pin as possible. In addition to supplying the first stage of the device with a DC voltage, there is also an RF signal present. |
| PKG BASE | GND | Ground | Provides DC and RF ground for amplifiers, as well as thermal heat sink. In order to match the device's rated performance, it is strongly recommended to use multiple 8mil vias beneath the package for optimal RF and thermal performance. Refer to evaluation board top layer graphic on schematic page. |

## Absolute Ratings

| Parameter | Symbol | Min. | Max. | Unit |
|---|---|---|---|---|
| Supply Voltage | $V_{DD}$ | 0 | 6 | V |
| RF Input Power: Load VSWR < 2:1, $V_{DD}$ < 6 V. | $P_{IN\ MAX}$ | | 22 | dBm |
| Operating Temperature (Package Heat Sink) | $T_{PKG\ BASE}$ | -40 | 115 | °C |
| Maximum Channel Temperature (MTTF > $10^6$ Hours) | $T_{MAX}$ | | 170 | °C |
| Maximum Dissipated Power | $P_{DISS\ MAX}$ | | TBD | W |
| **Electrostatic Discharge** | | | | |
| Human Body Model | HBM | TBD | | V |
| **Storage** | | | | |
| Storage Temperature | $T_{STG}$ | -65 | 150 | °C |
| Moisture Sensitivity Level | | | 1 | -- |

**Caution! ESD Sensitive Device.**

**Exceeding Absolute Maximum Rating conditions may cause permanent damage.**

Note: For additional information, please refer to Manufacturing Note MN-001 - Packaging and Manufacturing Information.

All Guerrilla RF products are provided in RoHS compliant lead (Pb)-free packaging. For additional information, please refer to the Certificate of RoHS Compliance.

## Recommended Operating Conditions

| Parameter | Symbol | Specification | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply Voltage | $V_{DD}$ | 2.7 | 5 | 5.25 | V | |
| Operating Temperature Range | $T_{PKG\ BASE}$ | -40 | | +115 | °C | |
| RF Frequency Range | $F_{RF}$ | 5.8 | 5.9 | 6 | GHz | 5.9 GHz tuning set **(note 1)**. |
| RF_IN Port Impedance | $Z_{RFIN}$ | | 50 | | Ω | Single ended, with respective matching elements from each tuning set. |
| RF_OUT Port Impedance | $Z_{RFOUT}$ | | 50 | | Ω | Single ended, with respective matching elements from each turning set. |

**Note 1:** Operation outside of this range is possible but with the degraded performance of some parameters.

## Nominal Operating Parameters - General

| Parameter | Symbol | Specification | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| $V_{EN1}$, $V_{EN2}$ Input Voltage Logic Levels | $V_{IL}$ | 0 | | 0.2 | V | Applies to $V_{EN1}$ and $V_{EN2/BYP}$ inputs. |
| | $V_{IH}$ | 1.5 | | $V_{DD}$ | V | Applies to $V_{EN1}$ and $V_{EN2/BYP}$ inputs. |
| $V_{EN1}$ Input Logic Current | $I_{IH-VEN1}$ | | 0.86 | | mA | $V_{EN1}$ = 5 V (Logic HIGH). $V_{EN2/BYP}$ = 5 V (Logic HIGH). |
| | $I_{IL-VEN1}$ | | 0.85 | | mA | $V_{EN1}$ = 0 V (Logic LOW). $V_{EN2/BYP}$ = 0 V (Logic LOW). |
| $V_{EN2}$ Input Logic Current | $I_{IH-VEN2}$ | | 1.65 | | mA | $V_{EN1}$ = 5 V (Logic HIGH). $V_{EN2/BYP}$ = 5 V (Logic HIGH). |
| | $I_{IL-VEN2}$ | | 0 | | mA | $V_{EN1}$ = 5 V (Logic HIGH). $V_{EN2/BYP}$ = 0 V (Logic LOW). |
| | | | 0 | | mA | $V_{EN1}$ = 0 V (Logic LOW). $V_{EN2/BYP}$ = 0 V (Logic LOW). |
| $V_{EN1}$ Switching Rise Time | $t_{VEN1-RISE}$ | | 50 | | ns | Turn ON time ($V_{EN1}$ Low to High, **note 2**). |
| $V_{EN1}$ Switching Fall Time | $t_{VEN1-FALL}$ | | 50 | | ns | Turn OFF time ($V_{EN1}$ High to Low, **note 3**). |
| $V_{EN2/BYP}$ Switching Rise Time | $t_{GAIN-RISE}$ | | 50 | | ns | Low to High gain mode switching ($V_{EN2/BYP}$ Low to High, **note 4**). |
| $V_{EN2/BYP}$ Switching Fall Time | $t_{GAIN-FALL}$ | | 50 | | ns | High to Low gain mode switching ($V_{EN2/BYP}$ High to Low, **note 5**). |

## Nominal Operating Parameters - General (continued)

### Disabled Mode

| | | | | | | |
|---|---|---|---|---|---|---|
| Standby Current | $I_{STBY}$ | | 675 | | µA | $V_{DD}$ = 5 V, $V_{EN1}$ = Low, $V_{EN2/BYP}$ = Low. |

### Thermal Data

| | | | | | | |
|---|---|---|---|---|---|---|
| Thermal Resistance (Infrared Scan) | $\theta_{JC}$ | | TBD | | °C/W | On Standard Evaluation Board. |
| Channel Temp @ +115 °C (Reference Package Heat Sink) | $T_{CHANNEL}$ | | TBD | | °C | $V_{DD}$ = 5 V, $I_{DDQ}$ = 66 mA, $P_{DISS}$ = TBD. No RF applied **(note 6).** |

**Note 2:** Switching Rise Time: 50% of $V_{EN1}$ to 90% of $P_{OUT}$.

**Note 3:** Switching Fall Time: 50% of $V_{EN1}$ to 10% of $P_{OUT}$.

**Note 4:** Switching Rise Time: 50% of $V_{EN2/BYP}$ to 90% of $P_{OUT}$.

**Note 5:** Switching Fall Time: 50% of $V_{EN2/BYP}$ to 10% of $P_{OUT}$.

**Note 6:** MTTF > $10^6$ hours for $T_{CHANNEL}$ < 170 °C.

# Nominal Operating Parameters - RF

## 5.9 GHz, 5 V Supply, High Gain Configuration

The following conditions apply unless noted otherwise: typical application schematic using the 5.9 GHz tuning set, $V_{EN1}$ = 5 V, $V_{EN2/BYP}$ = 5 V (high gain mode), $R_{BIAS1}$ = 4.75 kΩ, $R_{BIAS2}$ = 2 kΩ (low bias mode), 50 Ω system impedance, $V_{DD}$ = 5 V, $P_{OUT}$ = 0 dBm, $F_{TEST}$ = 5.9 GHz, $T_{PKG\ BASE}$ = 25 °C. Evaluation board losses are included within the specifications.

| Parameter | Symbol | Specification | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply Quiescent Current (High Bias Mode) | $I_{DDQ-HIGH}$ | | TBD | | mA | $R_{BIAS}$ = TBD, $R_{BIAS2}$ = TBD |
| Supply Quiescent Current (Low Bias Mode) | $I_{DDQ-LOW}$ | | 52 | | | $R_{BIAS}$ = 4.75 kΩ, $R_{BIAS2}$ = 2 kΩ |
| Supply Current with RF applied (High Bias Mode) | $I_{DD-HIGH}$ | | TBD | | mA | $P_{OUT}$ = 0 dBm, $R_{BIAS}$ = TBD, $R_{BIAS2}$ = TBD |
| Supply Current with RF applied (Low Bias Mode) | $I_{DD-LOW}$ | | 52 | | | $P_{OUT}$ = 0 dBm, $R_{BIAS}$ = 4.75 kΩ, $R_{BIAS2}$ = 2 kΩ |
| Gain | S21 | | 27.2 | | dB | $F_{RF}$ = 5.9 GHz |
| Gain Flatness | $S21_{FLAT}$ | | 1.3 | | dB | $F_{RF}$ = 5.8 to 6 GHz |
| Gain Variation Over Temp | $S21_{TEMP}$ | | 2.5 | | dB | $T_{PKG\ BASE}$ = -40 to 115 °C, Referenced to $T_{PKG\ BASE}$ = 25 °C |
| Standby Mode Gain | $S21_{STBY}$ | | TBD | | dB | $V_{EN1}$ = $V_{EN2/BYP}$ = 0 V |
| Input Return Loss | S11 | | < -10 | | dB | $F_{RF}$ = 5.9 GHz |
| Output Return Loss | S22 | | < -10 | | dB | $F_{RF}$ = 5.9 GHz |
| Reverse Isolation | S12 | | < -28 | | dB | $F_{RF}$ = 5.9 GHz |
| De-Embedded Noise Figure | NF | | TBD | | dB | $F_{RF}$ = 5.9 GHz |
| Evaluation Board Noise Figure | | | 1.2 | | | $F_{RF}$ = 5.9 GHz |
| Output 3rd Order Intercept Point | $OIP3_{HI\ BIAS}$ | | TBD | | dBm | $I_{DDQ}$ = TBD, 0 dBm $P_{OUT}$ per tone at 2 MHz spacing |
| | $OIP3_{LO\ BIAS}$ | | 33 | | | $I_{DDQ}$ = 52 mA, 0 dBm $P_{OUT}$ per tone at 2 MHz spacing |
| Output 1 dB Compression Power | $OP1dB_{HI\ BIAS}$ | | TBD | | dB | $I_{DDQ}$ = TBD |
| | $OP1dB_{LO\ BIAS}$ | | 16 | | | $I_{DDQ}$ = 52 mA |

# Nominal Operating Parameters - RF

## 5.9 GHz, 5 V Supply, Low Gain Configuration

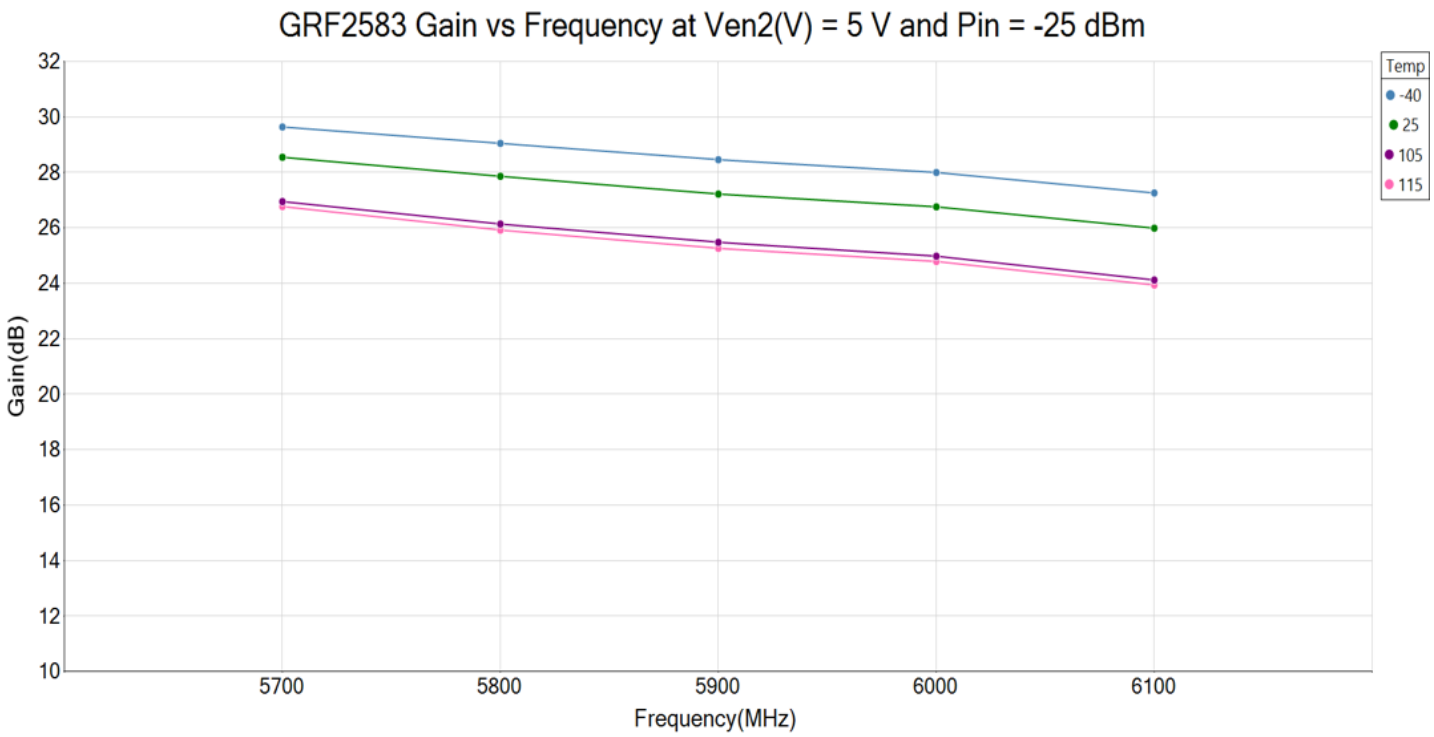
The following conditions apply unless noted otherwise: typical application schematic using the 5.9 GHz tuning set, $V_{EN1}$ = 5 V, $V_{EN2/BYP}$ = 0 V (low gain mode), $R_{BIAS1}$ = 4.75 kΩ, $R_{BIAS2}$ = 2 kΩ (low bias mode), 50 Ω system impedance, $V_{DD}$ = 5 V, $P_{OUT}$ = 0 dBm, $F_{TEST}$ = 5.9 GHz, $T_{PKG\ BASE}$ = 25 °C. Evaluation board losses are included within the specifications.

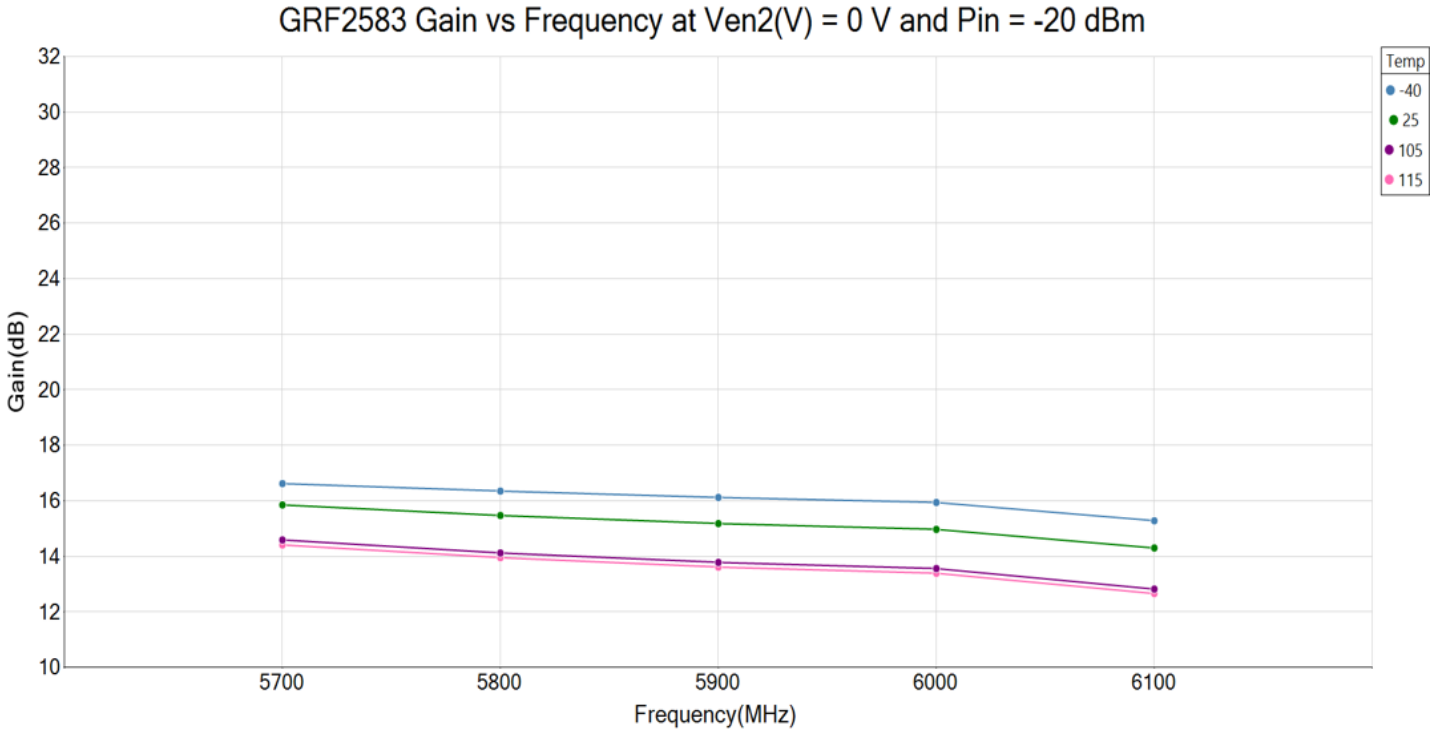
| Parameter | Symbol | Specification | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply Quiescent Current (High Bias Mode) | $I_{DDQ-HIGH}$ | | TBD | | mA | $R_{BIAS}$ = TBD, $R_{BIAS2}$ = TBD |
| Supply Quiescent Current (Low Bias Mode) | $I_{DDQ-LOW}$ | | 15 | | | $R_{BIAS}$ = 4.75 kΩ, $R_{BIAS2}$ = 2 kΩ |
| Supply Current with RF applied (High Bias Mode) | $I_{DD-HIGH}$ | | TBD | | mA | $P_{OUT}$ = 0 dBm, $R_{BIAS}$ = TBD, $R_{BIAS2}$ = TBD |
| Supply Current with RF applied (Low Bias Mode) | $I_{DD-LOW}$ | | 16 | | | $P_{OUT}$ = 0 dBm, $R_{BIAS}$ = 4.75 kΩ, $R_{BIAS2}$ = 2 kΩ |
| Gain | S21 | | 15 | | dB | $F_{RF}$ = 5.9 GHz |
| Gain Flatness | $S21_{FLAT}$ | | 0.5 | | dB | $F_{RF}$ = 5.8 to 6 GHz |
| Gain Variation Over Temp | $S21_{TEMP}$ | | 2.2 | | dB | $T_{PKG\ BASE}$ = -40 to 115 °C, Referenced to $T_{PKG\ BASE}$ = 25 °C |
| Standby Mode Gain | $S21_{STBY}$ | | TBD | | dB | $V_{EN1}$ = $V_{EN2/BYP}$ = 0 V |
| Input Return Loss | S11 | | < -9 | | dB | $F_{RF}$ = 5.9 GHz |
| Output Return Loss | S22 | | < -9 | | dB | $F_{RF}$ = 5.9 GHz |
| Reverse Isolation | S12 | | < -28 | | dB | $F_{RF}$ = 5.9 GHz |
| De-Embedded Noise Figure | NF | | TBD | | dB | $F_{RF}$ = 5.9 GHz |
| Evaluation Board Noise Figure | | | 1.25 | | | $F_{RF}$ = 5.9 GHz |
| Output 3rd Order Intercept Point | $OIP3_{HI\ BIAS}$ | | TBD | | dBm | $I_{DDQ}$ = TBD, 0 dBm $P_{OUT}$ per tone at 2 MHz spacing |
| | $OIP3_{LO\ BIAS}$ | | 21.2 | | | $I_{DDQ}$ = 15 mA, 0 dBm $P_{OUT}$ per tone at 2 MHz spacing |
| Output 1 dB Compression Power | $OP1dB_{HI\ BIAS}$ | | TBD | | dB | $I_{DDQ}$ = TBD |
| | $OP1dB_{LO\ BIAS}$ | | 10 | | | $I_{DDQ}$ = 15 mA |

## TRUTH TABLE

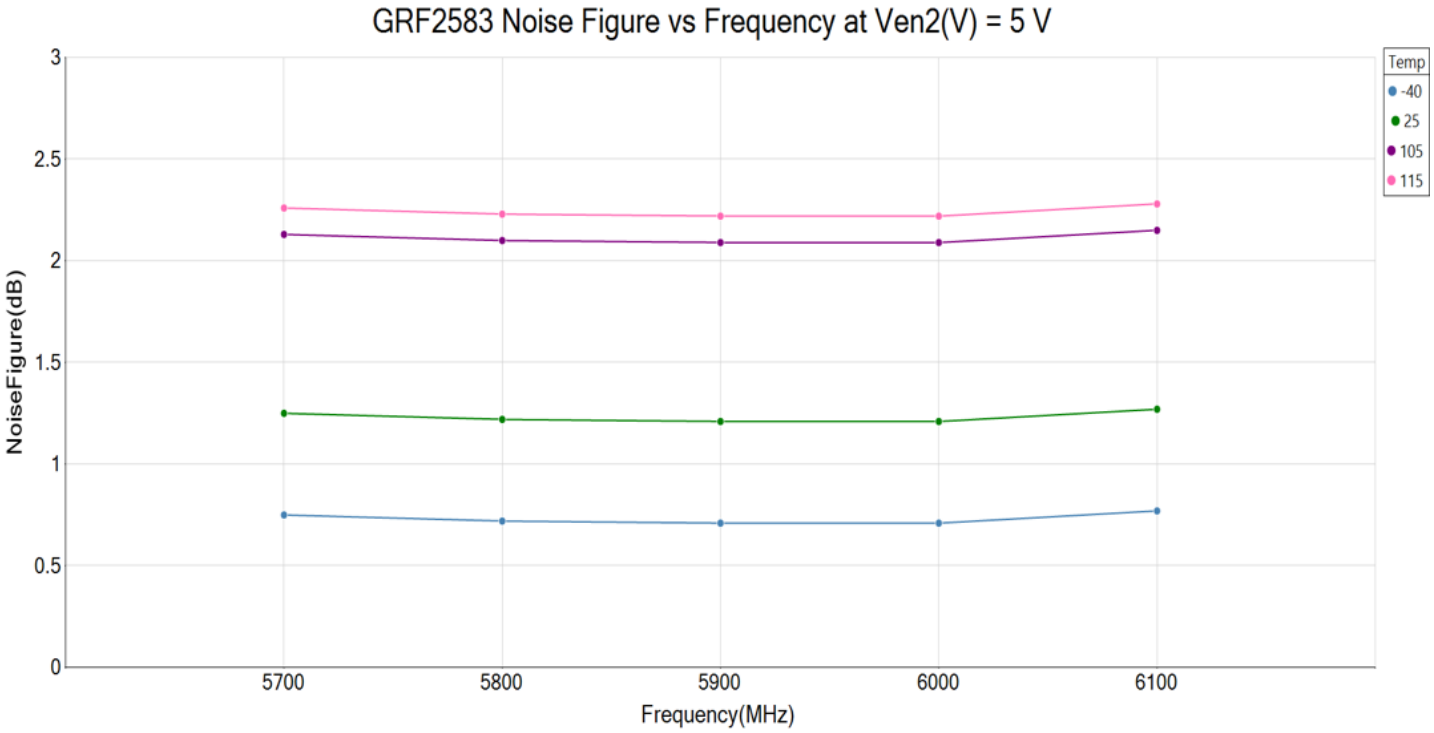
| Mode | Pin Logic | |
|---|---|---|
| | $V_{EN1}$ | $V_{EN2/BYP}$ |
| High Gain | HIGH | HIGH |
| Low Gain (2nd Stage Bypass) | HIGH | LOW |
| Standby | LOW | LOW |

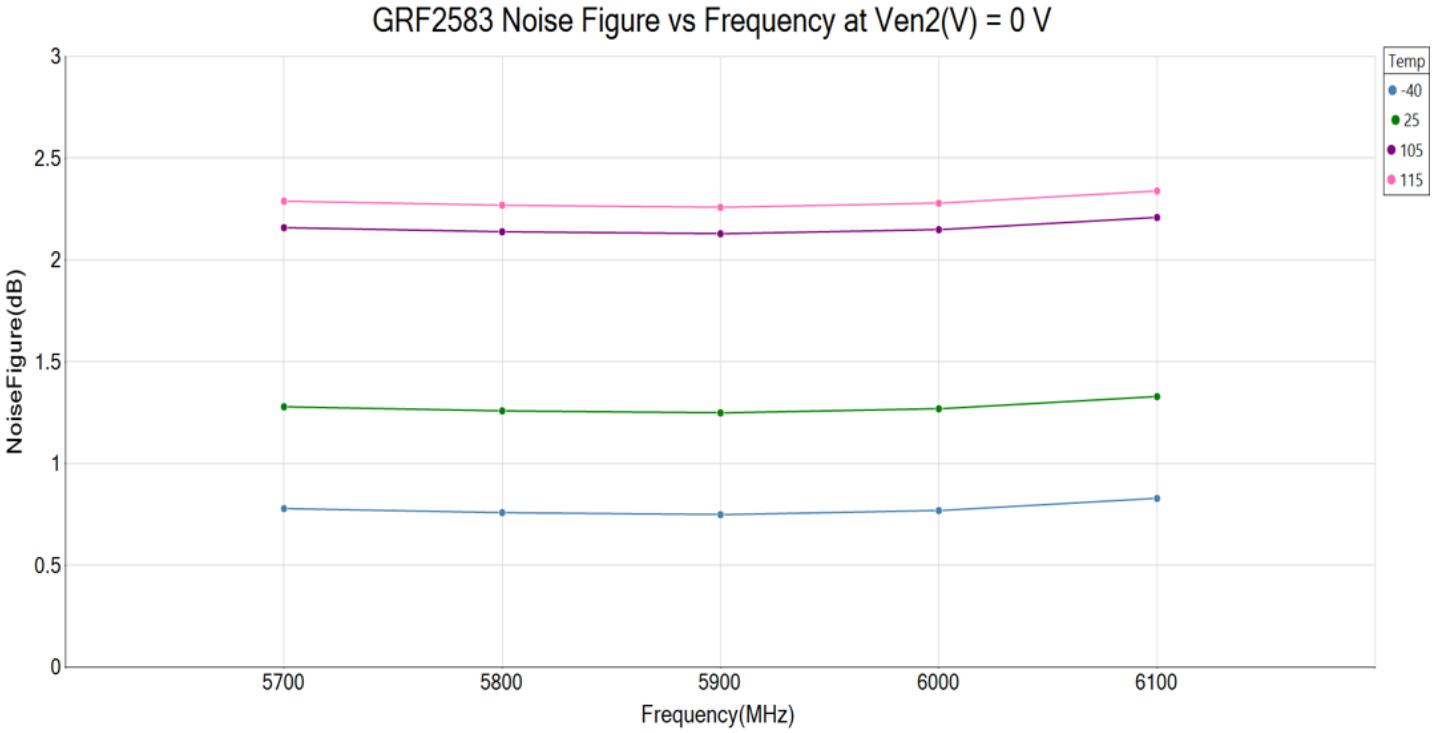
## GRF2583 Typical Operating Curves



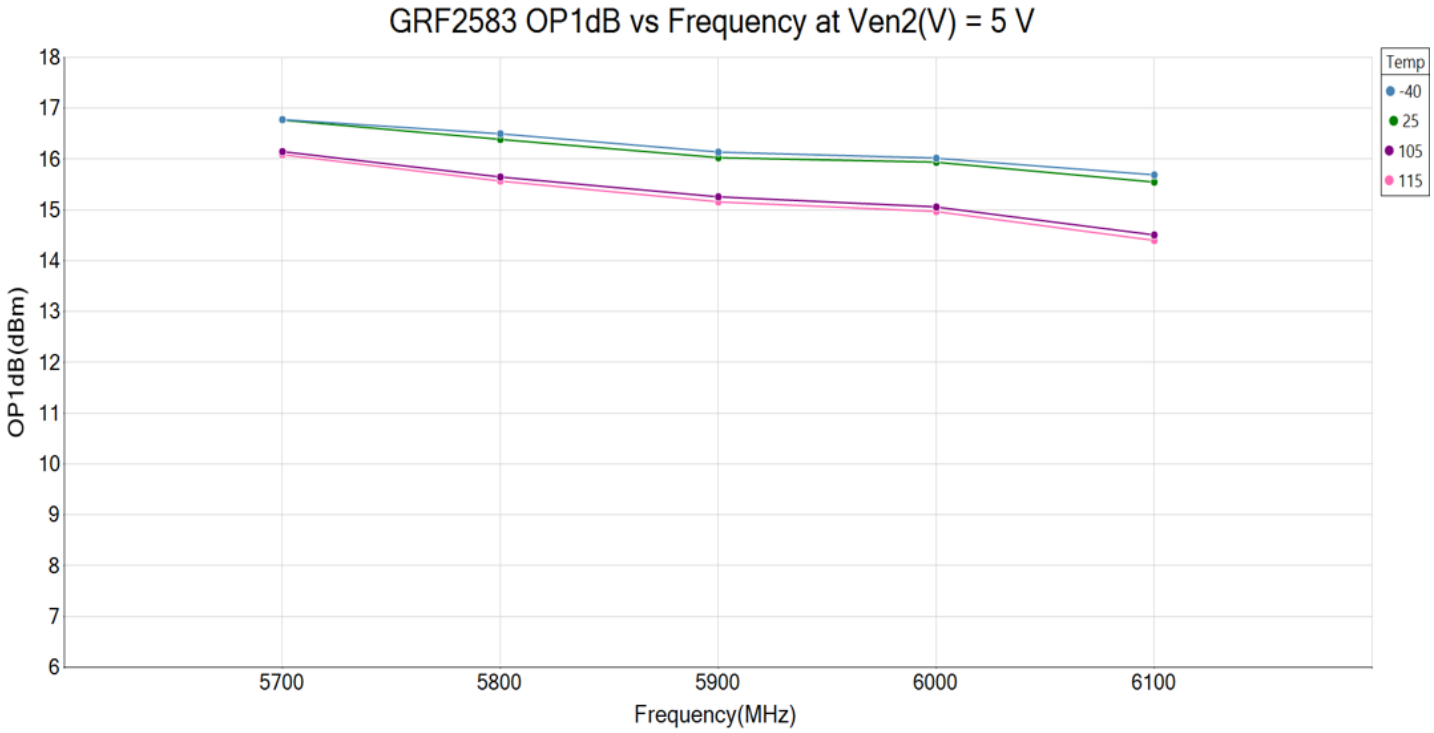



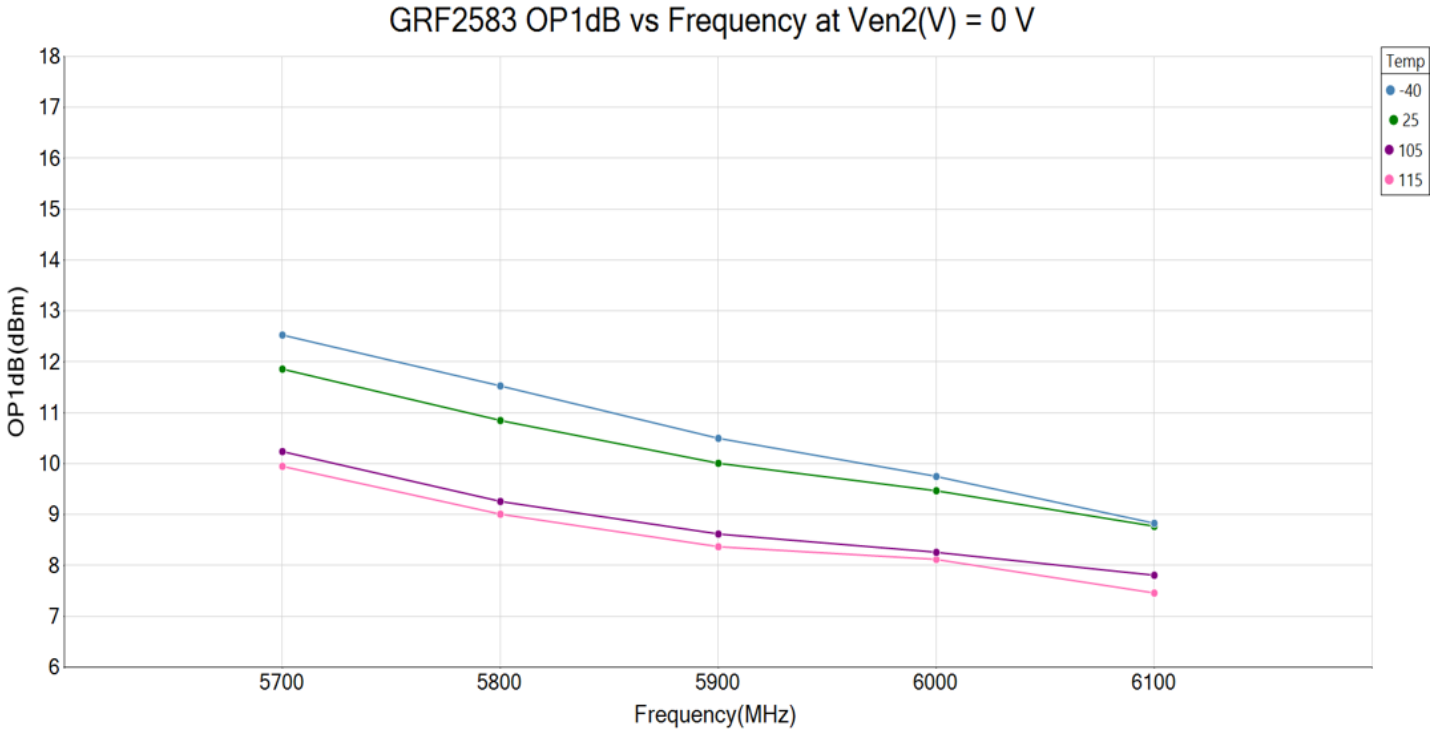
## GRF2583 Typical Operating Curves



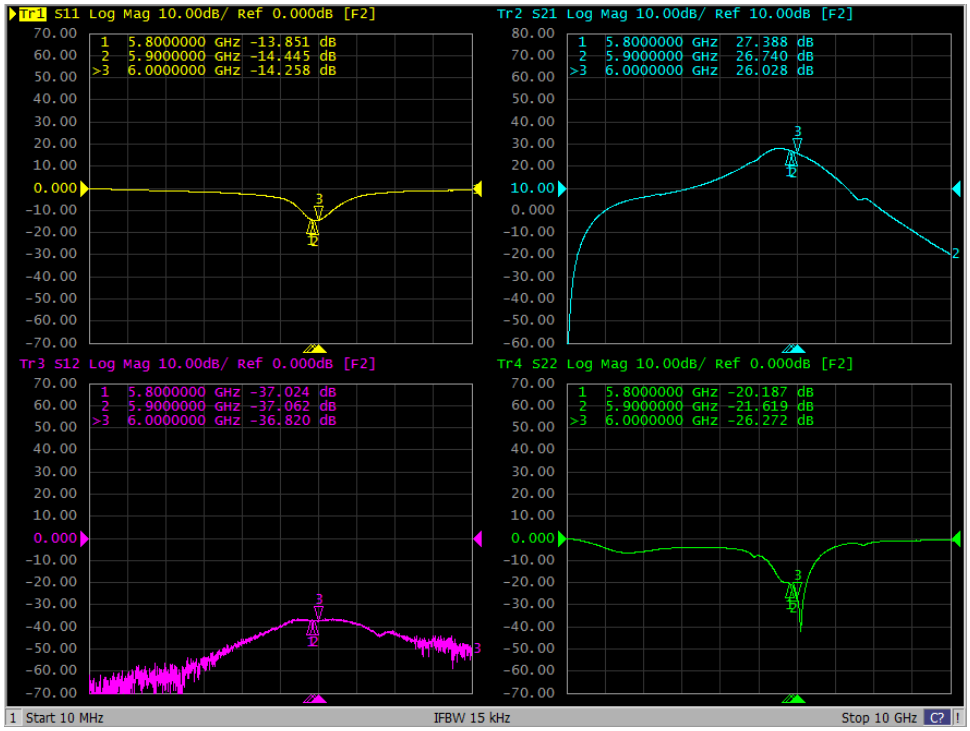



## GRF2583 Typical Operating Curves

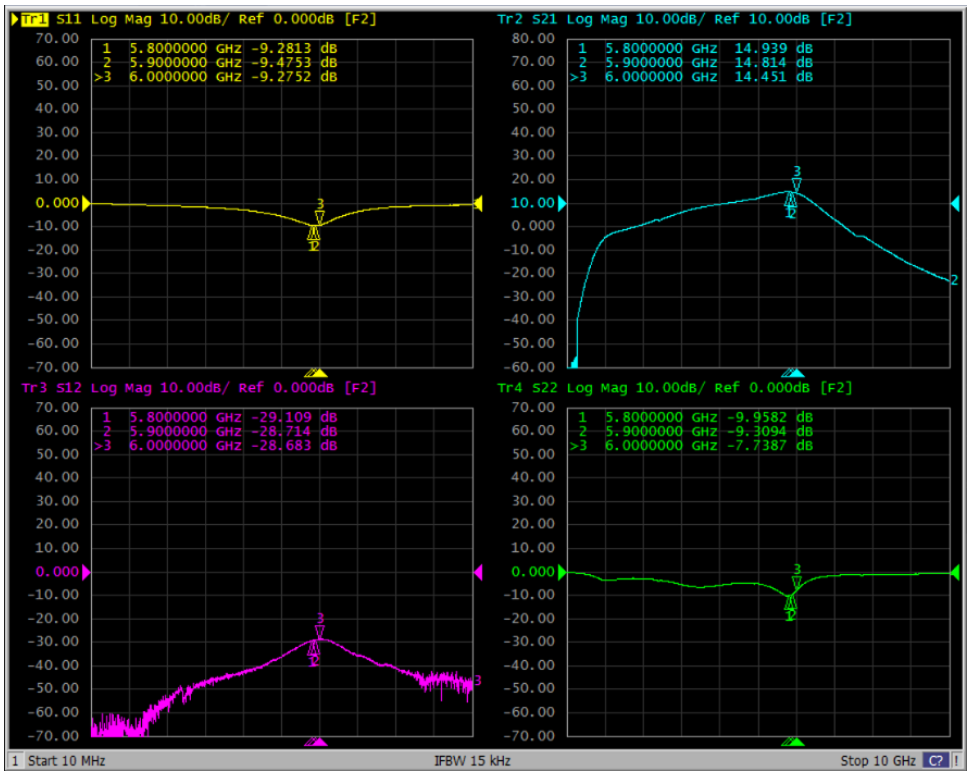


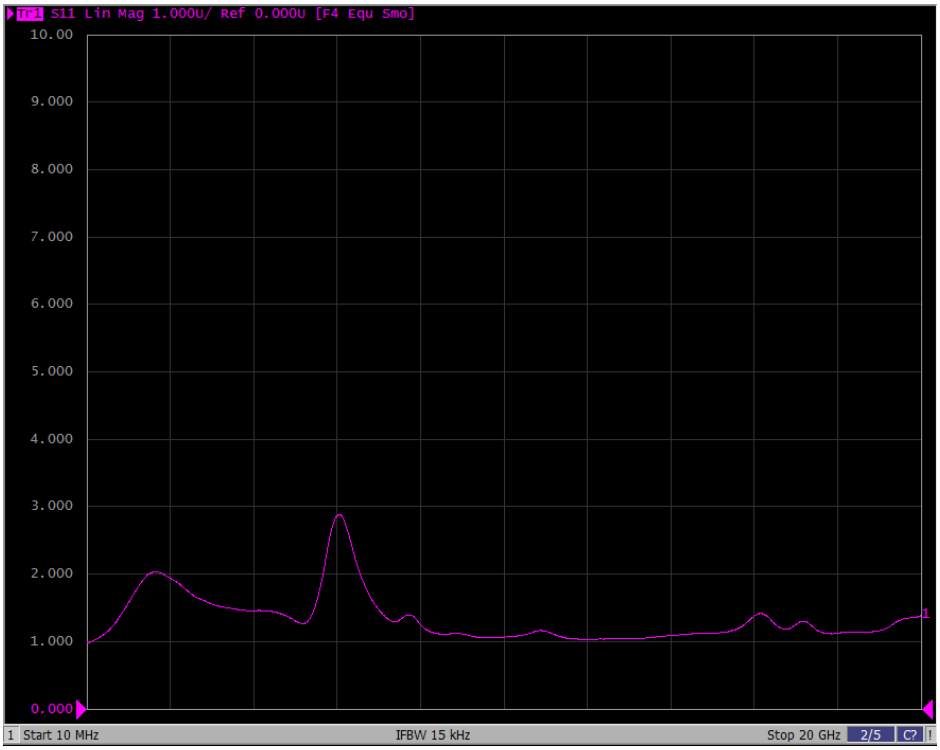
## GRF2583 S-Parameters: High Gain Mode (5.8 to 6 GHz)



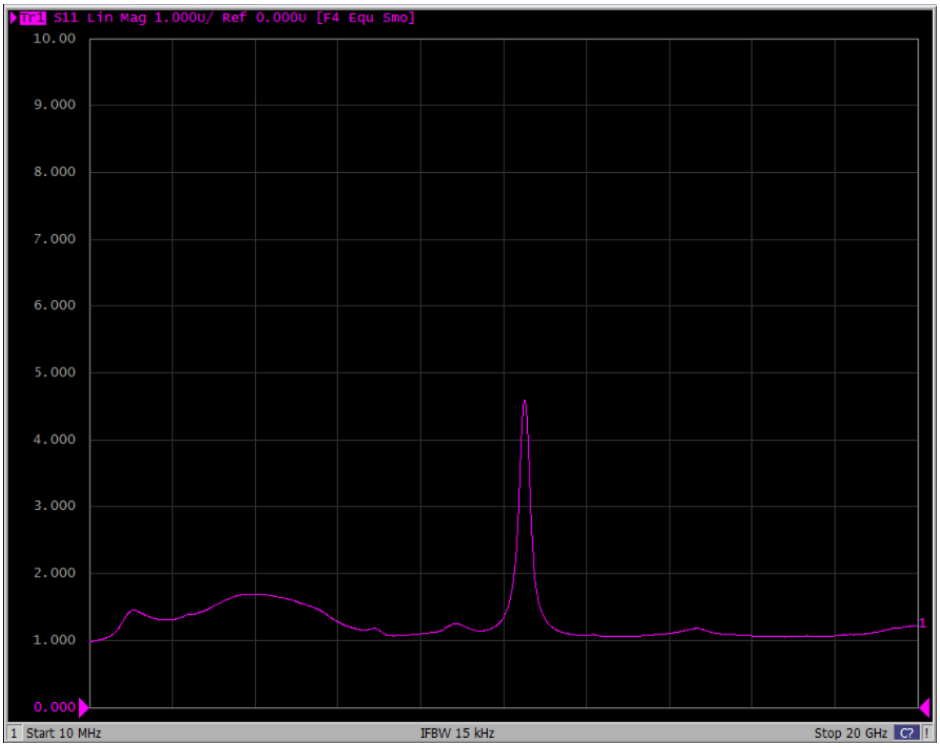

## GRF2583 S-Parameters: Low Gain Mode (5.8 to 6 GHz)

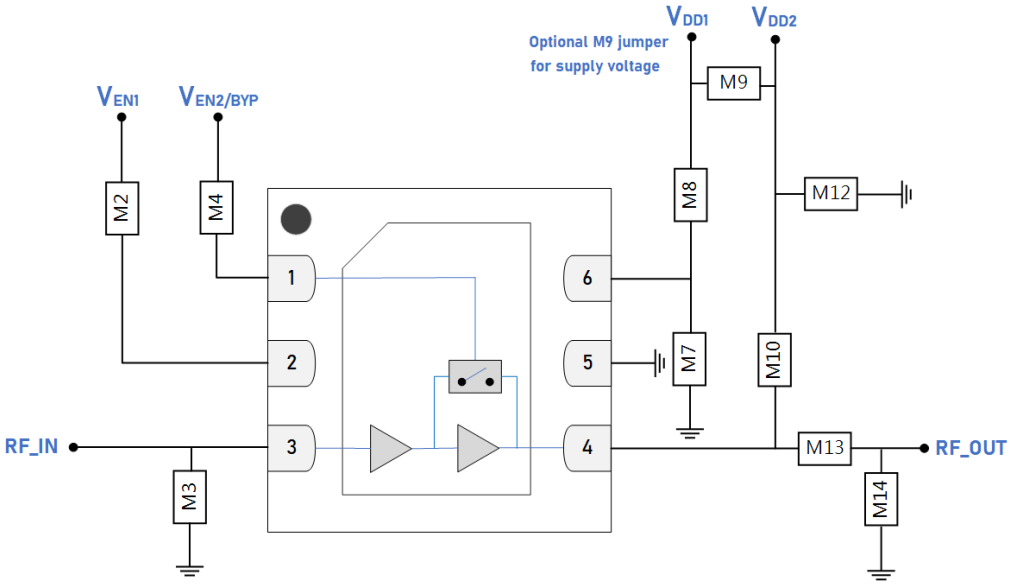


## GRF2583 Stability Mu Factor: High Gain Mode (10 MHz to 20 GHz)

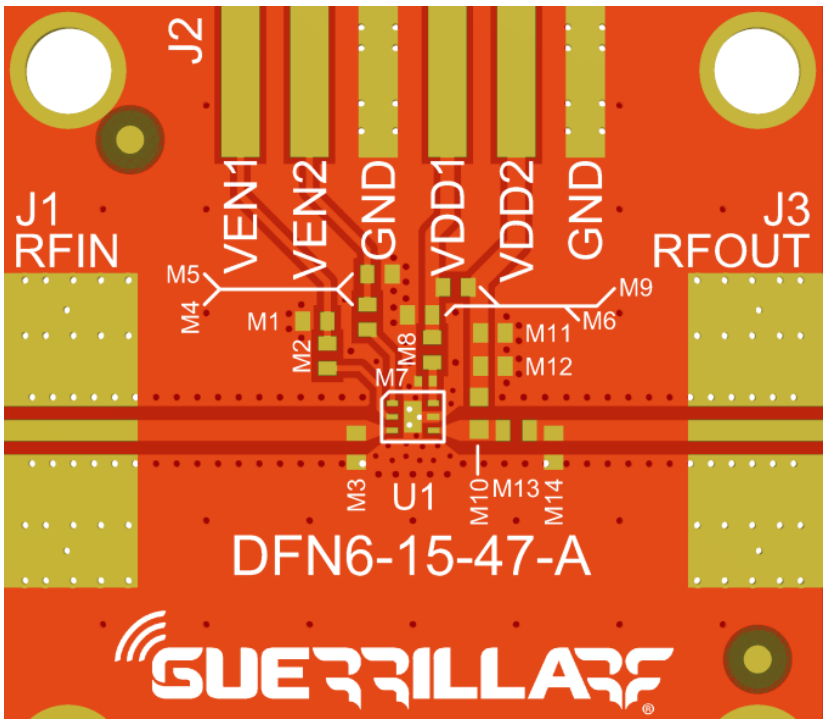



## GRF2583 Stability Mu Factor: Low Gain Mode (10 MHz to 20 GHz)






**GRF2583 Standard Evaluation Board Schematic**

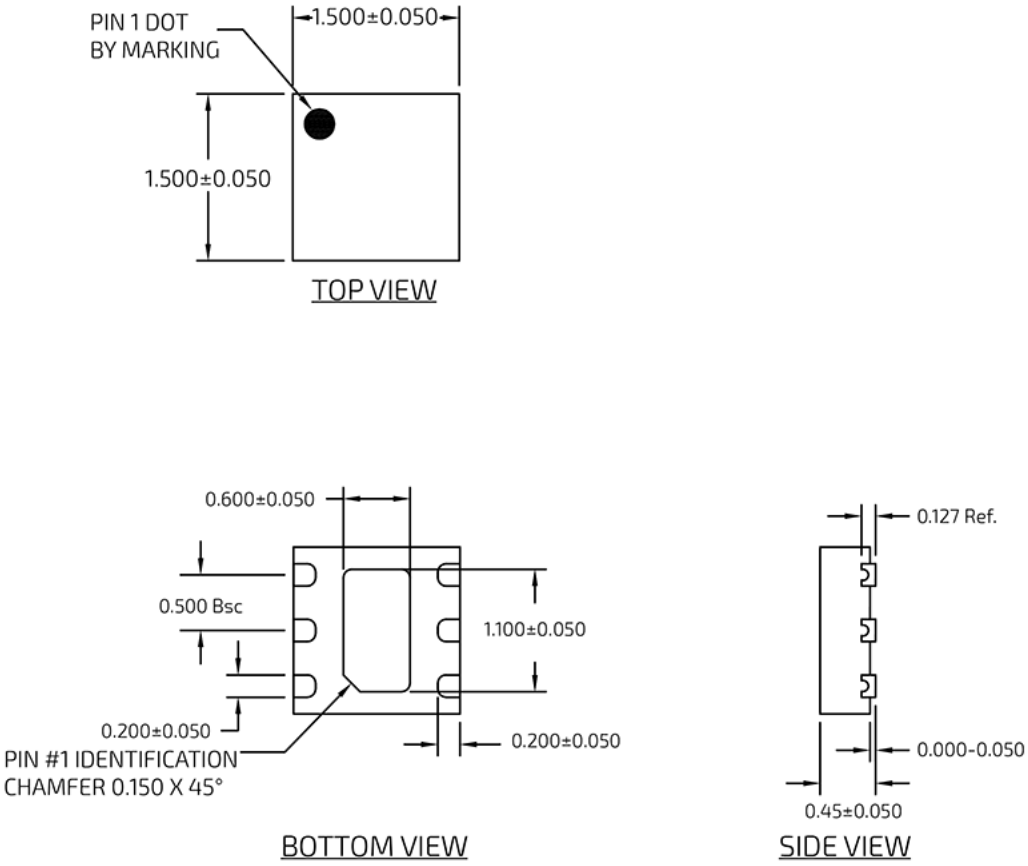



**GRF2583 Evaluation Board Assembly Drawing**

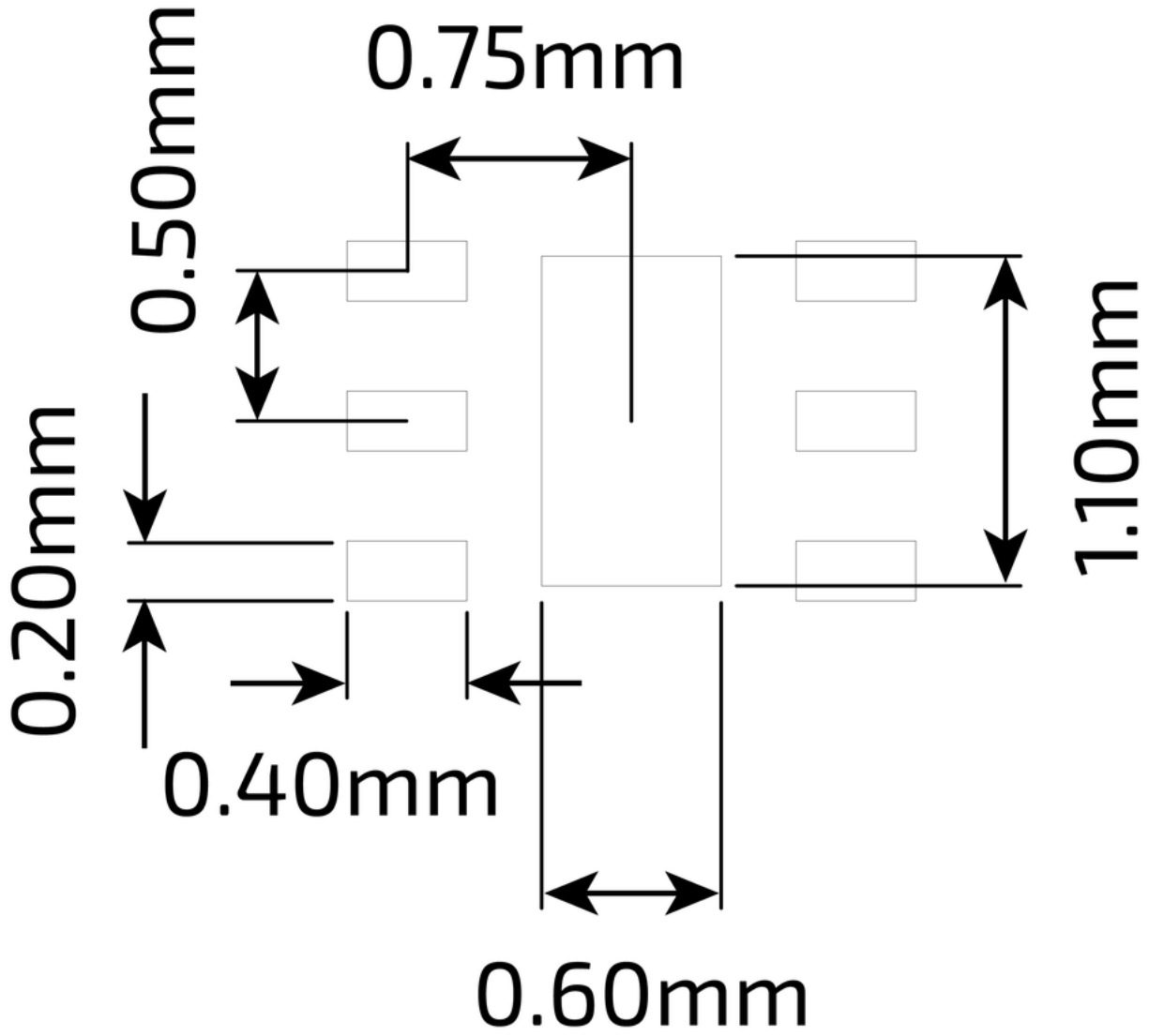
## GRF2583 Evaluation Board Assembly Diagram Reference

| Component | Type | Manufacturer | Family | Value | Package Size | Substitution |
|---|---|---|---|---|---|---|
| M2 | Resistor | Various | 5% | 4.75 kΩ | 0402 | ok |
| M3 | Capacitor | Murata | GJM | 0.5 pF | 0402 | ok |
| M4 | Resistor | Various | 5% | 2 kΩ | 0402 | ok |
| M7 | Capacitor | Murata | GJM | 0.1 µF | 0402 | ok |
| M8 | Resistor | Various | 5% | 3 Ω | 0402 | ok |
| M9 | Inductor | Murata | LQG-WH | 6.8 nH | 0402 | ok |
| M10 | Inductor | Murata | LQG | 5.6 nH | 0402 | ok |
| M12 | Capacitor | Murata | GJM | 0.1 µF | 0402 | ok |
| M13 | Capacitor | Murata | GJM | 18 pF | 0402 | ok |
| M14 | Capacitor | Murata | GJM | 0.5 pF | 0402 | ok |
| M1, M5, M6 M11 | DNP | -- | -- | -- | -- | -- |
| Evaluation Board | DFN6-15-47-A | | | | | |

**Note:** Standard evaluation board bias: $V_{DD}$ = 5 V.




**DFN 6 1.5x1.5mm Package Dimensions**



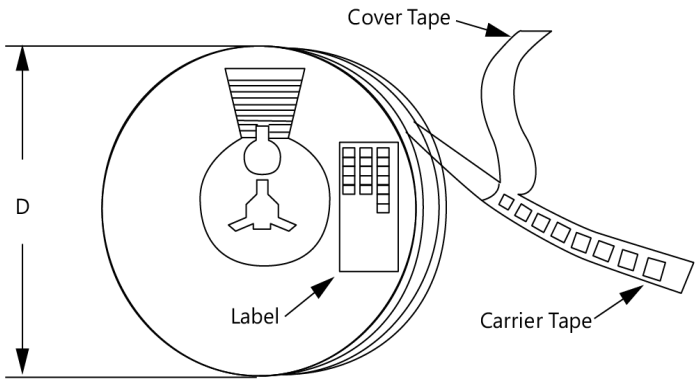

**DFN 6 1.5x1.5mm Suggested PCB Footprint (Top View)**

### Package Marking Diagram

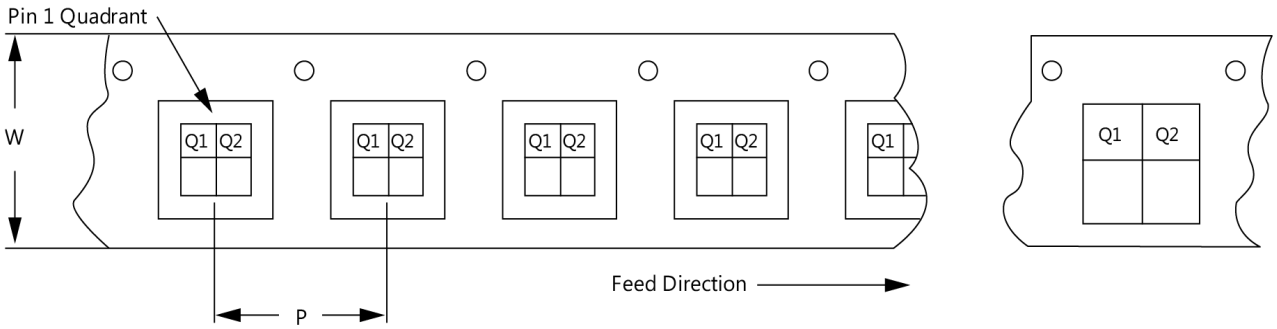

Line 1: "Y" = YEAR (single digit). "WW" = WORK WEEK the Device was assembled.
Line 2: "XXXX" = Device Part Number.

### Tape and Reel Information

Guerrilla RF's tape and reel specification complies with Electronics Industries Association (EIA) standards for "Embossed Carrier Tape of Surface Mount Components for Automatic Handling" (reference EIA-481). Devices are loaded with pins down into the carrier pocket with protective cover tape and reeled onto a plastic reel. Each reel is packaged in a cardboard box. There are product labels on the reel, the protective ESD bag, and the outside surface of the box. For the latest reel specifications and package information (including units/reel), please visit Package Manufacturing Information | Guerrilla RF (guerrilla-rf.com).




Tape and Reel Packaging with Reel Diameter Noted (D)




Carrier Tape Width (W), Pitch (P), Feed Direction and Pin 1 Quadrant Information

## Revision History

| Revision Date | Description of Change |
|---|---|
| May 21, 2024 | Preliminary Data Sheet. |

### Data Sheet Classifications

| Data Sheet Status | Notes |
|---|---|
| Advance | S-parameter and NF data based on EM simulations for the fully packaged device using foundry-supplied transistor S-parameters. Linearity estimates based on device size, bias condition and experience with related devices. |
| Preliminary | All data based on evaluation board measurements taken within the Gurerrilla RF Applications Lab. Any MIN/MAX limits represented within the data sheet are based solely on *estimated* part-to-part variations and process spreads. All parametric values are subject to change pending the collection of additional data. |
| Release Ø | All data based on measurements taken with *production-released* material. TYP values are based on a combination of ATE and bench-level measurements, with MIN/MAX limits defined using *modelled estimates* that account for part-to-part variations and expected process spreads. Although unlikely, future refinements to the TYP/MIN/MAX values may be in order as multiple lots are processed through the factory. |
| Release A-Z | All data based on measurements taken with production-released material *derived from multiple lots which have been fabricated over an extended period of time*. MIN/MAX limits may be refined over previous releases as more statistically significant data is collected to account for process spreads. |

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