G2R1000MT17J
1700 V 1000 mΩ SiC MOSFET

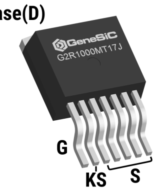
Silicon Carbide MOSFET
N-Channel Enhancement Mode

V_{DS}	=	1700 V
$R_{DS(ON)(Typ.)}$	=	1000 mΩ
$I_{D(T_C = 100°C)}$	=	3 A

Features

- G2R™ Technology
- Softer $R_{DS(ON)}$ v/s Temperature Dependency
- LoRing™ - Electromagnetically Optimized Design
- Smaller $R_{G(INT)}$ and Lower Q_G
- Low Device Capacitances (C_{OSS}, C_{RSS})
- Industry-Leading UIL & Short-Circuit Robustness
- Robust Body Diode with Low V_F and Low Q_{RR}
- Optimized Package with Separate Driver Source Pin

Package



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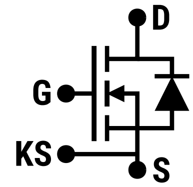


D = Drain
G = Gate
S = Source
KS = Kelvin Source

RoHS
REACH

Advantages

- Compatible with Commercial Gate Drivers
- Low Conduction Losses at all Temperatures
- Reduced Ringing
- Faster and More Efficient Switching
- Lesser Switching Spikes and Lower Losses
- Better Power Density and System Efficiency
- Ease of Paralleling without Thermal Runaway
- Superior Robustness and System Reliability

Applications

- Auxiliary Power Supply
- Solar Inverters (String and Central)
- Infrastructure Chargers
- Industrial Motors (AC Servos)
- General Purpose Inverters
- Pulsed Power
- Piezo Drivers
- Ion Beam Generators

Absolute Maximum Ratings (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 100 µA	1700	V	
Gate-Source Voltage (Dynamic)	$V_{GS(max)}$		-10 / +25	V	
Gate-Source Voltage (Static)	$V_{GS(op)}$	Recommended Operation	-5 / +20	V	
Continuous Forward Current	I_D	T_C = 25°C, V_{GS} = -5 / +20 V	5	A	Fig. 15
		T_C = 100°C, V_{GS} = -5 / +20 V	3		
		T_C = 135°C, V_{GS} = -5 / +20 V	3		
Pulsed Drain Current	$I_{D(pulse)}$	$t_P \leq$ 3µs, D ≤ 1%, V_{GS} = 20 V, Note 1	8	A	Fig. 14
Power Dissipation	P_D	T_C = 25°C	44	W	Fig. 16
Non-Repetitive Avalanche Energy	E_{AS}	L = 90 mH, I_{AS} = 1.0 A	45	mJ	
Operating and Storage Temperature	T_j , T_{stg}		-55 to 175	°C	

Thermal/Package Characteristics

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Thermal Resistance, Junction - Case	R_{thJC}			3.03	3.37	°C/W	Fig. 13
Weight	W_T			1.45		g	

Note 1: Pulse Width t_P Limited by $T_{j(max)}$

Electrical Characteristics (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 100 µA	1700			V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 1700 V, V_{GS} = 0 V		1		µA	
Gate Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 25 V V_{DS} = 0 V, V_{GS} = -10 V			100 -100	nA	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 2.0 mA V_{DS} = V_{GS}, I_D = 2.0 mA, T_j = 175°C	2.0	4.50 3.50		V	Fig. 9
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 2 A V_{DS} = 10 V, I_D = 2 A, T_j = 175°C		0.76 0.84		S	Fig. 4
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 20 V, I_D = 2 A V_{GS} = 20 V, I_D = 2 A, T_j = 175°C		1000 1479	1250	mΩ	Fig. 5-8
Input Capacitance	C_{iss}	V_{DS} = 1000 V, V_{GS} = 0 V f = 1 MHz, V_{AC} = 25mV		111		pF	Fig. 11
Output Capacitance	C_{oss}			19		pF	Fig. 11
Reverse Transfer Capacitance	C_{rss}			5.0		pF	Fig. 11
C_{oss} Stored Energy	E_{oss}			10		µJ	Fig. 12
C_{oss} Stored Charge	Q_{oss}			23		nC	
Effective Output Capacitance (Energy Related)	$C_{o(er)}$			20		pF	Note 2
Effective Output Capacitance (Time Related)	$C_{o(tr)}$			23		pF	Note 2
Gate-Source Charge	Q_{gs}	V_{DS} = 1000 V, V_{GS} = -5 / +20 V I_D = 2 A Per IEC607478-4		2		nC	Fig. 10
Gate-Drain Charge	Q_{gd}			7		nC	Fig. 10
Total Gate Charge	Q_g			11		nC	Fig. 10
Internal Gate Resistance	$R_{G(int)}$	f = 1 MHz, V_{AC} = 25 mV		5.0		Ω	
Turn-On Switching Energy (Body Diode)	E_{On}	T_j = 25°C, V_{GS} = -5/+20V, $R_{G(ext)}$ = 8 Ω, L = 1000.0 µH, I_D = 2 A, V_{DD} = 1200 V		44		µJ	Fig. 22,26
Turn-Off Switching Energy (Body Diode)	E_{Off}			11		µJ	Fig. 22,26
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 1200 V, V_{GS} = -5/+20V $R_{G(ext)}$ = 8 Ω, L = 1000.0 µH, I_D = 2 A Timing relative to V_{DS}, Inductive load		6		ns	Fig. 24
Rise Time	t_r			12		ns	Fig. 24
Turn-Off Delay Time	$t_{d(off)}$			8		ns	Fig. 24
Fall Time	t_f			8		ns	Fig. 24

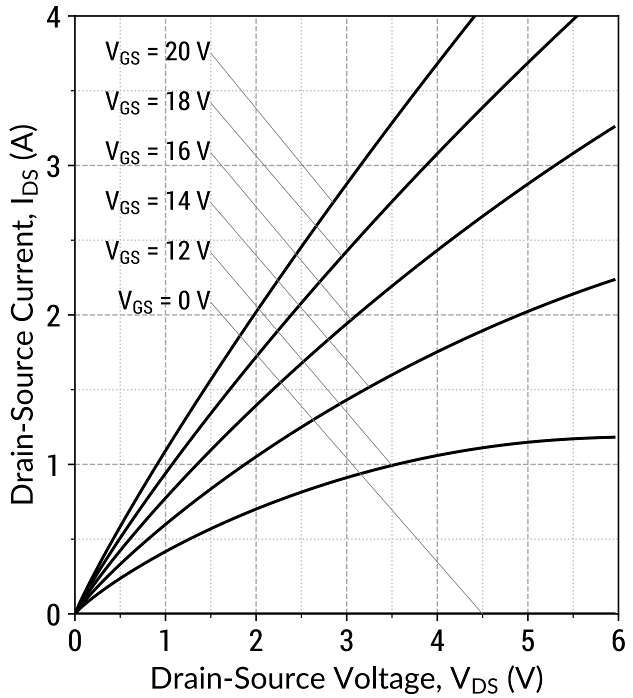
**The chip technology was characterized up to 200 V/ns. The measured dV/dt was limited by measurement test setup and package.*

Note 2: $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{OSS} while V_{DS} is rising from 0 to 1000V.
$C_{o(tr)}$, a lumped capacitance that gives same charging times as C_{OSS} while V_{DS} is rising from 0 to 1000V.

Reverse Diode Characteristics

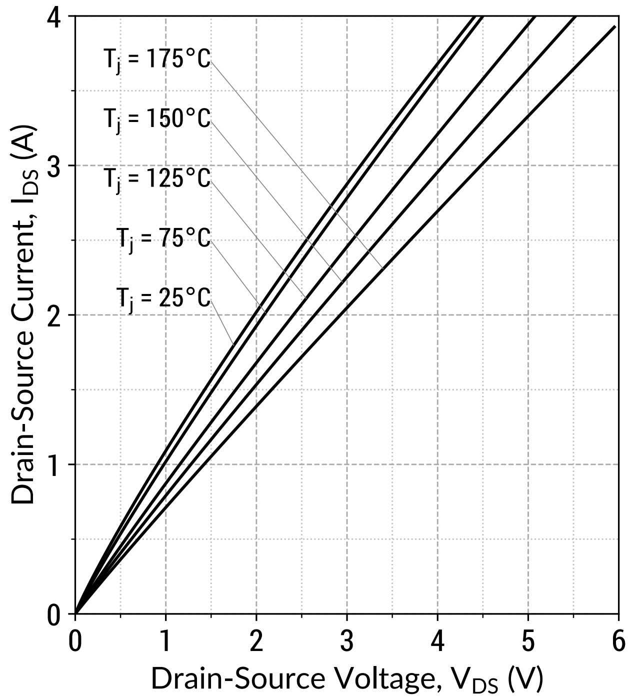
Parameter	Symbol	Conditions	Values Min.	Values Typ.	Values Max.	Unit	Note
Diode Forward Voltage	V_{SD}	V_{GS} = -5 V, I_{SD} = 1 A		4.0		V	Fig. 17-18
		V_{GS} = -5 V, I_{SD} = 1 A, T_j = 175°C		3.6			
Continuous Diode Forward Current	I_S	V_{GS} = -5 V, T_c = 100°C	3			A	
Diode Pulse Current	$I_{S(pulse)}$	V_{GS} = -5 V, Note 1		12		A	
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 2 A, V_R = 1200 V dif/dt = 550 A/μs, T_j = 25°C		21		ns	
Reverse Recovery Charge	Q_{rr}			27		nC	
Peak Reverse Recovery Current	I_{rrm}			2		A	
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 2 A, V_R = 1200 V dif/dt = 550 A/μs, T_j = 175°C		36		ns	
Reverse Recovery Charge	Q_{rr}			101		nC	
Peak Reverse Recovery Current	I_{rrm}			5		A	

Figure 1: Output Characteristics (T_j = 25°C)



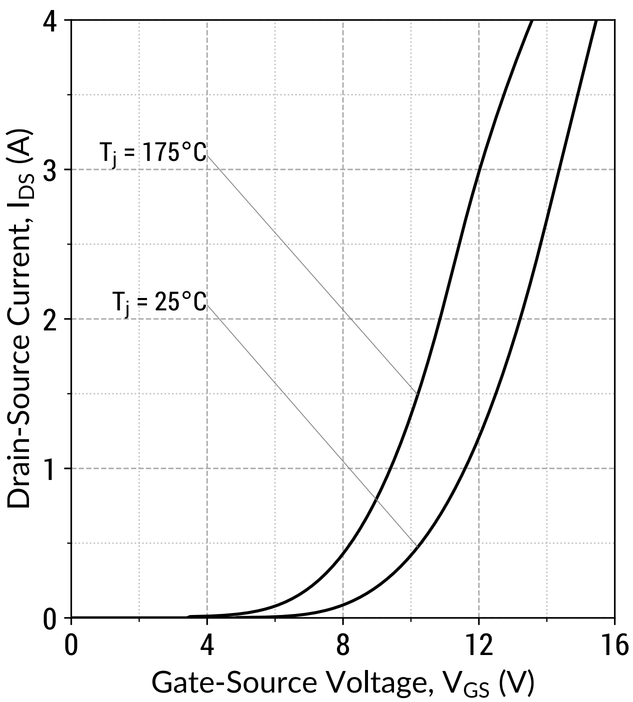
$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 2: Output Characteristics (V_{GS} = 20 V)



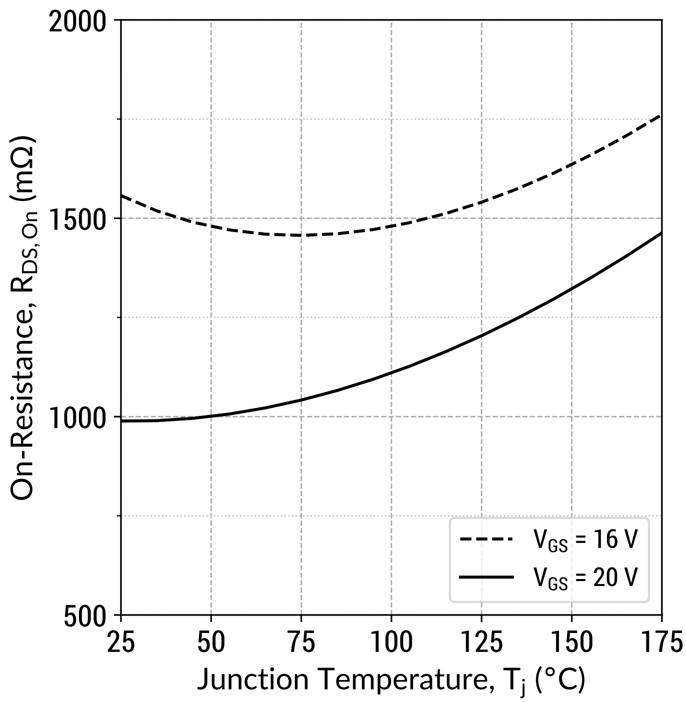
$I_D = f(V_{DS}, T_j)$; t_P = 250 µs

Figure 3: Transfer Characteristics (V_{DS} = 10 V)



$I_D = f(V_{GS}, T_j)$; t_P = 100 µs

Figure 4: On-State Resistance v/s Temperature



$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 250 µs; I_D = 2 A

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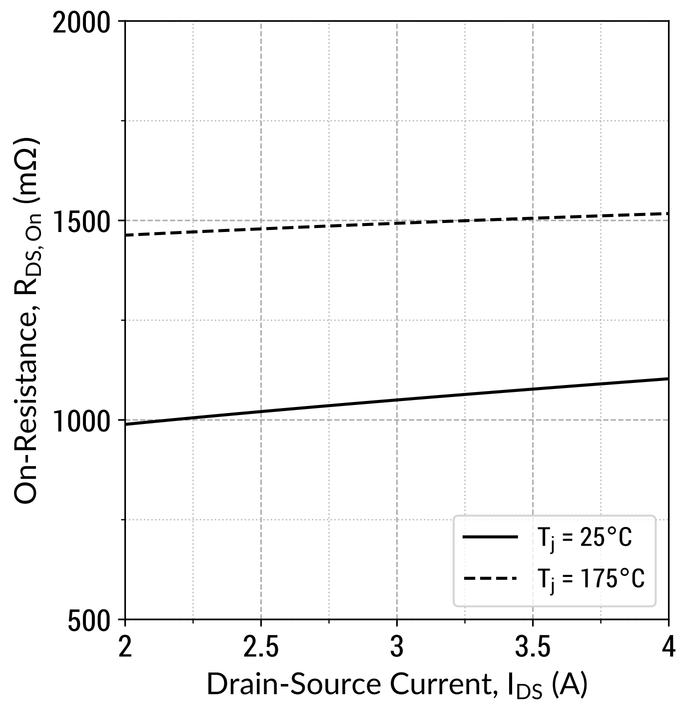
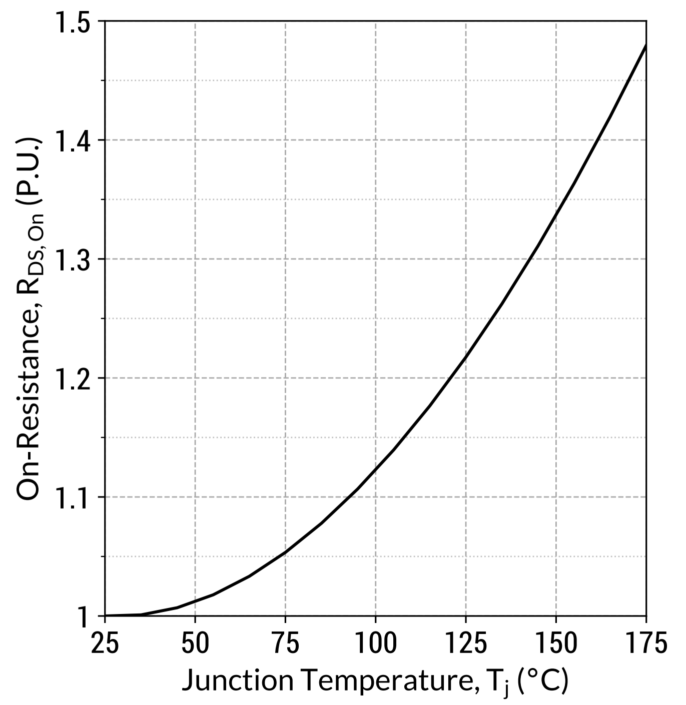
Figure 5: On-State Resistance v/s Drain Current



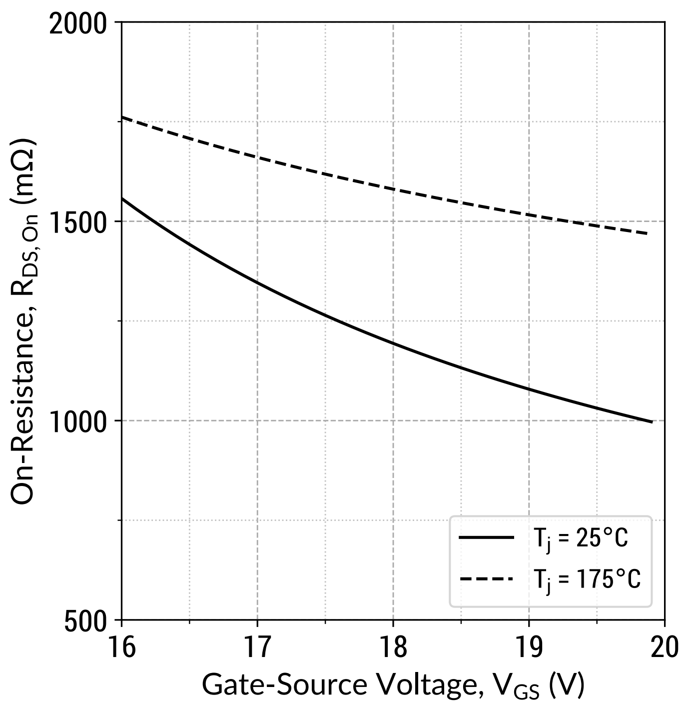
$R_{DS(ON)} = f(T_j, I_D)$; t_P = 250 µs; V_{GS} = 20 V

Figure 6: Normalized On-State Resistance v/s Temperature



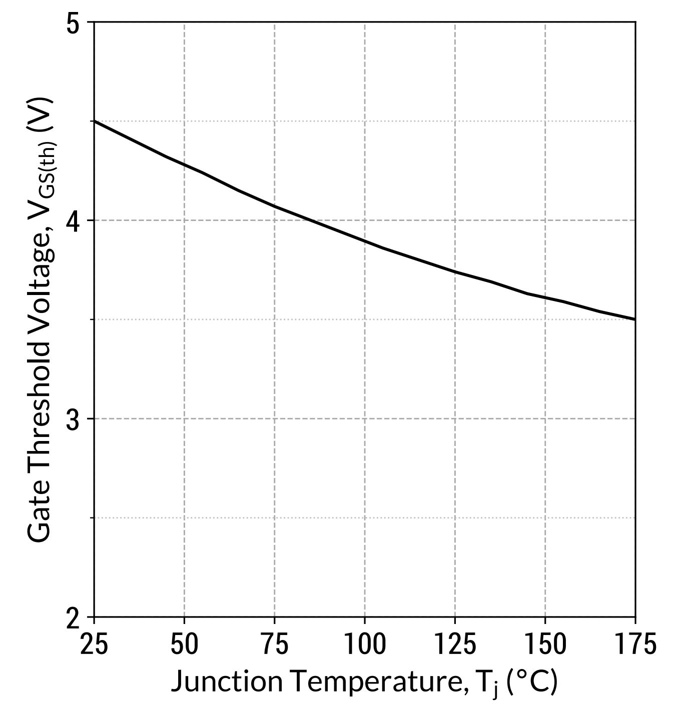
$R_{DS(ON)} = f(T_j)$; t_P = 250 µs; I_D = 2 A; V_{GS} = 20 V

Figure 7: On-State Resistance v/s Gate Voltage



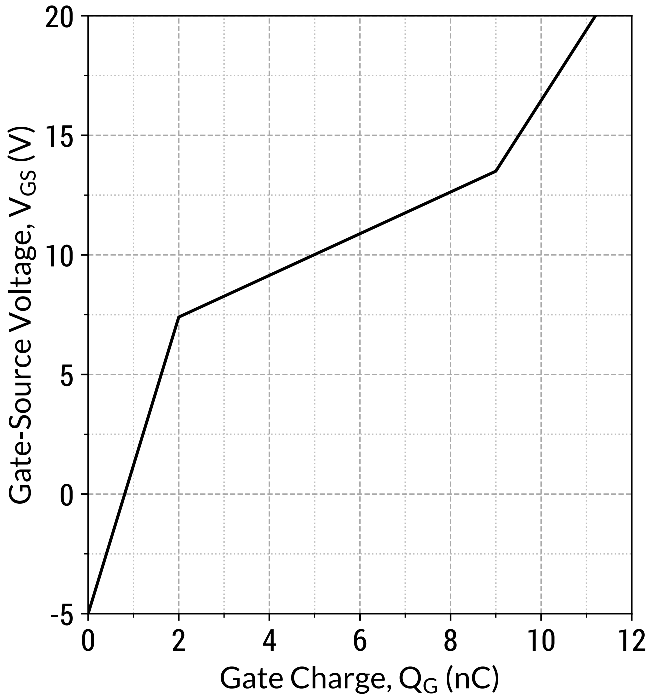
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 250 µs; I_D = 2 A

Figure 8: Threshold Voltage Characteristics



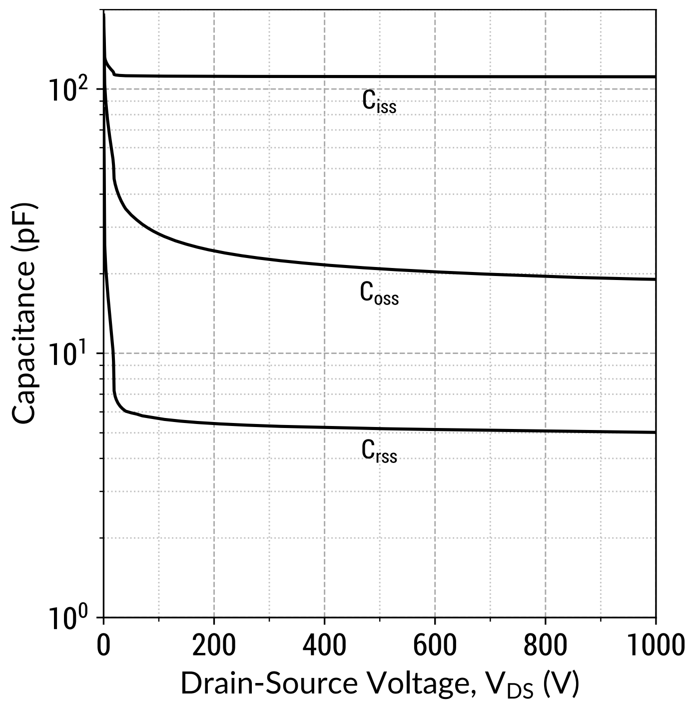
$V_{GS(th)} = f(T_j)$; $V_{DS} = V_{GS}$; I_D = 2.0 mA

Figure 9: Gate Charge Characteristics



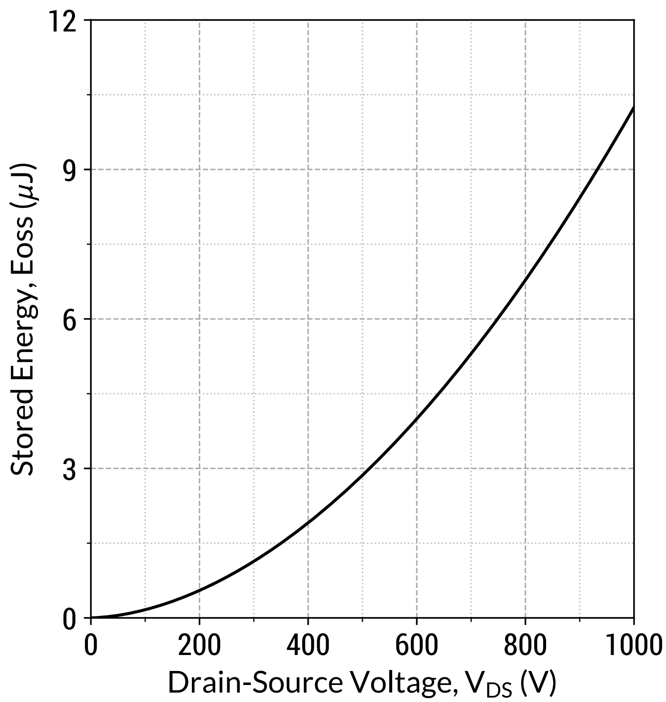
I_D = 2 A; V_{DS} = 1000 V; T_c = 25°C

Figure 10: Capacitance v/s Drain-Source Voltage



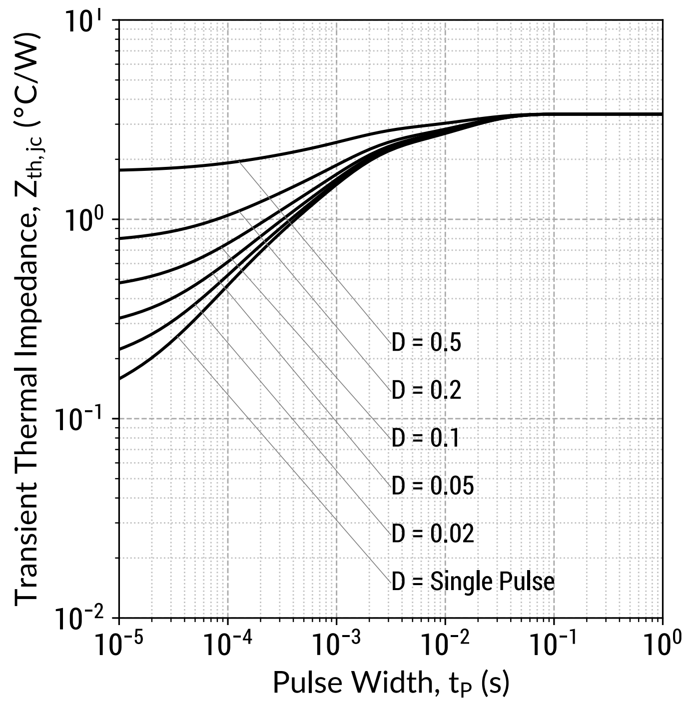
f = 1 MHz; V_{AC} = 25mV

Figure 11: Output Capacitor Stored Energy



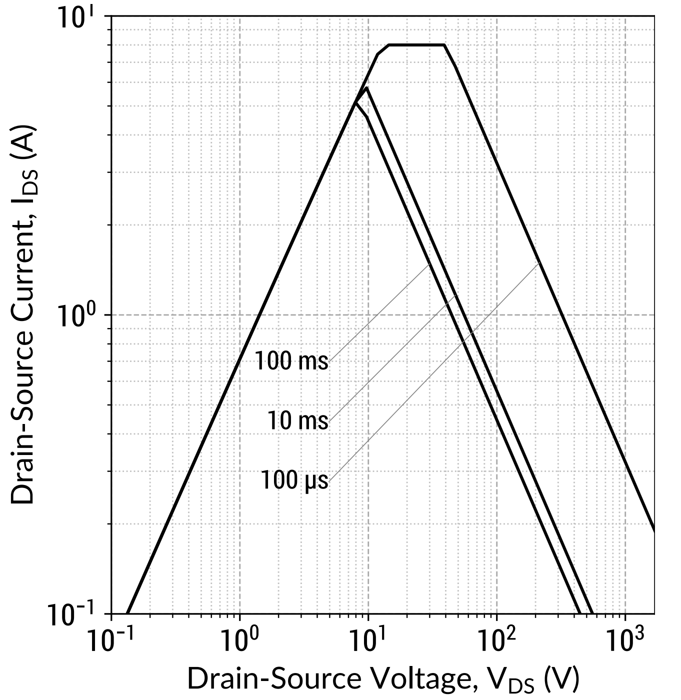
$E_{oss} = f(V_{DS})$

Figure 12: Transient Thermal Impedance



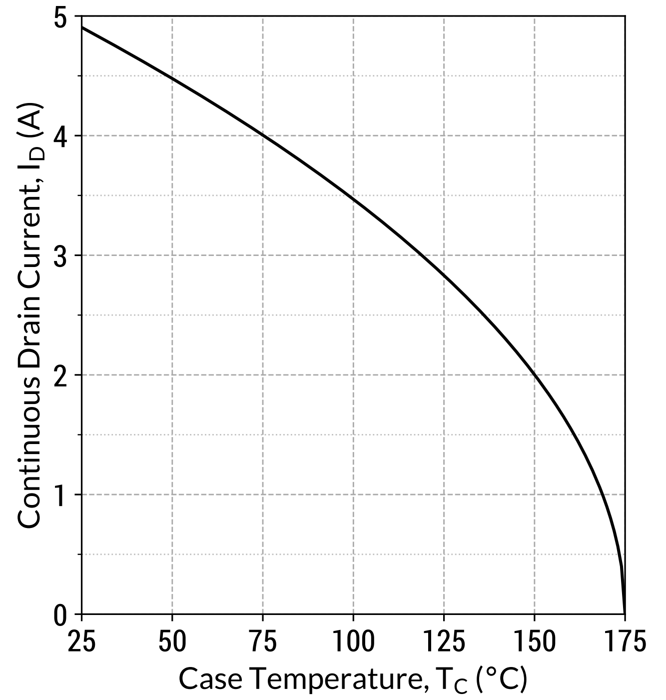
$Z_{th,jc} = f(t_P, D)$; $D = t_P/T$

Figure 13: Safe Operating Area (T_c = 25°C)



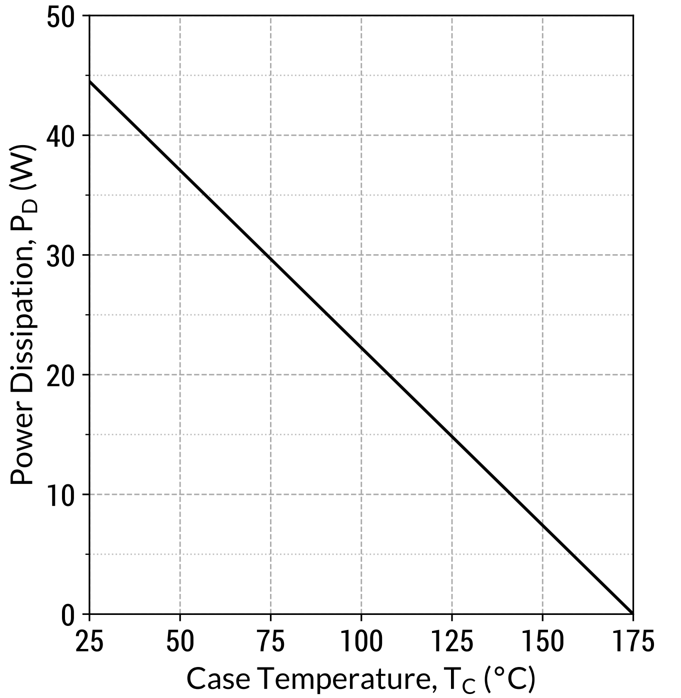
$I_D = f(V_{DS}, t_P)$; $T_j \leq 175°C$; D = 0

Figure 14: Current De-rating Curve



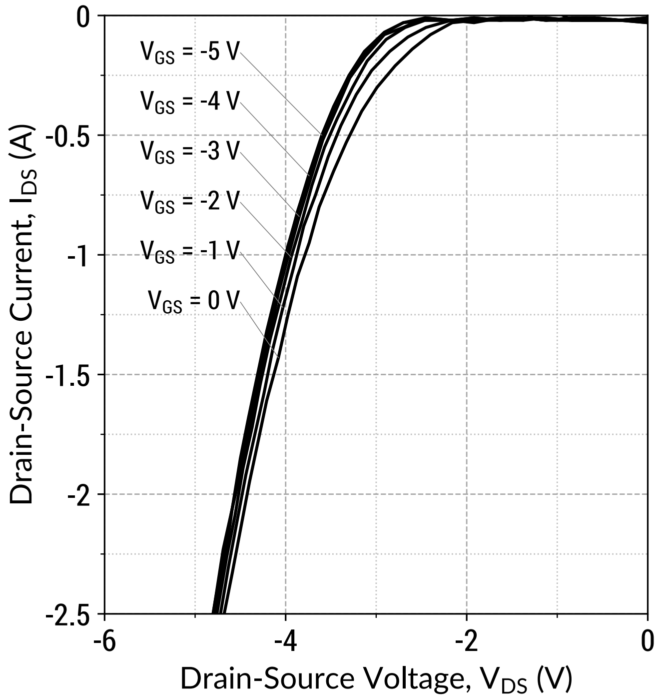
$I_D = f(T_C)$; $T_j \leq 175°C$

Figure 15: Power De-rating Curve



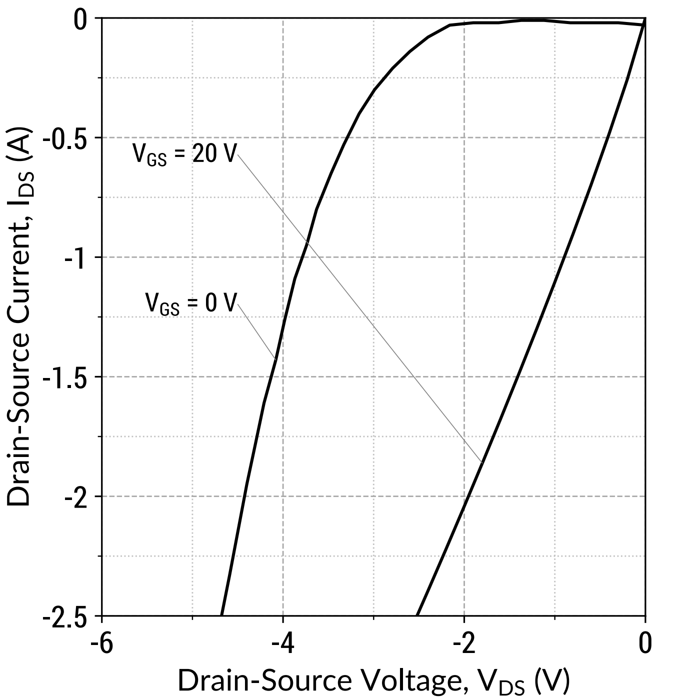
$P_D = f(T_C)$; $T_j \leq 175°C$

Figure 16: Body Diode Characteristics (T_j = 25°C)



$I_D = f(V_{DS}, V_{GS})$; t_P = 250 µs

Figure 17: Third Quadrant Characteristics (T_j = 25°C)

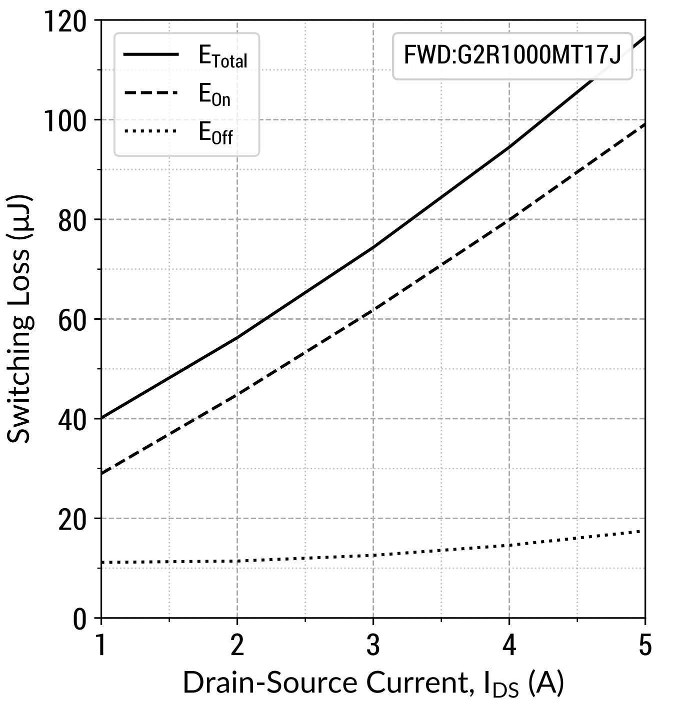


I_D = f(V_{DS}, V_{GS}); t_P = 250 µs

Figure 18: Inductive Switching Energy v/s Drain Current (V_{DD} = 1000V)

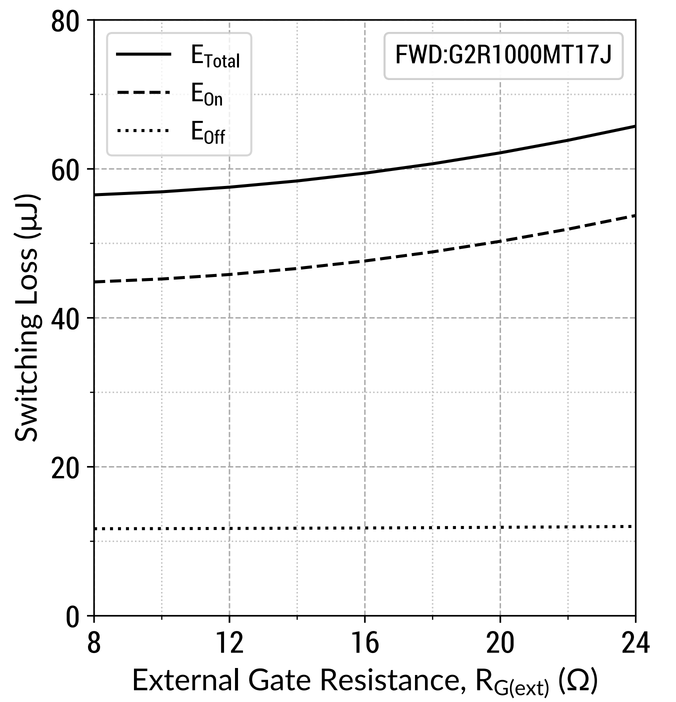
T_j = 25°C; V_{GS} = -5/+20V; $R_{G(ext)}$ = 8 Ω; L = 1000.0µH

Figure 19: Inductive Switching Energy v/s Drain Current (V_{DD} = 1200V)



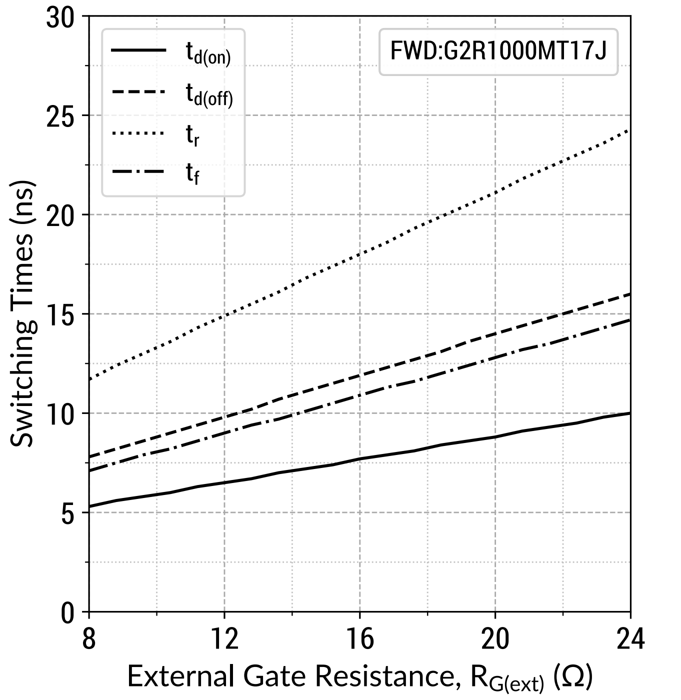
T_j = 25°C; V_{GS} = -5/+20V; $R_{G(ext)}$ = 8 Ω; L = 1000.0µH

Figure 20: Inductive Switching Energy v/s $R_{G(ext)}$ (V_{DD} = 1200V)



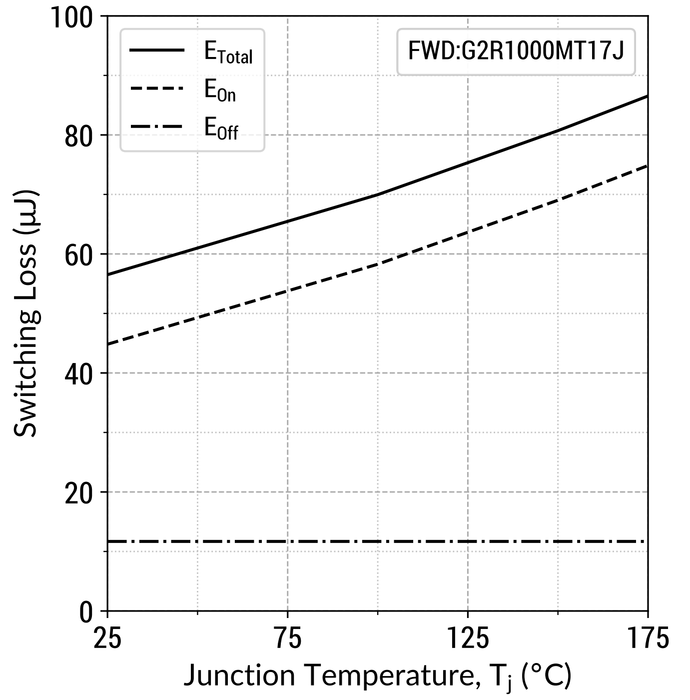
T_j = 25°C; V_{GS} = -5/+20V; I_{DS} = 2 A; L = 1000.0µH

Figure 21: Switching Time v/s $R_{G(ext)}$
(V_{DD} = 1200V)



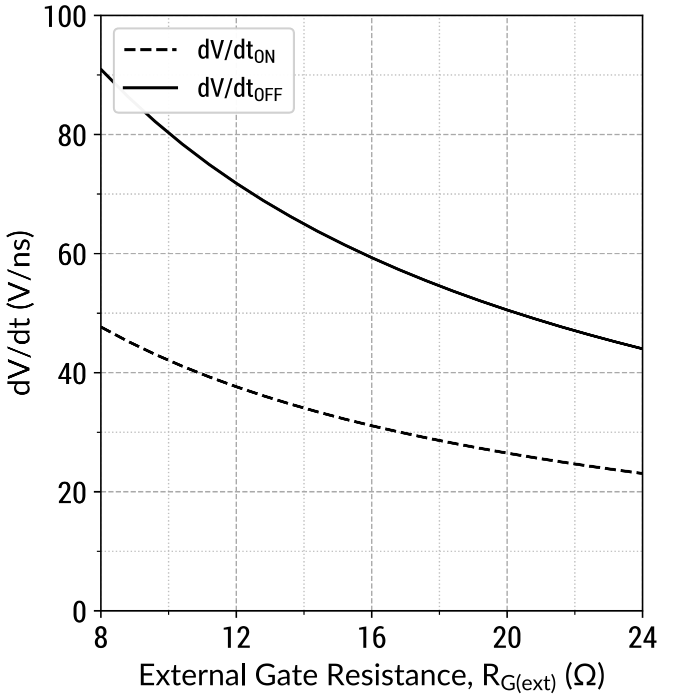
T_j = 25°C; V_{GS} = -5/+20V; I_{DS} = 2 A; L = 1000.0µH

Figure 22: Inductive Switching Energy v/s Temperature
(V_{DD} = 1200V)



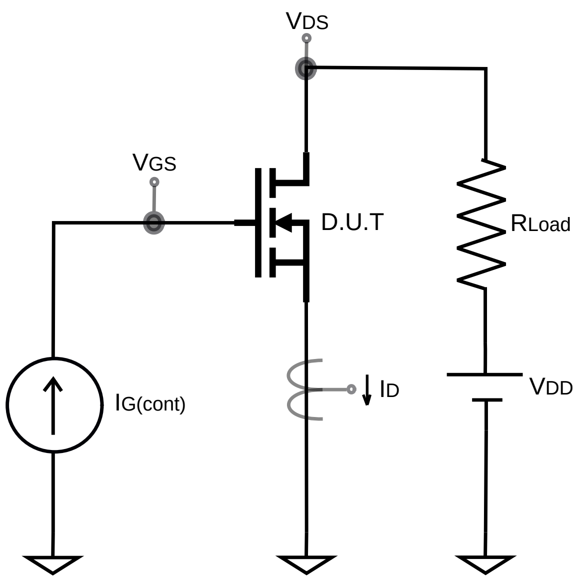
T_j = 25°C; V_{GS} = -5/+20V; $R_{G(ext)}$ = 8 Ω; I_{DS} = 2 A; L = 1000.0µH

Figure 23: dV/dt v/s $R_{G(ext)}$
(V_{DD} = 1200V)

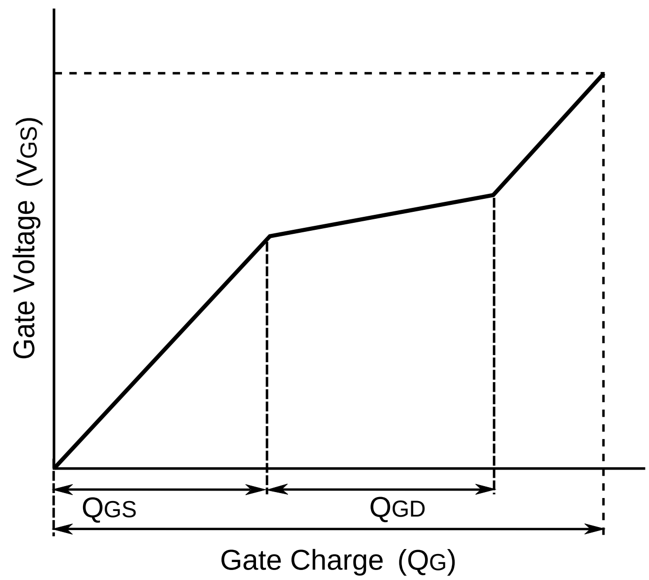


T_j = 25°C; V_{GS} = -5/+20V; I_{DS} = 2 A; L = 1000.0µH

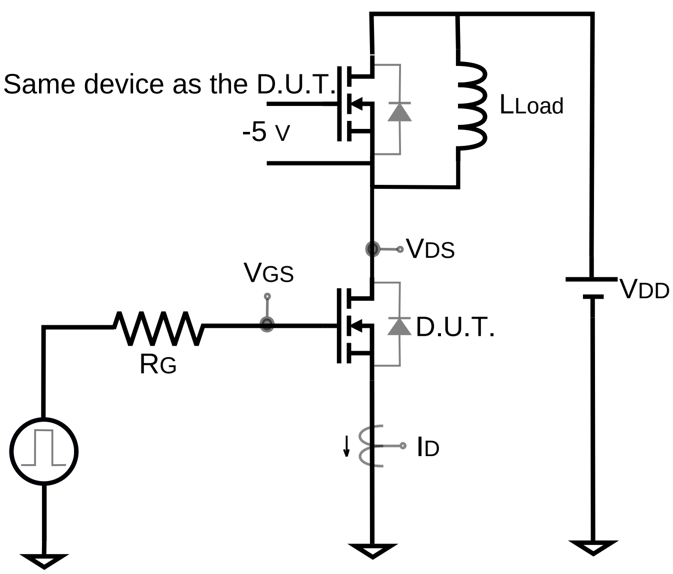
Gate Charge Circuit



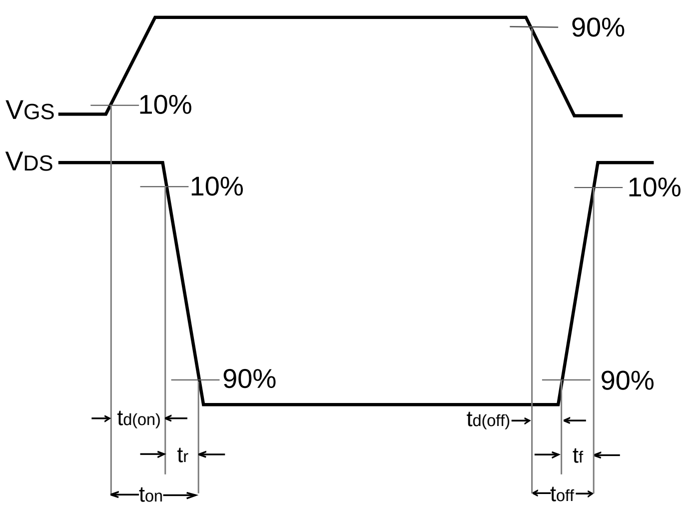
Gate Charge Waveform



Switching Time Circuit



Switching Time Waveform



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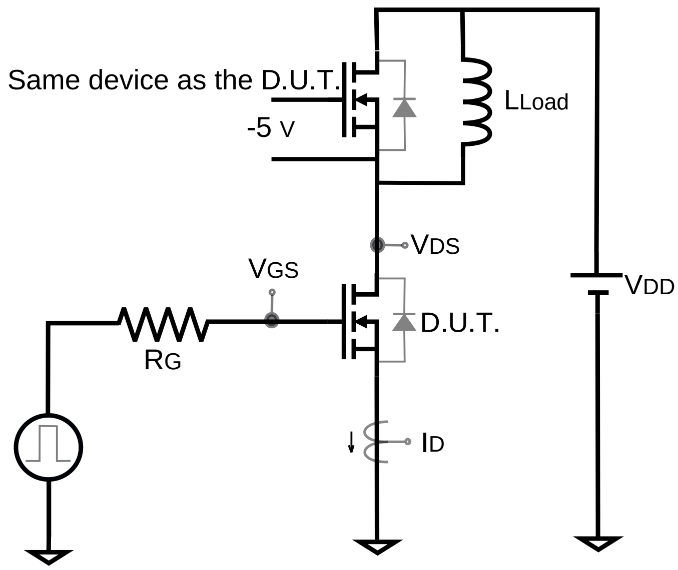
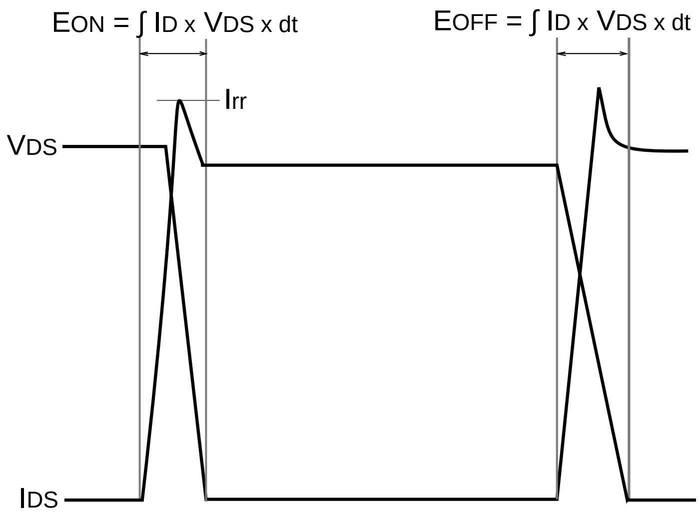
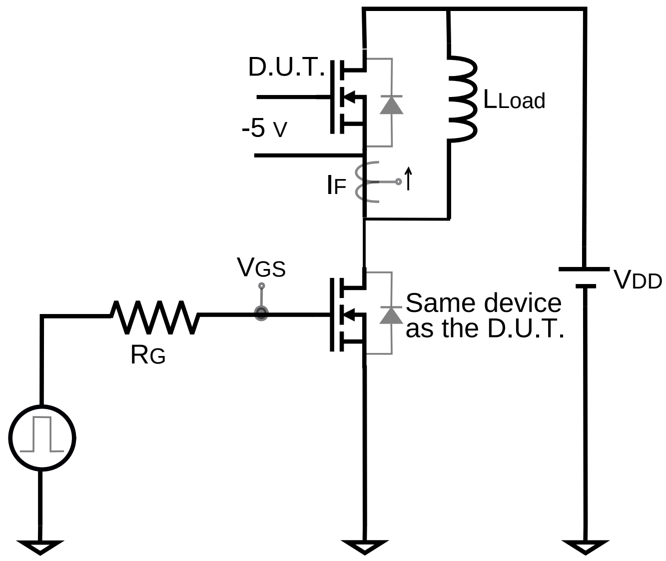
Switching Energy Circuit



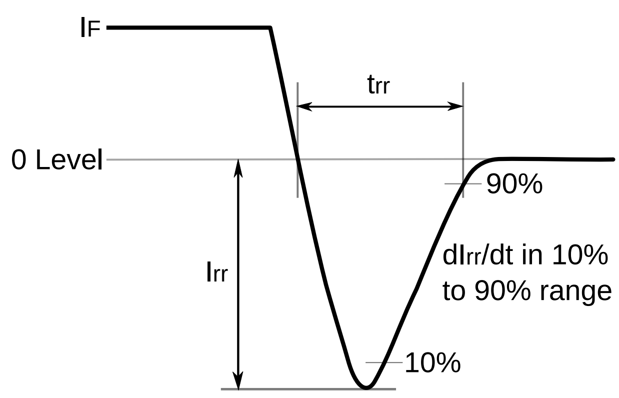
Switching Energy Waveform



Reverse Recovery Circuit

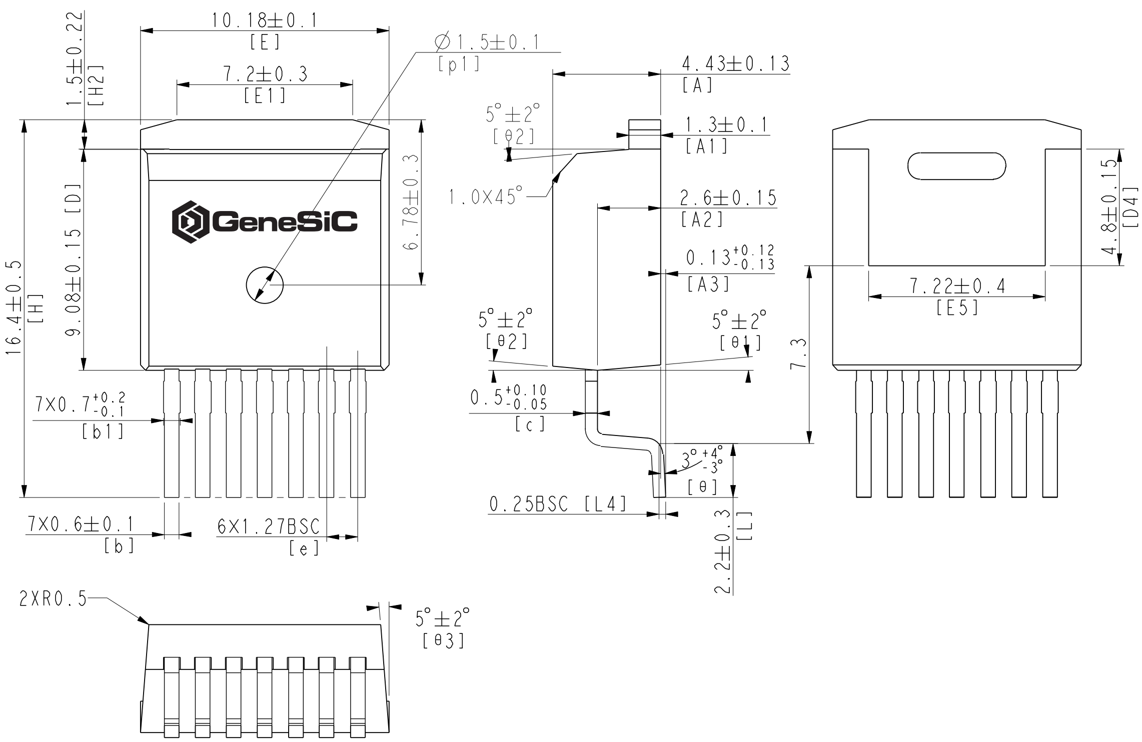


Reverse Recovery Waveform

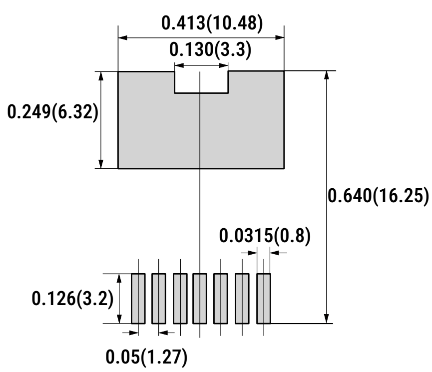


Package Dimensions

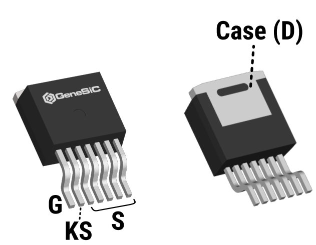
TO-263-7 Package Outline



Recommended Solder Pad Layout



Package View



NOTE

1. CONTROLLED DIMENSION IS INCH. DIMENSION IN BRACKET IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.
3. THE SOURCE AND KELVIN-SOURCE PINS ARE NOT INTERCHANGABLE. THEIR EXCHANGE MIGHT LEAD TO MALFUNCTION.

Compliance

RoHS Compliance

The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS 2), as adopted by EU member states on January 2, 2013 and amended on March 31, 2015 by EU Directive 2015/863. RoHS Declarations for this product can be obtained from your GeneSiC representative.

REACH Compliance

REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a GeneSiC representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.

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Related Links

- SPICE Models: https://www.genesicsemi.com/sic-mosfet/G2R1000MT17J/G2R1000MT17J_SPICE.zip
- PLECS Models: https://www.genesicsemi.com/sic-mosfet/G2R1000MT17J/G2R1000MT17J_PLECS.zip
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- Gate Driver Reference: https://www.genesicsemi.com/technical-support
- Evaluation Boards: https://www.genesicsemi.com/technical-support
- Reliability: https://www.genesicsemi.com/reliability
- Compliance: https://www.genesicsemi.com/compliance
- Quality Manual: https://www.genesicsemi.com/quality

Revision History

- Rev 21/May: Updated minimum Vth to 2V
- Supersedes: Rev 20/Jun, Rev 20/Aug, Rev 21/Feb

www.genesicsemi.com/sic-mosfet/

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