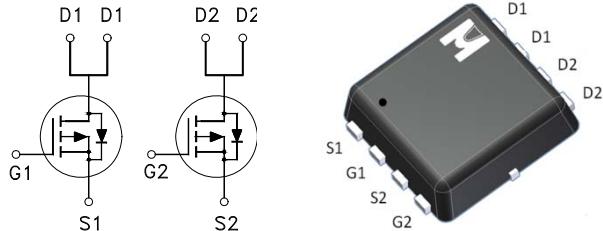


**P-Channel Logic Level Enhancement Mode Field Effect Transistor**

**Product Summary:**

BV <sub>DSS</sub>	-20V
R <sub>DSON</sub> (MAX.)	20mΩ
I <sub>D</sub>	-8.5A



Pb-Free Lead Plating & Halogen Free



**ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25 °C Unless Otherwise Noted)**

PARAMETERS/TEST CONDITIONS		SYMBOL	LIMITS	UNIT
Gate-Source Voltage		V <sub>GS</sub>	±12	V
Continuous Drain Current	T <sub>A</sub> = 25 °C	I <sub>D</sub>	-8.5	A
	T <sub>A</sub> = 70 °C		-6	
Pulsed Drain Current <sup>1</sup>		I <sub>DM</sub>	-34	
Power Dissipation	T <sub>A</sub> = 25 °C	P <sub>D</sub>	2	W
	T <sub>A</sub> = 70 °C		1.28	
Operating Junction & Storage Temperature Range		T <sub>j</sub> , T <sub>stg</sub>	-55 to 150	°C

**THERMAL RESISTANCE RATINGS**

THERMAL RESISTANCE	SYMBOL	TYPICAL	MAXIMUM	UNIT
Junction-to-Case	R <sub>θJC</sub>	25	62.5	°C / W
Junction-to-Ambient <sup>3</sup>	R <sub>θJA</sub>			

<sup>1</sup>Pulse width limited by maximum junction temperature.

<sup>2</sup>Duty cycle ≤ 1%

<sup>3</sup>62.5°C / W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.

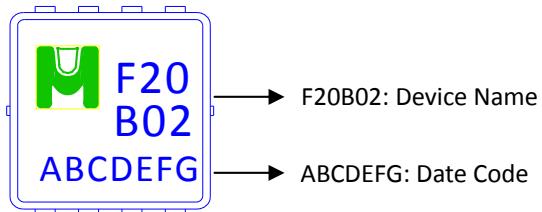
ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , Unless Otherwise Noted)

PARAMETER	SYMBOL	TEST CONDITIONS	LIMITS			UNIT
			MIN	TYP	MAX	
STATIC						
Drain-Source Breakdown Voltage	$V_{(\text{BR})\text{DSS}}$	$V_{GS} = 0\text{V}, I_D = -250\mu\text{A}$	-20			V
Gate Threshold Voltage	$V_{GS(\text{th})}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-0.4	-0.75	-1.2	
Gate-Body Leakage	$I_{GSS}$	$V_{DS} = 0\text{V}, V_{GS} = \pm 12\text{V}$			$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -16\text{V}, V_{GS} = 0\text{V}$			-1	$\mu\text{A}$
		$V_{DS} = -12\text{V}, V_{GS} = 0\text{V}, T_J = 125^\circ\text{C}$			-10	
On-State Drain Current <sup>1</sup>	$I_{D(\text{ON})}$	$V_{DS} = -5\text{V}, V_{GS} = -4.5\text{V}$	-8.5			A
Drain-Source On-State Resistance <sup>1</sup>	$R_{DS(\text{ON})}$	$V_{GS} = -4.5\text{V}, I_D = -8.5\text{A}$		15	20	$\text{m}\Omega$
		$V_{GS} = -2.5\text{V}, I_D = -4.5\text{A}$		19	25	
		$V_{GS} = -1.8\text{V}, I_D = -2.5\text{A}$		26	40	
Forward Transconductance <sup>1</sup>	$g_{fs}$	$V_{DS} = -5\text{V}, I_D = -8.5\text{A}$		22		S
DYNAMIC						
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{V}, V_{DS} = -10\text{V}, f = 1\text{MHz}$		3050		$\text{pF}$
Output Capacitance	$C_{oss}$			460		
Reverse Transfer Capacitance	$C_{rss}$			410		
Total Gate Charge <sup>1,2</sup>	$Q_g(V_{GS}=-4.5\text{V})$	$V_{DS} = -10\text{V}, V_{GS} = -4.5\text{V}, I_D = -8.5\text{A}$		27		$\text{nC}$
	$Q_g(V_{GS}=-2.5\text{V})$			16.5		
Gate-Source Charge <sup>1,2</sup>	$Q_{gs}$			2.2		
Gate-Drain Charge <sup>1,2</sup>	$Q_{gd}$			6.8		
Turn-On Delay Time <sup>1,2</sup>	$t_{d(\text{on})}$	$V_{DS} = -10\text{V}, I_D = -1\text{A}, V_{GS} = -4.5\text{V}, R_{GS} = 6\Omega$		20		$\text{nS}$
Rise Time <sup>1,2</sup>	$t_r$			50		
Turn-Off Delay Time <sup>1,2</sup>	$t_{d(\text{off})}$			90		
Fall Time <sup>1,2</sup>	$t_f$			60		
SOURCE-DRAIN DIODE RATINGS AND CHARACTERISTICS ( $T_c = 25^\circ\text{C}$ )						
Continuous Current	$I_S$				-2.3	A
Pulsed Current <sup>3</sup>	$I_{SM}$				-9.2	
Forward Voltage <sup>1</sup>	$V_{SD}$	$I_F = I_S, V_{GS} = 0\text{V}$			-1.2	V

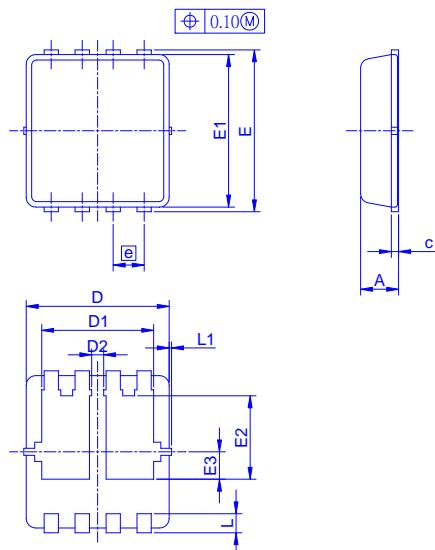
<sup>1</sup>Pulse test : Pulse Width  $\leq 300\text{ }\mu\text{sec}$ , Duty Cycle  $\leq 2\%$ .<sup>2</sup>Independent of operating temperature.<sup>3</sup>Pulse width limited by maximum junction temperature.

### Ordering & Marking Information:

Device Name: EMF20B02V for EDFN 3 x 3



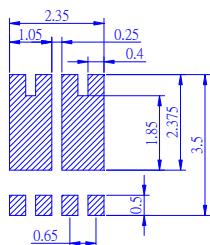
### Outline Drawing



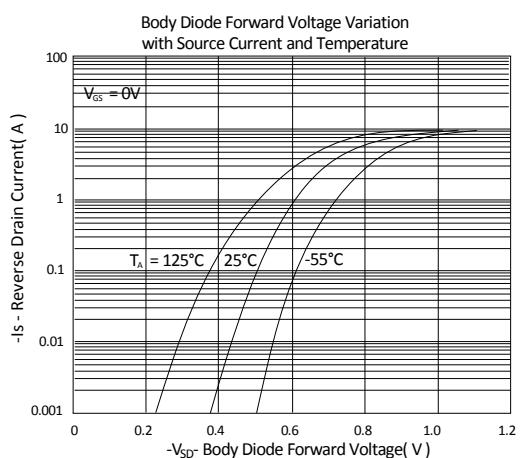
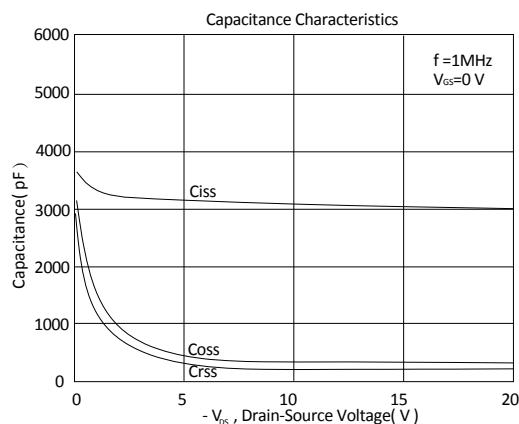
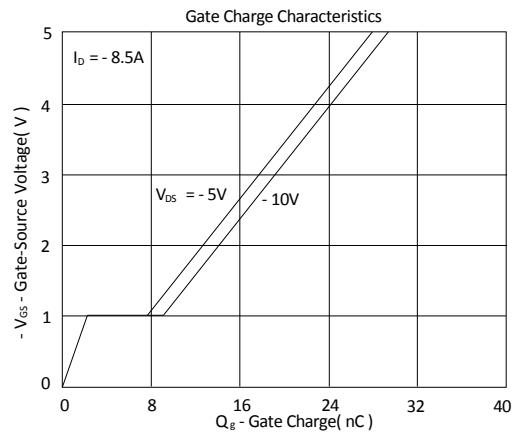
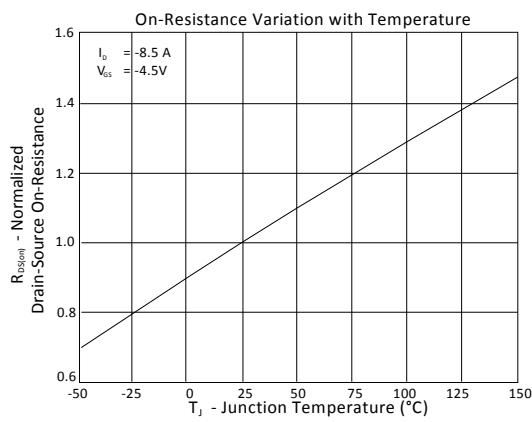
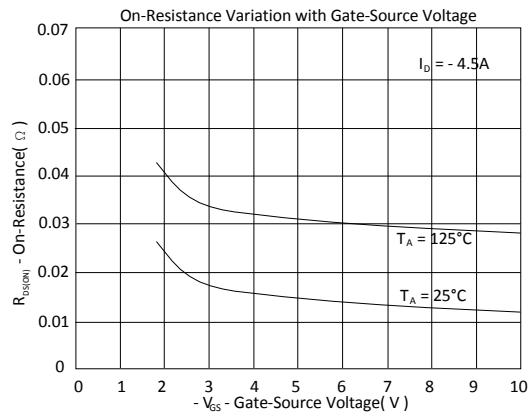
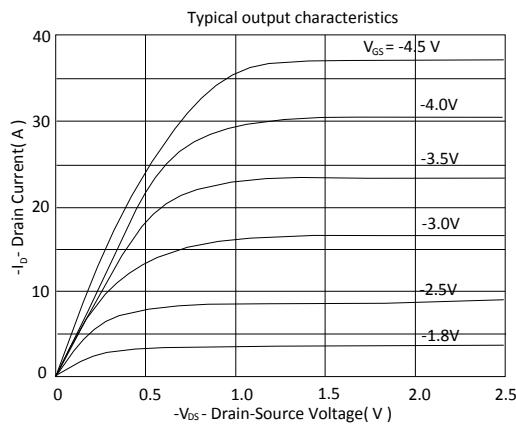
Dimension in mm

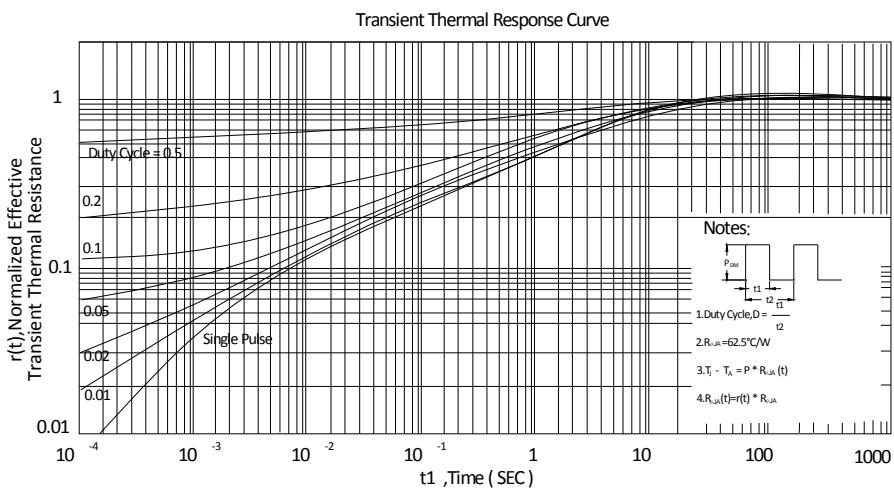
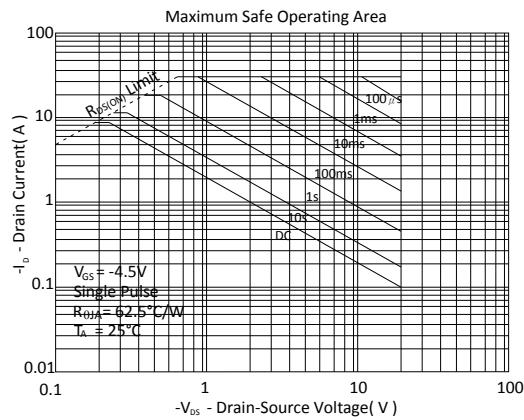
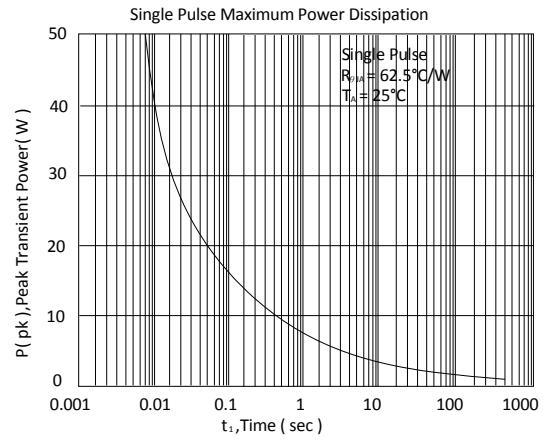
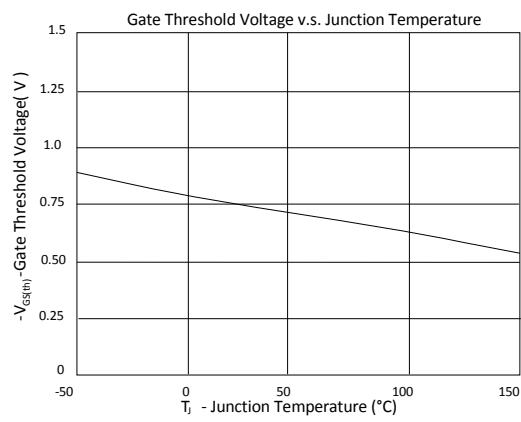
Dimension	A	A1	b	c	D	D1	D2	E	E1	E2	E3	e	L	L1	$\theta_1$
Min.	0.70	0	0.24	0.10	2.95	2.25		3.15	2.95	1.65			0.30	0	0°
Typ.	0.80		0.30	0.152	3.00	2.35	0.225	3.20	3.00	1.75	0.575	0.65	0.40		10°
Max.	0.90	0.05	0.35	0.25	3.05	2.45		3.25	3.05	1.85			0.50	0.10	12°

### Recommended minimum pads



## TYPICAL CHARACTERISTICS





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