

Description

The PAM8013 is a 3W mono filter-less class-D amplifier with high PSRR and differential input that eliminate noise and RF rectification.

Features like 90% efficiency and small PCB area make the PAM8013 class-D amplifier ideal for cellular handsets. The filter-less architecture requires no external output filter, fewer external components, less PCB area and lower system costs, and simplifies application design.

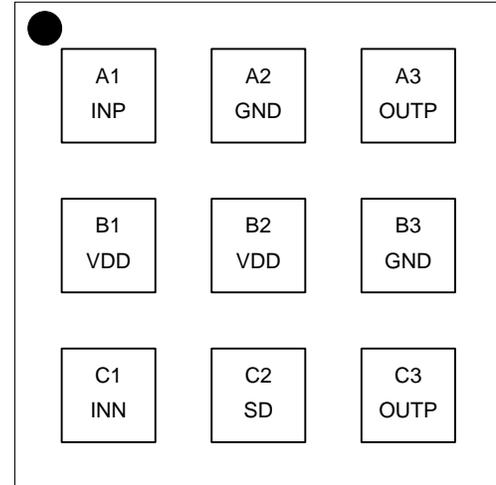
The PAM8013 features short circuit protection and thermal shutdown.

The PAM8013 is available in U-FLGA151-9 packages.

Features

- Ultra Low EMI, -20dB Better Than FCC Class-B @ 300MHz
- High Efficiency up to 90% @1W with an 8Ω Speaker
- Shutdown Current <1μA
- 3W@10% THD Output with a 4Ω Load at 5V Supply
- Demanding Few External Components
- Superior Low Noise without Input
- Supply Voltage from 2.8V to 5.5 V
- Short Circuit Protection
- Thermal Shutdown
- Available in Space Saving U-FLGA1515-9 Packages
- Pb-Free Package

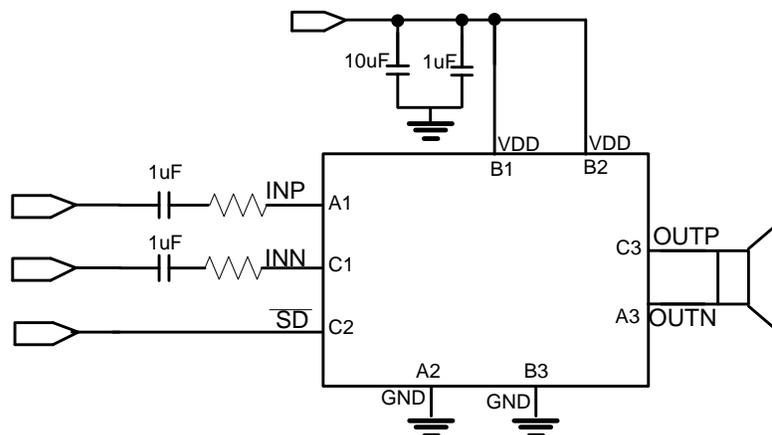
Pin Assignments



Applications

- Cellular Phones/Smart Phones
- MP4/MP3
- GPS
- Digital Photo Frame
- Electronic Dictionary
- Portable Game Machines

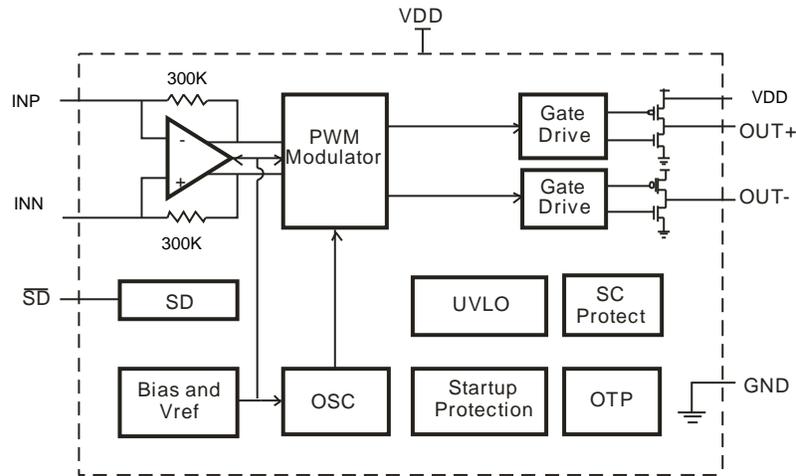
Typical Applications Circuit



Pin Descriptions

Pin Number	U-FLGA1515-9	Function
A1	INP	Positive differential input
A2	GND	Ground
A3	OUTN	Negative BTL output
B1	VDD	Power supply
B2	VDD	Power supply
B3	GND	Ground
C1	INN	Negative differential input
C2	SD	SD terminal to disable the chip
C3	OUTP	Positive BTL output

Functional Block Diagram



Absolute Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Parameter	Rating	Unit
Supply Voltage (VDD)	6.0	V
Input Voltage(IN+, IN-, CTRL)	-0.3 to V _{DD} +0.3	V
Storage Temperature	-65 to +150	°C
Maximum Junction Temperature	150	°C

Recommended Operating Conditions (@T_A = +25°C, unless otherwise specified.)

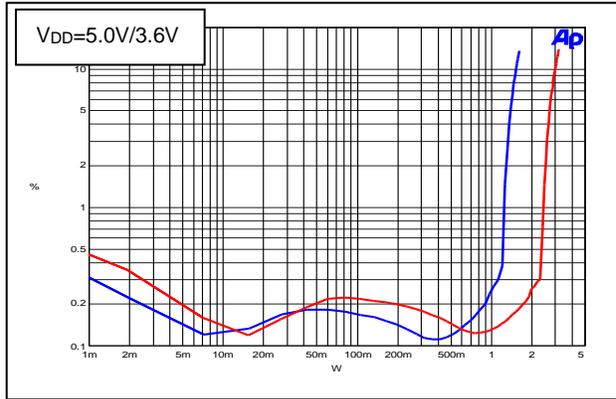
Symbol	Parameter	Min	Max	Unit
V _{DD}	Supply Voltage	2.8	5.5	V
T _A	Operating Ambient Temperature Range	-25	+85	°C
T _J	Junction Temperature Range	-40	+125	

Electrical Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, Gain = 18dB, $R_L = L(33\mu\text{H})+R+L(33\mu\text{H})$, unless otherwise noted.)

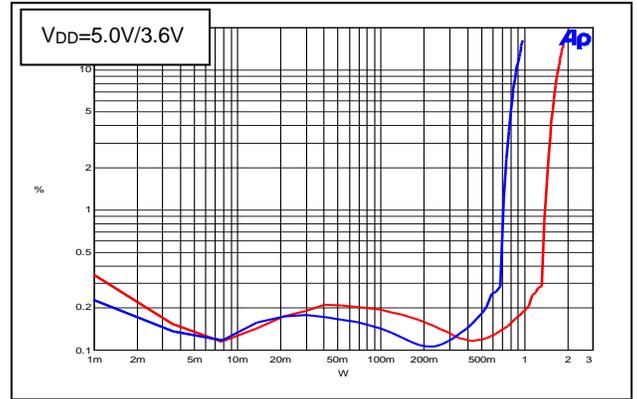
Symbol	Parameter	Test Conditions		Min	Typ	Max	Unit
V_{DD}	Supply Voltage			2.8		5.5	V
P_o	Output Power	THD+N = 10%, f = 1kHz, R = 4 Ω	$V_{DD} = 5.0\text{V}$		3.0		W
			$V_{DD} = 3.6\text{V}$		1.5		
			$V_{DD} = 3.2\text{V}$		1.2		
		THD+N = 1%, f = 1kHz, R = 4 Ω	$V_{DD} = 5.0\text{V}$		2.4		W
			$V_{DD} = 3.6\text{V}$		1.25		
			$V_{DD} = 3.2\text{V}$		1.0		
		THD+N = 10%, f = 1kHz, R = 8 Ω	$V_{DD} = 5.0\text{V}$		1.75		W
			$V_{DD} = 3.6\text{V}$		0.90		
			$V_{DD} = 3.2\text{V}$		0.70		
		THD+N = 1%, f = 1kHz, R = 8 Ω	$V_{DD} = 5.0\text{V}$		1.40		W
			$V_{DD} = 3.6\text{V}$		0.72		
			$V_{DD} = 3.2\text{V}$		0.60		
THD+N	Total Harmonic Distortion Plus Noise	f = 1kHz	$V_{DD} = 5.0\text{V}$, $P_o = 1\text{W}$, R = 8 Ω		0.17		%
			$V_{DD} = 3.6\text{V}$, $P_o = 0.1\text{W}$, R = 8 Ω		0.16		
			$V_{DD} = 3.2\text{V}$, $P_o = 0.1\text{W}$, R = 8 Ω		0.14		
		f = 1kHz	$V_{DD} = 5.0\text{V}$, $P_o = 0.5\text{W}$, R = 4 Ω		0.14		%
			$V_{DD} = 3.6\text{V}$, $P_o = 0.2\text{W}$, R = 4 Ω		0.16		
			$V_{DD} = 3.2\text{V}$, $P_o = 0.1\text{W}$, R = 4 Ω		0.17		
PSRR	Power Supply Ripple Rejection	$V_{DD} = 3.6\text{V}$, Inputs ac-grounded with C = 1 μF	f = 217Hz		-68		dB
			f = 1kHz		-70		
			f = 10kHz		-67		
Dyn	Dynamic Range	$V_{DD} = 5\text{V}$, THD = 1%, R = 8 Ω	f = 1kHz		95		dB
V_n	Output Noise	Inputs ac-grounded	No A weighting		170		μV
			A-weighting		130		
η	Efficiency	$R_L = 8\Omega$, THD = 10%	f = 1kHz		93		%
		$R_L = 4\Omega$, THD = 10%			86		
I_Q	Quiescent Current	$V_{DD} = 5\text{V}$	No Load		5		mA
I_{SD}	Shutdown Current	$V_{DD} = 2.8\text{V}$ to 5V	CTRL = 0V			1	μA
$R_{DS(ON)}$	Static Drain-to Source On-state Resistor	High Side PMOS, I = 500mA	$V_{DD} = 5.0\text{V}$		325		$\text{m}\Omega$
		Low Side NMOS, I = 500mA	$V_{DD} = 5.0\text{V}$		200		$\text{m}\Omega$
fsw	Switching Frequency	$V_{DD} = 2.8\text{V}$ to 5V			400		kHz
Gv	Closed-loop Gain	$V_{DD} = 2.8\text{V}$ to 5V			300K/ R_{IN}		V/V
R_{IN}	Input Impedance	$V_{DD} = 2.8\text{V}$ to 5V			28.5		K Ω
V_o	Output Offset Voltage	Input ac-ground, $V_{DD} = 5\text{V}$				20	mV
V_{IH}	SD Input High Voltage	$V_{DD} = 5\text{V}$		1.4			V
V_{IL}	SD Input Low Voltage	$V_{DD} = 5\text{V}$				1.0	

Performance Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, Gain = 18dB, $R_L = L(33\mu\text{H})+R+L(33\mu\text{H})$, unless otherwise noted.)

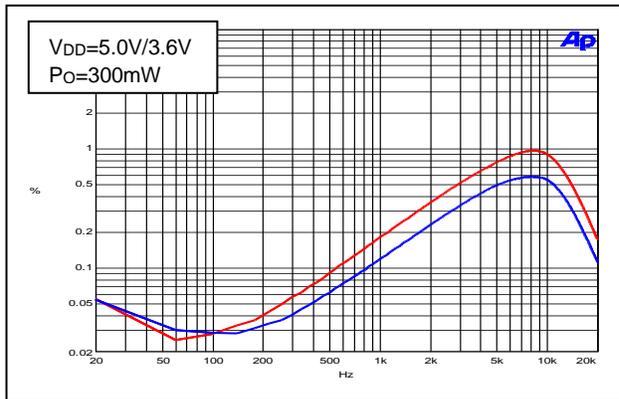
THD+N Vs. Output Power (RL=4Ω)



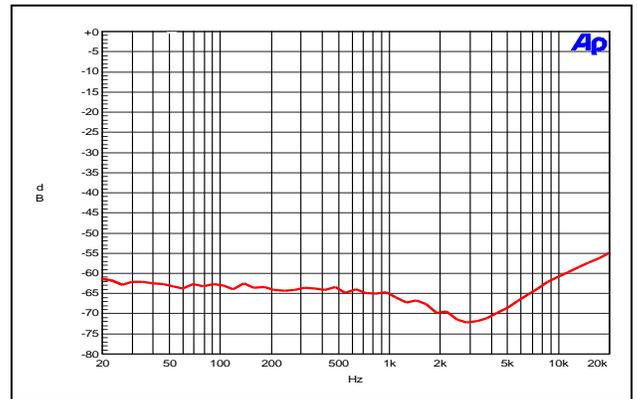
THD+N Vs. Output Power (RL=8Ω)



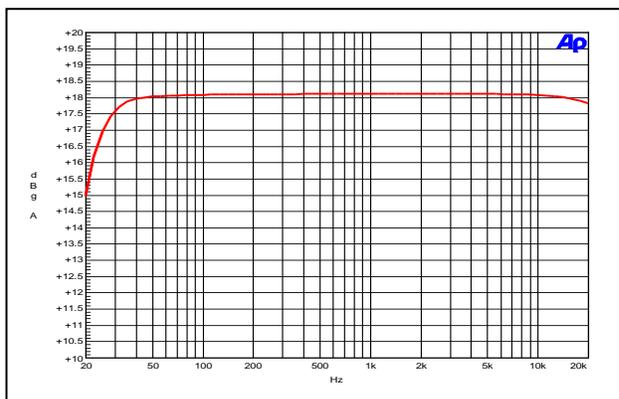
THD+N Vs. Frequency



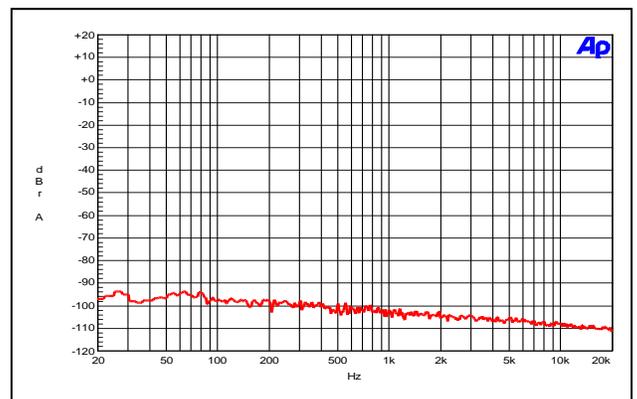
PSRR Vs. Frequency



Frequency Response

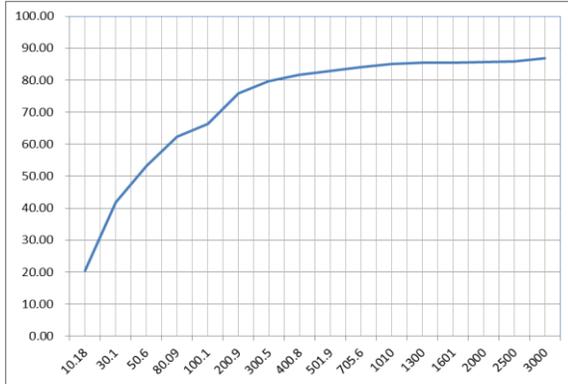


Noise Floor

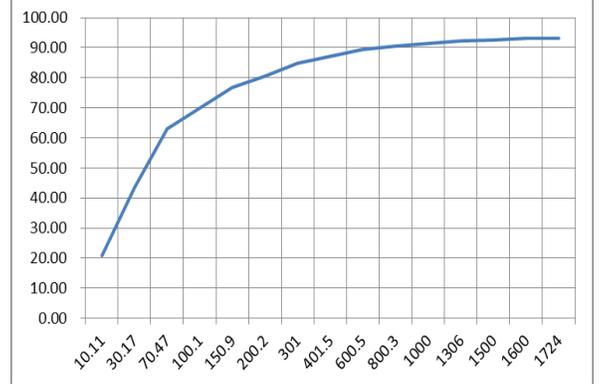


Performance Characteristics (@ $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{V}$, Gain = 18dB, $R_L = L(33\mu\text{H})+R+L(33\mu\text{H})$, unless otherwise noted.)

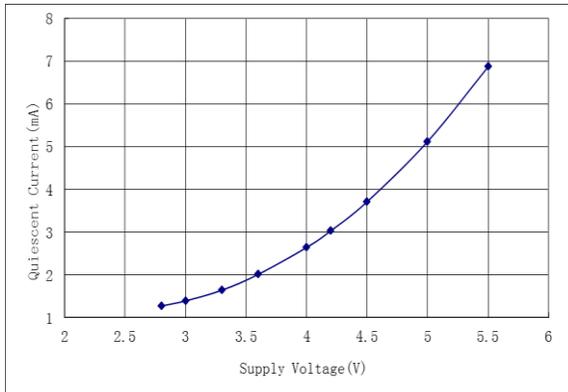
Efficiency Vs. Output Power (RL=4Ω)



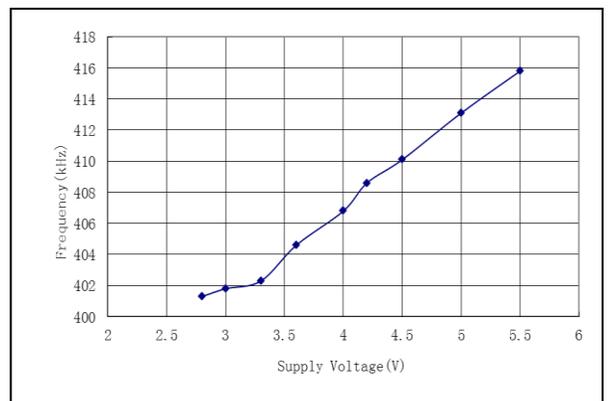
Efficiency Vs. Output Power (RL=8Ω)



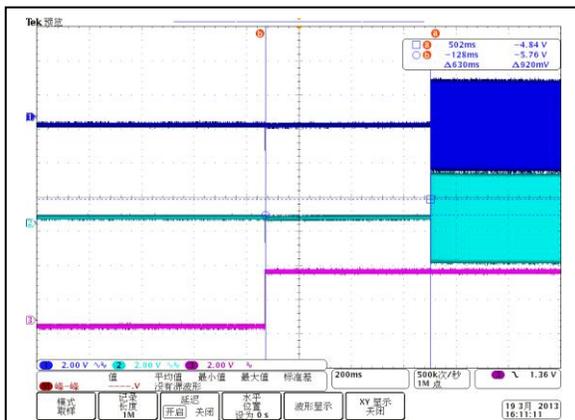
Quiescent Current vs. Supply Voltage



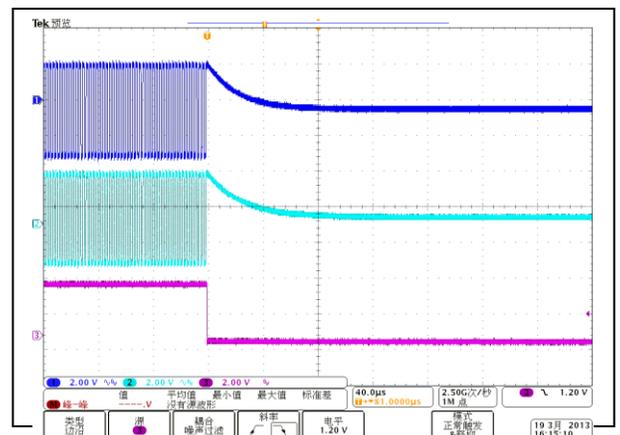
OSC Frequency vs. Supply Voltage



Start-up Response



Shutdown Response



Application Information

Input Capacitors (Ci)

In the typical application, an input capacitor, Ci, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, Ci and the minimum input impedance Ri form a high-pass filter with the corner frequency determined in the following equation:

$$f_c = \frac{1}{(2\pi R_i C_i)}$$

It is important to consider the value of Ci as it directly affects the low frequency performance of the circuit. For example, when Ri is 150kΩ and the specification calls for a flat bass response are down to 150Hz. Equation is reconfigured as followed:

$$C_i = \frac{1}{(2\pi R_i f_c)}$$

When input resistance variation is considered, the Ci is 7nF, so one would likely choose a value of 10nF. A further consideration for this capacitor is the leakage path from the input source through the input network (Ci, Ri + Rf) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level is held at VDD/2, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Decoupling Capacitor (CS)

The PAM8013 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 1μF, is placed as close as possible to the device VDD pin for the best operation. For filtering lower frequency noise signals, a large ceramic capacitor of 10μF or greater placed near the audio power amplifier is recommended.

How to Reduce EMI

Most applications require a ferrite bead filter for EMI elimination shown at Figure 1. The ferrite filter reduces EMI around 1MHz and higher. When selecting a ferrite bead, choose one with high impedance at high frequencies, but low impedance at low frequencies.

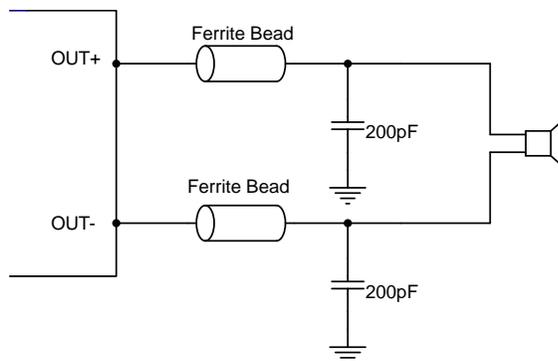


Figure 1: Ferrite Bead Filter to Reduce EMI

Application Information (cont.)

Shutdown operation

In order to reduce power consumption while not in use, the PAM8013 contains shutdown circuitry amplifier off when logic low is placed on the CTRL pin. By switching the shutdown pin connected to GND, the PAM8013 supply current draw will be minimized in idle mode.

Under Voltage Lock-out (UVLO)

The PAM8013 incorporates circuitry designed to detect low supply voltage. When the supply voltage drops to 2.0V or below, the PAM8013 goes into a state of shutdown, and the device comes out of its shutdown state and restore to normal function only when VDD higher than 2.2V.

Short Circuit Protection (SCP)

The PAM8013 has short circuit protection circuitry on the outputs to prevent the device from damage when output-to-output shorts or output-to-GND shorts occur. When a short circuit occurs, the device immediately goes into shutdown state. Once the short is removed, the device will be reactivated.

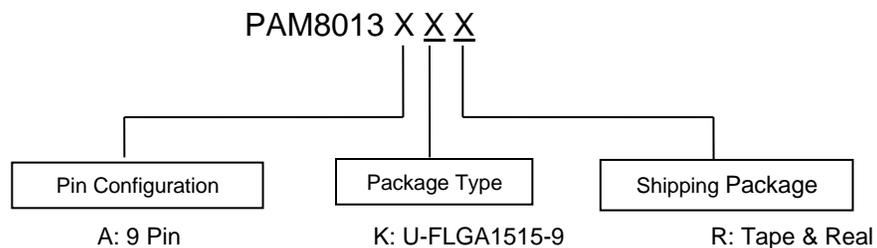
Over Temperature Protection (OTP)

Thermal protection on the PAM8013 prevents the device from damage when the internal die temperature exceeds 150°C. There is a 15°C tolerance on this trip point from device to device. Once the die temperature exceeds the set point, the device will enter the shutdown state and the outputs are disabled. This is not a latched fault. The thermal fault is cleared once the temperature of the die decreased by 40°C. This large hysteresis will prevent motor boating sound well and the device begins normal operation at this point with no external system interaction.

POP and Click Circuitry

The PAM8013 contains circuitry to minimize turn-on and turn-off transients or "click and pops", where turn-on refers to either power supply turn-on or device recover from shutdown mode. When the device is turned on, the amplifiers are internally muted. An internal current source ramps up the internal reference voltage. The device will remain in mute mode until the reference voltage reach half supply voltage, 1/2 V_{DD}. As soon as the reference voltage is stable, the device will begin full operation. For the best power-off pop performance, the amplifier should be set in shutdown mode prior to removing the power supply voltage.

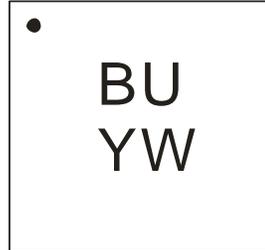
Ordering Information



Part Number	Package	Standard Package
PAM8013AKR	U-FLGA1515-9	3,000Units/Tape&Real

Marking Information

U-FLGA1515-9



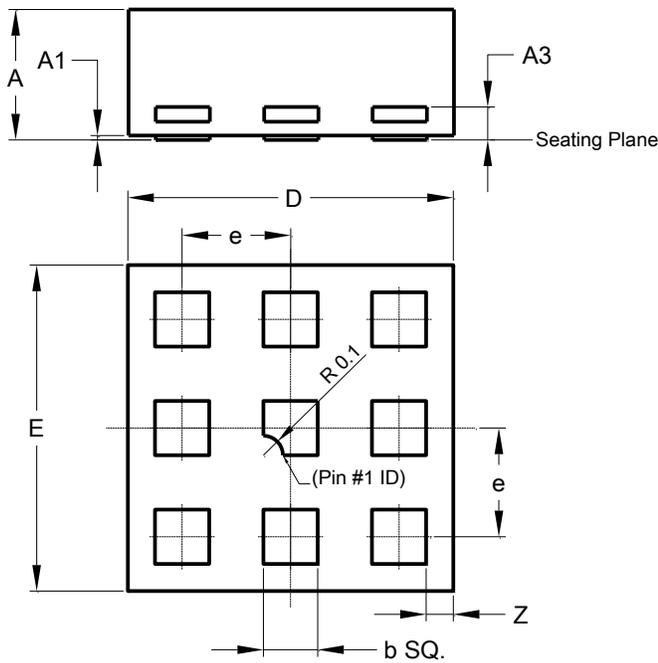
BU: Product Code

Y: Year

W: Week

Package Outline Dimensions (All dimensions in mm.)

Package: U-FLGA1515-9



U-FLGA515-9			
Dim	Min	Max	Typ
A	0.55	0.65	0.60
A1	0	0.05	0.02
A3	0.13 BSC		
b	0.20	0.30	0.25
D	1.45	1.55	1.50
E	1.45	1.55	1.50
e	0.50 BSC		
Z	0.125 BSC		
All Dimensions in mm			

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