Description

The AMS32M2006A series of industrial microcontrollers is based on the ARM® Cortex®-M0 processor core and operates at a frequency of up to 92MHz. The AMS32M2006A series is optimized for motor control, power conversion, home appliances, and general-purpose applications. The AMS32M2006A operates in the -40°C to +105°C temperature range from 2.3V to 5.5V wide voltage supply.

Features

- **CPU Subsystem**
  - CPU Core
    - ARM® Cortex®-M0 32-bit CPU (92MHz max) with Code Fetch Accelerator
    - Nested Vectored Interrupt Controller (NVIC) with 32 interrupt sources
    - 24-bit SysTick timer
    - Single cycle 32bit multiplier instruction
  - MATH Co-processor (MATH)
    - 24-bit trigonometric calculation (CORDIC)
    - Hardware Divider
- **Memories**
  - 8K bytes SRAM (Up to 12KB is configurable)
  - 4K bytes System Memory for loader
  - 60K bytes (max) Program Memory
    - Configurable Data Memory supported
- **Clock Management**
  - Internal oscillator: 8MHz±1.5%@ 2.3V~5.5V / -40°C~105°C
  - Internal oscillator: 32KHz±50%
  - External crystal oscillator : 4MHz ~ 12MHz
  - Phase Lock Loop : 92MHz(max)
    - The PLL output frequency based on M/N Coefficient
- **Power Management**
  - In SLEEP mode: Only the CPU stopped.
  - In DEEPSLEEP mode: All clocks are stopped.
- **System Control**
  - Up to 8 channels, DMA controller
    - Support peripheral: Timers, eCCU6, CCU4, ADCs, I^2Cs, UARTs, SPIs
  - Watchdog Timer (WDG) for safety sensitive applications
  - System Management Unit (SMU) for system configuration and control
  - 96-bit Unique ID
- **Reset Management**
  - Power On Reset (PORRESETn)
  - PAD Reset (PADRESETn)
  - Master Reset (MRESETn)
  - System Reset (SRESETn)
- **Analog Peripherals**
  - Up to 2 A/D Converters with 1M SPS and 17 analog inputs
  - Up to 2 fast Analog Comparators (ACMP)
  - Up to 4 Operational Amplifier (OPA)
    - With Unity gain frequency 20 MHz
    - Differential or Single input available
  - Die Temperature Sensor
  - Low Voltage Reset (2.1V, 2.7V, 3.2V, 4.2V)
  - Low Voltage Detector (2.4V, 2.9V, 3.4V, 4.4V)
- **Industrial Control Peripherals**
  - 16-bit Capture/Compare/PWM Units 4 (CCU4)
  - 16-bit Enhance Capture/Compare/PWM Units 6 (eCCU6)
    - For motor control and power conversion
  - 24-bit Position Interfaces (POSIF)
    - For hall and quadrature encoders and motor positioning
- **I/O Ports**
  - Max 40 fast multifunction bi-directional I/Os
    - All I/Os support external interrupt vectors
    - Built-in pull-up/pull-down resistor
    - I/O ports with 15mA/20mA source/sink current
- **Timer**
  - Up to 2 16bit general timer
- **Communication peripherals**
  - Up to 2 I2C
  - Up to 2 SPI (Clock 24MHz max)
  - Up to 3 UART
    - Full duplex & half duplex supported
- **Security**
  - 4 Security Levels supported
- **Debug System**
  - ARM serial wire debug (SWD)
  - 4 hardware breakpoints
  - 2 watch points
- **Operation Temperature**
  - -40°C to 105°C
- **Reliability**
  - HBM 4KV; MM 400V; CDM 500V
- **Package**
  - LQFP48
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/104/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please contact us or your local Diodes representative. https://www.diodes.com/quality/product-definitions/**

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

AMS 32 M 2 0 0 6 A

AMS	Diodes Analog Mixed-Signal MCU
32	32-bit ARM Cortex-M0 CPU
M	Motor control series
2	3-Phase FOC BLDC
0	General MCU With Motor Control function
06	2^6=64KB Flash size
A	IC Version

Figure 1. Part number rule

Selection Guide

The following table lists the available features of each device type for the AMS32M2006A series.

Table 1. AMS32M2006A Series Selection Guide

Features		AMS32M2006A
CPU Frequency		92MHz
Operating Temperature		Ambient temperature -40 to +105 °C
Operating Voltage		2.3 V to 5.5 V
Program Memory (Kbytes)		60
SRAM (Kbytes)		8+4
System Memory (Kbytes)		4
Security ROM (Kbytes)		--
Data Memory		V
MATH Processor		1
Industrial Control	**CCU4**	1
	eCCU6	1
	POSIF	1
Communication	**UART**	3
	I^2C	2
	SPI	2
Analog	**ADC**	2
	ACMP	2
	OPA	4
	LVR	1
	LVD	1
I/Os		40
Package		LQFP48

Package Pinout

LQFP48 package pinout

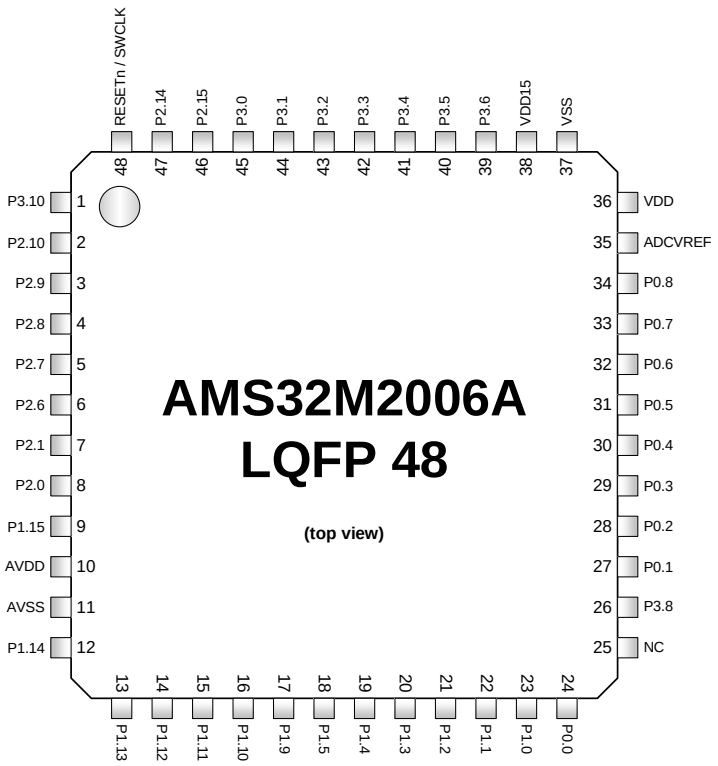


Figure 2. LQFP48 pinout

Pin Descriptions

ALT* = Alternate Functions Mode
P = Power Pin
G = Ground Pin
A = Analog Pin
I/O = Bidirectional Pin

Table 2. AMS32M2006A pin description

LQFP48	Pin Name	Type	ALT*	Description
1	P3.10	I/O	ALT = 0	General purpose I/O Port 3.10
	ADC1_CH6	A	ALT = 2	ADC1 analog input channel 6.
	CCU40_OUT3	I/O	ALT = 4	CCU40 output pin 3.
	I2C0_SCL	I/O	ALT = 8	I2C0 clock pin.
	SPI0_SS	I/O	ALT = 9	SPI0 slave select pin.
	UART1_TX	O	ALT = 10	UART1 TX pin.
	POSIF0_IN0	I	ALT = 11	Position Interface 0 input pin 0.
2	P2.10	I/O	ALT = 0	General purpose I/O Port 2.10
	ACMP3_OUT	O	ALT = 5	Comparator3 output pin.
	I2C1_SDA	I/O	ALT = 8	I2C1 data pin.
	SPI1_MOSI	I/O	ALT = 9	SPI1 master output slave input pin.
	UART2_TX	O	ALT = 10	UART2 TX pin.
3	P2.9	I/O	ALT = 0	General purpose I/O Port 2.9
	ACMP3_N5	A	ALT = 5	Comparator3 negative pin 5.
	I2C0_SCL	I/O	ALT = 8	I2C0 clock pin.
	SPI1_SCLK	I/O	ALT = 9	SPI1 serial clock pin.
	UART2_RX	I	ALT = 10	UART2 RX pin.
4	P2.8	I/O	ALT = 0	General purpose I/O Port 2.8
	ACMP2_OUT	O	ALT = 5	Comparator2 output pin.
	I2C0_SDA	I/O	ALT = 8	I2C0 data pin.
	SPI1_SS	I/O	ALT = 9	SPI1 slave select pin.
5	P2.7	I/O	ALT = 0	General purpose I/O Port 2.7
	ACMP2_N5	A	ALT = 5	Comparator2 negative pin 5.
	I2C0_SCL	I/O	ALT = 8	I2C0 clock pin.

LQFP48	Pin Name	Type	ALT*	Description
	UART1_TX	O	ALT = 10	UART1 TX pin.
6	P2.6	I/O	ALT = 0	General purpose I/O Port 2.6
	ACMP2_P5 / ACMP3_P5	A	ALT = 5	Comparator2 positive pin 5 / Comparator3 positive pin 5.
	I2C0_SDA	I/O	ALT = 8	I2C0 data pin.
	UART1_RX	I	ALT = 10	UART1 RX pin.
7	P2.1	I/O	ALT = 0	General purpose I/O Port 2.1
	OPA2_N	A	ALT = 6	Operation Amplifier 2 negative port.
8	P2.0	I/O	ALT = 0	General purpose I/O Port 2.0
	OPA2_P	A	ALT = 6	Operation Amplifier 2 positive port.
9	P1.15	I/O	ALT = 0	General purpose I/O Port 1.15
	OPA2_O	A	ALT = 6	Operation Amplifier 2 output port.
10	AVDD	P	--	ADC and OPA Supply Voltage. Capacitor is needed.
11	AVSS	G	--	ADC and OPA Ground.
12	P1.14	I/O	ALT = 0	General purpose I/O Port 1.14
	OPA1_N	A	ALT = 6	Operation Amplifier 1 negative port.
13	P1.13	I/O	ALT = 0	General purpose I/O Port 1.13
	OPA1_P	A	ALT = 6	Operation Amplifier 1 positive port.
14	P1.12	I/O	ALT = 0	General purpose I/O Port 1.12
	OPA1_O	A	ALT = 6	Operation Amplifier 1 output port.
15	P1.11	I/O	ALT = 0	General purpose I/O Port 1.11
	OPA0_O	A	ALT = 6	Operation Amplifier 0 output port.
16	P1.10	I/O	ALT = 0	General purpose I/O Port 1.10
	OPA0_P	A	ALT = 6	Operation Amplifier 0 positive port.
17	P1.9	I/O	ALT = 0	General purpose I/O Port 1.9
	OPA0_N	A	ALT = 6	Operation Amplifier 0 negative port.
18	P1.5	I/O	ALT = 0	General purpose I/O Port 1.5
	ADC1_CH5	A	ALT = 2	ADC1 analog input channel 5.
	OPA3_N	A	ALT = 6	Operation Amplifier 3 negative port.
	SPI1_SS	I/O	ALT = 9	SPI1 slave select pin.

LQFP48	Pin Name	Type	ALT*	Description
19	P1.4	I/O	ALT = 0	General purpose I/O Port 1.4
	ADC1_CH4	A	ALT = 2	ADC1 analog input channel 4.
	OPA3_P	A	ALT = 6	Operation Amplifier 3 positive port.
	SPI1_MISO	I/O	ALT = 9	SPI1 master input slave output pin.
20	P1.3	I/O	ALT = 0	General purpose I/O Port 1.3
	ADC1_CH3	A	ALT = 2	ADC1 analog input channel 3.
	OPA3_O	A	ALT = 6	Operation Amplifier 3 output port.
	SPI1_MOSI	I/O	ALT = 9	SPI1 master output slave input pin.
21	P1.2	I/O	ALT = 0	General purpose I/O Port 1.2
	ADC1_CH2	A	ALT = 2	ADC1 analog input channel 2.
	SPI1_SCLK	I/O	ALT = 9	SPI1 serial clock pin.
22	P1.1	I/O	ALT = 0	General purpose I/O Port 1.1
	ADC1_CH1	A	ALT = 2	ADC1 analog input channel 1.
	eCCU6_EXT_CK	I	ALT = 3	eCCU6 external clock input pin.
	CCU4_EXT_CK	I	ALT = 4	CCU40 external clock input pin.
	ACMP2_N4 / ACMP3_N4	A	ALT = 5	Comparator2 negative pin 4 / Comparator3 negative pin 4.
	TMU1_EXT_CK	I	ALT = 7	TMU1 external clock input pin.
	UART2_RX	I	ALT = 10	UART2 RX pin.
23	P1.0	I/O	ALT = 0	General purpose I/O Port 1.0
	ADC1_CH0	A	ALT = 2	ADC1 analog input channel 0.
	ACMP2_N6 / ACMP3_P6	A	ALT = 5	Comparator2 negative pin 6 / Comparator3 positive pin 6.
	CAP1	I	ALT = 7	TMU1 input capture channel.
	UART2_TX	O	ALT = 10	UART2 TX pin.
24	P0.0	I/O	ALT = 0	General purpose I/O Port 0.0
	ADC0_CH0	A	ALT = 2	ADC0 analog input channel 0.
	CAP0	I	ALT = 7	TMU0 input capture channel.
25	NC			It is recommended to connect to VSS.
26	P3.8	I/O	ALT = 0	General purpose I/O Port 3.8
	ADC1_CH7	A	ALT = 2	ADC1 analog input channel 7.

LQFP48	Pin Name	Type	ALT*	Description
	eCCU61_OUT0	I/O	ALT = 3	eCCU61 output pin 0.
	CCU40_OUT1	I/O	ALT = 4	CCU40 output pin 1.
	I2C1_SCL	I/O	ALT = 8	I2C1 clock pin.
	SPI0_MOSI	I/O	ALT = 9	SPI0 master output slave input pin.
	UART0_RX	I	ALT = 10	UART0 RX pin.
	POSIF0_IN1	I	ALT = 11	Position Interface 0 input pin 1.
27	P0.1	I/O	ALT = 0	General purpose I/O port 0.1
	ADC0_CH1	A	ALT = 2	ADC0 analog input channel 1.
	ACMP2_P4 / ACMP3_P4	A	ALT = 5	Comparator2 positive pin 4 / Comparator3 positive pin 4.
	TMU0_EXT_CK	I	ALT = 7	TMU0 external clock input pin.
28	P0.2	I/O	ALT = 0	General purpose I/O port 0.2
	ADC0_CH2	A	ALT = 2	ADC0 analog input channel 2.
	I2C1_SCL	I/O	ALT = 8	I2C1 clock pin.
	SPI0_SCLK	I/O	ALT = 9	SPI0 serial clock pin.
	UART0_TX	O	ALT = 10	UART0 TX pin.
29	P0.3	I/O	ALT = 0	General purpose I/O port 0.3
	ADC0_CH3	A	ALT = 2	ADC0 analog input channel 3.
	CCU40_OUT0	I/O	ALT = 4	CCU40 output pin 0.
	I2C1_SDA	I/O	ALT = 8	I2C1 data pin.
	SPI0_MOSI	I/O	ALT = 9	SPI0 master output slave input pin.
	UART0_RX	I	ALT = 10	UART0 RX pin.
30	P0.4	I/O	ALT = 0	General purpose I/O port 0.4
	ADC0_CH4	A	ALT = 2	ADC0 analog input channel 4.
	SPI0_MISO	I/O	ALT = 9	SPI0 master input slave output pin.
31	P0.5	I/O	ALT = 0	General purpose I/O Port 0.5
	ADC0_CH5	A	ALT = 2	ADC0 analog input channel 5.
	CCU40_OUT1	I/O	ALT = 4	CCU40 output pin 1.
	SPI0_SS	I/O	ALT = 9	SPI0 slave select pin.
32	P0.6	I/O	ALT = 0	General purpose I/O port 0.6

LQFP48	Pin Name	Type	ALT*	Description
	ADC0_CH6	A	ALT = 2	ADC0 analog input channel 6.
	ACMP2_P6	A	ALT = 5	Comparator2 positive pin 6.
	POSIF0_IN0	I	ALT = 11	Position Interface 0 input pin 0.
33	P0.7	I/O	ALT = 0	General purpose I/O port 0.7
	ADC0_CH7	A	ALT = 2	ADC0 analog input channel 7.
	CCU40_OUT2	I/O	ALT = 4	CCU40 output pin 2.
	ACMP2_P7	A	ALT = 5	Comparator2 positive pin 7.
	I2C0_SDA	I/O	ALT = 8	I2C0 data pin.
	POSIF0_IN1	I	ALT = 11	Position Interface 0 input pin 1.
34	P0.8	I/O	ALT = 0	General purpose I/O port 0.8
	ADC0_CH8	A	ALT = 2	ADC0 analog input channel 8.
	CCU40_OUT3	I/O	ALT = 4	CCU40 output pin 3.
	I2C0_SCL	I/O	ALT = 8	I2C0 clock pin.
	POSIF0_IN2	I	ALT = 11	Position Interface 0 input pin 2.
35	ADCVREF	P	--	ADC reference voltage. 2.2µF capacitor is needed on pin.
36	VDD	P	--	I/O ports, Regulator, LVD and LVR Supply Voltage.
37	VSS	G	--	System Ground.
38	VDD15	P	--	Regulator Output Voltage 1.5v. 2.2 µF capacitor is needed on pin.
39	P3.6	I/O	ALT = 0	General purpose I/O Port 3.6
	eCCU61_OVC	I	ALT = 3	eCCU61 over current detected input pin.
	SPI0_SS	I/O	ALT = 9	SPI0 slave select pin.
40	P3.5	I/O	ALT = 0	General purpose I/O Port 3.5
	eCCU61_OUT5	I/O	ALT = 3	eCCU61 output pin 5.
	SPI0_MISO	I/O	ALT = 9	SPI0 master input slave output pin.
41	P3.4	I/O	ALT = 0	General purpose I/O Port 3.4
	eCCU61_OUT4	I/O	ALT = 3	eCCU61 output pin 4.
	SPI0_MOSI	I/O	ALT = 9	SPI0 master output slave input pin.
42	P3.3	I/O	ALT = 0	General purpose I/O Port 3.3
	eCCU61_OUT3	I/O	ALT = 3	eCCU61 output pin 3.

LQFP48	Pin Name	Type	ALT*	Description
	SPI0_SCLK	I/O	ALT = 9	SPI0 serial clock pin.
43	P3.2	I/O	ALT = 0	General purpose I/O Port 3.2
	CKO	O	ALT = 1	Clock output pin.
	eCCU61_OUT2	I/O	ALT = 3	eCCU61 output pin 2.
44	P3.1	I/O	ALT = 0	General purpose I/O Port 3.1
	XTL_OUT	A	ALT = 1	XTAL output pin.
	eCCU61_OUT1	I/O	ALT = 3	eCCU61 output pin 1.
	UART1_TX	O	ALT = 10	UART1 TX pin.
45	P3.0	I/O	ALT = 0	General purpose I/O Port 3.0
	XTL_IN	A	ALT = 1	XTAL input pin.
	eCCU61_OUT0	I/O	ALT = 3	eCCU61 output pin 0.
	UART1_RX	I	ALT = 10	UART1 RX pin.
46	P2.15	I/O	ALT = 0	General purpose I/O Port 2.15
	SWDAT	I/O	ALT = 1	Serial Wire Debug Port data pin.
	I2C1_SDA	I/O	ALT = 8	I2C1 data pin.
	UART0_TX	O	ALT = 10	UART0 TX pin.
47	P2.14	I/O	ALT = 0	General purpose I/O Port 2.14
	ACMP3_N7	A	ALT = 5	Comparator3 negative pin 7.
	I2C1_SCL	I/O	ALT = 8	I2C1 clock pin.
	SPI1_MISO	I/O	ALT = 9	SPI1 master input slave output pin.
	UART0_RX	I	ALT = 10	UART0 RX pin.
48	RESETn / SWCLK	I	--	Reset pin with Serial Wire Debug clock pin function.

Alternative Functions

ALT* = Alternate Functions Mode

Table 3. Alternative functions map

GPIO	ICE/XTAL	ADC	eCCU6	CCU4	ACMP	OPA	TIMER	I2C	SPI	UART	POSIF
ALT=0	ALT=1	ALT=2	ALT=3	ALT=4	ALT=5	ALT=6	ALT=7	ALT=8	ALT=9	ALT=10	ALT=11
P0.0		ADC0_CH0	A				CPA0	I			
P0.1		ADC0_CH1	A				TM0_EXT_CK	I			
P0.2		ADC0_CH2	A		ACMP2_P4/ACMP3_P4	A		I2C1_SCL	I/O	SPI0_SCLK	I/O	UART0_TX	O		
P0.3		ADC0_CH3	A	CCU40_OUT0	I/O			I2C1_SDA	I/O	SPI0_MOSI	I/O	UART0_RX	I		
P0.4		ADC0_CH4	A							SPI0_MISO	I/O				
P0.5		ADC0_CH5	A	CCU40_OUT1	I/O					SPI0_SS	I/O				
P0.6		ADC0_CH6	A											POSIFO_IN0	I
P0.7		ADC0_CH7	A	CCU40_OUT2	I/O	ACMP2_P7	A	I2C0_SCL	I/O					POSIFO_IN1	I
P0.8		ADC0_CH8	A	CCU40_OUT3	I/O			I2C0_SDA	I/O					POSIFO_IN2	I
P1.0		ADC1_CH0	A			ACMP2_N6/ACMP3_P6	A					UART2_TX	O		
P1.1		ADC1_CH1	A	eCCU6_EXT_CK	I	ACMP2_N4/ACMP3_N3	A					UART2_RX	I		
P1.2		ADC1_CH2	A							SPI1_SCLK	I/O				
P1.3		ADC1_CH3	A							SPI1_MOSI	I/O				
P1.4		ADC1_CH4	A							SPI1_MISO	I/O				
P1.5		ADC1_CH5	A							SPI1_SS	I/O				
P1.9															
P1.10															
P1.11															
P1.12															
P1.13															
P1.14															
P1.15															
P2.0															
P2.1															
P2.6						ACMP2_P5/ACMP3_P5	A									
P2.7						ACMP2_N5	A	I2C0_SCL	I/O			UART1_TX	O		
P2.8						ACMP2_OUT	O	I2C0_SDA	I/O	SPI1_SS	I/O				
P2.9						ACMP3_N5	A	I2C0_SCL	I/O	SPI1_SCLK	I/O	UART2_RX	I		
P2.10						ACMP3_OUT	O	I2C1_SDA	I/O	SPI1_MOSI	I/O	UART2_TX	O		
P2.14						ACMP3_N7	A	I2C1_SCL	I/O	SPI1_MISO	I/O	UART0_RX	I		
P2.15	SWDAT	I/O						I2C1_SDA	I/O			UART0_TX	O		
P3.0	XTL_IN	A	eCCU61_OUT0	I/O								UART1_RX	I		
P3.1	XTL_OUT	A	eCCU61_OUT1	I/O								UART1_TX	O		
P3.2	CKO	O	eCCU61_OUT2	I/O											
P3.3			eCCU61_OUT3	I/O						SPI0_SCLK	I/O				
P3.4			eCCU61_OUT4	I/O						SPI0_MOSI	I/O				
P3.5			eCCU61_OUT5	I/O						SPI0_MISO	I/O				
P3.6			eCCU61_OVC	I						SPI0_SS	I/O				
P3.8		ADC1_CH7	A	eCCU61_OUT0	I/O	CCU40_OUT1	I/O			I2C1_SCL	I/O	SPI0_MOSI	I/O	UART0_RX	I	POSIFO_IN1	I
P3.10		ADC1_CH6	A	eCCU61_OUT1	I/O	CCU40_OUT3	I/O			I2C0_SCL	I/O	SPI0_SS	I/O	UART1_TX	O	POSIFO_IN0	I

Block Diagram - AMS32M2006A

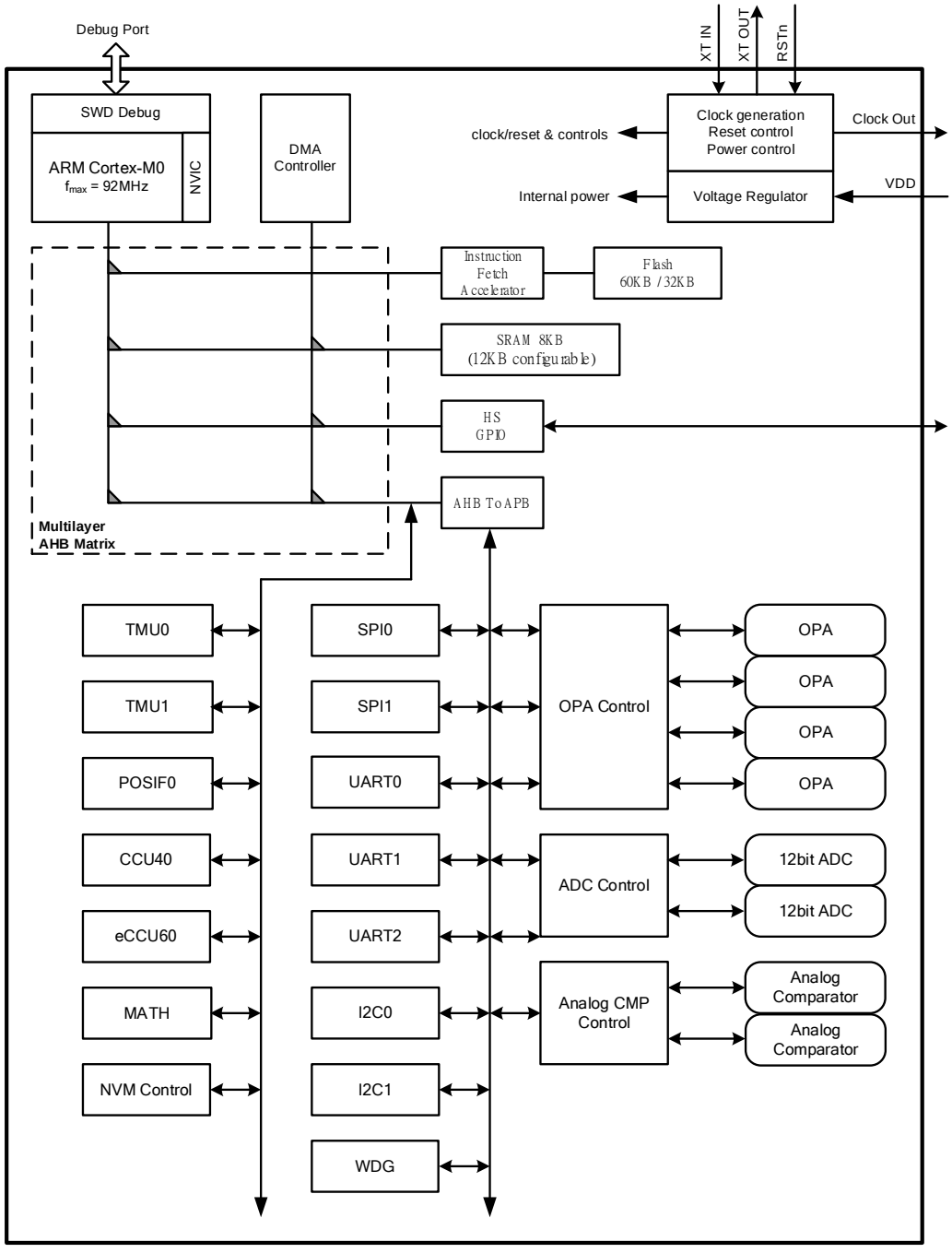


Figure 3. Function block diagram

Memory Organization - AMS32M2006A

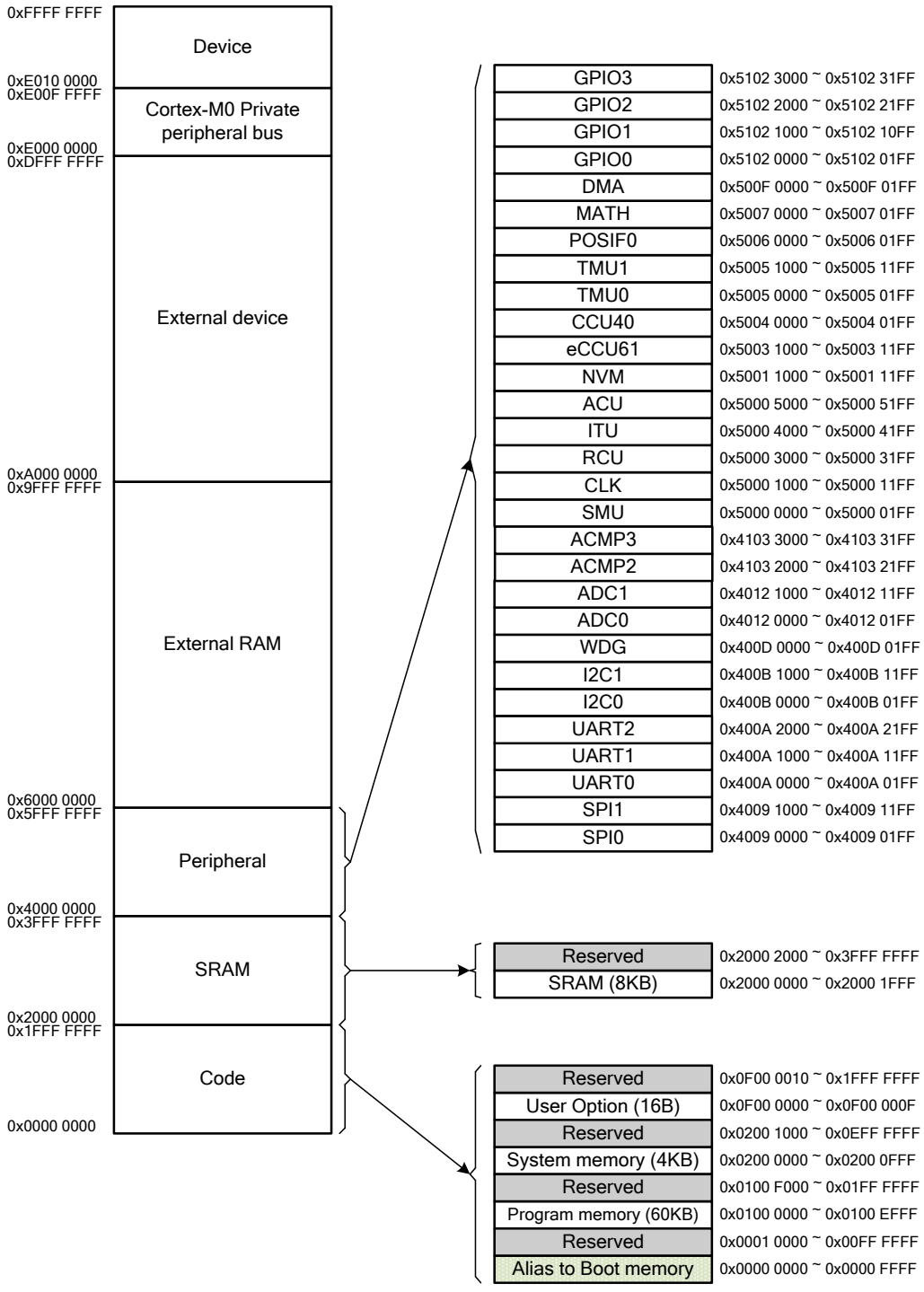


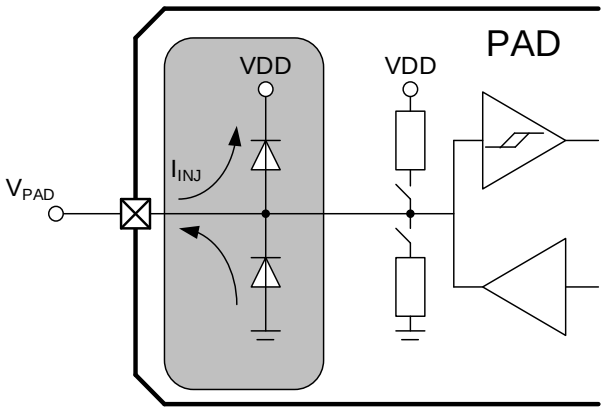
Figure 4. Memory map of AMS32M2006A

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Symbol	Parameter	Conditions	Min.	Max.	Unit
VDD	Input/Output/Regulator Supply Voltage	VDD to VSS	-0.3	6	V
AVDD	ADC Supply Voltage	AVDD to AVSS	-0.3	6	V
ADCVREF	ADC Reference Voltage	ADCVREF to AVSS	-0.3	6	V
VDD15	Regulator Output Voltage	VDD15 to VSS	1.35	1.8	V
V_{PAD}	Input Voltage On Pin	All I/O Pins	-0.3	6	V
ΣI_{VDD} (Note 4)	Total Current Into Power Lines (Source)	--		120	mA
ΣI_{VSS} (Note 4)	Total Current Out of Ground Lines (Sink)	--		-120	mA
I_{INJ} (Note 5)	Injected Current on Any Pin	V_{PAD} = VDD + 1.0v (Note 6) V_{PAD} = VSS - 1.0v (Note 6)	-5	5	mA
ΣI_{INJ} (Note 7)	Total Injected Current	Sum of All Pins	-25	25	mA

Notes: 4. In the permitted range, all main power (VDD, AVDD) and ground (VSS, AVSS) pins must always be connected to the external power supply.
5. Negative injection disturbs the analog performance of the device.
6. A positive injection is induced by V_{PAD} > VDD while a negative injection is induced by V_{PAD} < VSS. I_{INJ} must never be exceeded.
7. When several inputs are submitted to a current injection, the maximum ΣI_{INJ} is the absolute sum of the positive and negative injected currents (instantaneous values).



Electrostatic Discharge Ratings

Electrostatic discharges are applied to the pins of each sample according to each pin combination.

Symbol	Parameter	Conditions	Max.	Unit
V_{ESD}	Electrostatic Discharge Voltage	Human Body Model; All Pins. conforming to JESD22-A114	4000	V
		Machine Model. conforming to JESD22-A115-C	400	V
		Charged-Device Model, conforming to JESD22-C101	500	V
I_{LATCH}	I/O Latch-Up Current	Latch-Up test. conforming to JESD78	100	mA

Operation Conditions

The following operating conditions must not be exceeded in order to ensure correct operation and reliability of the AMS32M2006A. All parameters specified in the following tables refer to these operating conditions, unless noted otherwise.

Symbol	Parameter	Conditions	Min.	Max.	Unit
VDD	Standard operating voltage	TA = -40°C ~ +105°C	2.3	5.5	V
AVDD	ADC and OPA Operation Voltage	TA = -40°C ~ +105°C	2.3	5.5	V
f_{HCLK}	Internal AHB clock frequency	--	0(Note 8)	92	MHz
f_{PCLK}	Internal APB clock frequency	--	0(Note 8)	92	MHz
T_A	Ambient Temperature	--	- 40	+105	°C

Note: 8. Operation in deep sleep mode.

Power-Up/Down and Reset Characteristics

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

T_A = - 40°C to +105°C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$SR_{VDDRISE}$	VDD up slew rate	Slope during power-on or power up again after LVR event occurs	--	--	0.125	V/µs
$SR_{VDDFALL}$	VDD down slew rate	Slope during supply falling out of the +/-10% limits	--	--	0.04	V/µs
V_{POR}	Power-On Reset	--	--	1.1	--	V
V_{POR_ST}	VDD start voltage to ensure power-on reset	--	--	--	100	mV
tPCOV	Power-On Recovery Time	Time for VDD at or below V_{POR_ST}	1	--		ms
V_{LVR}	Low Voltage Reset	LVR_SEL = 00	-3%	2.1	+3%	V
		LVR_SEL = 01	-3%	2.7	+3%	V
		LVR_SEL = 10	-3%	3.2	+3%	V
		LVR_SEL = 11	-3%	4.2	+3%	V
V_{LVD}	Low Voltage Detect	LVD_SEL = 00	-3%	2.4	+3%	V
		LVD_SEL = 01	-3%	2.9	+3%	V
		LVD_SEL = 10	-3%	3.4	+3%	V
		LVD_SEL = 11	-3%	4.4	+3%	V

Supply Current Characteristics

Stresses above the values listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

T_A = +25°C; VDD = 5.5V, unless otherwise specified

Symbol	Parameter	Conditions	VDD (V)	All Peripheral ON.			All Peripheral OFF			Unit
				Min.	Typ.	Max.	Min.	Typ.	Max.	
IDD	Supply current in Normal Run, executing from Flash. Code: while (Note 9);	HCLK = 92MHz, from PLL (PLL input clock HSIRC 8MHz)	5.5	--	19.6	--	--	14.6	--	mA
			5	--	18.2	--	--	13.3	--	
			4.5	--	17.3	--	--	12.5	--	
			3.6	--	16.1	--	--	11.3	--	
			3.3	--	15.8	--	--	11.0	--	
			3	--	15.5	--	--	10.8	--	
			2.7	--	15.3	--	--	10.5	--	
			2.3	--	15.0	--	--	10.2	--	

Note: 9. Guaranteed by characterization results, not tested in production.

T_A = -40°C to +105°C; VDD = 2.3V to 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	Typ. @T_A (Note 10)						Unit
			-40˚C	-10˚C	0˚C	25˚C	85˚C	105˚C	
IDD_{STB}	Supply current in Deep-Sleep mode	VDD = 5.5V	5.99	6.05	6.09	6.50	15.34	28.18	μA
		VDD = 5.0V	5.25	5.30	5.38	5.78	14.50	27.13	
		VDD = 4.5V	4.80	4.83	4.88	5.31	13.85	26.38	
		VDD = 3.6V	4.18	4.24	4.29	4.74	13.14	25.47	
		VDD = 3.3V	4.04	4.08	4.13	4.53	12.97	25.35	
		VDD = 3.0V	3.92	3.95	4.07	4.43	12.81	24.97	
		VDD = 2.7V	3.72	3.76	3.83	4.20	12.56	24.69	
		VDD = 2.3V	3.55	3.61	3.65	4.06	12.37	24.47	

Note: 10. Guaranteed by characterization results, not tested in production.

GPIO Pin Characteristics

Below table provides the characteristics of the input/output pins.

TA = -40°C to +105°C; VDD = 2.3V to 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Standard IO Input Low Level Voltage	VDD=2.3V~5.5V,Schmitt Trigger Off	--	--	0.3*VDD	V
V_{IH}	Standard IO Input High Level Voltage	VDD=2.3V~5.5V, Schmitt Trigger Off	0.7*VDD	--	--	V
V_{T+}	Schmitt Trigger Positive Going Threshold	VDD=2.3V~5.5V, Schmitt Trigger On	--	0.66* VDD	--	V
V_{T-}	Schmitt Trigger Negative Going Threshold	VDD=2.3V~5.5V, Schmitt Trigger On	--	0.42* VDD	--	V
V_{HYS}	Standard IO Schmitt Trigger Voltage Hysteresis	VDD=2.3V~5.5V, Schmitt Trigger On	--	0.26* VDD	--	V
V_{OL} (Note 11)	Standard IO Output Low Level Voltage	OSPD =0, VDD = 3.3V, I_{sink} = 3.0mA	--	--	0.2*VDD	V
V_{OH} (Note 11)	Standard IO Output High Level Voltage	OSPD =0, VDD = 3.3V, I_{source} = 4.5mA	0.8*VDD	--	--	V
R_{PU} (Note 11)	Weak Pull-Up Equivalent Resistor	VDD = 3.3v, V_{PAD} = VSS	37	55	68	KΩ
R_{PD} (Note 11)	Weak Pull-Down Equivalent Resistor	VDD = 3.3V, V_{PAD} = 3.3V	37	55	68	KΩ
I_{LKG}	Input Leakage Current	VSS ≤ V_{PAD} ≤ VDD	-1	--	1	μA
I_{OL} (Note 11)	Standard IO Output Low Current	OSPD=0, VDD = 3.3v, V_{PAD} =0.2*VDD	--	5	--	mA
		OSPD =1, VDD = 3.3v, V_{PAD} =0.2*VDD	--	14.6	--	mA
I_{OH} (Note 11)	Standard IO Output High Current	OSPD =0, VDD = 3.3v, V_{PAD} =0.8*VDD	--	6.5	--	mA
		OSPD =1, VDD = 3.3v, V_{PAD} =0.8*VDD	--	12.5	--	mA
T_{FALL} (Note 12)	Output High to Low Level Fall Time	CL=30p, OSPD =0, SR = 0, VDD = 2.7v	--	9.73	--	ns
		CL=30p, OSPD =0, SR = 1, VDD = 2.7v	--	14.89	--	ns
		CL=30p, OSPD =1, SR = 0, VDD = 2.7v	--	3.68	--	ns
		CL=30p, OSPD =1, SR = 1, VDD = 2.7v	--	13.04	--	ns
T_{RISE} (Note 12)	Output Low to High Level Rise Time	CL=30p, OSPD =0, SR = 0, VDD = 2.7v	--	6.12	--	ns
		CL=30p, OSPD =0, SR = 1, VDD = 2.7v	--	11.42	--	ns
		CL=30p, OSPD =1, SR = 0, VDD = 2.7v	--	3.44	--	ns
		CL=30p, OSPD =1, SR = 1, VDD = 2.7v	--	10.54	--	ns
C_{IO}	I/O Pin Capacitance	--	--	5	--	pF

Notes: 11. Guaranteed by characterization results, not tested in production.
12. Guaranteed by design, not tested in production.

RESETn pin Characteristics

Below table provides the characteristics of the RESETn/SWCLK pins.

T_A = -40°C to +105°C; VDD = 2.3V to 5.5V, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Schmitt Trigger Positive Going Threshold	VDD=2.3V~5.5V, Schmitt Trigger On	--	--	0.3*VDD	V
V_{IH}	Schmitt Trigger Negative Going Threshold	VDD=2.3V~5.5V, Schmitt Trigger On	0.7*VDD	--	--	V
V_{HYS}	Standard IO Schmitt trigger voltage hysteresis	VDD=2.3V~5.5V, Schmitt Trigger On	--	0.26 VDD	--	V
R_{PU} (Note 13)	Weak pull-up equivalent resistor	VDD = 3.3V, V_{PAD} = VSS	15	21	27	KΩ
I_{LKG}	Input leakage current	VSS ≤ V_{PAD} ≤ VDD	-1	--	1	μA
C_{IO}	I/O pin capacitance	--	--	5	--	pF

Note: 13. Guaranteed by characterization results, not tested in production

External Crystal Oscillator Clock Characteristics

Below table provides the characteristics of the external crystal oscillator clock

T_A = -40°C to +105°C; VDD = 2.3V to 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSXTL}	Oscillator frequency	--	4	8	12	MHz
R_F (Note 15)	Feedback resistor	T_A = 25˚c , VDD = 5.5v	--	1500	--	KΩ
C_L (Note 14)	Recommended load capacitance versus equivalent serial resistance of the crystal (RS)	4MHz RS = 180Ω (Note 14) 8MHz RS = 60Ω (Note 14) 12MHz RS = 30Ω (Note 14)	--	20	--	pF
Duty (Note 14)	Duty cycle	--	45	50	55	%

Notes: 14. Guaranteed by characterization results, not tested in production.
15. Guaranteed by design, not tested in production.

Internal RC Clock Characteristics

High Speed Internal RC Clock Characteristics

Below table provides the characteristics of the high speed internal RC oscillator clock.

TA = -40°C to +105°C; VDD = 2.3V to 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{HSIRC}	Internal high speed RC frequency	--	--	8	--	MHz
Duty(Note 16)	Duty cycle	--	45	50	55	%
ACC_{HSIRC}	Accuracy of the HS oscillator	--	-1.5	--	1.5	%

Note: 16. Guaranteed by characterization results, not tested in production.

Low Speed Internal RC Clock Characteristics

Below table provides the characteristics of the low speed internal RC oscillator clock.

T_A = -40˚c to +105˚C; VDD = 2.3V to 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{LSIRC}	Internal low speed RC frequency	--	--	32	--	KHz
Duty	Duty cycle	--	40	50	60	%
ACC_{LSIRC}	Accuracy of the LS oscillator	--	-50	--	50	%

Phase Locked Loop (PLL) Characteristics

Below table provides the characteristics of the Phase Locked Loop.

T_A = -40˚C to +105˚C; VDD = 2.3V to 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
f_{PLL_IN}	PLL input clock	--	4	8	12	MHz
	PLL input clock duty cycle	--	45	50	55	%
f_{PLL_OUT}	PLL multiplier output clock	--	48	--	92	MHz
t_{LOCK}(Note 17)	PLL lock time	--	--	--	150	µS
Jitter(Note 18)	Cycle-to-Cycle Jitter (RMS)	VDD and VSS are ideal @ 92MHz	--	--	82.5	pS

Notes: 17. Guaranteed by characterization results, not tested in production.
18. Guaranteed by design, not tested in production.

12-bit Analog to Digital Converters (ADC) Characteristics

Below table provides the characteristics of the 12bit ADC.

T_A = -40˚C to +105˚C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD_{ADC}	ADC supply voltage	--	2.7	--	5.5	V
V_{ADCREF}	Built-in ADC reference voltage	ADC_GCTRL. ADC_VREF_SEL = 000@ VDD = 5.5V	-3%	1.8	+3%	V
		ADC_GCTRL. ADC_VREF_SEL = 001@ VDD = 5.5V	-3%	2.0	+3%	V
		ADC_GCTRL. ADC_VREF_SEL = 010@ VDD = 5.5V	-3%	2.4	+3%	V
		ADC_GCTRL. ADC_VREF_SEL = 011@ VDD = 5.5V	-3%	2.6	+3%	V
		ADC_GCTRL. ADC_VREF_SEL = 100@ VDD = 5.5V	-1.2%	3.0	+1.2%	V
		ADC_GCTRL. ADC_VREF_SEL = 101@ VDD = 5.5V	-3%	3.2	+3%	V
		ADC_GCTRL. ADC_VREF_SEL = 110@ VDD = 5.5V	-3%	3.4	+3%	V
		ADC_GCTRL. ADC_VREF_SEL = 111@ VDD = 5.5V	--	VDD_{ADC}	--	V
V_{ADCIN}	Conversion voltage range	--	0	--	V_{ADCREF}	V
RES_{ADC}	Resolution	--	--	12	--	Bit
t_{stable}	ADC stable time	ADC: From ADC enabled to the allowed reception 1st S&H.	0.65	--	--	µS
f_{ADC}	ADC clock frequency	VDD_{ADC} ≥ 5V	--	--	22	MHz
f_{SAMP} (Note 19)	Sampling rate	f_{ADC} = 22MHz, ts = 6 * 1/f_{ADC}	--	--	1.1	MHz
Rint (Note 20)	Sampling switch resistance	VDD_{ADC} = 5.5V	--	0.25	--	KΩ
C_S (Note 20)	Internal sample and hold capacitor	--	--	7	10	pF
Ts	Sampling time	f_{ADC} = 16MHz	0.0625	--	12.5	µS
			1	--	200	1/f_{ADC}
tconv (Note 20)	Total conversion time (including sampling time)	f_{ADC} = 16MHz	0.875	--	13.31	µS
			14 to 213 (ts for sampling +13 for successive approximation)			1/f_{ADC}
ED (Note 19)	Differential linearity error	VDD_{ADC} = 5.5V f_{ADC} = 22MHz	--	±1	--	LSB
EL (Note 19)	Integral linearity error		--	±3	--	LSB
ENOB	Effective Number Of Bits		--	10.3	--	Bits

Notes: 19. Guaranteed by characterization results, not tested in production.
20. Guaranteed by design, not tested in production.

Operation Amplifier (OPA) Characteristics

Below table provides the characteristics of the OPA.

T_A = -40˚C to +105˚C; VDD = 2.7V to 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
VDD_{OPA}	OPA supply voltage	--	2.7	--	5.5	V
V_{CMIR}	Common Mode Input Range	--	0	--	VDD_{OPA}-1	V
VOH_{OP}	High Saturation Voltage	VDD_{OPA} = 5.5V R_{LOAD} = 1K ohm，Gain = 10X。	5.1	--	--	V
VOL_{OP}	Low Saturation Voltage	VDD_{OPA} = 5.5V R_{LOAD} = 1K ohm，Gain = 10X。	--	--	0.2	V
V_{OFFSET}	Input Offset Voltage (Calibrated)	T_A = 25˚c,VDD_{OPA} = 5V	-3	--	+3	mV
PSRR(Note 21)	Power Supply Rejection Ratio	DC, VDD_{OPA} = 3.3V	--	80	--	dB
		T_A = 25˚c, VDD_{OPA} = 3.3V, At 10KHz/ 1Vp-p Ripple	--	70	--	dB
GBW(Note 21)	Bandwidth	T_A = 25˚c, VDD_{OPA} = 5V	--	20	--	MHz
SR(Note 21)	Slew Rate	T_A = 25˚c, VDD_{OPA} = 5.5V , Cload=50pF, Rload =10KΩ	--	15.3	--	V/μs

Note: 21. Guaranteed by characterization results, not tested in production.

Analog Comparator (ACMP) Characteristics

Below table provides the characteristics of the ACMP.

T_A = -40˚C to +105˚C; VDD = 2.3V to 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ACMP}	ACMP supply voltage	--	2.3	--	5.5	V
V_{ACMPIN}	Input voltage	--	-0.05	--	VDD	V
$V_{ACMPOFSET}$(Note 22)	Offset voltage	CMPx_HYS_EN = 0	--	10	--	mV
V_{ACMPIN}	Hysteresis window voltage	CMPx_HYS_EN = 1 CMPx_HYS_SEL= 00	--	20	--	mV
		CMPx_HYS_EN = 1 CMPx_HYS_SEL= 01	--	60	--	mV
		CMPx_HYS_EN = 1 CMPx_HYS_SEL= 10	--	120	--	mV
		CMPx_HYS_EN = 1 CMPx_HYS_SEL= 11	--	195	--	mV
t_{DELAY}(Note 23)	Propagation Delay	--	--	33	--	ns

Notes: 22. Guaranteed by characterization results, not tested in production.
23. Guaranteed by design, not tested in production.

Die Temperature Sensor Characteristics

Below table provides the characteristics of the Temperature Sensor.

T_A = -40˚C to +105˚C; VDD = 2.3V to 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Avg_Slope	Average slope	VDD = 5.0V	--	2.08	--	mV/˚C
V25 (Note 24)	Voltage at +25°C	VDD = 5.0V	--	0.579	--	V

Note: 24. Guaranteed by characterization results, not tested in production.

Flash Memory Characteristics

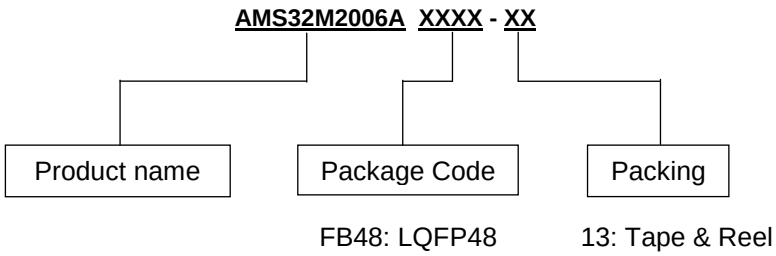
Below table provides the characteristics of the Flash Memory.

T_A = -40˚C to +105˚C; VDD = 2.3V to 5.5V, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
t_{PROG}	Programming time	--	23	--	--	μS
t_{PE}	Page (1K Bytes) erase time	--	2.2	--	--	mS
t_{ME}	Mass erase time	--	22	--	--	mS
t_{RET} (Note 25)	Data retention	at T_A = +25˚C	10	--	--	Years
N_{ECYC} (Note 25)	Endurance	erase/program	20000	--	--	Cycles

Note: 25. Guaranteed by characterization results, not tested in production.

Ordering Information (Note 26)



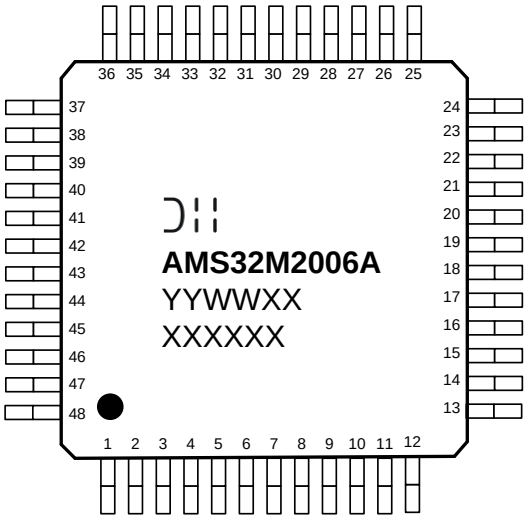
Part Number	Package Code	Packing	
		Qty.	Carrier
AMS32M2006A	FB48	2,000	13

Note: 26. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information

L-QFP7070-48

(Top View)



Logo :

Marking : AMS32M2006A

YY : Year : 22, 23, 24~

WW : Week : 01~52; 52 represents 52 and 53 week

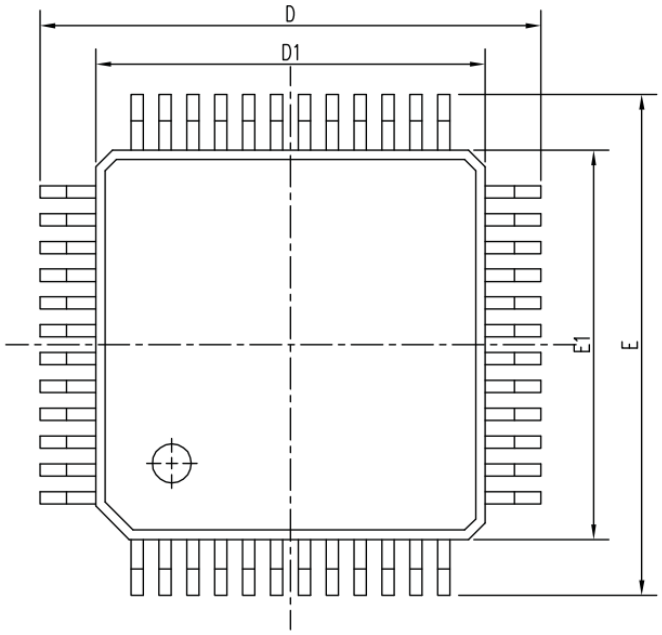
XX : Internal Code

XXXXXX : The primary 6 characters of the wafer lot

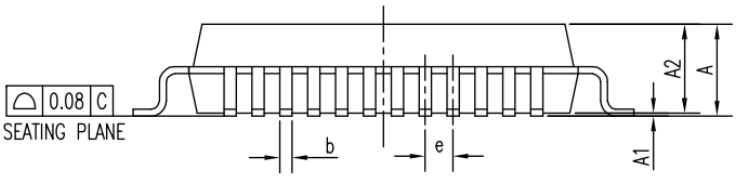
Package Outline Dimensions

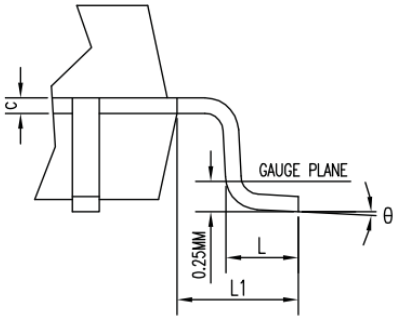
Please see http://www.diodes.com/package-outlines.html for the latest version.

LQFP48 (7x7x1.4mm footprint)



SYMBOL	DIMENSION IN MM		
	MIN.	NOM	MAX.
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
D	8.90	9.00	9.10
D1	6.90	7.00	7.10
E	8.90	9.00	9.10
E1	6.90	7.00	7.10
c	0.09	--	0.20
b	0.17	0.22	0.27
e	0.50 BSC.		
L1	1.00 REF.		
L	0.45	0.60	0.75
θ	0	3.5	7





Note:

1. ALL DIMENSIONS IN MM
2. REFER JEDEC MS-026/BBC
3. PACKAGE OUTLINE DIMENSIONS DO NOT INCLUDE MOLD FLASH AND METAL BURR

Revision History

Date	Revision #	Description	Pages
Dec. 15, 2023	1	Qualified data sheet, Web released	1-28
Feb. 06, 2024	2	Clarified analog peripherals	1

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