

## Description

The AL5887Q is comprised of 36 programmable LED current channels, each with internal 12-bit PWM for color and brightness control through I<sup>2</sup>C or SPI digital interface. The AL5887Q is ideal for lighting applications and features up to 12 RGB LED modules with 3 programmable banks (A, B, C) for software control of each color. An external resistor can set up the global output current of all 36 channels. Each channel current can be digitally configured up to 70mA under the thermal limitation of the package.

Features of the AL5887Q are controlled via a I<sup>2</sup>C/SPI digital interface, which is selectable by the INT\_SEL pin. The AL5887Q has a 30kHz, 12-bit PWM generator for each channel, as well as channel/module independent color mixing and brightness control registers to enable vivid LED effects with zero audible noise. Users can benefit from the device's ultra-low shutdown current (I<sub>Q</sub>, Power Saving Mode) and easy software programming.

The device operates over the -40°C to +125°C ambient temperature range, and is available in the wettable flank W-QFN6060-52/SWP (Type A1) package.

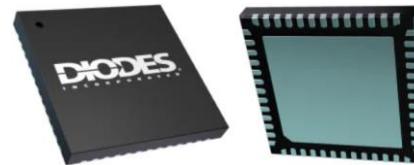
## Features

- AEC-Q100 Grade 1
- Input Voltage: 2.7V to 5.5V
- 36 Precision LED Current Sinks
  - OUT Pins Voltage Max. 5.5V
  - Maximum of 70mA per Channel Current
  - 12-Bit PWM Register with 30kHz Internal PWM Generator
  - PWM Phase Shifting
  - 6-Bit Global Current Dimming
  - Independent Color-Mixing Register per Channel
  - Independent Brightness-Control Register per RGB Module
  - Logarithmic or Linear Scale Brightness Control
  - Three Programmable Banks (A, B, C)
- Hardware-Selectable I<sup>2</sup>C or SPI Digital Interface
  - Support 400kHz I<sup>2</sup>C Interface and 4MHz SPI
- Diagnosis Protections Configurable Registers
  - Open Drain Fault Pin for Fault Indication
  - Individual Fault Mask Registers & Open/Short Registers
  - Overtemperature Protection (OTP) with Pre-OTP Warning
- Ultra-Low Quiescent Shutdown 1µA:
  - Power-Saving Mode: 15µA (Max.)
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The AL5887Q is suitable for automotive applications requiring specific change control; this part is AEC-Q100 qualified, PPAP capable, and manufactured in IATF 16949 certified facilities.**

<https://www.diodes.com/quality/product-definitions/>

## Pin Assignments

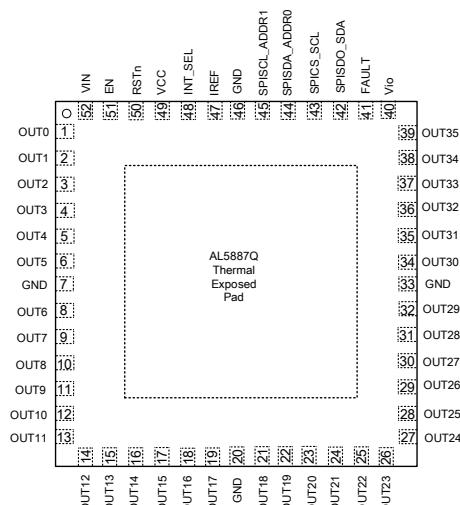
W-QFN6060-52/SWP (Type A1)



Top View

Bottom View

(Top View – Not to Scale)



W-QFN6060-52/SWP (Type A1)

## Applications

- Automotive interior and exterior lighting
- Infotainment displays
- Automotive status indicator lights
- Touch panels and LCD display backlights

## Device Information

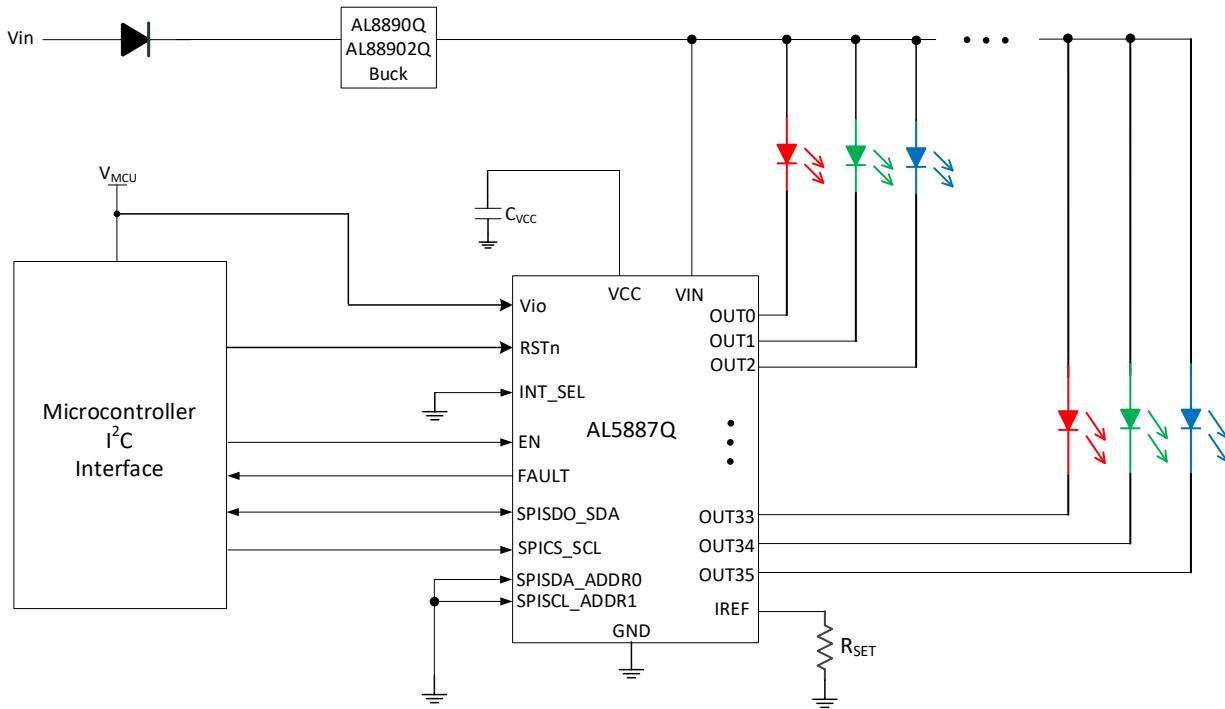
Orderable Part Number	Package	Body Size
AL5887QJAZW52-13	W-QFN6060-52/SWP (Type A1)	6mm x 6mm

Notes:

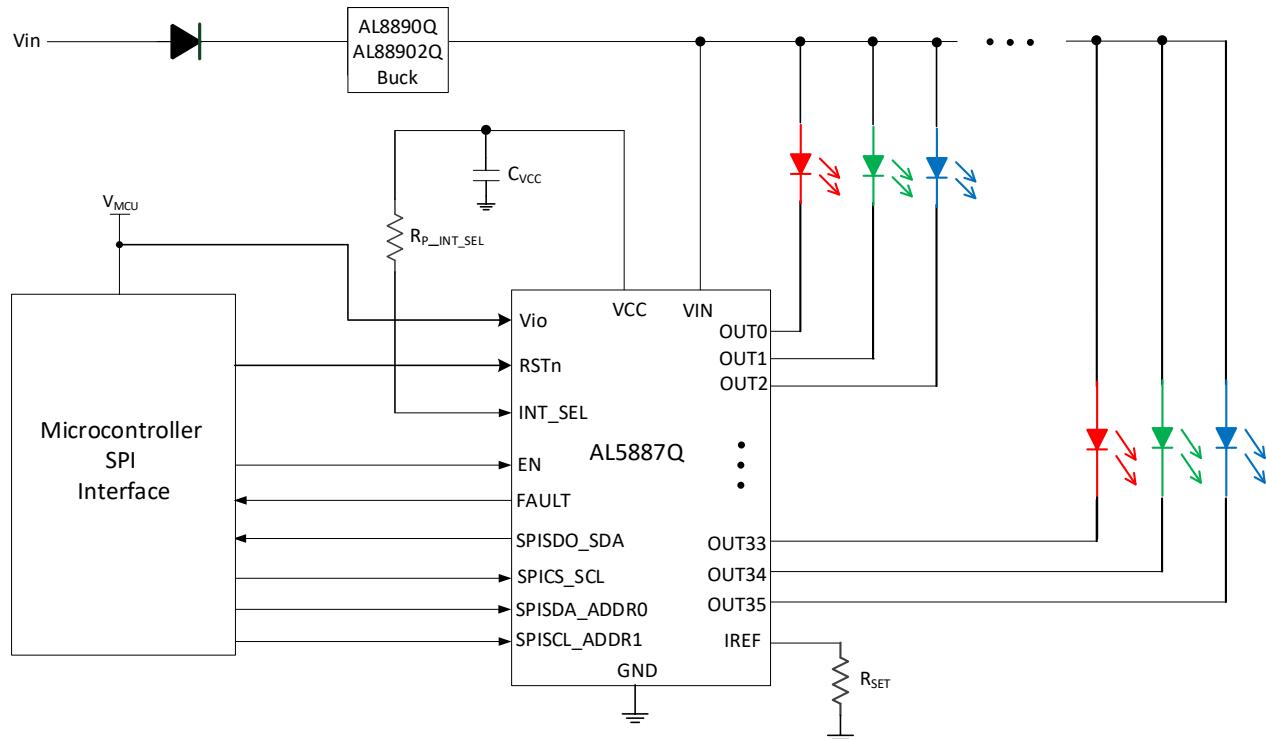
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

## Typical Applications Circuit

### 1) For I<sup>2</sup>C Interface

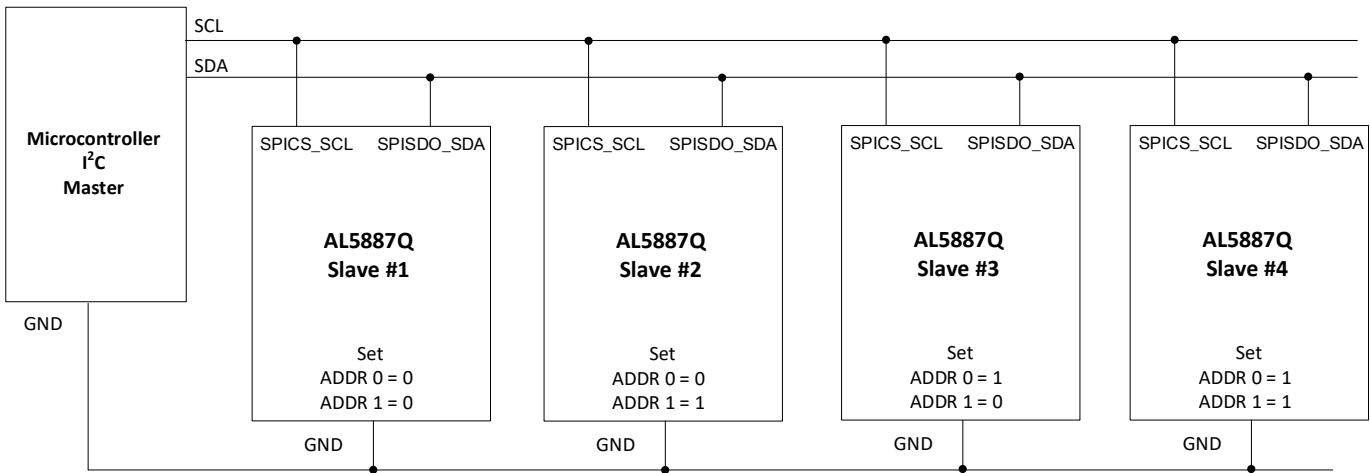


### 2) For SPI Interface

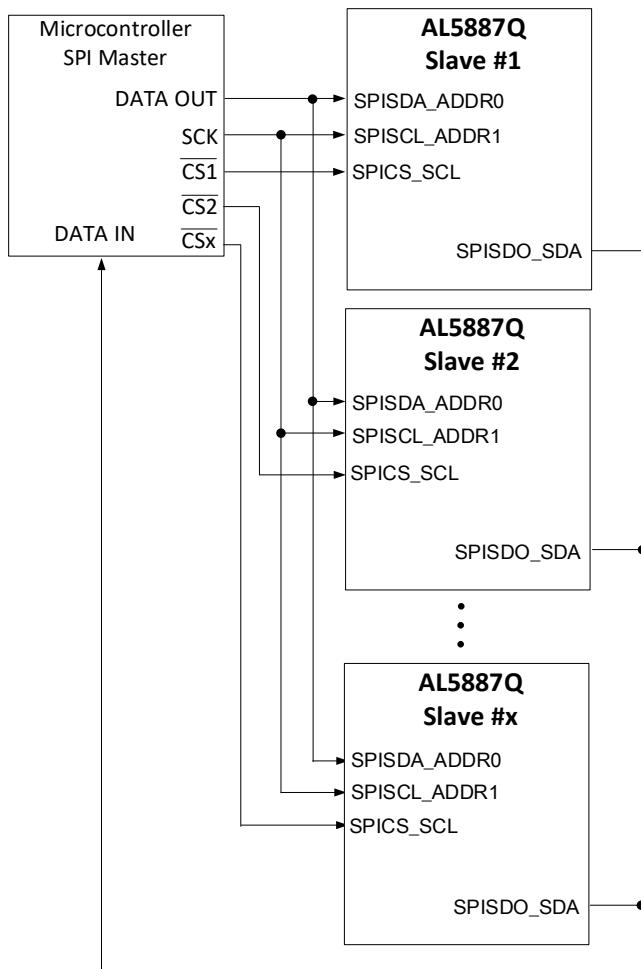


## Typical Applications Circuit (continued)

3) Four AL5887Q connected together with external hardware pins setup



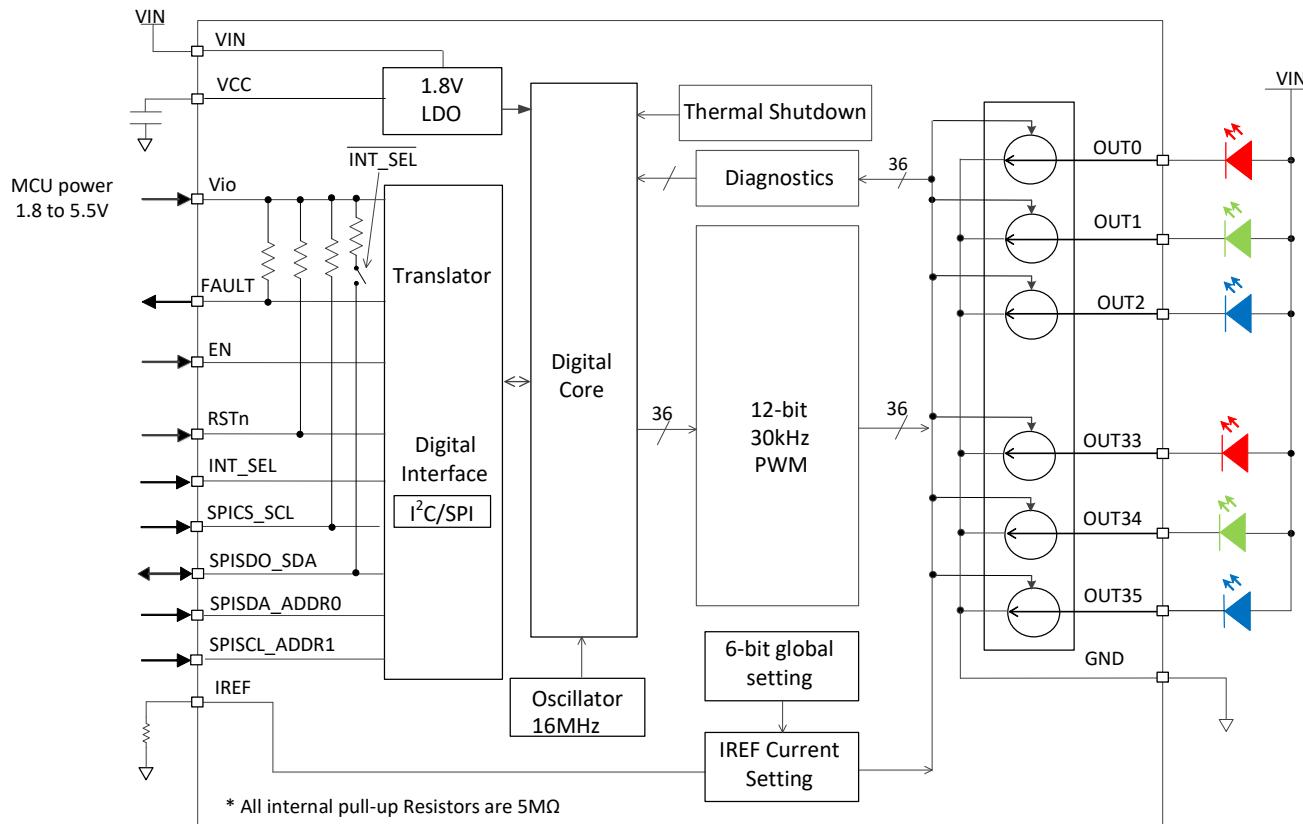
4) AL5887Q (SPI interface) connected in parallel



## Pin Descriptions

Pin Name	Pin Number	Type	Function
OUT0 to OUT5	1 to 6	O	Current sink output for LED 0 to LED 5
OUT6 to OUT17	8 to 19	O	Current sink output for LED 6 to LED 17
OUT18 to OUT29	21 to 32	O	Current sink output for LED 18 to LED 29
OUT30 to OUT35	34 to 39	O	Current sink output for LED 30 to LED 35
Vio	40	I	Input power from MCU power rail
FAULT	41	O	Analog output with open drain internal pull up 5MΩ resistor to Vio for fault indication
SPISDO_SDA	42	I/O	INT_SEL = HIGH, SPI master input slave output, serial data line INT_SEL = LOW, I <sup>2</sup> C Data line If not used, this pin must be connected to GND or VIN. (Default = HIGH for I <sup>2</sup> C)
SPICS_SCL	43	I	INT_SEL = HIGH, SPI active low chip select INT_SEL = LOW, I <sup>2</sup> C bus clock line If not used, this pin must be connected to GND or VIN. (Default = HIGH)
SPISDA_ADDR0	44	I	INT_SEL = HIGH, SPI master output slave input, serial data line INT_SEL = LOW, I <sup>2</sup> C slave-address selection pin This pin must not be left floating. (Default = LOW)
SPISCL_ADDR1	45	I	INT_SEL = HIGH, SPI serial clock line from SPI master (FPGA) INT_SEL = LOW, I <sup>2</sup> C slave-address selection pin This pin must not be left floating. (Default = LOW)
IREF	47	O	Connect an external resistor to regulate all channel output current.
INT_SEL	48	I	Selects the required communication interface. INT_SEL = LOW selects I <sup>2</sup> C and INT_SEL = HIGH selects SPI. This pin must not be left floating. (Default = LOW)
VCC	49	O	Internal LDO 1.8V output pin, this pin must be connected to a 1μF capacitor to GND.
RSTn	50	I	Resets digital interface only but retains other register values if pulled down for time between 1ms to 20ms. Resets all register values if pulled down for time more than 20ms. Needs to be pulled high for powering up the internal digital block. (Default = HIGH)
EN	51	I	Active low to shut down the chip. (Default = LOW)
VIN	52	Power	Power supply
GND	7, 20, 33, 46	GND	Ground
—	Thermal Exposed Pad	GND	Thermal exposed pad also serves as a ground for the device.

## Functional Block Diagram



## Absolute Maximum Ratings (Note 4)

Symbol	Parameter	Rating	Unit
<b>V<sub>IN</sub></b>	Input Voltage, Voltage Relative to GND	-0.3 to 6	V
<b>I<sub>OUTx</sub></b>	OUT <sub>x</sub> Output Current	160	mA
<b>V<sub>OUTx</sub>, EN, FAULT, RSTn, Vio, INT_SEL, SPICS_SCL, SPISDO_SDA, SPISDA_ADDR0, SPISCL_ADDR1, IREF</b>	High-Voltage Pins	-0.3 to 6V	V
<b>V<sub>CC</sub></b>	Low-Voltage Pins	-0.3 to 2V	V
<b>T<sub>J</sub></b>	Junction Temperature	-40 to +150	°C
<b>T<sub>STG</sub></b>	Storage Temperature	-65 to +150	°C
<b>ESD</b>	HBM	2000	V
	CDM	1000	V

Note: 4. Stresses greater than those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to *Absolute Maximum Ratings* for extended periods can affect device reliability. Semiconductor devices are ESD sensitive and may be damaged by exposure to ESD events. Suitable ESD precautions should be taken when handling and transporting these devices.

## Package Thermal Data (Note 5)

Symbol	Thermal Resistance	W-QFN6060-52/SWP (Type A1)	Unit
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	19.23	°C/W
$R_{\Theta JC(\text{top})}$	Junction-to-case (top) thermal resistance	7.76	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	3.58	°C/W
$\Psi_{JT}$	Junction-to-top characterization parameter	0.07	°C/W
$\Psi_{JB}$	Junction-to-board characterization parameter	3.36	°C/W
$R_{\Theta JC(\text{bot})}$	Junction-to-case (bottom) thermal resistance	0.72	°C/W

Note: 5. Test condition: Device mounted on FR-4 PCB (51mm x 51mm 2oz copper, minimum recommended pad layout on top layer and thermal vias to bottom layer with maximum area ground plane. For better thermal performance, larger copper pad for heat-sink is needed.

## Recommended Operating Conditions (@ $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$ , unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit
$V_{IN}$	Device supply voltage	2.7	—	5.5	V
$V_{IO}$	Input power from MCU rail	1.8	3.3	5.5	V
$I_{OUTx}$	OUTx output current (Note 6)	—	39	70	mA
$T_A$	Ambient temperature (Note 6)	-40	—	+125	°C
$T_J$	Junction temperature	-40	—	+150	°C

Note: 6. Dependent on ambient temperature, LED voltage, package thermal limitation, and PCB layout.

## Electrical Characteristics (VIN = 3.3V, -40°C < TA < +125°C, unless otherwise specified.)

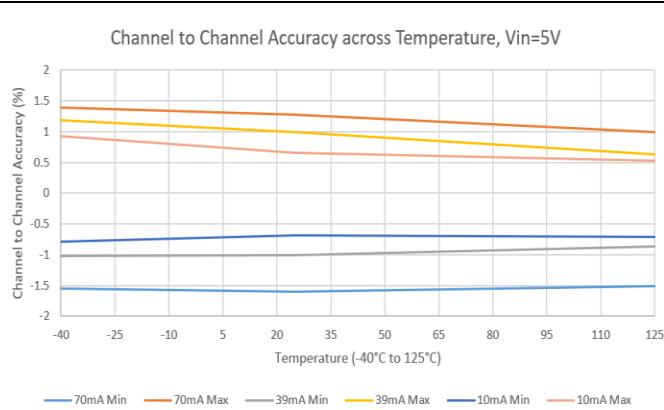
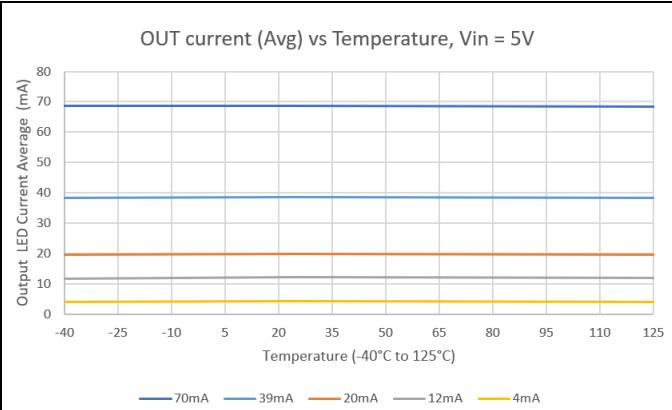
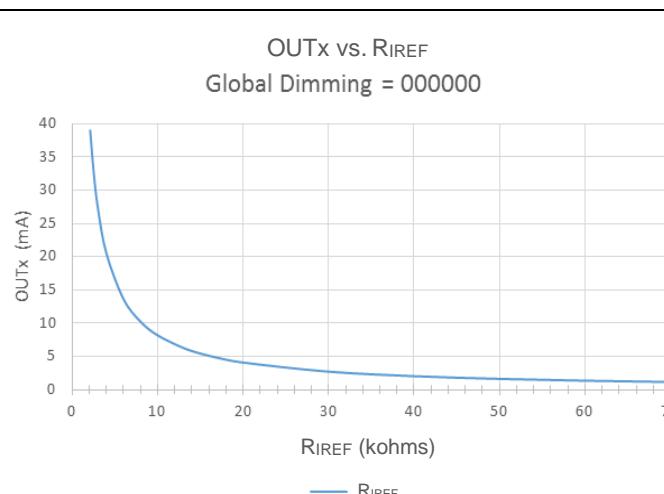
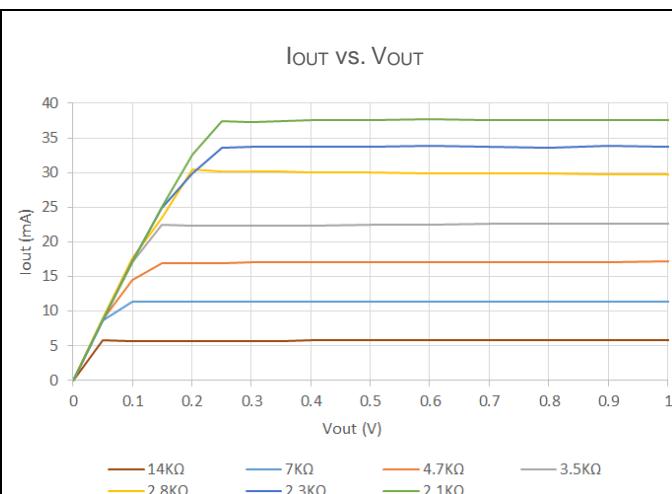
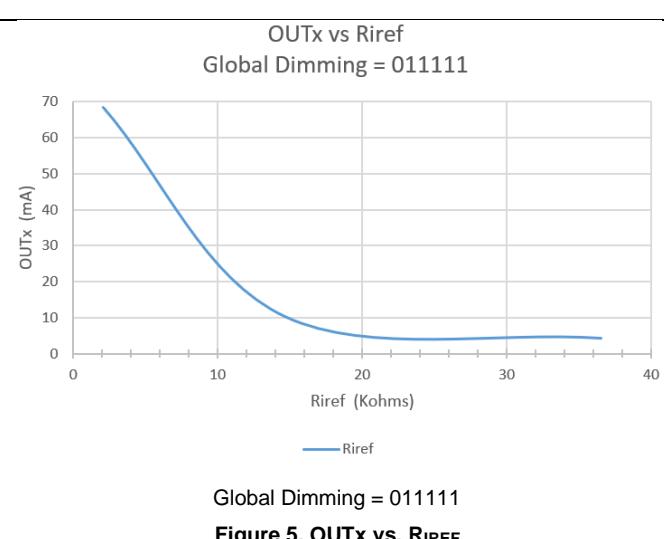
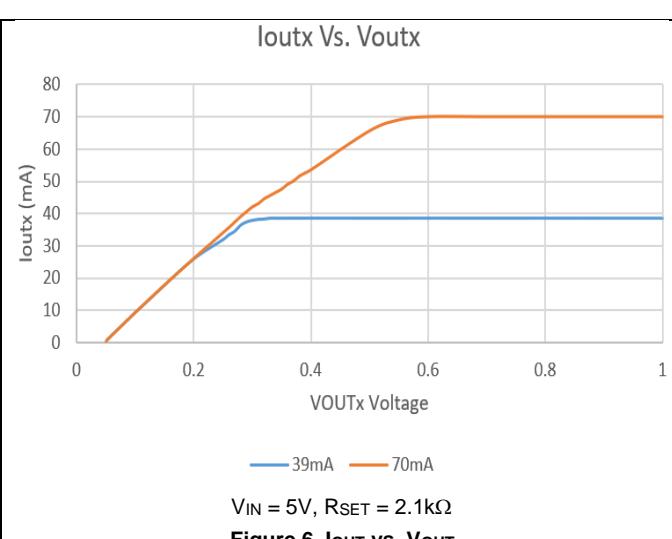
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>POWER SUPPLY</b>						
VIN	Supply voltage	—	2.7	3.3	5.5	V
VCC	Internal 1.8V LDO output	—	1.75	1.8	1.84	V
IVIN	Shut down supply current	V <sub>EN</sub> = 0V	—	0.2	6	µA
	Standby supply current	V <sub>EN</sub> = 3.3V, Chip_EN = 0 (bit)	—	12	33	µA
	Normal-mode supply current	With 39mA LED current per OUTx	—	7	9	mA
	Power-save mode supply current	V <sub>EN</sub> = 3.3V, Chip_EN = 1 (bit), Power_Save_EN = 1 (bit), All LEDs turned off for time > 30ms	—	12	33	µA
UVLO+	VIN UVLO rising	—	2	2.36	2.6	V
UVLO-	VIN UVLO falling	—	1.8	2.16	2.4	V
UVLO_Hys	—	—	—	0.2	—	V
V <sub>IREF</sub>	Output voltage of I <sub>REF</sub> pin	—	0.690	0.7	0.710	V
<b>CURRENT SINK (Note 7), Max_Current_Option set in Device Config 1 Register, G5:G0 set in LED Global Dimming Register (See page 24)</b>						
I <sub>MAX</sub>	Maximum global output current (Channel average current, Color Register = FF, Brightness Register = FF)	V <sub>IN</sub> in full range, R <sub>SET</sub> = 2.1kΩ Max_Current_Option = 0, G5:G0 = 000000	—	29.25	—	mA
		V <sub>IN</sub> in full range, R <sub>SET</sub> = 2.1kΩ Max_Current_Option = 1, G5:G0 = 100000 (Note 10)	—	7	—	mA
		V <sub>IN</sub> in full range, R <sub>SET</sub> = 2.1kΩ Max_Current_Option = 1 G5:G0 = 000000	—	39	—	mA
		V <sub>IN</sub> in full range, R <sub>SET</sub> = 2.1kΩ Max_Current_Option = 1 G5:G0 = 011111 (Note 10)	—	70	—	mA
I <sub>LIM</sub>	Internal current limit	V <sub>IN</sub> = 3.3V Max_Current_Option = 1, V <sub>IREF</sub> = 0V G5:G0 = 011111	—	75	155	mA
I <sub>D2D</sub> (Note 8)	Device to device (I <sub>avg</sub> -I <sub>set</sub> )/I <sub>set</sub> x 100	V <sub>IN</sub> = 2.7 – 5.5V. R <sub>SET</sub> = 2.1K, all channels' current set to 10mA. PWM = 100%. G5:G0=100011 (I <sub>MAX</sub> =10mA)	—	±3	—	%
I <sub>C2C</sub> (Note 9)	Channel to channel (I <sub>outx</sub> -I <sub>avg</sub> )/I <sub>avg</sub> x 100	V <sub>IN</sub> = 2.7 – 5.5V. R <sub>SET</sub> = 2.1K, all channels' current set to 10mA. PWM = 100%. G5:G0=100011 (I <sub>MAX</sub> =10mA)	—	±3	—	%
I <sub>lk</sub>	LEDx leakage current	PWM = 0%	—	0.01	2.2	µA
V <sub>SAT</sub>	Output Saturation Voltage	V <sub>IN</sub> in full range, Max_Current_Option = 1 (bit), R <sub>SET</sub> = 2.1kΩ, PWM=100%, the voltage when the LED current has dropped 5%, G5:G0 = 000000	—	0.2	0.6	V
V <sub>OPEN_th_rising</sub>	LED open threshold	V <sub>IN</sub> = 3.3V, V <sub>OUTx</sub> < V <sub>OPEN_th_rising</sub>	0.10	0.2	0.35	V
V <sub>SC_th_rising</sub>	LED short threshold (V <sub>IN</sub> - V <sub>OUTx</sub> )	V <sub>IN</sub> = 3.3V, V <sub>IN</sub> - V <sub>OUTx</sub> < V <sub>SC_th_rising</sub>	0.31	0.62	0.9	V

- Notes:
7. For understanding of PWM generation process, please refer to [Section 2.1.3](#).
  8. I<sub>D2D</sub>: Accuracy of average of all 36 channels current with respect to design target. Not production tested, guaranteed by design.
  9. I<sub>C2C</sub>: Accuracy of individual channel current with respect to average of all 36 channels current within a device. Channel current: average, or mean current (not RMS current) on a channel. Not production tested, guaranteed by design.
  10. Not production tested, guaranteed by design.

**Electrical Characteristics** ( $V_{IN} = 3.3V$ ,  $-40^{\circ}C < T_A < +125^{\circ}C$ , unless otherwise specified.) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>PWM GROUP DIMMING</b>						
fPWM	PWM frequency	—	25	30	36	kHz
fosc	Internal oscillator frequency (Note 10)	—	—	15.5	—	MHz
tIOUTx_rise	IOUTx rise time (Note 10)	Time for 0% to 90% rise of IOUTx	—	8	—	ns
<b>PROTECTION (Note 10)</b>						
T <sub>(PRETSD)</sub>	Pre-thermal warning threshold	—	—	+145	—	°C
T <sub>(PRETSD_HYS)</sub>	Pre-thermal warning hysteresis	—	—	+20	—	°C
T <sub>SD</sub>	Thermal shutdown temperature	—	—	+165	—	°C
T <sub>HYS</sub>	Thermal shutdown temperature hysteresis	—	—	+20	—	°C

Note: 10. Not production tested, guaranteed by design.

**Typical Performance Characteristics** ( $V_{IN} = 5V$ ,  $-40^{\circ}C < T_A < +125^{\circ}C$ , unless otherwise specified.)

**Figure 1. Channel to Channel Accuracy vs. Temperature**

**Figure 2. OUT Current vs. Temperature**

**Figure 3. OUTx vs. R<sub>REF</sub>**

**Figure 4. I<sub>OUT</sub> vs. V<sub>OUT</sub>**

**Figure 5. OUTx vs. R<sub>REF</sub>**

**Figure 6. I<sub>OUT</sub> vs. V<sub>OUT</sub>**

## Functional Descriptions

### 1. General Operation

One of the I<sup>2</sup>C or SPI protocols can be selected using the INT\_SEL pin. Using the I<sup>2</sup>C/SPI interface, the AL5887Q controls the LED's color and brightness through four primary mechanisms:

1. Use RSET to set full range for LED current I<sub>MAX</sub> (up to 70mA).
2. Set I<sub>MAX</sub> by using a 6-bit global dimming register, which is termed as LED GLOBAL DIMMING in the register's map.
3. Set color/brightness registers for LED color and brightness (see *Registers Map Description*).
4. Further select various dimming and protection features as described in *Registers Map Description*.

### 2. Feature Description

#### 2.1 Each Channel PWM Control

The AL5887Q device is designed with independent color mixing and brightness control, which make it easier to achieve the RGB LED color effects needed. With the inputs of the color-mixing register and the brightness-control register, the final PWM generator output for each channel is a 12-bit resolution and 30kHz dimming frequency, which help achieve a smooth dimming effect and eliminate audible noise. See Figure 7.

For example, yellow color has the red, green, and blue components as 255, 255, and 0 respectively. So, to get the color yellow for the first RGB LED module, the color registers at the addresses 14h, 15h, and 16h—with values 255, 255, and 0 respectively. The brightness register for the first RGB LED module (at the address 8h) can be configured based on the amount of brightness needed, 255 being the maximum brightness.

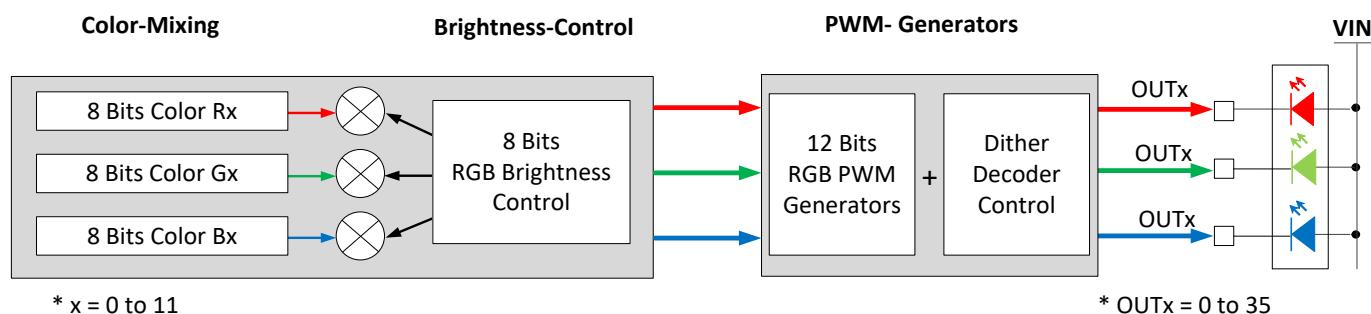


Figure 7. PWM Control Scheme for Each Channel

##### 2.1.1 Independent Color Mixing Per RGB LED Module

Each output channel has its own individual 8-bit color-setting register (OUTx\_COLOR). The device allows every RGB LED module to achieve > 16 million (256 x 256 x 256) color mixing.

##### 2.1.2 Independent Brightness Control per RGB LED Module

When color is fixed, the independent brightness control is used to achieve accurate and flexible dimming control for every RGB LED module.

###### 2.1.2.1 Brightness-Control Register Configuration

Every three consecutive output channels are assigned to their respective brightness-control register (RGBx\_BRIGHTNESS). For example, LED0, LED1, and LED2 are assigned to RGB0\_BRIGHTNESS, so it is recommended to connect the RGB LEDs in the sequence as shown in Table 1. The AL5887Q allows 256-step brightness control for each RGB LED module, which helps achieve a smooth dimming effect.

Keeping FFh (default value) in the RGB0\_BRIGHTNESS register results in 100% dimming brightness. With this setting, users can configure the color-mixing register by channel to achieve the target dimming effect in a single-color LED application.

## Functional Descriptions (continued)

### 2.1.2.2 Logarithmic- or Linear-Scale Brightness Control

For human-eye-friendly visual performance, a logarithmic-scale dimming curve is usually implemented in LED drivers. For RGB LEDs and if using a single register to achieve both color mixing and brightness control, color distortion can be observed easily when using a logarithmic scale. The AL5887Q, with independent color-mixing and brightness-control registers, implements the logarithmic scale dimming control inside the brightness-control function, which effectively solves the color distortion issue (See Figure 8). The AL5887Q also allows users to configure the dimming scale either logarithmically or linearly through the global Log\_Scale\_EN register bit. If a special dimming curve is desired, using the linear scale with software correction is the most flexible approach.

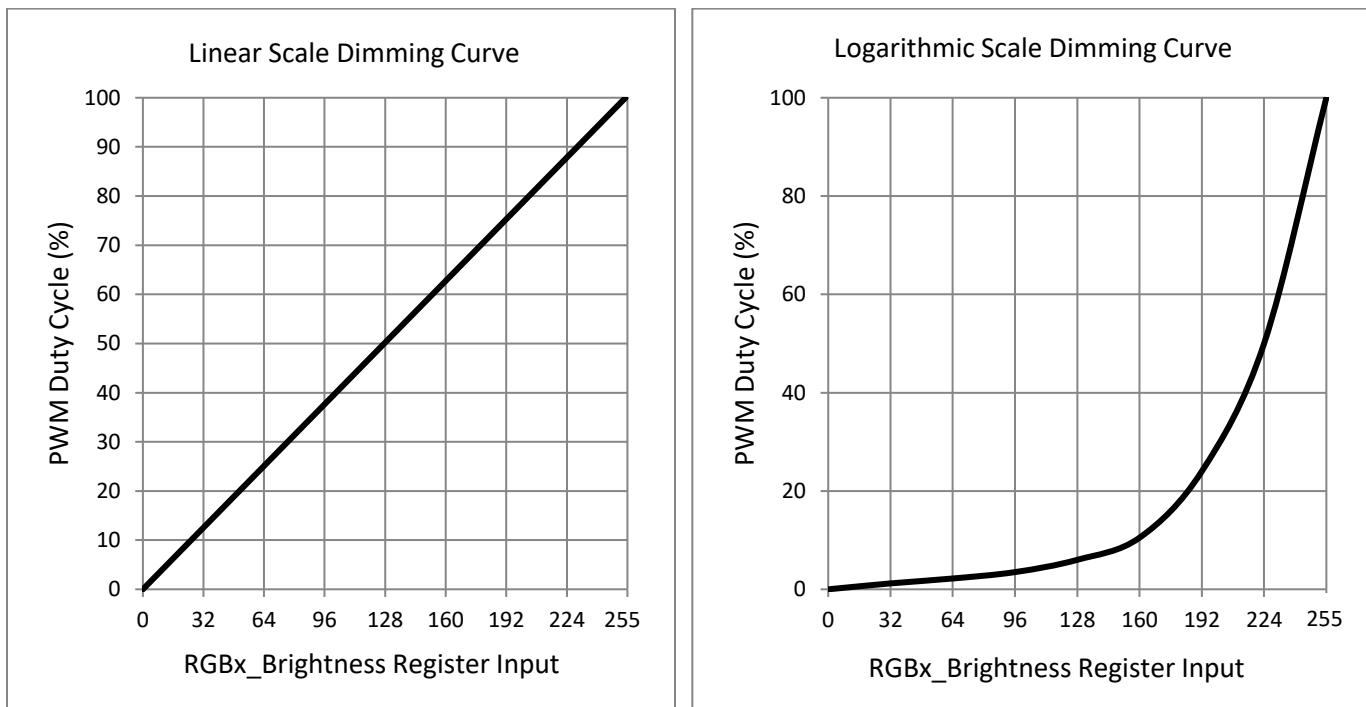


Figure 8. Logarithmic vs Linear Dimming Curve

### 2.1.3 12-Bit, 30kHz PWM Generator per Channel

With the inputs of the color mixing and the brightness control, the final output PWM duty cycle is defined as the product obtained by multiplying the color-mixing register value by the related brightness-control register value. The final output PWM duty cycle has 12 bits of control resolution, which is achieved by 9 bits of pure PWM resolution and 3 bits of dithering digital control. The AL5887Q allows users to enable or disable the dithering function through the PWM\_Dithering\_EN register. When enabled (default), the output PWM duty-cycle resolution is 12 bits. When disabled, the output PWM duty-cycle resolution is 9 bits.

When 3-bit dithering is enabled, dither effect is generated with  $8 (2^3 = 8)$  possible dither values: "0", "1", "2", ..., "7", where 0 means no dithering; "1" means every 8<sup>th</sup> PWM pulse is made 1 LSB longer to increase the final average duty cycle by 1 LSB/8 (duty cycle is termed as DT); "2" means in every group of 8 PWM pulses, the 7<sup>th</sup> and 8<sup>th</sup> PWM pulses are both made 1 LSB longer to increase DT by 2 LSB/8, etc. The AL5887Q uses 512 clocks in a 100% PWM DT period to achieve 9-bit pure PWM resolution ( $2^9 = 512$ ), thus 1 LSB PWM DT is 1/512. Therefore, dither value "1" adds  $1/(8 \times 512) = 0.0244\%$  additional DT to pure PWM DT. For example, combining with dither value "1", the pure PWM DT of 25% will generate DT = 25.0244% for LED current regulation; while with dither value "2", pure PWM DT of 25% will generate DT = 25.05%. Though the AL5887Q's pure PWM resolution is 1/512 = 0.195%, the 3-bit dither scheme enhances PWM resolution to 0.0244%.

## Functional Description (continued)

### 2.1.4 PWM Phase-Shifting

A PWM phase-shifting scheme allows for a delay in time when each LED driver is active. When the LED drivers are not activated simultaneously, the peak load current from the pre-stage power supply is significantly decreased. The scheme also reduces input-current ripple and ceramic-capacitor audible ringing. LED drivers are grouped into three different phases:

- Phase 1 - The rising edge of the PWM pulse is fixed. The falling edge of the pulse is changed when the duty cycle changes. Phase 1 is applied to LED0, LED3, ..., LED[3 × (n – 1)].
- Phase 2 - The middle point of the PWM pulse is fixed. The pulse spreads in both directions when the PWM duty cycle is increased. Phase 2 is applied to LED1, LED4, ..., LED[3 × (n – 1) + 1].
- Phase 3 - The falling edge of the PWM pulse is fixed. The rising edge of the pulse is changed when the duty cycle changes. Phase 3 is applied to LED2, LED5, ..., LED[3 × (n – 1) + 2].

### 2.2 LED Bank Control

For most LED-animation effects, like blinking and breathing, all the RGB LEDs have the same lighting pattern. Instead of controlling the individual LED separately, which occupies the microcontroller resources heavily, the AL5887Q device provides an easy coding approach, the LED bank control. Each channel can be configured as either independent control or bank control through the LEDx\_Bank\_EN register. When LEDx\_Bank\_EN = 0 (default), the LED is controlled independently by the related color-mixing and brightness-control registers. When LEDx\_Bank\_EN = 1, the AL5887Q drives the LED in LED bank-control mode. The LED bank has its own independent PWM control scheme, which is the same structure as the PWM scheme of each channel. When a channel is configured in LED bank-control mode, the related color-mixing and brightness control are governed by the bank-control registers (BANK\_A\_COLOR, BANK\_B\_COLOR, BANK\_C\_COLOR, and BANK\_BRIGHTNESS), regardless of the inputs on its own color-mixing and brightness-control registers.

Table 1. Bank Number and RGB Number Assignment

Out Number	Bank Number	RGB Module Number	Out Number	Bank Number	RGB Module Number
OUT0	Bank A	RGB0	OUT18	Bank A	RGB6
OUT1	Bank B		OUT19	Bank B	
OUT2	Bank C		OUT20	Bank C	
OUT3	Bank A	RGB1	OUT21	Bank A	RGB7
OUT4	Bank B		OUT22	Bank B	
OUT5	Bank C		OUT23	Bank C	
OUT6	Bank A	RGB2	OUT24	Bank A	RGB8
OUT7	Bank B		OUT25	Bank B	
OUT8	Bank C		OUT26	Bank C	
OUT9	Bank A	RGB3	OUT27	Bank A	RGB9
OUT10	Bank B		OUT28	Bank B	
OUT11	Bank C		OUT29	Bank C	
OUT12	Bank A	RGB4	OUT30	Bank A	RGB10
OUT13	Bank B		OUT31	Bank B	
OUT14	Bank C		OUT32	Bank C	
OUT15	Bank A	RGB5	OUT33	Bank A	RGB11
OUT16	Bank B		OUT34	Bank B	
OUT17	Bank C		OUT35	Bank C	

With the bank-control configuration, the AL5887Q enables users to achieve smooth and live LED effects globally with an ultra-simple software effort.

For example (as shown in Figure 9), if we want to configure RGB0 in independent mode and the rest of RGB1 to RGB11 in BANK mode, we can configure the LED\_CONFIG0 register to FEh and LED\_CONFIG1 register to 0Fh. By doing this, the RGB0 module operating in independent mode will be using RGB0\_BRIGHTNESS for brightness and R0\_COLOR, G0\_COLOR, and B0\_COLOR for R, G, and B colors respectively, while the other RGB modules in bank mode would use BANK\_BRIGHTNESS for brightness and BANK\_A, BANK\_B, and BANK\_C for R, G, and B colors respectively.

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## Functional Description (continued)

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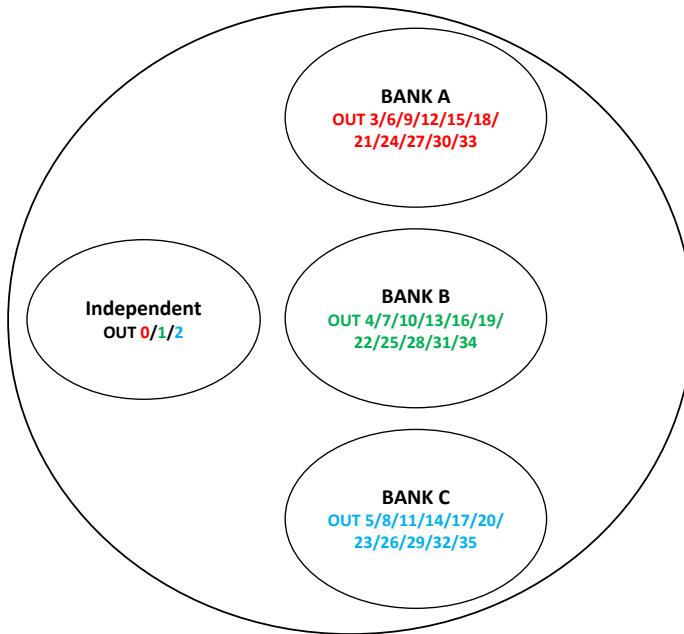


Figure 9. Bank PWM Control Example

### 2.3 Automatic Power-Save Mode

When all the LED outputs are inactive, the AL5887Q is able to enter power-save mode automatically, thus lowering idle-current consumption down to 25 $\mu$ A (maximum). Automatic power-save mode is enabled when the register bit Power\_Save\_EN = 1 (default) and all LEDs are off (both color and brightness registers = 00H) for a duration of > 30ms. Almost all analog blocks are powered down in power-save mode. If any I<sup>2</sup>C/SPI command to the device occurs, the AL5887Q returns to NORMAL mode.

### 2.4 Protection Features

#### 2.4.1 LED Open-Circuit Diagnostics

The AL5887Q integrates LED open-circuit diagnostics to allow users to monitor the LED status in real time. The device monitors OUTx voltage to determine if there is any open-circuit failure.

If the voltage V<sub>OUTx</sub> for any of the channels goes below threshold V<sub>OPEN\_th\_rising</sub> and if the open persists for more than t<sub>FAULT\_WAIT</sub>, the AL5887Q pulls the FAULT pin low to report the fault, and sets the flag registers OFx and FLAG\_OPEN to 1. Once the open-circuit failure is removed, the controller needs to send CLR\_FAULT to clear the FLAG\_OPEN after fault removal. The fault delay is decided based on the below table.

Table 2. Fault Wait Time

FW1	FW0	t <sub>FAULT_WAIT</sub>
0	0	8 PWM clock count
0	1	16 PWM clock count
1	0	24 PWM clock count
1	1	32 PWM clock count

#### 2.4.2 LED Short-Circuit Diagnostics

The AL5887Q monitors the voltage difference between supply (VIN) and OUTx to determine if there is any short-circuit failure. If the difference voltage (VIN - V<sub>OUTx</sub>) for any of the channels falls below the threshold (V<sub>SC\_th\_rising</sub>), and if the short persists for more than t<sub>FAULT\_WAIT</sub>, the AL5887Q pulls the FAULT pin low to report the fault and also sets flag register SFx and FLAG\_SHORT to 1. The MCU should turn off the channel that detects a short fault to avoid overstressing the device. Once the short-circuit failure is removed, the controller needs to send CLR\_FAULT to clear the FLAG\_SHORT after fault removal.

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## Functional Description (continued)

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### 2.4.3 Pre-OTP Warning & Thermal Shutdown

The AL5887Q has a pre-thermal warning threshold of +145°C (typical) and thermal shutdown threshold of +165°C (typical)

When the AL5887Q's junction temperature rises above the pre-thermal warning threshold of +145°C (typical) and persists for more than 33μs, the device reports a pre-thermal warning by pulling the FAULT pin low and sets the flag register FLAG\_PREOTP to 1. The device releases pre-OTP warning once the temperature goes below +125°C. Once the fault is removed, the controller needs to send CLR\_FAULT to clear the flag register after fault removal.

The AL5887Q also implements a thermal-shutdown mechanism to protect the device from damage due to overheating when the junction temperature rises further than +165°C (typical). In this mode, the FAULT pin state will change to LOW, Flag register (65h), and the default value of 10h will change to 14h. All the OUTx outputs will be shut down. To return to NORMAL mode, write 02h to Mask and CLR register (68h) and decrease the junction temperature below +150°C (typical). The FAULT pin state will then change to HIGH, and the device will return to NORMAL mode.

### 2.4.4 Pre-UVLO Warning

The AL5887Q provides a pre-UVLO feature that warns the MCU if the supply (VIN) is low. When VIN goes below the pre-UVLO threshold and persists for more than 33μs, the FAULT pin is pulled low and the flag register FLAG\_PREUVLO is set to 1. The device releases pre-UVLO warning once the VIN goes above pre-UVLO+ threshold. Once the fault is cleared, the controller needs to send CLR\_FAULT to clear the flag register after fault removal.

### 2.4.5 UVLO

The AL5887Q has an internal comparator that monitors the voltage at VIN. When VIN is below UVLO-, reset is active and the AL5887Q is in the INITIALIZATION state. When the VIN supply goes below the UVLO- threshold, the FAULT pin is pulled low to indicate the fault.

### 2.4.6 Digital POR Indicator

The AL5887Q has a digital bit FLAG\_POR to indicate the power on reset. The default value of this bit is high to indicate the power on reset of digital block. The controller can set CLR\_POR during the start of the operation to reset FLAG\_POR so that the next power on reset to digital block can be captured.

### 2.4.7 Fault Masking

OMx prevents the output open-circuit fault of individual channels from being reported to the FAULT pin, while Open\_Mask prevents any of the channels open fault from being reported to the FAULT pin.

SMx prevents the output short-circuit fault of individual channels from being reported to the FAULT pin, while Short\_Mask prevents any of the channels short fault from being reported to the FAULT pin.

Pre OTP\_Mask prevents the pre OTP fault from being reported to the FAULT pin.

Pre\_UVLOMask prevents the pre\_UVLO fault from being reported to the FAULT pin.

POR\_Mask prevents the POR event from being reported to the FAULT pin.

## Functional Description (continued)

### 2.4.8 Output

The FAULT pin is a fault indicator pin. It can be used as an interrupt output to the master controller in case of any fault. The FAULT pin is an NMOS open-drain output with an internal  $5\text{M}\Omega$  pull-up resistor, pulled to  $\text{V}_{\text{IO}}$ , and additionally this pin can be pulled up externally to the controller supply using a smaller resistor such as  $10\text{k}\Omega$ , as shown in the figure below. When one or any of the faults are triggered; such as UVLO, OTP, pre-UVLO, pre-OTP, channel open, and channel short; the FAULT pin is pulled low continuously. Once the FAULT pin output is triggered, the controller needs to take necessary action and to deal with the fault and reset the fault flag. The AL5887Q acts only for UVLO and OTP faults. For any other fault, the AL5887Q only reports the fault and the controller must take action.

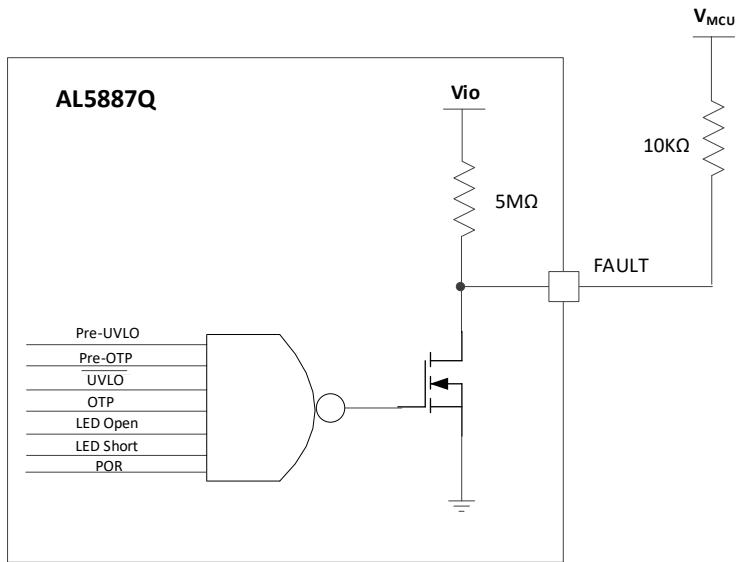


Figure 10. FAULT Internal Block Diagram

### 2.5 Interface Selection

Interface selection between I<sup>2</sup>C or SPI is done using an external pin INT\_SEL. When tied low, I<sup>2</sup>C is selected. When connected high, SPI is selected.

### 2.6 Digital Communication Enhancements

Pulling the external pin RSTn high enables the internal digital block. Pulling down for a duration between 1ms to 20ms resets only the digital interface and keeps other register values unaltered. Pulling down for a duration of more than 20ms resets all registers. There is an internal pull-up resistor that, by default, pulls up this pin to HIGH.

## Functional Description (continued)

### 2.7 Current Setting for all Channels

The maximum global output current for all 36 channels can be adjusted by the external resistor,  $R_{SET}$ , as described below.

$$I_{MAX} = K_{IREF} \times V_{IREF} / R_{SET} \times [ (Max\_Current\_Option/4) + (3/4) ] \quad (1)$$

where,

$I_{MAX}$  = Channel average current, Color Register = FF, Brightness Register = FF

$V_{IREF}$  = 0.7 V

$R_{SET}$  = External dimming resistor (2.1kΩ recommended)

$Max\_Current\_Option$  = 1 (default) or 0, see *Register Map*.

$K_{IREF} = 21 + (N \times 3)$ , is the current multiplication factor which can be programmed using a 6-bit global dimming register G5:G0 (Address = 66H), which is an analog dimming register and N is the decimal equivalent of  $\overline{G5} G4 G3 G2 G1 G0$ .

For example, if all global dimming register bits are 0, the N will be the decimal equivalent of 100000, which is 32. Hence,  $K_{IREF} = 21 + (32 \times 3) = 117$ .

Using equation (1) above, for  $R_{SET} = 2.1k\Omega$  and  $Max\_Current\_Option = 1$ , below is the table that shows  $I_{MAX}$  variation with respect to the global dimming register bits. From Table 3, we can see that the default value = 39mA, minimum value = 7mA, and maximum value = 70mA.

Table 3.  $I_{MAX}$  vs. Global Dimming @  $R_{SET} = 2.1k\Omega$

G5	G4	G3	G2	G1	G0	$I_{MAX}$ (mA)	$K_{IREF}$
0	0	0	0	0	0	39 (Default)	117 (Default)
0	0	0	0	0	1	40	120
0	0	0	0	1	0	41	123
0	0	0	0	1	1	42	126
•						•	•
•						•	•
•						•	•
0	1	1	1	0	0	67	201
0	1	1	1	0	1	68	204
0	1	1	1	1	0	69	207
0	1	1	1	1	1	70 (Max)	210 (Max)
1	0	0	0	0	0	7 (Min)	21 (Min)
1	0	0	0	0	1	8	24
1	0	0	0	1	0	9	27
1	0	0	0	1	1	10	30
•						•	•
•						•	•
•						•	•
1	1	1	1	0	1	36	108
1	1	1	1	1	0	37	111
1	1	1	1	1	1	38	114

## Functional Description (continued)

Similarly, using equation (1) above, for global dimming register setting of 000000H and Max\_Current\_Option = 1, below is the table that shows  $I_{MAX}$  variation with respect to the  $R_{SET}$ .

**Table 4.  $I_{MAX}$  vs.  $R_{SET}$  @ G5:G0 = 000000**

$R_{SET}$ (k $\Omega$ )	$I_{MAX}$ (mA)	$K_{IREF}$
2.1 (Recommended)	39	117
14.7	5.57	117
36.5	2.24	117

Table 5 shows  $I_{MAX}$  range using global dimming at different  $R_{SET}$  values.

**Table 5.  $I_{MAX}$  vs. Global Dimming Bits @ Various  $R_{SET}$**

$R_{SET}$ (k $\Omega$ )	$I_{MAX}$ (mA)		
	Min	Default	Max
2.1 (Recommended)	7	39	70
14.7	1	5.57	10
36.5	0.4	2.24	4

### 2.7.1 Thermal Considerations

As  $V_{INMAX}$  increases to 5.5V, the voltage on the OUTx nodes can go as high as 3V for RED LEDs and 2V for GREEN and BLUE LEDs. In the situation where the user configures G5:G0 or  $R_{EXT}$  for higher currents, the device may overheat and hit the thermal shutdown voltage.

Hence, the channels'  $V_{IN}$  and  $I_{OUTx}$  should be chosen in such a way that the device junction temperature does not exceed its thermal shutdown temperature. Below is the formula relating the power dissipation and  $\theta_{JA}$  to avoid thermal shutdown.

$$T_J = T_A + (\theta_{JA} \times P_{TOTAL})$$

Where,

$T_J$  is the junction temperature.

$T_A$  is the ambient temperature.

$\theta_{JA}$  is the junction to ambient thermal resistance.

$P_{TOTAL}$  is the device's total power dissipation.

Example: If all 36 channels are turned on and carry the same current  $I_{MAX}$ , then the device total power dissipation is given by,

$$P_{TOTAL} = (12 \times V_{(OUT0)} \times I_{MAX}) + (12 \times V_{(OUT1)} \times I_{MAX}) + (12 \times V_{(OUT2)} \times I_{MAX})$$

### 2.8 Microcontroller (MCU) Supply

The AL5887Q can recognize interface logic levels from 1.8V to 5.5V. So, an MCU interacting with the AL5887Q can operate in the range 1.8V to 5.5V. However, the information of the supply used by the MCU is required to be shared with the AL5887Q by connecting the MCU supply to the AL5887Q's Vio pin.

## Functional Description (continued)

### 2.9 Device Functional Modes

- **INITIALIZATION:** The device enters INITIALIZATION mode when EN = High. In this mode, all the registers are reset. Entry can also be from any state if the RESET (register) = FFh or UVLO is active.
- **NORMAL:** The device enters NORMAL mode when Chip\_EN (register) = 1. I<sub>VIN</sub> is 7mA (typical).
- **POWER SAVE:** The device automatically enters POWER SAVE mode when Power\_Save\_EN (register) = 1 and all the LEDs are off for a duration of > 30ms. In POWER SAVE mode, analog blocks are disabled to minimize power consumption, but the registers retain the data and keep it available via I<sup>2</sup>C/SPI. I<sub>VIN</sub> is 33µA (max). In the occurrence of any I<sup>2</sup>C/SPI command, the device goes back to NORMAL mode.
- **SHUTDOWN:** The device enters SHUTDOWN mode from all states on VIN power down or when EN = Low > 25ms. I<sub>VIN</sub> is < 6µA (max).
- **STANDBY:** The device enters STANDBY mode when Chip\_EN (register bit) = 0. In this mode, all OUTx are shut down, but the registers retain data and keep it available via I<sup>2</sup>C/SPI. STANDBY is the low-power-consumption mode when all circuit functions are disabled. I<sub>VIN</sub> is 33µA (max).
- **THERMAL SHUTDOWN:** The device automatically enters THERMAL SHUTDOWN mode when the junction temperature exceeds +165°C (typical). In this mode, the FAULT pin state will change to LOW, Flag register (65h), and the default value 10h will change to 14h. All OUTx outputs will shut down.

Addr.	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	FDV
65h	FLAG		Reserved		FLAG_POR	FLAG_PREUVLO	FLAG_PREOTP	FLAG_SHORT	FLAG_OPEN	10h

- **RETURN TO NORMAL MODE:** Write 02h to Mask and CLR register (68h) to clear the Fault bit.

Addr.	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	FDV
68h	MASK and CLR	Reserved	POR_Mask	PreUVLO_Mask	PreOTP_Mask	Short_Mask	Open_Mask	CLR_Fault	CLR_POR	00h

Write 40h to DEVICE\_CONFIG0 register (00h) to enable the device back to normal mode, then decrease the junction temperature below +145°C (typical). FAULT pin state will change to HIGH, then the device returns to NORMAL mode.

Addr.	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	FDV
00h	DEVICE_CONFIG0	Reserved	CHIP_EN			Reserved				00h

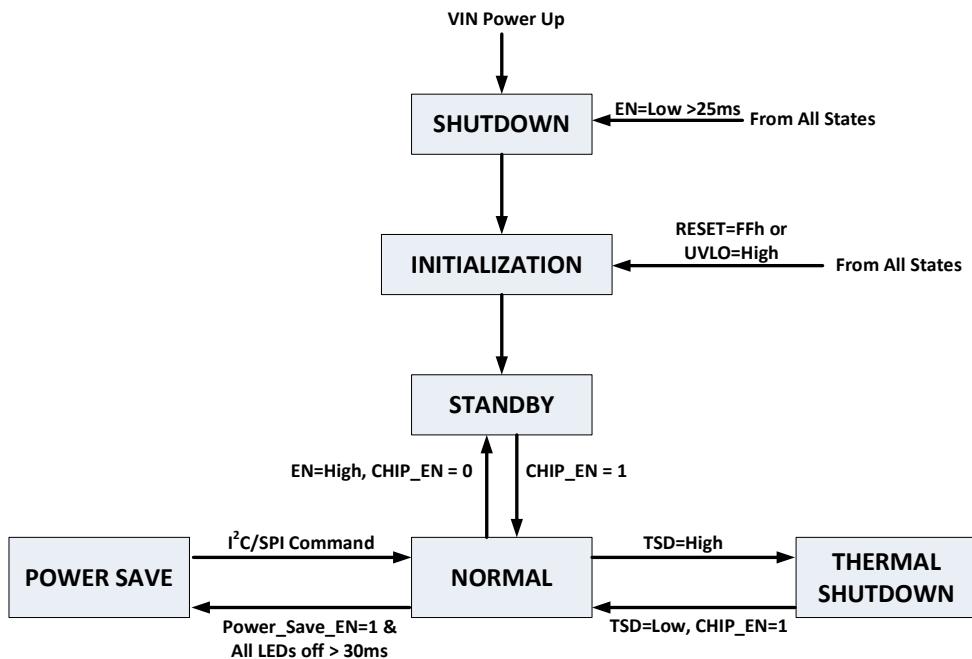


Figure 11. Functional Mode

## Functional Description (continued)

### 3. Programming (SPI)

#### 3.1 SPI-Compatible Interface

The AL5887Q is compatible with SPI serial-bus specification and operates as a slave.

##### 3.1.1 SPI INITIALIZATION

Upon the release of power-on-reset (POR), the SPI peripheral in the Digital Block waits for the chip-selection signal (SPICS\_SCL) from the SPI Controller. The output SPISDA\_ADDR0 of the AL5887Q is at high impedance until the reception of an active low on the select line.

The duration of the select line (SPICS\_SCL) should be compliant with lead- and lag-time requirements.

Lead time: 1) The time from SPICS\_SCL low to SPISCL\_ADDR1 high.  
2) Least lead time is half clock period.

Lag time: 1) The time from SPISCL\_ADDR1 low to SPICS\_SCL high.  
2) Least lag time is one clock period.

The AL5887Q is configured to communicate in Mode 0. Data read on rising edge. Clock Polarity in Idle State is Logic Low.

##### 3.1.2 Write Operation

A '1' on bit (R/W) of the SPI request frame indicates a write request from the SPI Controller. Bits A6 to A0 provide the address of the register to which the data is to be written. The contents of the frame from bit D7 to D0 are written into the respective register, with the last positive edge of the SPISCL\_ADDR1 being in the current SPI frame.

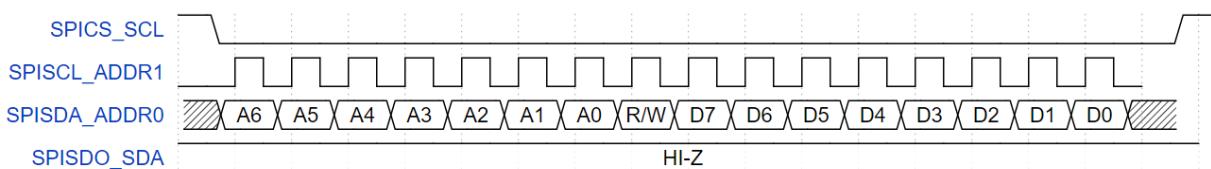


Figure 12. SPI Write Transaction

##### 3.1.3 Read Operation

A read request from the SPI Controller is decoded with the read/write enable bit (R/W). A '0' on bit (R/W) of the frame indicates a read request from the Controller.

Bits A6 to A0 provide the address of the register. For a valid address, the 8-bit contents of the respective register are read out. For invalid addresses (out-of range/unused addresses) the response will be a default value (zero). The peripheral responds to the read request one clock cycle later by setting up data on the falling edge; the Controller reads data on the rising edge.

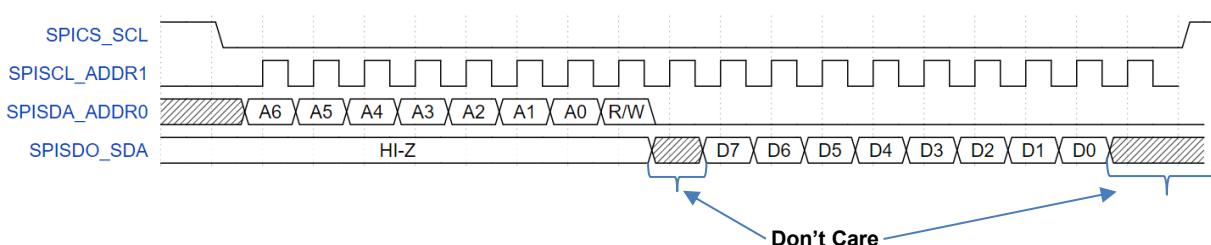


Figure 13. SPI Read Transaction

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## Functional Description (continued)

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### 4. Programming (I<sup>2</sup>C)

#### 4.1 I<sup>2</sup>C Interface

The I<sup>2</sup>C-compatible two-wire serial interface provides access to the programmable functions and registers on the device. This protocol uses a two-wire interface for bidirectional communications between the devices connected to the bus. The two interface lines are the serial data line (SDA) and the serial clock line (SCL). Every device on the bus is assigned a unique address and acts as either a master or a slave depending on whether it generates or receives the serial clock, SCL. The SCL and SDA lines should each have a pull-up resistor placed somewhere on the line and remain HIGH even when the bus is idle.

##### 4.1.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock signal (SCL). In other words, the state of the data line can only be changed when the clock signal is LOW.

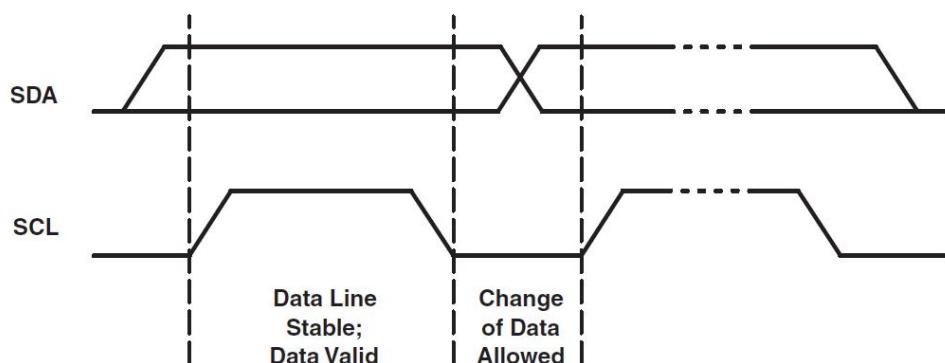


Figure 14. Data Validity

##### 4.1.2 Start and Stop Conditions

START and STOP conditions classify the beginning and the end of the data transfer session. A START condition is defined as the SDA signal transitioning from HIGH to LOW while the SCL line is HIGH. A STOP condition is defined as the SDA transitioning from LOW to HIGH while SCL is HIGH. The bus master always generates START and STOP conditions. The bus is considered to be busy after a START condition, and free after a STOP condition. During data transmission, the bus master can generate repeated START conditions. First START and repeated START conditions are functionally equivalent.

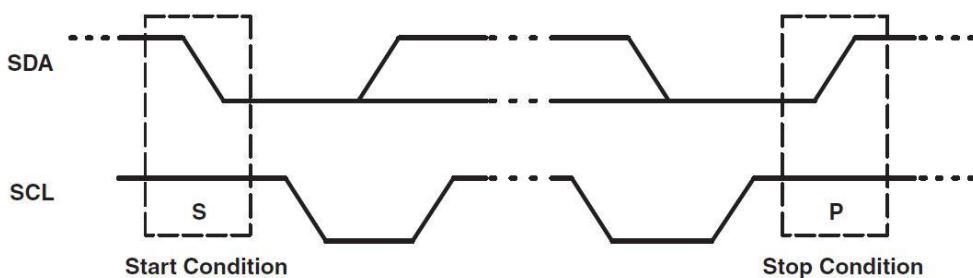


Figure 15. Start and Stop Conditions

## Functional Description (continued)

### 4.1.3 Transferring Data

Every byte put on the SDA line must be eight bits long, with the most significant bit (MSB) being transferred first. Each byte of data must be followed by an acknowledge bit. The acknowledge-related clock pulse is generated by the master. The master releases the SDA line (HIGH) during the acknowledge clock pulse. The device pulls down the SDA line during the 9th clock pulse, signifying an acknowledge. The device generates an acknowledge after each byte has been received.

There is one exception to the acknowledge-after-every-byte rule. When the master is the receiver, it must indicate to the transmitter an end of data by not acknowledging (negative acknowledge) the last byte clocked out of the slave. This negative acknowledge still includes the acknowledge clock pulse (generated by the master), but the SDA line is not pulled down.

After the START condition, the bus master sends a chip address. This address is seven bits long followed by an eighth bit, which is a data direction bit (READ or WRITE). For the eighth bit, a 0 indicates a WRITE, and a 1 indicates a READ. The second byte selects the register to which the data is written. The third byte contains data to write to the selected register.

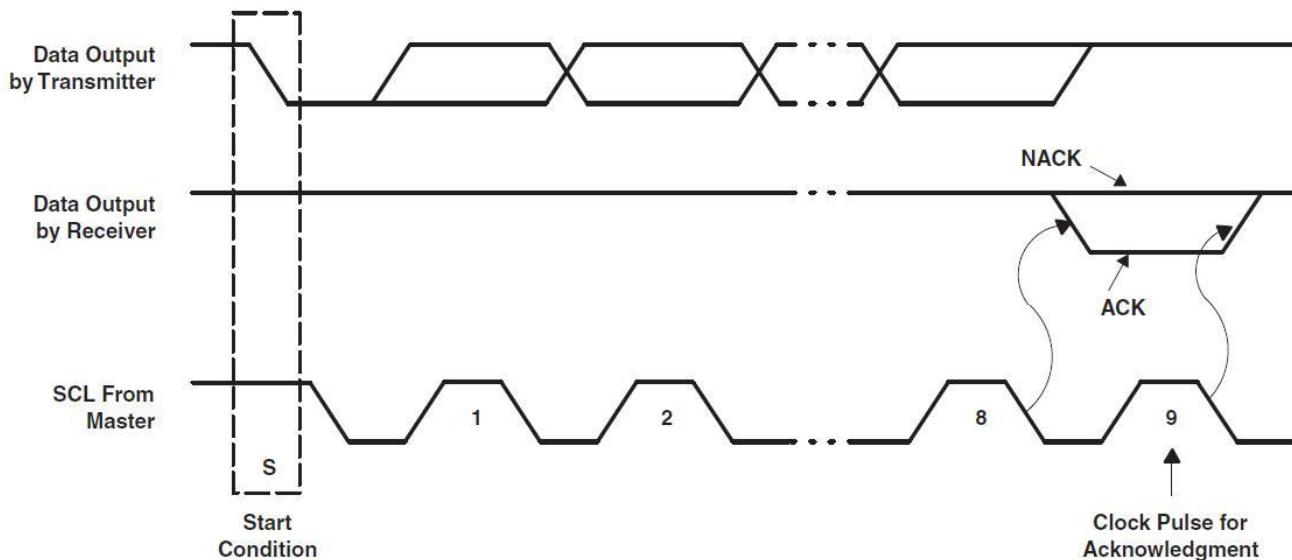


Figure 16. Acknowledge and Not Acknowledge on I<sup>2</sup>C Bus

**Functional Description** (continued)**4.1.4 I<sup>2</sup>C Slave Addressing**

The AL5887Q slave address is defined by connecting GND or VIO to the SPISDA\_ADDR0 and SPISCL\_ADDR1 pins. A total of four independent slave addresses can be realized by combinations when GND or VIO are connected to the SPISDA\_ADDR0 and SPISCL\_ADDR1 pins (see Table 6 and Table 7).

The device has a slave address for Broadcast Mode which allows MCU to configure multiple AL5887Q devices simultaneously. The device responds to a broadcast slave address regardless of the setting of the SPISDA\_ADDR0 and SPISCL\_ADDR1 pins. Global writing to the broadcast address can be used for configuring all devices simultaneously. The device supports global read using a broadcast address; however, the data read is only valid if all devices on the I<sup>2</sup>C bus contain the same value in the addressed register.

**Table 6. Slave-Address Combinations**

SPISCL_ADDR1	SPISDA_ADDR0	Slave Address	
		Independent	Broadcast
GND	GND	011 0000	001 1100
GND	Vio	011 0001	
Vio	GND	011 0010	
Vio	Vio	011 0011	

**Table 7. Chip Address**

	Slave Address								R/W
	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Independent	0	1	1	0	0	SPISCL_ADDR1	SPISDA_ADDR0	1 or 0	
Broadcast	0	0	1	1	1	0	0	1 or 0	

**4.1.5 Control-Register Write Cycle**

- The master device generates a start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/W = 0).
- The slave device sends an acknowledge signal if the slave address is correct.
- The master device sends the control register address (8 bits).
- The slave device sends an acknowledge signal.
- The master device sends the data byte to be written to the addressed register.
- The slave device sends an acknowledge signal.
- If the master device sends further data bytes, the control register address of the slave is incremented by 1 after the acknowledge signal. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits. In this Auto Incrementation Mode MCU can write or read consecutive registers within one transmission.
- The write cycle ends when the master device creates a stop condition.

**Figure 17. Write Cycle**

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## Functional Description (continued)

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### 4.1.6 Control-Register Read Cycle

- The master device generates a start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/W = 0).
- The slave device sends an acknowledge signal if the slave address is correct.
- The master device sends the control register address (8 bits).
- The slave device sends an acknowledge signal.
- The master device generates a repeated-start condition.
- The master device sends the slave address (7 bits) and the data direction bit (R/W = 1).
- The slave device sends an acknowledge signal if the slave address is correct.
- The slave device sends the data byte from the addressed register.
- If the master device sends an acknowledge signal, the control-register address is incremented by 1. The slave device sends the data byte from the addressed register. To reduce program load time, the device supports address auto incrementation. The register address is incremented after each 8 data bits.
- The read cycle ends when the master device does not generate an acknowledge signal after a data byte and generates a stop condition.

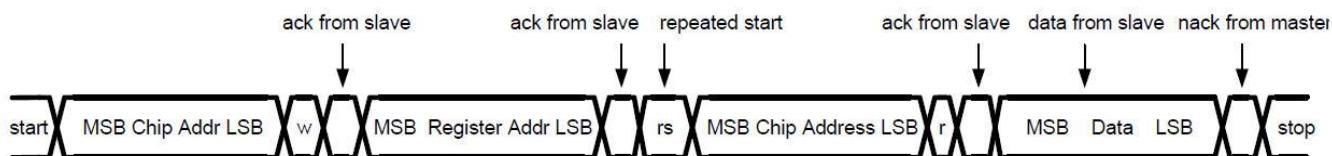


Figure 18. Read Cycle

## Register Map Description

### 5. Registers Map

Addr.	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	FDV
00h	DEVICE_CONFIG0	Reserved	CHIP_EN							00h
01h	DEVICE_CONFIG1	Phase_Shift_EN	Reserved	Log_Scale_EN	Power_Save_EN	Reserved	Dither_EN	Max_Current_Option	LED_Global_Off	AEh
02h	LED_CONFIG0	LED7_Bank_EN	LED6_Bank_EN	LED5_Bank_EN	LED4_Bank_EN	LED3_Bank_EN	LED2_Bank_EN	LED1_Bank_EN	LED0_Bank_EN	00h
03h	LED_CONFIG1			Reserved		LED11_Bank_EN	LED10_Bank_EN	LED9_Bank_EN	LED8_Bank_EN	00h
04h	BANK_BRIGHTNESS					Bank_Brightness				FFh
05h	BANK_A_COLOR					Bank_A_Color				00h
06h	BANK_B_COLOR					Bank_B_Color				00h
07h	BANK_C_COLOR					Bank_C_Color				00h
08h	RGB0_BRIGHTNESS					RGB0_Brightness				FFh
09h	RGB1_BRIGHTNESS					RGB1_Brightness				FFh
0Ah	RGB2_BRIGHTNESS					RGB2_Brightness				FFh
0Bh	RGB3_BRIGHTNESS					RGB3_Brightness				FFh
0Ch	RGB4_BRIGHTNESS					RGB4_Brightness				FFh
0Dh	RGB5_BRIGHTNESS					RGB5_Brightness				FFh
0Eh	RGB6_BRIGHTNESS					RGB6_Brightness				FFh
0Fh	RGB7_BRIGHTNESS					RGB7_Brightness				FFh
10h	RGB8_BRIGHTNESS					RGB8_Brightness				FFh
11h	RGB9_BRIGHTNESS					RGB9_Brightness				FFh
12h	RGB10_BRIGHTNESS					RGB10_Brightness				FFh
13h	RGB11_BRIGHTNESS					RGB11_Brightness				FFh
14h	R0_COLOR					R0_Color				00h
15h	G0_COLOR					G0_Color				00h
16h	B0_COLOR					B0_Color				00h
17h	R1_COLOR					R1_Color				00h
18h	G1_COLOR					G1_Color				00h
19h	B1_COLOR					B1_Color				00h
1Ah	R2_COLOR					R2_Color				00h
1Bh	G2_COLOR					G2_Color				00h
1Ch	B2_COLOR					B2_Color				00h
1Dh	R3_COLOR					R3_Color				00h
1Eh	G3_COLOR					G3_Color				00h
1Fh	B3_COLOR					B3_Color				00h
20h	R4_COLOR					R4_Color				00h
21h	G4_COLOR					G4_Color				00h
22h	B4_COLOR					B4_Color				00h
23h	R5_COLOR					R5_Color				00h
24h	G5_COLOR					G5_Color				00h
25h	B5_COLOR					B5_Color				00h
26h	R6_COLOR					R6_Color				00h
27h	G6_COLOR					G6_Color				00h
28h	B6_COLOR					B6_Color				00h
29h	R7_COLOR					R7_Color				00h
2Ah	G7_COLOR					G7_Color				00h
2Bh	B7_COLOR					B7_Color				00h
2Ch	R8_COLOR					R8_Color				00h
2Dh	G8_COLOR					G8_Color				00h
2Eh	B8_COLOR					B8_Color				00h
2Fh	R9_COLOR					R9_Color				00h
30h	G9_COLOR					G9_Color				00h
31h	B9_COLOR					B9_Color				00h
32h	R10_COLOR					R10_Color				00h
33h	G10_COLOR					G10_Color				00h
34h	B10_COLOR					B10_Color				00h
35h	R11_COLOR					R11_Color				00h
36h	G11_COLOR					G11_Color				00h
37h	B11_COLOR					B11_Color				00h
38h	RESET					RESET				00h
65h	FLAG		Reserved		FLAG_POR	FLAG_PREUVLO	FLAG_PREOTP	FLAG_SHORT	FLAG_OPEN	10h
66h	LED_GLOBAL_DIMMING		Reserved	G5	G4	G3	G2	G1	G0	00h
67h	FAULT_WAIT				Reserved			FW1	FW0	00h
68h	MASK and CLR	Reserved	POR_Mask	PreUVLO_Mask	PreOTP_Mask	Short_Mask	Open_Mask	CLR_Fault	CLR_POR	00h

\* FDV = Factory Default Value

## Register Map Description (continued)

Addr.	Name	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0	FDV
6Ah	OM0	OM_OUT7	OM_OUT6	OM_OUT5	OM_OUT4	OM_OUT3	OM_OUT2	OM_OUT1	OM_OUT0	00h
6Bh	OM1	OM_OUT15	OM_OUT14	OM_OUT13	OM_OUT12	OM_OUT11	OM_OUT10	OM_OUT9	OM_OUT8	00h
6Ch	OM2	OM_OUT23	OM_OUT22	OM_OUT21	OM_OUT20	OM_OUT19	OM_OUT18	OM_OUT17	OM_OUT16	00h
6Dh	OM3	OM_OUT31	OM_OUT30	OM_OUT29	OM_OUT28	OM_OUT27	OM_OUT26	OM_OUT25	OM_OUT24	00h
6Eh	OM4	Reserved					OM_OUT35	OM_OUT34	OM_OUT33	OM_OUT32
6Fh	SM0	SM_OUT7	SM_OUT6	SM_OUT5	SM_OUT4	SM_OUT3	SM_OUT2	SM_OUT1	SM_OUT0	00h
70h	SM1	SM_OUT15	SM_OUT14	SM_OUT13	SM_OUT12	SM_OUT11	SM_OUT10	SM_OUT9	SM_OUT8	00h
71h	SM2	SM_OUT23	SM_OUT22	SM_OUT21	SM_OUT20	SM_OUT19	SM_OUT18	SM_OUT17	SM_OUT16	00h
74h	SM3	SM_OUT31	SM_OUT30	SM_OUT29	SM_OUT28	SM_OUT27	SM_OUT26	SM_OUT25	SM_OUT24	00h
75h	SM4	Reserved					SM_OUT35	SM_OUT34	SM_OUT33	SM_OUT32
76h	OF0	OF_OUT7	OF_OUT6	OF_OUT5	OF_OUT4	OF_OUT3	OF_OUT2	OF_OUT1	OF_OUT0	00h
77h	OF1	OF_OUT15	OF_OUT14	OF_OUT13	OF_OUT12	OF_OUT11	OF_OUT10	OF_OUT9	OF_OUT8	00h
78h	OF2	OF_OUT23	OF_OUT22	OF_OUT21	OF_OUT20	OF_OUT19	OF_OUT18	OF_OUT17	OF_OUT16	00h
79h	OF3	OF_OUT31	OF_OUT30	OF_OUT29	OF_OUT28	OF_OUT27	OF_OUT26	OF_OUT25	OF_OUT24	00h
7Ah	OF4	Reserved					OF_OUT35	OF_OUT34	OF_OUT33	OF_OUT32
7Bh	SF0	SF_OUT7	SF_OUT6	SF_OUT5	SF_OUT4	SF_OUT3	SF_OUT2	SF_OUT1	SF_OUT0	00h
7Ch	SF1	SF_OUT15	SF_OUT14	SF_OUT13	SF_OUT12	SF_OUT11	SF_OUT10	SF_OUT9	SF_OUT8	00h
7Dh	SF2	SF_OUT23	SF_OUT22	SF_OUT21	SF_OUT20	SF_OUT19	SF_OUT18	SF_OUT17	SF_OUT16	00h
7Eh	SF3	SF_OUT31	SF_OUT30	SF_OUT29	SF_OUT28	SF_OUT27	SF_OUT26	SF_OUT25	SF_OUT24	00h
7Fh	SF4	Reserved					SF_OUT35	SF_OUT34	SF_OUT33	SF_OUT32

\* OMx = Open Maskx

\* SMx = Short Maskx

\* OFx = Open Faultx

\* SFx = Short Faultx

\* FDV = Factory Default Value

Table 8. Access Type Codes

Access Type	Code	Description
<b>Read Type</b>		
R	R	Read
<b>Write Type</b>		
W	W	Write
<b>Power On Reset or Default value</b>		
(xxh)	(xxh)	Value after POR or default value

### 5.1 DEVICE\_CONFIG0 (Address = 00h) [default = 00h]

Table 9. DEVICE\_CONFIG0 Register

7	6	5	4	3	2	1	0
Reserved	Chip_EN	Reserved					
Reserved	R/W-(00h)	Reserved					
Reserved	0 = AL5887Q Disabled 1 = AL5887Q Enabled	Reserved					

## Register Map Description (continued)

### 5.2 DEVICE\_CONFIG1 (Address = 01h) [default = AEh]

Table 10. DEVICE\_CONFIG1 Register

7	6	5	4	3	2	1	0
Phase_Shift_EN	Reserved	Log_Scale_EN	Power_Save_EN	Reserved	Dither_EN	Max_Current_Option	LED_Global_Off
R/W-(01h)	R/W-(00h)	R/W-(01h)	R/W-(00h)	R/W-(01h)	R/W-(01h)	R/W-(01h)	R/W-(00h)
0 = Disabled 1 = Enabled	—	0 = Linear curve Enabled 1 = Logarithmic curve Enabled	0 = Power Save Mode Disabled 1 = Power Save Mode Enabled	—	0 = Disabled 1 = Enabled	0 = 29.25mA 1 = 39mA	0 = Normal Operation 1 = Shutdown all LEDs

### 5.3 LED\_CONFIG0 (Address = 02h) [default = 00h]

Table 11. LED\_CONFIG0 Register

7	6	5	4	3	2	1	0
LED7_Bank_EN	LED6_Bank_EN	LED5_Bank_EN	LED4_Bank_EN	LED3_Bank_EN	LED2_Bank_EN	LED1_Bank_EN	LED0_Bank_EN
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* 0 = Independent Mode Enabled

\* 1 = Bank Mode Enabled

### 5.4 LED\_CONFIG1 (Address = 03h) [default = 00h]

Table 12. LED\_CONFIG1 Register

7	6	5	4	3	2	1	0
Reserved			LED11_Bank_EN	LED10_Bank_EN	LED9_Bank_EN	LED8_Bank_EN	
R/W-(00h)							
Reserved			0/1	0/1	0/1	0/1	0/1

\* 0 = Independent Mode Enabled

\* 1 = Bank Mode Enabled

### 5.5 BANK\_BRIGHTNESS (Address = 04h) [default = FFh]

Table 13. BANK\_BRIGHTNESS Register

7	6	5	4	3	2	1	0
BANK_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness							
...							
80h = 50% of full brightness							
...							
FFh = 100 % of full brightness							

### 5.6 BANK\_A\_COLOR (Address = 05h) [default = 00h]

Table 14. BANK\_A\_COLOR Register

7	6	5	4	3	2	1	0
BANK_A_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
...							
80h = The color mixing percentage is 50%							
...							
FFh = The color mixing percentage is 100%							

## Register Map Description (continued)

### 5.7 BANK\_B\_COLOR (Address = 06h) [default = 00h]

Table 15. BANK\_B\_COLOR Register

7	6	5	4	3	2	1	0
BANK_B_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
... 80h = The color mixing percentage is 50%							
... FFh = The color mixing percentage is 100%							

### 5.8 BANK\_C\_COLOR (Address = 07h) [default = 00h]

Table 16. BANK\_C\_COLOR Register

7	6	5	4	3	2	1	0
BANK_C_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
... 80h = The color mixing percentage is 50%							
... FFh = The color mixing percentage is 100%							

### 5.9 RGB0 to RGB11\_BRIGHTNESS (Address = 08h to 13h) [default = FFh]

Table 17. RGB0 to RGB11\_BRIGHTNESS Register

7	6	5	4	3	2	1	0
RGB0 to RGB11_BRIGHTNESS							
R/W-(FFh)							
00h = 0% of full brightness							
... 80h = 50% of full brightness							
... FFh = 100 % of full brightness							

### 5.10 Rx\_COLORx = 0 to 11 (Address = 14h to 1Eh) [default = 00h]

Table 18. Rx\_COLOR Register

7	6	5	4	3	2	1	0
Rx_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
... 80h = The color mixing percentage is 50%							
... FFh = The color mixing percentage is 100%							

## Register Map Description (continued)

### 5.11 Gx\_COLORx = 0 to 11 (Address = 1Fh to 2Ah) [default = 00h]

Table 19. Gx\_COLOR Register

7	6	5	4	3	2	1	0
Gx_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
... 80h = The color mixing percentage is 50%							
... FFh = The color mixing percentage is 100%							

### 5.12 Bx\_COLORx = 0 to 11 (Address = 2Bh to 37h) [default = 00h]

Table 20. Bx\_COLOR Register

7	6	5	4	3	2	1	0
Bx_COLOR							
R/W-(00h)							
00h = The color mixing percentage is 0%							
... 80h = The color mixing percentage is 50%							
... FFh = The color mixing percentage is 100%							

### 5.13 RESET (Address = 38h) [default = 00h]

Table 21. RESET Register

7	6	5	4	3	2	1	0
RESET							
W-(00h)							
FFh = Resets all the registers to default value.							

### 5.14 FLAG (Address = 65h) [default = 00h]

Table 22. FLAG Register

7	6	5	4	3	2	1	0
Reserved	FLAG_POR	FLAG_PREUVLO	FLAG_PREOTP	FLAG_SHORT	FLAG_OPEN		
R/W-(00h)							
Reserved	0 = No POR fault reported. 1 = POR fault reported.	0 = No Pre_UVLO fault reported. 1 = Pre_UVLO fault reported.	0 = No Pre OTP fault reported. 1 = Pre OTP fault reported.	0 = No short fault reported on any channel. 1 = Short fault reported on any of the channels.	0 = No open fault reported on any channel. 1 = Open fault reported on any of the channels.		

### 5.15 LED\_GLOBAL\_DIMMING (Address = 66h) [default = 00h]

Table 23. LED\_GLOBAL\_DIMMING Register

7	6	5	4	3	2	1	0
Reserved	G5	G4	G3	G2	G1	G0	
R/W-(00h)							
Reserved	6-bit LED Global current setting. See <a href="#">Table 3</a> for details.						

## Register Map Description (continued)

### 5.16 FAULT\_WAIT (Address = 67h) [default = 00h]

Table 24. FAULT\_WAIT Register

7	6	5	4	3	2	1	0
Reserved				FW1		FW0	
R/W-(00h)							
Reserved				0 = as per <a href="#">Table 2</a> 1 = as per <a href="#">Table 2</a>		0 = as per <a href="#">Table 2</a> 1 = as per <a href="#">Table 2</a>	

### 5.17 MASK and CLR (Address = 68h) [default = 00h]

Table 25. MASK and CLR Register

7	6	5	4	3	2	1	0
Reserved	POR_Mask	PreUVLOMask	PreOTP_Mask	Short_Mask	Open_Mask	CLR_Fault	CLR_POR
R/W-(00h)							
Reserved	0 = POR mask turned off 1 = POR mask turned on	0 = Pre-UVLO mask turned off 1 = Pre-UVLO mask turned on	0 = Pre-OTP mask turned off 1 = Pre-OTP mask turned on	0 = Short Detection Mask off 1 = Short Detection Mask on	0 = Open Detection Mask off 1 = Open Detection Mask on	0 = Clearing faults turned off 1 = Clears the faults	0 = Clearing POR turned off 1 = Clears the POR faults

### 5.18 OM0 (Address = 6Ah) [default = 00h]

Table 26. OM0 Register

7	6	5	4	3	2	1	0
*OM_OUT7	OM_OUT6	OM_OUT5	OM_OUT4	OM_OUT3	OM_OUT2	OM_OUT1	OM_OUT0
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* OM = Open Maskx

\* 0 = Open Detection Mask Off

\* 1 = Open Detection Mask On

### 5.19 OM1 (Address = 6Bh) [default = 00h]

Table 27. OM1 Register

7	6	5	4	3	2	1	0
*OM_OUT15	OM_OUT14	OM_OUT13	OM_OUT12	OM_OUT11	OM_OUT10	OM_OUT9	OM_OUT8
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* OM = Open Maskx

\* 0 = Open Detection Mask Off

\* 1 = Open Detection Mask On

### 5.20 OM2 (Address = 6Ch) [default = 00h]

Table 28. OM2 Register

7	6	5	4	3	2	1	0
*OM_OUT23	OM_OUT22	OM_OUT21	OM_OUT20	OM_OUT19	OM_OUT18	OM_OUT17	OM_OUT16
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* OM = Open Maskx

\* 0 = Open Detection Mask Off

\* 1 = Open Detection Mask On

## Register Map Description (continued)

### 5.21 OM3 (Address = 6Dh) [default = 00h]

**Table 29. OM3 Register**

7	6	5	4	3	2	1	0
OM_OUT31	OM_OUT30	OM_OUT29	OM_OUT28	OM_OUT27	OM_OUT26	OM_OUT25	OM_OUT24
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* OM = Open Maskx

\* 0 = Open Detection Mask Off

\* 1 = Open Detection Mask On

### 5.22 OM4 (Address = 6Eh) [default = 00h]

**Table 30. OM4 Register**

7	6	5	4	3	2	1	0
			Reserved	OM_OUT35	OM_OUT34	OM_OUT33	OM_OUT32
R/W-(00h)							
			Reserved	0/1	0/1	0/1	0/1

\* OM = Open Maskx

\* 0 = Open Detection Mask Off

\* 1 = Open Detection Mask On

### 5.23 SM0 (Address = 6Fh) [default = 00h]

**Table 31. SM0 Register**

7	6	5	4	3	2	1	0
SM_OUT7	SM_OUT6	SM_OUT5	SM_OUT4	SM_OUT3	SM_OUT2	SM_OUT1	SM_OUT0
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* SM = Short Maskx

\* 0 = Short Detection Mask Off

\* 1 = Short Detection Mask On

### 5.24 SM1 (Address = 70h) [default = 00h]

**Table 32. SM1 Register**

7	6	5	4	3	2	1	0
SM_OUT15	SM_OUT14	SM_OUT13	SM_OUT12	SM_OUT11	SM_OUT10	SM_OUT9	SM_OUT8
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* SM = Short Maskx

\* 0 = Short Detection Mask Off

\* 1 = Short Detection Mask On

## Register Map Description (continued)

### 5.25 SM2 (Address = 71h) [default = 00h]

Table 33. SM2 Register

7	6	5	4	3	2	1	0
SM_OUT23	SM_OUT22	SM_OUT21	SM_OUT20	SM_OUT19	SM_OUT18	SM_OUT17	SM_OUT16
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* SM = Short Maskx

\* 0 = Short Detection Mask Off

\* 1 = Short Detection Mask On

### 5.26 SM3 (Address = 74h) [default = 00h]

Table 34. SM3 Register

7	6	5	4	3	2	1	0
SM_OUT31	SM_OUT30	SM_OUT29	SM_OUT28	SM_OUT27	SM_OUT26	SM_OUT25	SM_OUT24
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* SM = Short Maskx

\* 0 = Short Detection Mask Off

\* 1 = Short Detection Mask On

### 5.27 SM4 (Address = 75h) [default = 00h]

Table 35. SM4 Register

7	6	5	4	3	2	1	0
Reserved				SM_OUT35	SM_OUT34	SM_OUT33	SM_OUT32
R/W-(00h)							
Reserved				0/1	0/1	0/1	0/1

\* SM = Short Maskx

\* 0 = Short Detection Mask Off

\* 1 = Short Detection Mask On

### 5.28 OF0 (Address = 76h) [default = 00h]

Table 36. OF0 Register

7	6	5	4	3	2	1	0
OF_OUT7	OF_OUT6	OF_OUT5	OF_OUT4	OF_OUT3	OF_OUT2	OF_OUT1	OF_OUT0
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* OF = Open Faultx

\* 0 = Open Fault Not Detected

\* 1 = Open Fault Detected

## Register Map Description (continued)

### 5.29 OF1 (Address = 77h) [default = 00h]

Table 37. OF1 Register

7	6	5	4	3	2	1	0
OF_OUT15	OF_OUT14	OF_OUT13	OF_OUT12	OF_OUT11	OF_OUT10	OF_OUT9	OF_OUT8
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* OF = Open Faultx

\* 0 = Open Fault Not Detected

\* 1 = Open Fault Detected

### 5.30 OF2 (Address = 78h) [default = 00h]

Table 38. OF2 Register

7	6	5	4	3	2	1	0
OF_OUT23	OF_OUT22	OF_OUT21	OF_OUT20	OF_OUT19	OF_OUT18	OF_OUT17	OF_OUT16
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* OF = Open Faultx

\* 0 = Open Fault Not Detected

\* 1 = Open Fault Detected

### 5.31 OF3 (Address = 79h) [default = 00h]

Table 39. OF3 Register

7	6	5	4	3	2	1	0
OF_OUT31	OF_OUT30	OF_OUT29	OF_OUT28	OF_OUT27	OF_OUT26	OF_OUT25	OF_OUT24
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* OF = Open Faultx

\* 0 = Open Fault Not Detected

\* 1 = Open Fault Detected

### 5.32 OF4 (Address = 7Ah) [default = 00h]

Table 40. OF4 Register

7	6	5	4	3	2	1	0
Reserved				OF_OUT35	OF_OUT34	OF_OUT33	OF_OUT32
R/W-(00h)							
Reserved				0/1	0/1	0/1	0/1

\* OF = Open Faultx

\* 0 = Open Fault Not Detected

\* 1 = Open Fault Detected

## Register Map Description (continued)

### 5.33 SF0 (Address = 7Bh) [default = 00h]

**Table 41. SF0 Register**

7	6	5	4	3	2	1	0
SF_OUT7	SF_OUT6	SF_OUT5	SF_OUT4	SF_OUT3	SF_OUT2	SF_OUT1	SF_OUT0
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* SF = Short Faultx

\* 0 = Short Fault Not Detected

\* 1 = Short Fault Detected

### 5.34 SF1 (Address = 7Ch) [default = 00h]

**Table 42. SF1 Register**

7	6	5	4	3	2	1	0
SF_OUT15	SF_OUT14	SF_OUT13	SF_OUT12	SF_OUT11	SF_OUT10	SF_OUT9	SF_OUT8
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* SF = Short Faultx

\* 0 = Short Fault Not Detected

\* 1 = Short Fault Detected

### 5.35 SF2 (Address = 7Dh) [default = 00h]

**Table 43. SF2 Register**

7	6	5	4	3	2	1	0
SF_OUT23	SF_OUT22	SF_OUT21	SF_OUT20	SF_OUT19	SF_OUT18	SF_OUT17	SF_OUT16
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* SF = Short Faultx

\* 0 = Short Fault Not Detected

\* 1 = Short Fault Detected

### 5.36 SF3 (Address = 7Eh) [default = 00h]

**Table 44. SF3 Register**

7	6	5	4	3	2	1	0
SF_OUT31	SF_OUT30	SF_OUT29	SF_OUT28	SF_OUT27	SF_OUT26	SF_OUT25	SF_OUT24
R/W-(00h)							
0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

\* SF = Short Faultx

\* 0 = Short Fault Not Detected

\* 1 = Short Fault Detected

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**Register Map Description (continued)**


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**5.37 SF4 (Address = 7Fh) [default = 00h]**
**Table 45. SF4 Register**

7	6	5	4	3	2	1	0
			Reserved	SF_OUT35	SF_OUT34	SF_OUT33	SF_OUT32
R/W-(00h)							
			Reserved	0/1	0/1	0/1	0/1

\* SF = Short Fault

\* 0 = Short Fault Not Detected

\* 1 = Short Fault Detected

## Application Information

### Timing Requirements for I<sup>2</sup>C interface (Note 11)

Symbol	Parameter	Min	Typ	Max	Unit
fsCL	I <sup>2</sup> C clock frequency	—	—	400	kHz
tEN_H	EN first rising edge until first I <sup>2</sup> C access	—	—	500	μs
tEN_L	EN first falling edge until first I <sup>2</sup> C reset	—	—	3	μs
1	Hold time (repeated) START condition	0.6	—	—	μs
2	Clock low time	1.3	—	—	μs
3	Clock high time	600	—	—	ns
4	Setup time for a repeated START condition	600	—	—	ns
5	Data hold time	0	—	—	ns
6	Data setup time	100	—	—	ns
7	Rise time of SDA and SCL	20 + 0.1 C <sub>b</sub>	—	300	ns
8	Fall time of SDA and SCL	15 + 0.1 C <sub>b</sub>	—	300	ns
9	Setup time for STOP condition	600	—	—	ns
10	Bus free time between a STOP and a START condition	1.3	—	—	ns
C <sub>b</sub>	Capacitive load parameter for each bus line. Load of 1pF corresponds to one nanosecond.	—	—	200	pF

Note: 11. Specified by design & ATE characterized.

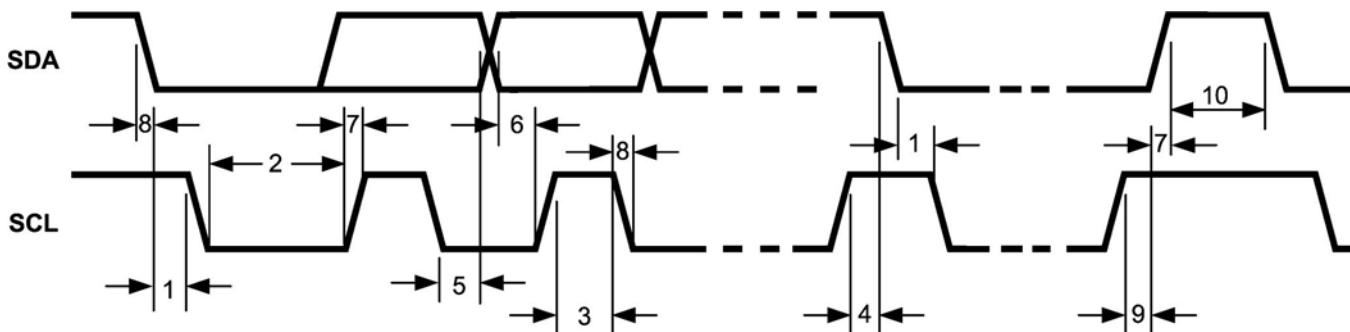


Figure 19. I<sup>2</sup>C Timing Parameters

Table 46. Input and Output Logic Levels

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>DIGITAL INPUT LOGIC LEVELS (EN, RSTn, INT_SEL)</b>						
V <sub>IL</sub>	Input logic low	V <sub>io</sub> = 1.8V	—	—	0.35	V
V <sub>IH</sub>	Input logic high		1.4	—	—	V
<b>DIGITAL INTERFACE LOGIC LEVELS (SPICS_SCL, SPISDO_SDA, SPISDA_ADDR0, SPISCL_ADDR1)</b>						
V <sub>IL</sub>	Input logic low	V <sub>io</sub> = 1.8V	—	—	0.4	V
V <sub>IH</sub>	Input logic high		1.4	—	—	V
V <sub>SDA</sub>	SDA output low level	I <sub>PULLUP</sub> = 5mA	—	—	0.4	V

## Application Information (continued)

### Timing Requirements for SPI interface (Note 12)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
fsCLK	SPI clock frequency	—	—	—	4	MHz
tcss	The time from SPICS_SCL low to SPISCL_ADDR1 high	—	250	—	—	ns
tCSH	The time from SPISCL_ADDR1 low to SPICS_SCL high	—	250	—	—	ns
tDS	Data set-up time	—	10	—	—	ns
tDH	Data hold time	—	0	—	—	ns
tCS_HI	Minimum chip select de-asserted HIGH time	—	250	—	—	ns
td(SDO)	SDO delay time	$C_L = 50\text{pF}$	—	—	20	ns
tLOW	LOW period of SCLK clock	—	125	—	—	ns
tHIGH	HIGH period of SCLK clock	—	125	—	—	ns

Note: 12. Specified by design & ATE characterized.

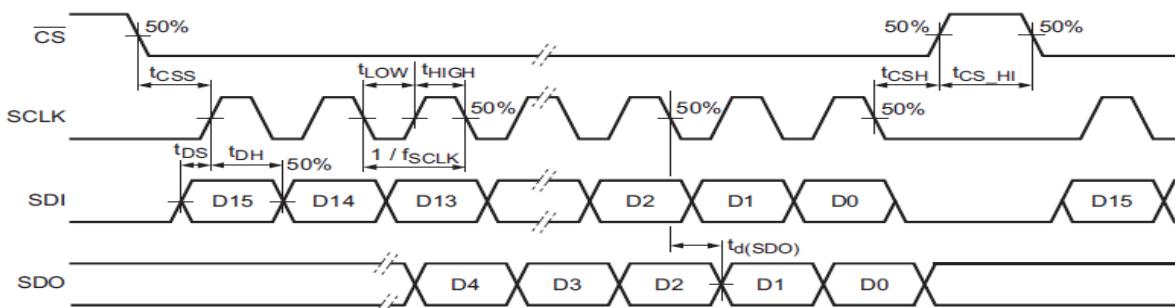


Figure 20. SPI Timing Parameters

### Design Tools (Note 13)

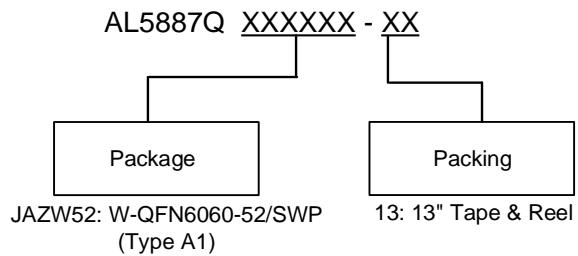
- AL5887QEVT1 Demo Board
- Labview Emulator for EV1
- AL5887QEVT2 Demo Board
- Arduino Sample Code for EV2
- Demo Board Gerber File for PCB Layout Reference
- PSPICE available

Note: 13. Diodes' design tools can be found on our website at <https://www.diodes.com/design/tools/>.

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## Ordering Information

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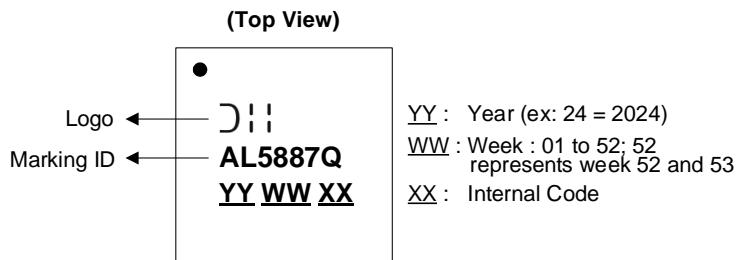
Orderable Part Number	Part Number Suffix	Package Code	Package (Note 13)	Packing	
				Qty.	Carrier
AL5887QJAZW52-13	-13	JAZW52	W-QFN6060-52/SWP (Type A1)	4,000	Tape & Reel

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## Marking Information

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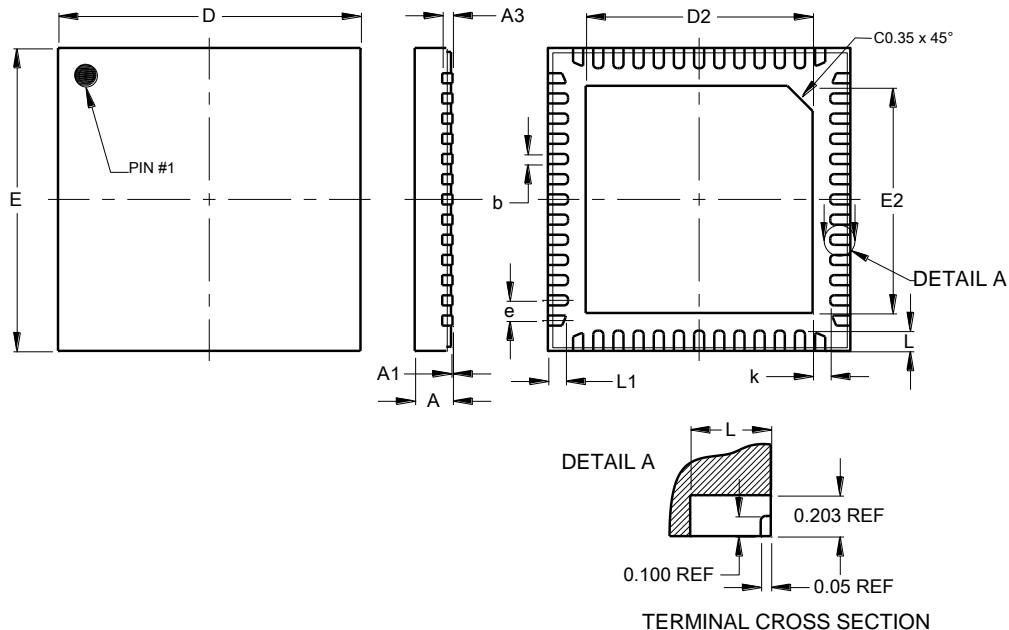
W-QFN6060-52/SWP (Type A1)



## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

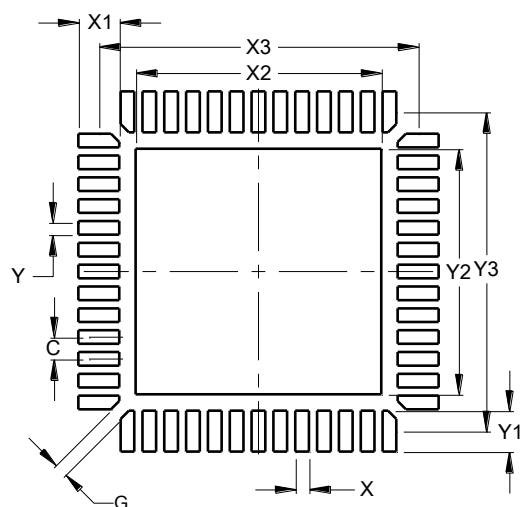
**W-QFN6060-52/SWP (Type A1)**



## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

**W-QFN6060-52/SWP (Type A1)**



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## Tape and Reel Information

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Please see <https://www.diodes.com/assets/Packaging-Support-Docs/AP02007.pdf> for tape and reel details.

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## Mechanical Data

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### Package W-QFN6060-52/SWP (Type A1)

- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – Matte Tin Plated Leads, Solderable per JESD22-B102 
- Weight: 0.0091 grams (Approximate)

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