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## Single-Chip Bluetooth Transceiver for Wireless Input Devices

### GENERAL DESCRIPTION

The Broadcom<sup>®</sup> BCM20734 is a Bluetooth 4.1-compliant, stand-alone baseband processor with an integrated 2.4 GHz transceiver. Manufactured using the industry's most advanced 40 nm CMOS low-power process, the BCM20734 employs the highest level of integration to eliminate all critical external components, thereby minimizing the device's footprint and the costs associated with implementing Bluetooth solutions.

The BCM20734 is the optimal solution for applications in wireless input devices including game controllers, remote, keyboards, and joysticks. Built-in firmware adheres to the Bluetooth Low Energy (BLE) profile and the BLE Human Interface Device (HID) profile.

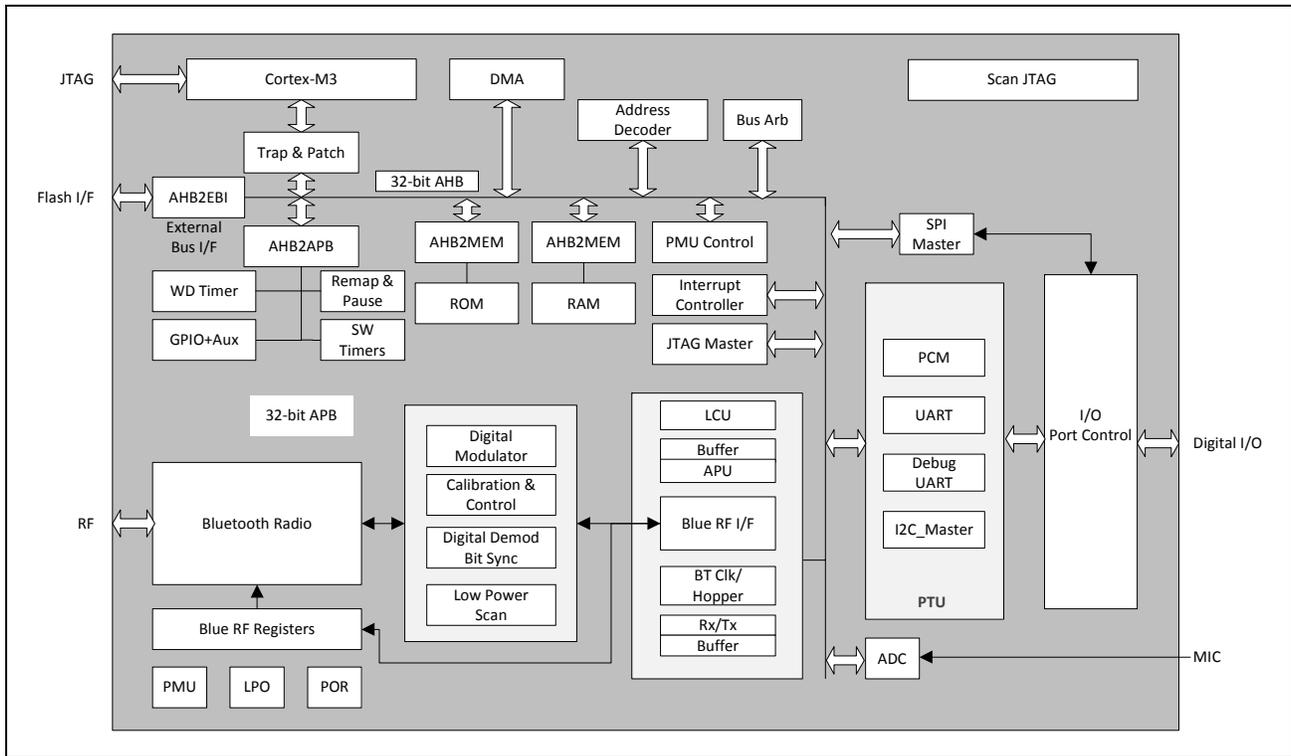
### APPLICATIONS

- Game controllers
- Wireless pointing devices (mice)
- Remote controls
- Wireless keyboards
- Joysticks
- Home automation
- Point-of-sale input devices
- 3D glasses
- Blood pressure monitors
- "Find me" devices
- Heart rate monitors
- Proximity sensors
- Thermometers

### FEATURES

- Complies with Bluetooth Core Specification version 4.1 including BR/EDR/BLE
- Supports Broadcom proprietary LE data rate up to 2 Mbps
- BLE HID profile version 1.00 compliant
- Bluetooth Device ID profile version 1.3 compliant
- Supports Generic Access Profile (GAP)
- Supports Adaptive Frequency Hopping (AFH)
- Excellent receiver sensitivity
- Programmable output power control
- Integrated ARM Cortex-M3 microprocessor core
- On-chip power-on reset (POR)
- Support for EEPROM and serial flash interfaces
- Integrated low dropout regulator (LDO)
- On-chip software controlled power management unit
- Programmable key scan matrix interface, up to 8 × 20 key-scanning matrix
- Three-axis quadrature signal decoder
- PCM/I<sup>2</sup>S Interface
- Infrared modulator
- IR learning
- Auxiliary ADC with up to 28 analog channels
- One mono microphone input
- On-chip support for serial peripheral interface (master and slave modes)
- Broadcom Serial Communications interface (compatible with NXP I<sup>2</sup>C slaves)
- Package type:
  - 90-pin FBGA package (8.5 mm × 8.5 mm)
  - RoHS compliant

**Figure 1: Functional Block Diagram**



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## Revision History

<b>Revision</b>	<b>Date</b>	<b>Change Description</b>
20734-DS109-R	10/21/14	<b>Updated:</b> <ul style="list-style-type: none"><li>• <a href="#">“External Reset” on page 13.</a></li></ul>
20734-DS108-R	09/25/14	<b>Updated:</b> <ul style="list-style-type: none"><li>• Table 8: “Absolute Maximum Voltages,” on page 38.</li><li>• Table 14: “Current Consumption For BR and EDR, Class 1,” on page 42.</li><li>• Table 15: “Current Consumption For BR and EDR, Class 2 (0 dBm),” on page 43.</li><li>• Table 16: “Receiver RF Specifications,” on page 44.</li><li>• Table 23: “PCM Interface Timing Specifications (Short Frame Sync, Master Mode),” on page 52.</li><li>• “PCM Interface Timing” on page 52.</li></ul>
20734-DS107-R	06/26/14	Refer to the earlier released documents for revision history details.

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## About This Document

### Purpose and Audience

The data sheet provides details of the functional, operational, and electrical characteristics of the Broadcom® BCM20734 device. It is intended for hardware, design, application, and OEM engineers.

### Acronyms and Abbreviations

In most cases, acronyms and abbreviations are defined on first use. Acronyms and abbreviations in this document are also defined in [Appendix A: “Acronyms and Abbreviations,” on page 62](#).

For a comprehensive list of acronyms and other terms used in Broadcom documents, go to: <http://www.broadcom.com/press/glossary.php>.

## Technical Support

Broadcom provides customer access to a wide range of information, including technical documentation, schematic diagrams, product bill of materials, PCB layout information, and software updates through its customer support portal (<https://support.broadcom.com>). For a CSP account, contact your Sales or Engineering support representative.

In addition, Broadcom provides other product support through its Downloads & Support site (<http://www.broadcom.com/support/>).

# Section 1: Functional Description

## Bluetooth Baseband Core

The Bluetooth Baseband Core (BBC) implements all of the time-critical functions required for high-performance Bluetooth operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules SCO/ACL and TX/RX transactions, monitors Bluetooth slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following transmit and receive functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), header error control (HEC), cyclic redundancy check (CRC), data decryption, and data dewatering in the receiver.
- Data framing, FEC generation, HEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

## Bluetooth 4.0 Features

The BBC supports all Bluetooth 4.0 features, with the following benefits:

- Dual-mode Bluetooth low energy (BT and BLE operation)
- Extended inquiry response (EIR): Shortens the time to retrieve the device name, specific profile, and operating mode.
- Encryption pause resume (EPR): Enables the use of Bluetooth technology in a much more secure environment.
- Sniff subrating (SSR): Optimizes power consumption for low duty cycle asymmetric data flow, which subsequently extends battery life.
- Secure simple pairing (SSP): Reduces the number of steps for connecting two devices, with minimal or no user interaction required.
- Link supervision time out (LSTO): Additional commands added to HCI and Link Management Protocol (LMP) for improved link time-out supervision.
- Quality of service (QoS) enhancements: Changes to data traffic control, which results in better link performance. Audio, human interface device (HID), bulk traffic, SCO, and enhanced SCO (eSCO) are improved with the erroneous data (ED) and packet boundary flag (PBF) enhancements.

## Bluetooth 4.1 Features

The BCM20734 supports the following Bluetooth v4.1 features.

- Secure connections (BR/EDR)
- Fast advertising interval
- Piconet clock adjust
- Connectionless broadcast
- LE privacy v1.1
- Low duty cycle directed advertising
- LE dual mode topology

## Link Control Layer

The link control layer is part of the Bluetooth link control functions that are implemented in dedicated logic in the link control unit (LCU). This layer consists of the command controller that takes commands from the software, and other controllers that are activated or configured by the command controller, to perform the link control tasks. Each task is performed in a different state or substate in the Bluetooth Link Controller.

- Major states:
  - Standby
  - Connection
- Substates:
  - Page
  - Page Scan
  - Inquiry
  - Inquiry Scan
  - Sniff

## Test Mode Support

The BCM20734 fully supports Bluetooth Test mode as described in Part I:1 of the Specification of the Bluetooth System Version 3.0. This includes the transmitter tests, normal and delayed loopback tests, and reduced hopping sequence.

In addition to the standard Bluetooth Test Mode, the BCM20734 also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing. These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Receiver output directed to I/O pin
  - Allows for direct BER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

## Frequency Hopping Generator

The frequency hopping sequence generator selects the correct hopping channel number based on the link controller state, Bluetooth clock, and device address.

---

## Microprocessor Unit

The BCM20734 microprocessor unit runs software from the link control (LC) layer up to the host controller interface (HCI). The microprocessor is based on the Cortex-M3 32-bit RISC processor with embedded ICE-RT debug and JTAG interface units. The microprocessor also includes 848 KB of ROM memory for program storage and boot ROM, 352 KB of RAM for data scratch-pad, and patch RAM code.

The internal boot ROM provides flexibility during power-on reset to enable the same device to be used in various configurations. At power-up, the lower layer protocol stack is executed from the internal ROM.

External patches can be applied to the ROM-based firmware to provide flexibility for bug fixes and features additions. These patches can be downloaded using external NVRAM. The device can also support the integration of user applications and profiles using an external serial flash memory.

## NVRAM Configuration Data and Storage

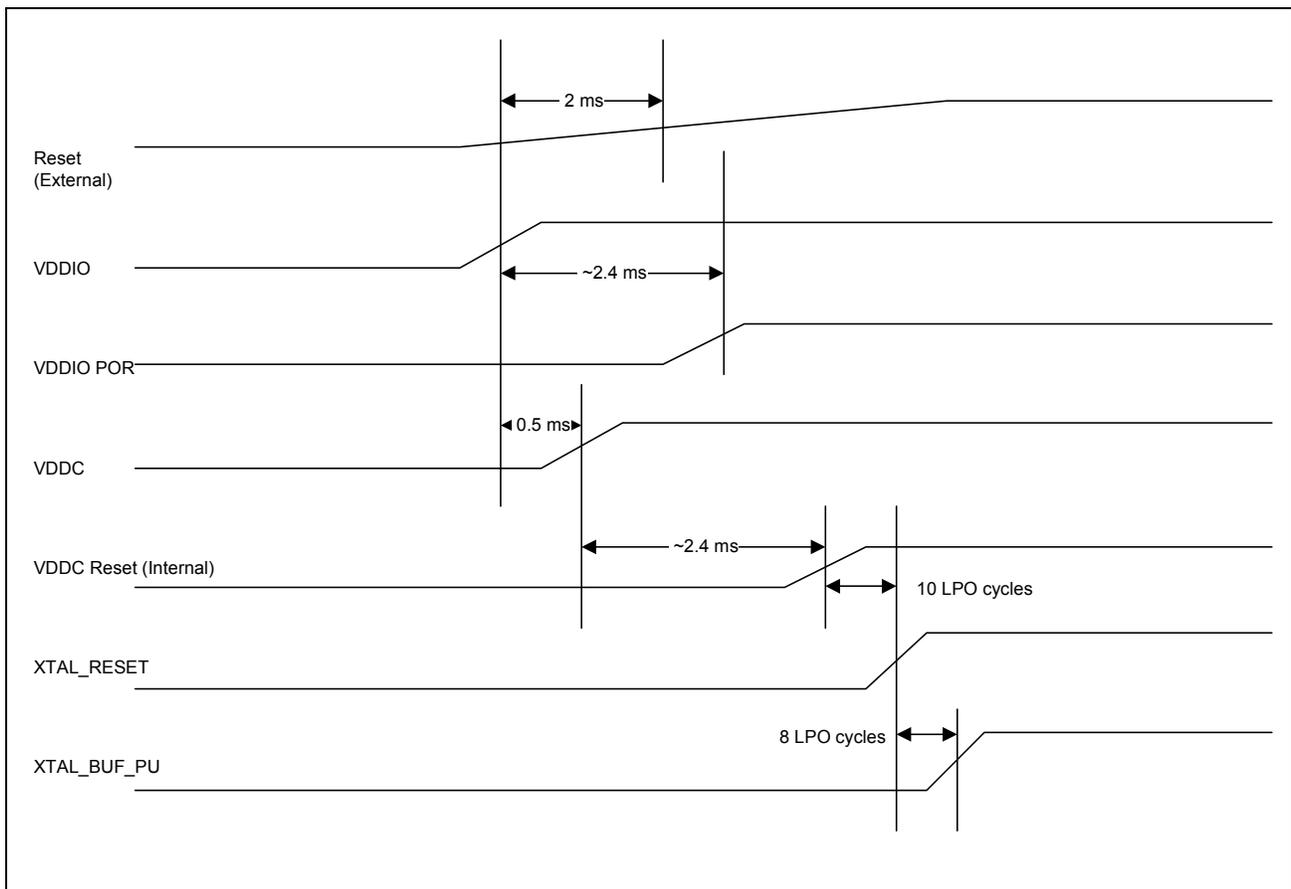
NVRAM contains configuration information about the customer application, including the following:

- Fractional-N information
- BD\_ADDR
- UART baud rate
- SDP service record
- File system information used for code, code patches, or data. The BCM20734 can use SPI Flash or I<sup>2</sup>C EEPROMs for NVRAM storage.

## External Reset

An external active-low reset signal, RESET\_N, can be used to put the BCM20734 in the reset state. An external RC is needed on the RESET\_N. The RESET\_N should be released only after the VDDO supply voltage level has been stabilized. A 10 kΩ pull-up and a 0.22 μF capacitor to GND on the RESET\_N is recommended.

Figure 2: Reset Timing



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## Integrated Radio Transceiver

The BCM20734 has an integrated radio transceiver that has been optimized for use in 2.4 GHz Bluetooth wireless systems. It has been designed to provide low-power, low-cost, robust communications for applications operating in the globally available 2.4 GHz unlicensed ISM band. The BCM20734 is fully compliant with the Bluetooth Radio Specification and enhanced data rate (EDR) specification and meets or exceeds the requirements to provide the highest communication link quality of service.

### Transmit

The BCM20734 features a fully integrated zero-IF transmitter. The baseband transmit data is GFSK-modulated in the modem block and upconverted to the 2.4 GHz ISM band in the transmitter path. The transmitter path consists of signal filtering, I/Q upconversion, output power amplifier, and RF filtering. The transmitter path also incorporates  $\pi/4$ -DQPSK for 2 Mbps and 8-DPSK for 3 Mbps to support EDR. The transmitter section is compatible to the Bluetooth Low Energy specification. The transmitter PA bias can also be adjusted to provide Bluetooth class 1 or class 2 operation.

### Digital Modulator

The digital modulator performs the data modulation and filtering required for the GFSK,  $\pi/4$ -DQPSK, and 8-DPSK signal. The fully digital modulator minimizes any frequency drift or anomalies in the modulation characteristics of the transmitted signal and is much more stable than direct VCO modulation schemes.

### Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit-synchronization algorithm.

### Power Amplifier

The fully integrated PA supports Class 1 or Class 2 output using a highly linearized, temperature-compensated design. This provides greater flexibility in front-end matching and filtering. Due to the linear nature of the PA combined with some integrated filtering, external filtering is required to meet the Bluetooth and regulatory harmonic and spurious requirements. For integrated mobile handset applications in which Bluetooth is integrated next to the cellular radio, external filtering can be applied to achieve near thermal noise levels for spurious and radiated noise emissions. The transmitter features a sophisticated on-chip transmit signal strength indicator (TSSI) block to keep the absolute output power variation within a tight range across process, voltage, and temperature.

## Receiver

The receiver path uses a low-IF scheme to downconvert the received signal for demodulation in the digital demodulator and bit synchronizer. The receiver path provides a high degree of linearity, an extended dynamic range, and high-order on-chip channel filtering to ensure reliable operation in the noisy 2.4 GHz ISM band. The front-end topology, with built-in out-of-band attenuation, enables the BCM20734 to be used in most applications with minimal off-chip filtering. For integrated handset operation, in which the Bluetooth function is integrated close to the cellular transmitter, external filtering is required to eliminate the desensitization of the receiver by the cellular transmit signal.

## Digital Demodulator and Bit Synchronizer

The digital demodulator and bit synchronizer take the low-IF received signal and perform an optimal frequency tracking and bit synchronization algorithm.

## Receiver Signal Strength Indicator

The radio portion of the BCM20734 provides a receiver signal strength indicator (RSSI) signal to the baseband, so that the controller can take part in a Bluetooth power-controlled link by providing a metric of its own receiver signal strength to determine whether the transmitter should increase or decrease its output power.

## Local Oscillator Generation

A local oscillator (LO) generation provides fast frequency hopping (1600 hops/second) across the 79 maximum available channels. The LO generation subblock employs an architecture for high immunity to LO pulling during PA operation. The BCM20734 uses an internal RF and IF loop filter.

## Calibration

The BCM20734 radio transceiver features an automated calibration scheme that is fully self-contained in the radio. No user interaction is required during normal operation or during manufacturing to provide optimal performance. Calibration tunes the performance of all the major blocks within the radio to within 2% of optimal conditions, including gain and phase characteristics of filters, matching between key components, and key gain blocks. This takes into account process variation and temperature variation. Calibration occurs transparently during normal operation during the settling time of the hops, and calibrates for temperature variations as the device cools and heats during normal operation in its environment.

## Internal LDO

The BCM20734 has a 1.2V internal LDO that supplies power to the baseband and the radio.

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# Peripheral Transport Unit

## Broadcom Serial Communications Interface

The BCM20734 provides a 2-pin master BSC interface, which can be used to retrieve configuration information from an external EEPROM or to communicate with peripherals such as track-ball or touch-pad modules, and motion tracking ICs used in mouse devices. The BSC interface is compatible with I<sup>2</sup>C slave devices. BSC does not support multimaster capability or flexible wait-state insertion by either master or slave devices.

The following transfer clock rates are supported by BSC:

- 100 kHz
- 400 kHz
- 800 kHz (Not a standard I<sup>2</sup>C-compatible speed.)
- 1 MHz (Compatibility with high-speed I<sup>2</sup>C-compatible devices is not guaranteed.)

The following transfer types are supported by BSC:

- Read (Up to 127 bytes can be read.)
- Write (Up to 127 bytes can be written.)
- Read-then-Write (Up to 127 bytes can be read and up to 127 bytes can be written.)
- Write-then-Read (Up to 127 bytes can be written and up to 127 bytes can be read.)

Hardware controls the transfers, requiring minimal firmware setup and supervision.

The clock pin (SCL) and data pin (SDA) are both open-drain I/O pins. Pull-up resistors external to the BCM20734 are required on both the SCL and SDA pins for proper operation.

## UART Interface

The UART physical interface is a standard, 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 6 Mbps. During initial boot, UART speeds may be limited to 750 kbps. The baud rate may be selected via a vendor-specific UART HCI command. The BCM20734 has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support enhanced data rates. The interface supports the Bluetooth UART HCI (H4) specification. The default baud rate for H4 is 115.2 kbaud.

The UART clock default setting is 24 MHz, and can be configured to run as high as 48 MHz to support up to 6 Mbps. The baud rate of the BCM20734 UART is controlled by two values. The first is a UART clock divisor (set in the DLBR register) that divides the UART clock by an integer multiple of 16. The second is a baud rate adjustment (set in the DHBR register) that is used to specify a number of UART clock cycles to stuff in the first or second half of each bit time. Up to eight UART cycles can be inserted into the first half of each bit time, and up to eight UART clock cycles can be inserted into the end of each bit time.

Table 1 contains example values to generate common baud rates with a 24 MHz UART clock.

**Table 1: Common Baud Rate Examples, 24 MHz Clock**

<b>Baud Rate (bps)</b>	<b>Baud Rate Adjustment</b>		<b>Mode</b>	<b>Error (%)</b>
	<b>High Nibble</b>	<b>Low Nibble</b>		
3M	0xFF	0xF8	High rate	0.00
2M	0xFF	0xF4	High rate	0.00
1M	0x44	0xFF	Normal	0.00
921600	0x05	0x05	Normal	0.16
460800	0x02	0x02	Normal	0.16
230400	0x04	0x04	Normal	0.16
115200	0x00	0x00	Normal	0.16
57600	0x00	0x00	Normal	0.16
38400	0x01	0x00	Normal	0.00
28800	0x00	0x00	Normal	0.16
19200	0x01	0x01	Normal	0.00
14400	0x00	0x00	Normal	0.16
9600	0x02	0x02	Normal	0.00

Table 2 contains example values to generate common baud rates with a 48 MHz UART clock.

**Table 2: Common Baud Rate Examples, 48 MHz Clock**

<b>Baud Rate (bps)</b>	<b>High Rate</b>	<b>Low Rate</b>	<b>Mode</b>	<b>Error (%)</b>
6M	0xFF	0xF8	High rate	0
4M	0xFF	0xF4	High rate	0
3M	0x0	0xFF	Normal	0
2M	0x44	0xFF	Normal	0
1.5M	0x0	0xFE	Normal	0
1M	0x0	0xFD	Normal	0
921600	0x22	0xFD	Normal	0.16
230400	0x0	0xF3	Normal	0.16
115200	0x1	0xE6	Normal	-0.08
57600	0x1	0xCC	Normal	0.04
38400	0x11	0xB2	Normal	0
19200	0x22	0x64	Normal	0

Normally, the UART baud rate is set by a configuration record downloaded after reset. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers.

The BCM20734 UART operates correctly with the host UART as long as the combined baud rate error of the two devices is within  $\pm 5\%$ .

## Peripheral UART Interface

The BCM20734 has a second UART that may be used to interface to other peripherals. This peripheral UART is accessed through the optional I/O ports, which can be configured individually and separately for each functional pin as shown in [Table 3](#).

**Table 3: BCM20734 Peripheral UART**

<i>Pin Name</i>	<i>pUART_TX</i>	<i>pUART_RX</i>	<i>pUART_CTS_N</i>	<i>pUART_RTS_N</i>
Configured pin name	P0	P2	P3	P1
	P5	P4	P7	P6
	P24	P25	P35	P30
	P31	P33	–	–
	P32	P34	–	–

## PCM Interface

The BCM20734 includes a PCM interface that shares pins with the I<sup>2</sup>S interface. The PCM Interface on the BCM20734 can connect to linear PCM codec devices in master or slave mode. In master mode, the BCM20734 generates the PCM\_CLK and PCM\_SYNC signals. In slave mode, these signals are provided by another master on the PCM interface and are inputs to the BCM20734.

The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

## Slot Mapping

The BCM20734 supports up to three simultaneous full-duplex SCO or eSCO channels through the PCM interface. These three channels are time-multiplexed onto the single PCM interface by using a time-slotting scheme where the 8 kHz or 16 kHz audio sample interval is divided into as many as 16 slots. The number of slots is dependent on the selected interface rate (128 kHz, 512 kHz, or 1024 kHz). The corresponding number of slots for these interface rate is 1, 2, 4, 8, and 16, respectively. Transmit and receive PCM data from an SCO channel is always mapped to the same slot. The PCM data output driver tristates its output on unused slots to allow other devices to share the same PCM interface signals. The data output driver tristates its output after the falling edge of the PCM clock during the last bit of the slot.

## Frame Synchronization

The BCM20734 supports both short- and long-frame synchronization in both master and slave modes. In short-frame synchronization mode, the frame synchronization signal is an active-high pulse at the audio frame rate that is a single-bit period in width and is synchronized to the rising edge of the bit clock. The PCM slave looks for a high on the falling edge of the bit clock and expects the first bit of the first slot to start at the next rising edge of the clock. In long-frame synchronization mode, the frame synchronization signal is again an active-high pulse at the audio frame rate; however, the duration is three bit periods and the pulse starts coincident with the first bit of the first slot.

## Data Formatting

The BCM20734 may be configured to generate and accept several different data formats. For conventional narrowband speech mode, the BCM20734 uses 13 of the 16 bits in each PCM frame. The location and order of these 13 bits can be configured to support various data formats on the PCM interface. The remaining three bits are ignored on the input and may be filled with 0s, 1s, a sign bit, or a programmed value on the output. The default format is 13-bit 2's complement data, left justified, and clocked MSB first.

## Burst PCM Mode

In this mode of operation, the PCM bus runs at a significantly higher rate of operation to allow the host to duty cycle its operation and save current. In this mode of operation, the PCM bus can operate at a rate of up to 24 MHz. This mode of operation is initiated with an HCI command from the host.

## Clock Frequencies

The BCM20734 uses a 24 MHz crystal oscillator (XTAL).

## Crystal Oscillator

The XTAL must have an accuracy of  $\pm 20$  ppm as defined by the Bluetooth specification. Two external load capacitors in the range of 5 pF to 30 pF are required to work with the crystal oscillator. The selection of the load capacitors is XTAL-dependent (see [Figure 3](#)).

**Figure 3: Recommended Oscillator Configuration—12 pF Load Crystal**

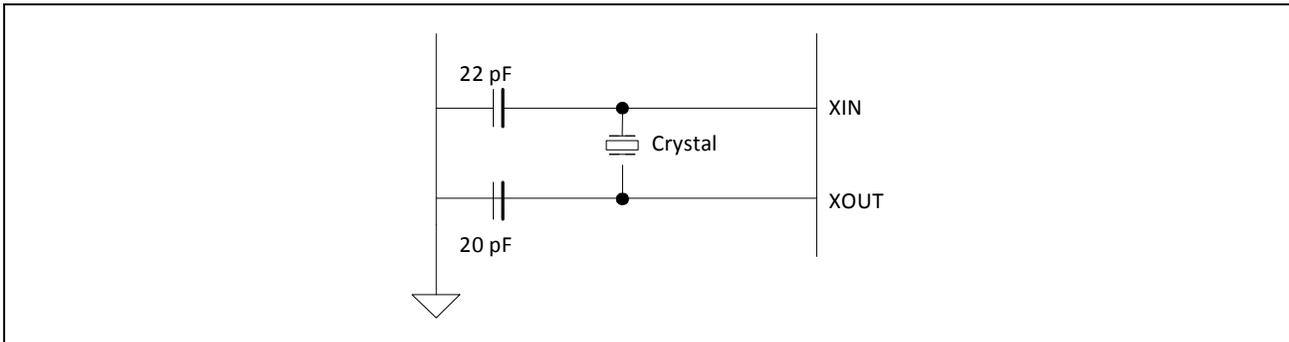


Table 4 shows the recommended crystal specifications.

**Table 4: Reference Crystal Electrical Specifications**

Parameter	Conditions	Minimum	Typical	Maximum	Unit
Nominal frequency	–	–	24.000	–	MHz
Oscillation mode	–	Fundamental		–	–
Frequency tolerance	@25°C	–	±10	–	ppm
Tolerance stability over temp	@0°C to +70°C	–	±10	–	ppm
Equivalent series resistance	–	–	–	50	Ω
Load capacitance	–	–	12	–	pF
Operating temperature range	–	0	–	+70	°C
Storage temperature range	–	–40	–	+125	°C
Drive level	–	–	–	200	μW
Aging	–	–	–	±10	ppm/year
Shunt capacitance	–	–	–	2	pF

## HID Peripheral Block

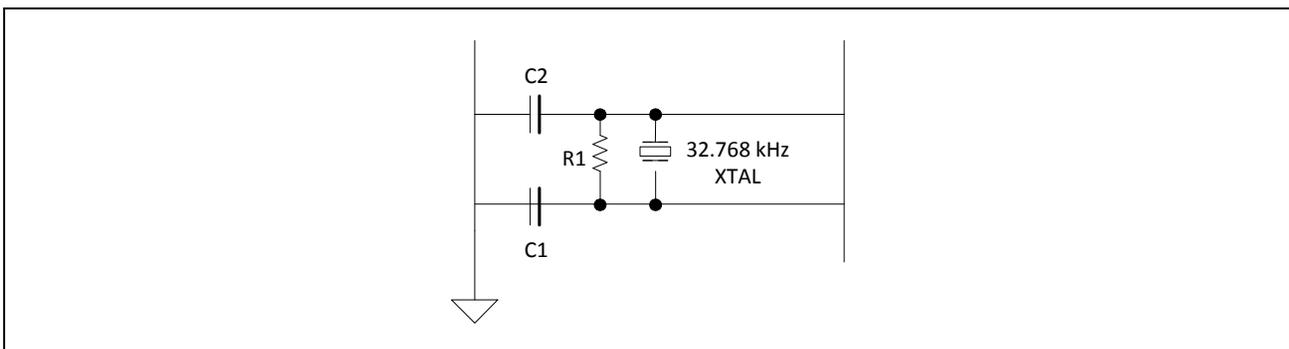
The peripheral blocks of the BCM20734 all run from a single 128 kHz low-power RC oscillator. The oscillator can be turned on at the request of any of the peripherals. If the peripheral is not enabled, it shall not assert its clock request line.

The keyboard scanner is a special case, in that it may drop its clock request line even when enabled, and then reassert the clock request line if a keypress is detected.

## 32 kHz Crystal Oscillator

Figure 4 shows the 32 kHz XTAL oscillator with external components and Table 5 lists the oscillator’s characteristics. It is a standard Pierce oscillator using a comparator with hysteresis on the output to create a single-ended digital output. The hysteresis was added to eliminate any chatter when the input is around the threshold of the comparator and is ~100 mV. This circuit can be operated with a 32 kHz or 32.768 kHz crystal oscillator or be driven with a clock input at similar frequency. The default component values are: R1 = 10 MΩ and C1 = C2 = ~10 pF. The values of C1 and C2 are used to fine-tune the oscillator.

**Figure 4: 32 kHz Oscillator Block Diagram**



**Table 5: XTAL Oscillator Characteristics**

<b>Parameter</b>	<b>Symbol</b>	<b>Conditions</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
Output frequency	$F_{\text{oscout}}$	–	–	32.768	–	kHz
Frequency tolerance	–	Crystal-dependent	–	100	–	ppm
Start-up time	$T_{\text{startup}}$	–	–	–	500	ms
XTAL drive level	$P_{\text{drv}}$	For crystal selection	0.5	–	–	$\mu\text{W}$
XTAL series resistance	$R_{\text{series}}$	For crystal selection	–	–	70	k $\Omega$
XTAL shunt capacitance	$C_{\text{shunt}}$	For crystal selection	–	–	1.3	pF

## GPIO Ports

The BCM20734 has 40 general-purpose I/Os (GPIOs) in a 90-pin package. All GPIOs support programmable pull-ups and are capable of driving up to 8 mA at 3.3V or 4 mA at 1.8V, except P26, P27, P28, and P29, which are capable of driving up to 16 mA at 3.3V or 8 mA at 1.8V.

### Port 0–Port 1, Port 8–Port 18, Port 20–Port 23, and Port 28–Port 38

All of these pins can be programmed as ADC inputs.

### Port 26–Port 29

P[26:29] consist of four pins. All pins are capable of sinking up to 16 mA for LEDs. These pins also have the PWM function, which can be used for LED dimming.

## Keyboard Scanner

The keyboard scanner is designed to autonomously sample keys and store them into buffer registers without the need for the host microcontroller to intervene. The scanner has the following features:

- Ability to turn off its clock if no keys are pressed.
- Sequential scanning of up to 160 keys in an 8 × 20 matrix.
- Programmable number of columns from 1 to 20.
- Programmable number of rows from 1 to 8.
- 16-byte key-code buffer (can be augmented by firmware).
- 128 kHz clock that allows scanning of full 160-key matrix in about 1.2 ms.
- N-key rollover with selective 2-key lockout if ghost is detected.
- Keys are buffered until host microcontroller has a chance to read it, or until overflow occurs.
- Hardware debouncing and noise/glitch filtering.
- Low-power consumption. Single-digit  $\mu\text{A}$ -level sleep current.

## Theory of Operation

The key scan block is controlled by a state machine with the following states:

### Idle

The state machine begins in the idle state. In this state, all column outputs are driven high. If any key is pressed, a transition occurs on one of the row inputs. This transition causes the 128 kHz clock to be enabled (if it is not already enabled by another peripheral) and the state machine to enter the scan state. Also in this state, an 8-bit row-hit register and an 8-bit key-index counter is reset to 0.

### Scan

In the scan state, a row counter counts from 0 up to a programmable number of rows minus 1. After the last row is reached, the row counter is reset and the column counter is incremented. This cycle repeats until the row and column counters are both at their respective terminal count values. At that point, the state machine moves into the Scan-End state.

As the keys are being scanned, the key-index counter is incremented. This counter value is compared to the modifier key codes stored in RAM, or in the key-code buffer if the key is not a modifier key. It can be used by the microprocessor as an index into a lookup table of usage codes.

Also, as the  $n$ th row is scanned, the row-hit register is ORed with the current 8-bit row input values if the current column contains two or more row hits. During the scan of any column, if a key is detected at the current row, and the row-hit register indicates that a hit was detected in that same row on a previous column, then a ghost condition may have occurred, and a bit in the status register is set to indicate this.

### Scan End

This state determines whether any keys were detected while in the scan state. If yes, the state machine returns to the scan state. If no, the state machine returns to the idle state, and the 128 kHz clock request signal is made inactive.



**Note:** The microcontroller can poll the key status register.

---

## Mouse Quadrature Signal Decoder

The mouse signal decoder is designed to autonomously sample two quadrature signals commonly generated by an optomechanical mouse. The decoder has the following features:

- Three pairs of inputs for X, Y, and Z (typical scroll wheel) axis signals. Each axis has two options:
  - For the X axis, choose P2 or P32 as X0 and P3 or P33 as X1.
  - For the Y axis, choose P4 or P34 as Y0 and P5 or P35 as Y1.
  - For the Z axis, choose P6 or P36 as Z0 and P7 or P37 as Z1.
- Control of up to four external high-current GPIOs to power external optoelectronics:

- Turn-on and turn-off time can be staggered for each HC-GPIO to avoid simultaneous switching of high currents and having multiple high-current devices on at the same time.
- Sample time can be staggered for each axis.
- Sense of the control signal can be active high or active low.
- Control signal can be tristated for off condition or driven high or low, as appropriate.

## Theory of Operation

The mouse decoder block has four 10-bit PWMs for controlling external quadrature devices and sampling the quadrature inputs at its core.

The GPIO signals may be used to control such items as LEDs, external ICs that may emulate quadrature signals, photodiodes, and photodetectors.

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## ADC Port

The ADC block is a single switched-cap  $\Sigma$ - $\Delta$  ADC core for audio and DC measurement. It operates at the 12 MHz clock rate and has 32 DC input channels, including 28 GPIO inputs. The internal bandgap reference has  $\pm 3\%$  accuracy without calibration. Different calibration and digital correction schemes can be applied to reduce ADC absolute error and improve measurement accuracy in DC mode.

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## Microphone Input

The BCM20734 integrates support for a differential or single-ended mono microphone. This reduces the requirement on external components because there is no need for a separate microphone amplifier. The microphone input has a user-programmable gain range of 0–42 dB with 3 dB steps. A microphone bias output from the chip is provided that can be used to bias an electret condenser-type microphone. The MIC Bias reference output voltage is 2.1V or 21/25 of the audio power supply. The MIC block can be powered down when it is not in use.

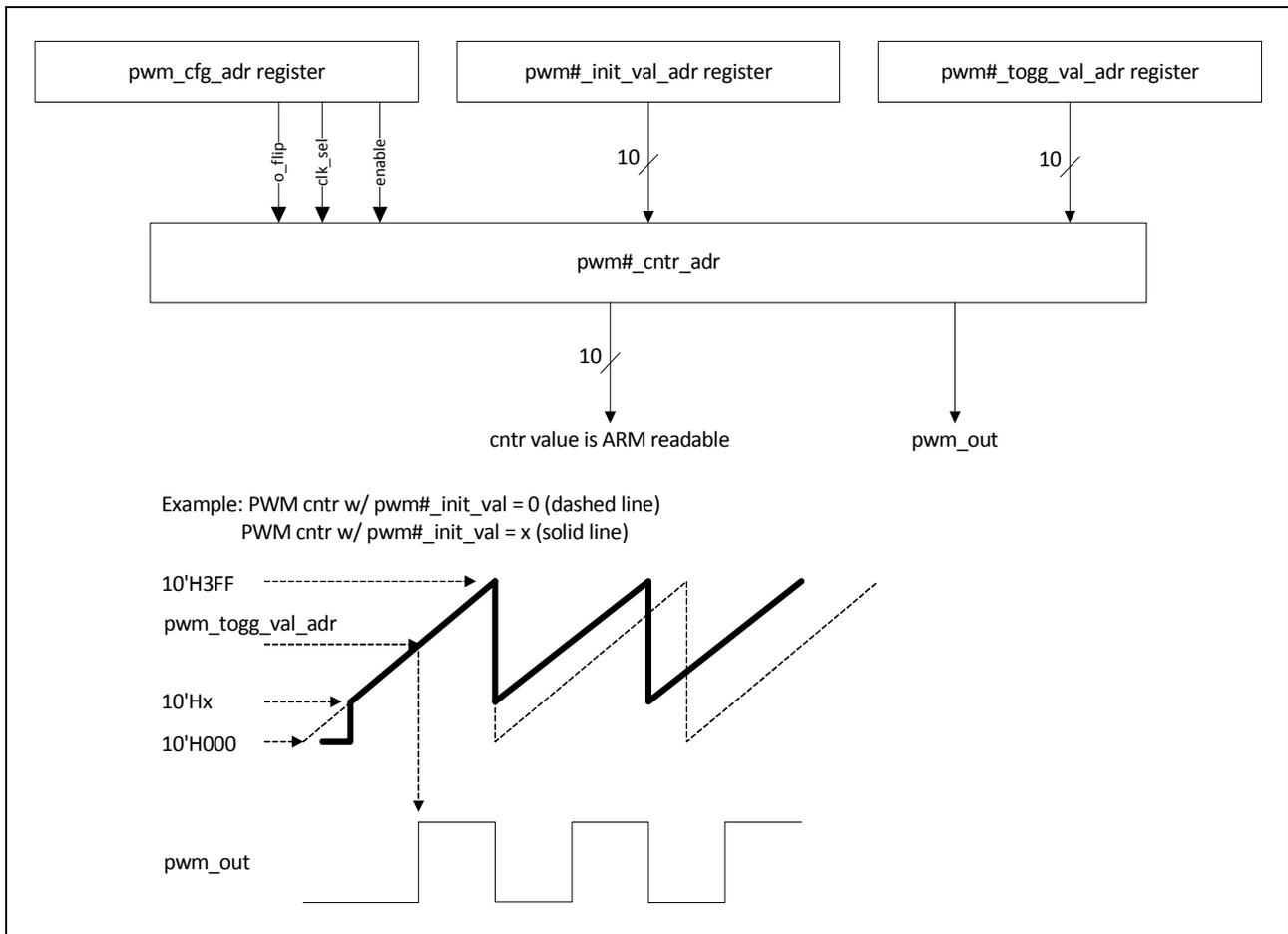
# PWM

The BCM20734 has four internal PWMs. The PWM module consists of the following:

- PWM1–4
- Each of the four PWM channels, PWM1–4, contains the following registers:
  - 10-bit initial value register (read/write)
  - 10-bit toggle register (read/write)
  - 10-bit PWM counter value register (read)
- PWM configuration register shared among PWM1–4 (read/write). This 12-bit register is used:
  - To configure each PWM channel
  - To select the clock of each PWM channel
  - To change the phase of each PWM channel

Figure 5 shows the structure of one PWM.

**Figure 5: PWM Block Diagram**



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## Shutter Control for 3D Glasses

The BCM20734, combined with the Broadcom Bluetooth host device, provides full system support for 3D glasses on televisions. The Broadcom Bluetooth host device gets frame synchronization signals from the TV, converts them into proprietary timing control messages, then passes the messages to the BCM20734. The BCM20734 uses these messages to synchronize the shutter control for the 3D glasses with the television frames.

The BCM20734 can provide up to four synchronized control signals for left and right eye shutter control. These four lines can output pulses with microsecond resolution for on and off timing. The total cycle time can be set for any period up to 65535 msec. The pulses are synchronized to each other for left and right eye shutters.

The BCM20734 seamlessly adjusts the timing of the control signals based on control messages from the Broadcom Bluetooth host device, ensuring that the 3D glasses remain synchronized to the TV display frame.

3D hardware control on the BCM20734 works independently of the rest of the system. The BCM20734 negotiates sniff with the Broadcom Bluetooth host device and, except for sniff resynchronization periods, most of the BCM20734 circuitry remains in a low power state while the 3D glasses subsystem continues to provide shutter timing and control pulses. This significantly reduces total system power consumption.

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## Triac Control

The BCM20734 includes hardware support for zero-crossing detection and trigger control for up to four triacs. The BCM20734 detects zero-crossing on the AC zero detection line and uses that to provide a pulse that is offset from the zero crossing. This allows the BCM20734 to be used in dimmer applications, as well as any other applications that require a control signal that is offset from an input event.

The zero-crossing hardware includes an option to suppress glitches.

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## Serial Peripheral Interface

The BCM20734 has two independent SPI interfaces. One is a master-only interface (SPI\_2) and the other (SPI\_1) can be either a master or a slave. Each interface has a 64-byte transmit buffer and a 64-byte receive buffer. To support more flexibility for user applications, the BCM20734 has optional I/O ports that can be configured individually and separately for each functional pin. The BCM20734 acts as an SPI master device that supports 1.8V or 3.3V SPI slaves. The BCM20734 can also act as an SPI slave device that supports a 1.8V or 3.3V SPI master.



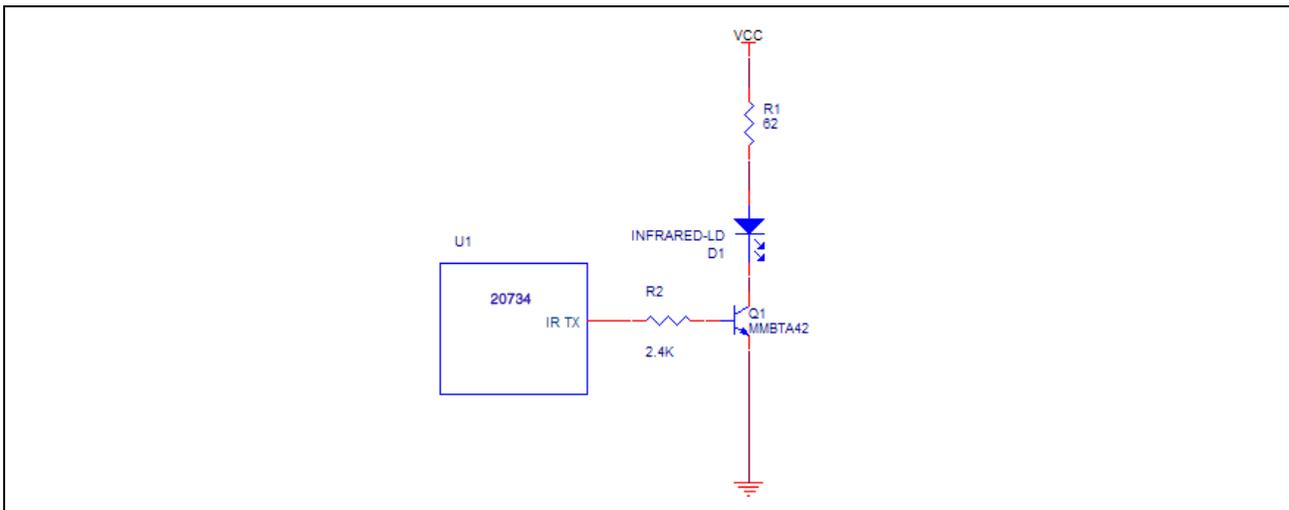
**Note:** SPI voltage depends on VDDO/VDDM; therefore, it defines the type of devices that can be supported.

## Infrared Modulator

The BCM20734 includes hardware support for infrared TX. The hardware can transmit both modulated and unmodulated waveforms. For modulated waveforms, hardware inserts the desired carrier frequency into all IR transmissions. IR TX can be sourced from firmware-supplied descriptors, a programmable bit, or the peripheral UART transmitter.

If descriptors are used, they include IR on/off state and the duration between 1–32767  $\mu\text{sec}$ . The BCM20734 IR TX firmware driver inserts this information in a hardware FIFO and makes sure that all descriptors are played out without a glitch due to underrun (see [Figure 6](#)).

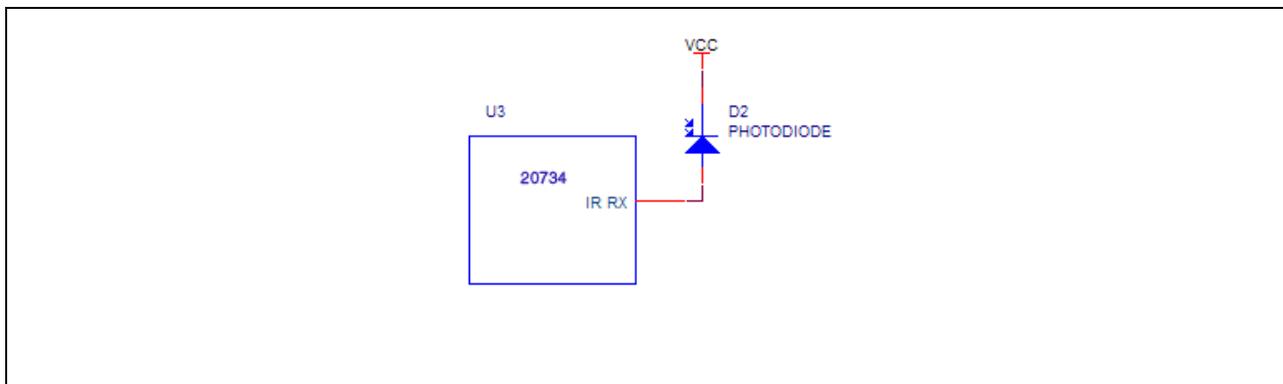
**Figure 6: Infrared TX**



## Infrared Learning

The BCM20734 includes hardware support for infrared learning. The hardware can detect both modulated and unmodulated signals. For modulated signals, the BCM20734 can detect carrier frequencies between 10 kHz and 500 kHz, and the duration that the signal is present or absent. The BCM20734 firmware driver supports further analysis and compression of the learned signal. The learned signal can then be played back through the BCM20734 IR TX subsystem (see [Figure 7](#)).

**Figure 7: Infrared RX**



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## Power Management Unit

The Power Management Unit (PMU) provides power management features that can be invoked by software through power management registers or packet-handling in the baseband core.

### RF Power Management

The BBC generates power-down control signals for the transmit path, receive path, PLL, and power amplifier to the 2.4 GHz transceiver, which then processes the power-down functions accordingly.

### Host Controller Power Management

Power is automatically managed by the firmware based on input device activity. As a power-saving task, the firmware controls the disabling of the on-chip regulator when in HIDEOFF (deep sleep) mode.

### BBC Power Management

There are several low-power operations for the BBC:

- Physical layer packet handling turns RF on and off dynamically within packet TX and RX.
- Bluetooth-specified low-power connection mode. While in these low-power connection modes, the BCM20734 runs on the Low Power Oscillator and wakes up after a predefined time period.

The BCM20734 automatically adjusts its power dissipation based on user activity. The following power modes are supported:

- Active mode
- Idle mode
- Sleep mode
- HIDEOFF (deep sleep) mode

The BCM20734 transitions to the next lower state after a programmable period of user inactivity. When user activity resumes, the BCM20734 immediately enters Active mode.

In HIDEOFF mode, the BCM20734 baseband and core are powered off by disabling power to VDDC\_OUT and PAVDD. The VDDO domain remains powered up and will turn the remainder of the chip on when it detects user events. This mode minimizes chip power consumption and is intended for long periods of inactivity.

## Section 2: Pin Assignments

### Pin Descriptions

Table 6: Pin Descriptions

Pin Number	Pin Name	I/O	Power Domain	Description
<b>Radio I/O</b>				
A1	RFOP	I/O	PAVDD	RF antenna port
<b>RF Power Supplies</b>				
D1	IFVDD1P2	I	IFVDD1P2	IFPLL power supply
B1	LNAVDD1P2	I	LNAVDD1P2	RF front-end supply
C1	VCOVDD1P2	I	VCOVDD1P2	VCO supply
B2	PLLVDD1P2	I	PLLVDD1P2	RFPLL and crystal oscillator supply
A3	PAVDD	O	PAVDD	PA supply
<b>Power Supplies</b>				
F1, G3	VDDC	I	VDDC	Baseband core supply
A9, K1	VDDO	I	VDDO	I/O pad and core supply
B6	MIC_AVDD	I	MIC_AVDD	Microphone supply
A5	ADC_AVBAT	I	ADC_AVBAT	ADC supply
A8	ADC_AVDDC	I	ADC_AVDDC	ADC supply
<b>Ground</b>				
A2, A10, B5, C2, C3, D3, F2, J1, K10	VSS	I	VSS	Ground
B8	AVSS	I	AVSS	Analog ground
<b>Clock Generator and Crystal Interface</b>				
B4	XTALI	I	PLLVDD1P2	Crystal oscillator input. See <a href="#">“Crystal Oscillator” on page 19</a> for options.
A4	XTALO	O	PLLVDD1P2	Crystal oscillator output.
E6	XTALI32K	I	PLLVDD1P2	Low-power oscillator input.
F6	XTALO32K	O	PLLVDD1P2	Low-power oscillator output.
<b>Core</b>				
H3	RESET_N	I/O PU	VDDO	Active-low system reset with open-drain output and internal pull-up resistor.
F5	TM1	I	VDDO	Device test mode control. Connect to GND for all applications.
E5	JTAG_SEL	I	VDDO	ARM JTAG debug mode control. Connect to GND for all applications.

**Table 6: Pin Descriptions (Cont.)**

<b>Pin Number</b>	<b>Pin Name</b>	<b>I/O</b>	<b>Power Domain</b>	<b>Description</b>
<b>Microphone</b>				
A7	MICP	I	MIC_AVDD	Microphone positive input
B7	MICN	I	MIC_AVDD	Microphone negative input
A6	MIC_BIAS	O	MIC_AVDD	Microphone bias supply
<b>PCM2/I<sup>2</sup>S</b>				
J3	PCM_SYNC	I/O, PD	VDDO	Frame synchronization for PCM interface. Alternate function: <ul style="list-style-type: none"> <li>I<sup>2</sup>S word select</li> </ul>
K2	PCM_CLK	I/O, PD	VDDO	Clock for PCM interface. Alternate function: <ul style="list-style-type: none"> <li>I<sup>2</sup>S clock</li> </ul>
K3	PCM_IN	I, PU	VDDO	Data input for PCM interface. Alternate function: <ul style="list-style-type: none"> <li>I<sup>2</sup>S data input</li> <li>SDA</li> </ul>
J2	PCM_OUT	O, PD	VDDO	Data output for PCM interface. Alternate function: <ul style="list-style-type: none"> <li>I<sup>2</sup>S data output</li> <li>SCL</li> </ul>
<b>UART</b>				
H5	UART_RXD	I	VDDO	UART serial input – Serial data input for the HCI UART interface.
H4	UART_TXD	O, PU	VDDO	UART serial output – Serial data output for the HCI UART interface.
J4	UART_RTS_N	O, PU	VDDO	Request to send (RTS) for HCI UART interface. Leave unconnected if not used.
J5	UART_CTS_N	I, PU	VDDO	Clear to send (CTS) for HCI UART interface. Leave unconnected if not used.
<b>BSC/SPI</b>				
H1	SPI_MISO_SCL	I/O	VDDO	BSC clock
G1	SPI_MOSI_SDA	I/O	VDDO	BSC data
G2	SPI_CLK	I/O	VDDO	Serial flash SPI clock
H2	SPI_CSN	I/O	VDDO	Serial flash active-low chip select
<b>LDO Regulator Power Supplies</b>				
B3	VBAT	I	VBAT	1.2V LDO input
E1	VDDC_OUT	O	VDDC_OUT	1.2V LDO output
<b>Reserved</b>				
F4	Reserved0	I	VDDO	Reserved. Leave unconnected.
D5	Reserved1	I	VDDO	Reserved. Leave unconnected.

**Table 6: Pin Descriptions (Cont.)**

<b>Pin Number</b>	<b>Pin Name</b>	<b>I/O</b>	<b>Power Domain</b>	<b>Description</b>
E3	Reserved2	I	VDDO	Reserved. Connect to GND.
E4	Reserved3	I	VDDO	Reserved. Leave unconnected.
D4	Reserved4	I	VDDO	Reserved. Connect to GND.

**Table 7: GPIO Pin Descriptions<sup>a</sup>**

<b>Pin Number</b>	<b>Pin Name</b>	<b>Default Direction</b>	<b>POR State</b>	<b>Power Domain</b>	<b>Alternate Function Description</b>
G7	P0	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P0</li> <li>Keyboard scan input (row): KSI0</li> <li>A/D converter input 29</li> <li>Peripheral UART: puart_tx</li> <li>SPI_1: MOSI (master and slave)</li> <li>IR_RX</li> <li>60Hz_main</li> </ul> <b>Note:</b> Not available during TM1 = 1.
G6	P1	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P1</li> <li>Keyboard scan input (row): KSI1</li> <li>A/D converter input 28</li> <li>Peripheral UART: puart_rts</li> <li>SPI_1: MISO (master and slave)</li> <li>IR_TX</li> </ul>
C9	P2	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P2</li> <li>Keyboard scan input (row): KSI2</li> <li>Quadrature: QDX0</li> <li>Peripheral UART: puart_rx</li> <li>SPI_1: SPI_CS (slave only)</li> <li>SPI_1: MOSI (master only)</li> </ul>
E9	P3	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P3</li> <li>Keyboard scan input (row): KSI3</li> <li>Quadrature: QDX1</li> <li>Peripheral UART: puart_cts</li> <li>SPI_1: SPI_CLK (master and slave)</li> </ul>
G10	P4	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P4</li> <li>Keyboard scan input (row): KSI4</li> <li>Quadrature: QDY0</li> <li>Peripheral UART: puart_rx</li> <li>SPI_1: MOSI (master and slave)</li> <li>IR_TX</li> </ul>

**Table 7: GPIO Pin Descriptions<sup>a</sup> (Cont.)**

<b>Pin Number</b>	<b>Pin Name</b>	<b>Default Direction</b>	<b>POR State</b>	<b>Power Domain</b>	<b>Alternate Function Description</b>
K4	P5	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P5</li> <li>Keyboard scan input (row): KSI5</li> <li>Quadrature: QDY1</li> <li>Peripheral UART: puart_tx</li> <li>SPI_1: MISO (master and slave)</li> <li>BSC: SDA</li> </ul>
G4	P6	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P6</li> <li>Keyboard scan input (row): KSI6</li> <li>Quadrature: QDZ0</li> <li>Peripheral UART: puart_rts</li> <li>SPI_1: SPI_CS (slave only)</li> <li>60Hz_main</li> </ul>
B10	P7	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P7</li> <li>Keyboard scan input (row): KSI7</li> <li>Quadrature: QDZ1</li> <li>Peripheral UART: puart_cts</li> <li>SPI_1: SPI_CLK (master and slave)</li> <li>BSC: SCL</li> </ul>
D7	P8	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P8</li> <li>Keyboard scan output (column): KSO0</li> <li>A/D converter input 27</li> <li>External T/R switch control: ~tx_pd</li> </ul>
D9	P9	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P9</li> <li>Keyboard scan output (column): KSO1</li> <li>A/D converter input 26</li> <li>External T/R switch control: tx_pd</li> </ul>
G8	P10	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P10</li> <li>Keyboard scan output (column): KSO2</li> <li>A/D converter input 25</li> <li>External PA ramp control: ~PA_Ramp</li> </ul>
G9	P11	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P11</li> <li>Keyboard scan output (column): KSO3</li> <li>A/D converter input 24</li> </ul>

**Table 7: GPIO Pin Descriptions<sup>a</sup> (Cont.)**

<b>Pin Number</b>	<b>Pin Name</b>	<b>Default Direction</b>	<b>POR State</b>	<b>Power Domain</b>	<b>Alternate Function Description</b>
C10	P12	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P12</li> <li>Keyboard scan output (column): KSO4</li> <li>A/D converter input 23</li> </ul>
E8	P13	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P13</li> <li>Keyboard scan output (column): KSO5</li> <li>A/D converter input 22</li> <li>PWM3</li> <li>Triac control 3</li> </ul>
J7	P14	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P14</li> <li>Keyboard scan output (column): KSO6</li> <li>A/D converter input 21</li> <li>PWM2</li> <li>Triac control 4</li> </ul>
J8	P15	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P15</li> <li>Keyboard scan output (column): KSO7</li> <li>A/D converter input 20</li> <li>IR_RX</li> <li>60Hz_main</li> </ul>
B9	P16	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P16</li> <li>Keyboard scan output (column): KSO8</li> <li>A/D converter input 19</li> </ul>
J10	P17	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P17</li> <li>Keyboard scan output (column): KSO9</li> <li>A/D converter input 18</li> </ul>
F9	P18	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P18</li> <li>Keyboard scan output (column): KSO10</li> <li>A/D converter input 17</li> </ul>
H7	P19	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P19</li> <li>Keyboard scan output (column): KSO11</li> <li>A/D converter input 16</li> </ul>
F10	P20	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P20</li> <li>Keyboard scan output (column): KSO12</li> </ul>

**Table 7: GPIO Pin Descriptions<sup>a</sup> (Cont.)**

<b>Pin Number</b>	<b>Pin Name</b>	<b>Default Direction</b>	<b>POR State</b>	<b>Power Domain</b>	<b>Alternate Function Description</b>
D10	P21	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P21</li> <li>Keyboard scan output (column): KSO13</li> <li>A/D converter input 14</li> <li>Triac control 3</li> </ul>
E6	P22	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P22</li> <li>Keyboard scan output (column): KSO14</li> <li>A/D converter input 13</li> <li>Triac control 4</li> <li>XTALO32K</li> </ul>
F6	P23	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P23</li> <li>Keyboard scan output (column): KSO15</li> <li>A/D converter input 12</li> <li>XTALI32K</li> </ul>
G5	P24	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P24</li> <li>Keyboard scan output (column): KSO16</li> <li>SPI_1: SPI_CLK (master and slave)</li> <li>Peripheral UART: puart_tx</li> </ul>
F7	P25	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P25</li> <li>Keyboard scan output (column): KSO17</li> <li>SPI_1: MISO (master and slave)</li> <li>Peripheral UART: puart_rx</li> </ul>
K8	P26 PWM0	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P26</li> <li>Keyboard scan output (column): KSO18</li> <li>SPI_1: SPI_CS (slave only)</li> <li>Optical control output: QOC0</li> <li>Triac control 1</li> </ul> <p>Current: 16 mA sink</p>
K9	P27 PWM1	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P27</li> <li>Keyboard scan output (column): KSO19</li> <li>SPI_1: MOSI (master and slave)</li> <li>Optical control output: QOC1</li> <li>Triac control 2</li> </ul> <p>Current: 16 mA sink</p>

**Table 7: GPIO Pin Descriptions<sup>a</sup> (Cont.)**

<b>Pin Number</b>	<b>Pin Name</b>	<b>Default Direction</b>	<b>POR State</b>	<b>Power Domain</b>	<b>Alternate Function Description</b>
K7	P28 PWM2	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P28</li> <li>Optical control output: QOC2</li> <li>A/D converter input 11</li> <li>LED1</li> </ul> Current: 16 mA sink
K6	P29 PWM3	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P29</li> <li>Optical control output: QOC3</li> <li>A/D converter input 10</li> <li>LED2</li> </ul> Current: 16 mA sink
J9	P30	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P30</li> <li>A/D converter input 9</li> <li>Peripheral UART: puart_rts</li> </ul>
H6	P31	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P31</li> <li>A/D converter input 8</li> <li>Peripheral UART: puart_tx</li> </ul>
H9	P32	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P32</li> <li>A/D converter input 7</li> <li>Quadrature: QDX0</li> <li>SPI_1: SPI_CS (slave only)</li> <li>Auxiliary clock output: ACLK0</li> <li>Peripheral UART: puart_tx</li> </ul>
H10	P33	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P33</li> <li>A/D converter input 6</li> <li>Quadrature: QDX1</li> <li>SPI_1: MOSI (slave only)</li> <li>Auxiliary clock output: ACLK1</li> <li>Peripheral UART: puart_rx</li> </ul>
H8	P34	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P34</li> <li>A/D converter input 5</li> <li>Quadrature: QDY0</li> <li>Peripheral UART: puart_rx</li> <li>External T/R switch control: tx_pd</li> </ul>
F8	P35	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>GPIO: P35</li> <li>A/D converter input 4</li> <li>Quadrature: QDY1</li> <li>Peripheral UART: puart_cts</li> <li>BSC: SDA</li> </ul>

**Table 7: GPIO Pin Descriptions<sup>a</sup> (Cont.)**

<b>Pin Number</b>	<b>Pin Name</b>	<b>Default Direction</b>	<b>POR State</b>	<b>Power Domain</b>	<b>Alternate Function Description</b>
D8	P36	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>• GPIO: P36</li> <li>• A/D converter input 3</li> <li>• Quadrature: QDZ0</li> <li>• SPI_1: SPI_CLK (master and slave)</li> <li>• Auxiliary Clock Output: ACLK0</li> <li>• External T/R switch control: ~tx_pd</li> </ul>
E7	P37	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>• GPIO: P37</li> <li>• A/D converter input 2</li> <li>• Quadrature: QDZ1</li> <li>• SPI_1: MISO (slave only)</li> <li>• Auxiliary clock output: ACLK1</li> <li>• BSC: SCL</li> </ul>
D6	P38	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>• GPIO: P38</li> <li>• A/D converter input 1</li> <li>• SPI_1: MOSI (master and slave)</li> <li>• IR_TX</li> </ul>
J6	P39	Input	Floating	VDDO	<ul style="list-style-type: none"> <li>• GPIO: P39</li> <li>• SPI_1: SPI_CS (slave only)</li> <li>• Infrared control: IR_RX</li> <li>• External PA ramp control: PA_Ramp</li> <li>• 60Hz_main</li> </ul>

a. During power-on reset, all inputs are disabled.

# Ball Map

The BCM20734 ball map is shown in [Figure 8](#).

**Figure 8: BCM20734 Ball Map**

	1	2	3	4	5	6	7	8	9	10	
A	RFOP	VSS	PAVDD	XTALO	ADC_AVBAT	MICBIAS	MICP	ADC_AVDDC	VDDO	VSS	A
B	LNAVDD1P2	PLLVD1P2	VBAT	XTALI	VSS	MIC_AVDD	MICN	AVSS	P16	P7	B
C	VCOVDD1P2	VSS	VSS						P2	P12	C
D	IFVDD1P2		VSS	RESERVED4	RESERVED1	P38	P8	P36	P9	P21	D
E	VDDC_OUT		RESERVED2	RESERVED3	JTAG_SEL	P22/ XTALI32K	P37	P13	P3		E
F	VDDC	VSS		RESERVED0	TM1	P23/ XTALO32K	P25	P35	P18	P20	F
G	SPI_MOSI_SDA	SPI_CLK	VDDC	P6	P24	P1	P0	P10	P11	P4	G
H	SPI_MISO_SCL	SPI_CSN	RESET_N	UART_TXD	UART_RXD	P31	P19	P34	P32	P33	H
J	VSS	PCM_OUT	PCM_SYNC	UART_RTS_N	UART_CTS_N	P39	P14	P15	P30	P17	J
K	VDDO	PCM_CLK	PCM_IN	P5		P29	P28	P26	P27	VSS	K
	1	2	3	4	5	6	7	8	9	10	

## Section 3: Specifications

### Electrical Characteristics

Table 8 shows the maximum electrical rating for voltages referenced to VDD pin.

**Table 8: Absolute Maximum Voltages**

<b>Requirement Parameter</b>	<b>Specification</b>			<b>Unit</b>
	<b>Minimum</b>	<b>Nominal</b>	<b>Maximum</b>	
Ambient Temperature of Operation	-30	25	85	°C
Storage temperature	-40	–	150	°C
ESD Tolerance HBM	-2000	–	2000	V
ESD Tolerance MM	-100	–	100	V
ESD Tolerance CDM	-500	–	500	V
Latch-up	–	200	–	mA
VDD Core	1.14	1.2	1.26	V
VDD IO	1.62	3.3	3.6	V
VDD RF (excluding class 1 PA)	1.14	1.2	1.26	V

Table 9 shows the power supply characteristics for the range  $T_J = 0^\circ\text{C}$  to  $125^\circ\text{C}$ .

**Table 9: Power Supply Specifications**

<b>Parameter</b>	<b>Conditions</b>	<b>Min.</b>	<b>Typical</b>	<b>Max.</b>	<b>Unit</b>
VBAT input	–	1.62	3.3	3.6	V
Operating temperature	Junction temperature	-40	50	125	°C
Total system leakage	Max value is defined at temp = 85°C	–	0.5	1.3	μA
PMU turn-on time	VBAT is ready.	TBD	–	300	μs

Table 10 shows the digital level characteristics for (VSS = 0V).

**Table 10: VDDC LDO Electrical Specifications**

Parameter	Conditions	Min.	Typical	Max.	Unit	
Input Voltage	–	1.62	3.3	3.6	V	
Nominal Output Voltage	–	–	1.2	–	V	
DC Accuracy	Accuracy at any step, including bandgap reference.	–5	–	5	%	
Output Voltage Programmability	Range	0.89	–	1.34	V	
	Step Size	–	30	–	mV	
Load Current	–	–	–	40	mA	
Dropout Voltage	$I_{load} = 40$ mA	–	–	200	mV	
Line Regulation	$V_{in}$ from 1.62V to 3.6V, $I_{load} = 40$ mA	–	–	0.2	%Vo/V	
Load Regulation	$I_{load} = 1$ mA to 40 mA, $V_{out} = 1.2$ V, Package + PCB R = 0.3 $\Omega$	–	0.02	0.05	%Vo/mA	
Quiescent Current	No load @ $V_{in} = 3.3$ V	–	18	23	$\mu$ A	
	Max load @ $V_{in} = 3.3$ V	–	–	0.56 0.65	mA	
Power down Current	$V_{in} = 3.3$ V @25C	–	0.2	–	$\mu$ A	
	$V_{in} = 3.6$ @80C	–	TBD	–	–	
Output Noise	$I_{load} = 15$ mA, 100 kHz	–	–	40	nV/sqrtHz	
	$I_{load} = 15$ mA, 2 MHz	–	–	14	nV/sqrtHz	
PSRR	$V_{in} = 3.3$ , $V_{out} = 1.2$ V, $I_{load} = 40$ mA	1 kHz	65	–	–	dB
		10 kHz	60	–	–	dB
		100 kHz	55	–	–	dB
Over Current Limit	–	100	–	–	mA	
Turn-on Time	VBAT = 3.3V, BG already on, LDO OFF to ON, $C_o = 1$ $\mu$ F, 90% of $V_{out}$	–	–	100	$\mu$ s	
In-rush current during turn-on	During start-up, $C_o = 1$ $\mu$ F	–	–	60	mA	
Transient Performance	$I_{load} = 1$ mA to 15 mA and 15 mA to 1 mA in 1 $\mu$ s	–	–	40	mV	
	$I_{load} = 15$ mA to 40 mA and 40 mA to 15 mA in 1 $\mu$ s	–	–	25	–	
External Output Capacitor	Ceramic cap with ESR $\leq 0.5\Omega$	0.8	1	4.7	$\mu$ F	
External Input Capacitor	Ceramic, X5R, 0402, $\pm 20\%$ , 10V.	–	1	–	$\mu$ F	

Table 11: ADC Microphone Specifications

Parameter	Symbol	Conditions/Comments	Min.	Typical	Max.	Unit
Analog supply voltage	AVBAT	Battery and I/O supply	1.62	3.3	3.6	V
Analog core supply	AVDDC	±10%	1.08	1.2	1.32	V
Audio supply	Mic_avdd	Only available for audio applications when audio supply is separated from battery supply	1.8	2.5	3.3	V
Current consumption	I <sub>TOT</sub>	–	–	1.2	–	mA
Power down current	–	–	–	0.5	–	µA
ADC reference voltage	VREF	From BG with ±3% accuracy	–	.85	–	V
Input clock frequency	–	From XTALOSC	–	24	26	MHz
ADC sampling clock	–	–	–	12	–	MHz
Absolute error	–	Includes gain error, offset, and distortion. <b>Note:</b> Before factory calibration	–	–	5	%
	–	Includes gain error, offset, and distortion. <b>Note:</b> After factory calibration	–	–	2	%
Effective number of bits (ENOB)	–	For static measurements	10	–	–	Bit
	–	For audio applications	12	–	–	
ADC input full scale	FS	For audio applications	–	1.7	–	V <sub>pp</sub>
		For static measurements	1.8	–	3.6	
Conversion rate	–	For audio applications	16	48	–	kHz
		For static measurements	50	100	–	
Signal bandwidth	–	For audio applications	20	–	8K	Hz
		For static measurements	–	DC	–	
Input impedance	R <sub>in</sub>	For audio applications	10	–	–	kΩ
		For static measurements	500	–	–	
Startup time	–	For audio applications	–	10	–	ms
		For static measurements	–	20	–	µs
MIC PGA gain range	–	–	0	–	18	dB
MIC PGA gain step	–	–	–	3	–	dB
MIC PGA gain error	–	Include part-to-part gain variation	–3	±1	3	dB
PGA input reference noise	–	• @ 18 dB PGA gain • A-weighted	–	–	15	µV
Passband gain flatness	–	• PGA + ADC • 100 Hz–4 kHz	–0.5	–	0.5	dB
MIC bias output voltage	–	@2.5Vsupply	–	2.1	–	V

**Table 11: ADC Microphone Specifications (Cont.)**

<b>Parameter</b>	<b>Symbol</b>	<b>Conditions/Comments</b>	<b>Min.</b>	<b>Typical</b>	<b>Max.</b>	<b>Unit</b>
MIC bias loading current	–	–	–	–	3	mA
MIC bias noise	–	<ul style="list-style-type: none"> <li>• PGA input referred. 6 dB attenuation is assumed from MIC bias output to PGA input.</li> <li>• 20 Hz to 8 kHz</li> <li>• A-weighted</li> </ul>	–	–	3	μV
ADC SNR	–	<ul style="list-style-type: none"> <li>• A-weighted</li> <li>• 0 dB PGA gain</li> </ul>	78	–	–	dB
ADC THD + N	–	<ul style="list-style-type: none"> <li>• –3 dBFS input</li> <li>• 0 dB PGA gain</li> </ul>	74	–	–	dB
GPIO input voltage	–	Must be lower than VBAT	–	–	3.6	V
GPIO source impedance <sup>a</sup>	–	Resistance	–	–	1	kΩ
	–	Capacitance	–	–	10	pF

a. Conditional requirement for the measurement time of 10 μs. Relaxed with longer measurement time for each GPIO input channel.

**Table 12: Digital I/O Characteristics**

<b>Characteristics</b>	<b>Symbol</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
Input low voltage (VDDO = 3.3V)	V <sub>IL</sub>	–	–	0.8	V
Input high voltage (VDDO = 3.3V)	V <sub>IH</sub>	2.0	–	–	V
Input low voltage (VDDO = 1.8V)	V <sub>IL</sub>	–	–	0.6	V
Input high voltage (VDDO = 1.8V)	V <sub>IH</sub>	1.1	–	–	V
Output low voltage	V <sub>OL</sub>	–	–	0.4	V
Output high voltage	V <sub>OH</sub>	VDDO – 0.4V	–	–	V
Input low current	I <sub>IL</sub>	–	–	1.0	μA
Input high current	I <sub>IH</sub>	–	–	1.0	μA
Output low current (VDDO = 3.3V, V <sub>OL</sub> = 0.4V)	I <sub>OL</sub>	–	–	2.0	mA
Output high current (VDDO = 3.3V, V <sub>OH</sub> = 2.9V)	I <sub>OH</sub>	–	–	4.0	mA
Output high current (VDDO = 1.8V, V <sub>OH</sub> = 1.4V)	I <sub>OH</sub>	–	–	TBD	mA
Input capacitance	C <sub>IN</sub>	–	–	0.4	pF



**Note:** In [Table 13](#), current consumption measurements are taken at VBAT with the assumption that VBAT is connected to VDDIO and LDOIN.

**Table 13: BLE Current Consumption**

<b>Operational Mode</b>	<b>Conditions</b>	<b>Typical</b>	<b>Max.</b>	<b>Unit</b>
Receive	Receiver and baseband are both operating, 100% ON.	–	TBD	mA
Transmit	Transmitter and baseband are both operating, 100% ON.	–	TBD	mA
Sleep	Internal LPO is in use.	TBD	–	μA
HIDOFF (Deep Sleep)	–	TBD	–	μA



**Note:** In [Table 14](#) and [Table 15 on page 43](#), current consumption measurements are taken at input of LDOIN, VDDIO, and VDDPA combined (LDOIN = VDDIO = VDDPA = 3.0V).

**Table 14: Current Consumption For BR and EDR, Class 1**

<b>Operational Mode</b>	<b>Conditions</b>	<b>Typical</b>	<b>Unit</b>
Receive (1 Mbps)	Peak current level during reception of a basic-rate packet.	26.373	mA
Transmit (1 Mbps)	Peak current level during the transmission of a basic-rate packet: GFSK output power = 10 dBm.	60.289	mA
Receive (EDR)	Peak current level during the reception of a 2 or 3 Mbps rate packet.	26.373	mA
Transmit (EDR)	Peak current level during the transmission of a 2 or 3 Mbps rate packet: EDR output power = 8 dBm.	52.485	mA
<b>Average Current</b>			
Page scan	Periodic scan rate is 1.28 sec.	0.486	mA
Sniff slave (495 ms)	Based on one attempt and no timeout.	254	μA
Sniff slave (22.5 ms)	–	2.6	mA
Sniff slave (11.25 ms)	–	4.95	mA
HIDOFF (Deep Sleep)	–	2.69	μA

**Table 15: Current Consumption For BR and EDR, Class 2 (0 dBm)**

<b>Operational Mode</b>	<b>Conditions</b>	<b>Typical</b>	<b>Unit</b>
Receive (1 Mbps)	Peak current level during reception of a basic-rate packet.	TBD	mA
Transmit (1 Mbps)	Peak current level during the transmission of a basic-rate packet: GFSK output power = 10 dBm.	TBD	mA
Receive (EDR)	Peak current level during the reception of a 2 or 3 Mbps rate packet.	TBD	mA
Transmit (EDR)	Peak current level during the transmission of a 2 or 3 Mbps rate packet: EDR output power = 8 dBm.	TBD	mA
<b>Average Current</b>			
Page scan	–	TBD	mA
Sniff slave (495 ms)	Based on one attempt and no timeout parameter. Quality connection that rarely requires more than minimum packet exchange. Sniff master follows the optimal sniff protocol of the BCM20734 master.	TBD	μA
Sniff slave (22.5 ms)	–	TBD	mA
Sniff slave (11.25 ms)	–	TBD	mA
HIDOFF (Deep Sleep)	–	TBD	mA

## RF Specifications



### Note:

- All specifications in [Table 16](#) are for industrial temperatures.
- All specifications in [Table 16](#) are single-ended. Unused inputs are left open.

**Table 16: Receiver RF Specifications**

<i>Parameter</i>	<i>Conditions</i>	<i>Minimum</i>	<i>Typical<sup>a</sup></i>	<i>Maximum</i>	<i>Unit</i>
<b>General</b>					
Frequency range	–	2402	–	2480	MHz
RX sensitivity <sup>b</sup>	GFSK, 0.1% BER, 1 Mbps	–	–93.5	–	dBm
	LE GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
	$\pi/4$ -DQPSK, 0.01% BER, 2 Mbps	–	–95.5	–	dBm
	8-DPSK, 0.01% BER, 3 Mbps	–	–89.5	–	dBm
Maximum input	GFSK, 1 Mbps	–	–	–20	dBm
Maximum input	$\pi/4$ -DQPSK, 8-DPSK, 2/3 Mbps	–	–	–20	dBm
<b>Interference Performance</b>					
C/I cochannel	GFSK, 0.1% BER	–	9.5	11	dB
C/I 1 MHz adjacent channel	GFSK, 0.1% BER	–	–5	0	dB
C/I 2 MHz adjacent channel	GFSK, 0.1% BER	–	–40	–30.0	dB
C/I $\geq$ 3 MHz adjacent channel	GFSK, 0.1% BER	–	–49	–40.0	dB
C/I image channel	GFSK, 0.1% BER	–	–27	–9.0	dB
C/I 1 MHz adjacent to image channel	GFSK, 0.1% BER	–	–37	–20.0	dB
C/I cochannel	$\pi/4$ -DQPSK, 0.1% BER	–	11	13	dB
C/I 1 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	–	–8	0	dB
C/I 2 MHz adjacent channel	$\pi/4$ -DQPSK, 0.1% BER	–	–40	–30.0	dB
C/I $\geq$ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–50	–40.0	dB
C/I image channel	$\pi/4$ -DQPSK, 0.1% BER	–	–27	–7.0	dB
C/I 1 MHz adjacent to image channel	$\pi/4$ -DQPSK, 0.1% BER	–	–40	–20.0	dB
C/I cochannel	8-DPSK, 0.1% BER	–	17	21	dB
C/I 1 MHz adjacent channel	8-DPSK, 0.1% BER	–	–5	5	dB
C/I 2 MHz adjacent channel	8-DPSK, 0.1% BER	–	–40	–25.0	dB
C/I $\geq$ 3 MHz adjacent channel	8-DPSK, 0.1% BER	–	–47	–33.0	dB
C/I Image channel	8-DPSK, 0.1% BER	–	–20	0	dB
C/I 1 MHz adjacent to image channel	8-DPSK, 0.1% BER	–	–35	–13.0	dB

**Table 16: Receiver RF Specifications (Cont.)**

<b>Parameter</b>	<b>Conditions</b>	<b>Minimum</b>	<b>Typical<sup>a</sup></b>	<b>Maximum</b>	<b>Unit</b>
<b>Out-of-Band Blocking Performance (CW)<sup>c</sup></b>					
30 MHz–2000 MHz	0.1% BER	–	–10.0	–	dBm
2000–2399 MHz	0.1% BER	–	–27	–	dBm
2498–3000 MHz	0.1% BER	–	–27	–	dBm
3000 MHz–12.75 GHz	0.1% BER	–	–10.0	–	dBm
<b>Out-of-Band Blocking Performance, Modulated Interferer</b>					
776–764 MHz	CDMA	–	–10 <sup>d</sup>	–	dBm
824–849 MHz	CDMA	–	–10 <sup>d</sup>	–	dBm
1850–1910 MHz	CDMA	–	–23 <sup>d</sup>	–	dBm
824–849 MHz	EDGE/GSM	–	–10 <sup>d</sup>	–	dBm
880–915 MHz	EDGE/GSM	–	–10 <sup>d</sup>	–	dBm
1710–1785 MHz	EDGE/GSM	–	–23 <sup>d</sup>	–	dBm
1850–1910 MHz	EDGE/GSM	–	–23 <sup>d</sup>	–	dBm
1850–1910 MHz	WCDMA	–	–23 <sup>d</sup>	–	dBm
1920–1980 MHz	WCDMA	–	–23 <sup>d</sup>	–	dBm
<b>Intermodulation Performance<sup>e</sup></b>					
BT, Df = 5 MHz	–	–39.0	–	–	dBm
<b>Spurious Emissions<sup>f</sup></b>					
30 MHz to 1 GHz	–	–	–	–62	dBm
1 GHz to 12.75 GHz	–	–	–	–47	dBm
65 MHz to 108 MHz	FM Rx	–	–147	–	dBm/Hz
746 MHz to 764 MHz	CDMA	–	–147	–	dBm/Hz
851–894 MHz	CDMA	–	–147	–	dBm/Hz
925–960 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1805–1880 MHz	EDGE/GSM	–	–147	–	dBm/Hz
1930–1990 MHz	PCS	–	–147	–	dBm/Hz
2110–2170 MHz	WCDMA	–	–147	–	dBm/Hz

- Typical operating conditions are 1.22V operating voltage and 25°C ambient temperature.
- The receiver sensitivity is measured at BER of 0.1% on the device interface.
- Meets this specification using front-end band pass filter.
- Numbers are referred to the pin output with an external BPF filter.
- $f_0 = -64$  dBm Bluetooth-modulated signal,  $f_1 = -39$  dBm sine wave,  $f_2 = -39$  dBm Bluetooth-modulated signal,  $f_0 = 2f_1 - f_2$ , and  $|f_2 - f_1| = n \times 1$  MHz, where  $n$  is 3, 4, or 5. For the typical case,  $n = 4$ .
- Includes baseband radiated emissions.

**Note:**

- All specifications in [Table 17](#) are for industrial temperatures.
- All specifications in [Table 17](#) are single-ended. Unused inputs are left open.

**Table 17: Transmitter RF Specifications**

<b>Parameter</b>	<b>Conditions</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
<b>General</b>					
Frequency range	–	2402	–	2480	MHz
Class1: GFSK Tx power <sup>a</sup>	–	–	12	–	dBm
Class1: EDR Tx power <sup>b</sup>	–	–	9	–	dBm
Class 2: GFSK Tx power	–	–	2	–	dBm
Power control step	–	2	4	8	dB
<b>Modulation Accuracy</b>					
$\pi/4$ -DQPSK Frequency Stability	–	–10	–	10	kHz
$\pi/4$ -DQPSK RMS DEVM	–	–	–	20	%
$\pi/4$ -QPSK Peak DEVM	–	–	–	35	%
$\pi/4$ -DQPSK 99% DEVM	–	–	–	30	%
8-DPSK frequency stability	–	–10	–	10	kHz
8-DPSK RMS DEVM	–	–	–	13	%
8-DPSK Peak DEVM	–	–	–	25	%
8-DPSK 99% DEVM	–	–	–	20	%
<b>In-Band Spurious Emissions</b>					
1.0 MHz <  M – N  < 1.5 MHz	–	–	–	–26	dBc
1.5 MHz <  M – N  < 2.5 MHz	–	–	–	–20	dBm
M – N  $\geq$ 2.5 MHz	–	–	–	–40	dBm
<b>Out-of-Band Spurious Emissions</b>					
30 MHz to 1 GHz	–	–	–	–36.0 <sup>c</sup>	dBm
1 GHz to 12.75 GHz	–	–	–	–30.0 <sup>c, d</sup>	dBm
1.8 GHz to 1.9 GHz	–	–	–	–47.0	dBm
5.15 GHz to 5.3 GHz	–	–	–	–47.0	dBm

- a. TBD dBm output for GFSK measured with PAVDD = 2.5V.  
 b. TBD dBm output for EDR measured with PAVDD = 2.5V.  
 c. Maximum value is the value required for Bluetooth qualification.  
 d. Meets this spec using a front-end band-pass filter.

**Table 18: BLE RF Specifications**

<b>Parameter</b>	<b>Conditions</b>	<b>Minimum</b>	<b>Typical</b>	<b>Maximum</b>	<b>Unit</b>
Frequency range	N/A	2402	–	2480	MHz
Rx sense <sup>a</sup>	GFSK, 0.1% BER, 1 Mbps	–	–96.5	–	dBm
Tx power <sup>b</sup>	N/A	–	9	–	dBm
Mod Char: Delta F1 average	N/A	225	255	275	kHz
Mod Char: Delta F2 max <sup>c</sup>	N/A	99.9	–	–	%
Mod Char: Ratio	N/A	0.8	0.95	–	%

a. Dirty Tx is Off.

b. The BLE Tx power can be increased to compensate for front-end losses such as BPF, diplexer, switch, etc. The output is capped at 12 dBm out. The BLE Tx power at the antenna port cannot exceed the 10 dBm EIRP specification limit.

c. At least 99.9% of all delta F2 max frequency values recorded over 10 packets must be greater than 185 kHz.

# Timing and AC Characteristics

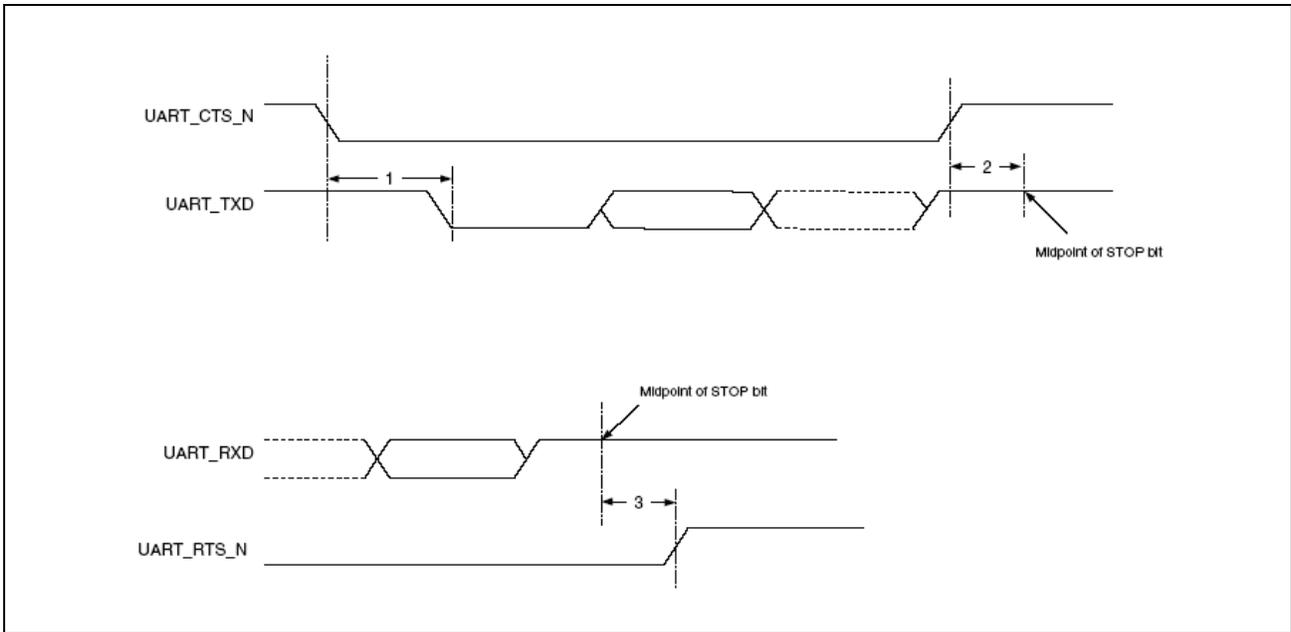
In this section, use the numbers listed in the **Reference** column of each table to interpret the following timing diagrams.

## UART Timing

**Table 19: UART Timing Specifications**

Reference	Characteristics	Min.	Max.	Unit
1	Delay time, UART_CTS_N low to UART_TXD valid	–	24	Baud out cycles
2	Setup time, UART_CTS_N high before midpoint of stop bit	–	10	ns
3	Delay time, midpoint of stop bit to UART_RTS_N high	–	2	Baud out cycles

**Figure 9: UART Timing**



## SPI Timing

The SPI interface can be clocked up to 12 MHz.

Table 20 and Figure 10 show the timing requirements when operating in SPI Mode 0 and 2.

**Table 20: SPI Mode 0 and 2**

Reference	Characteristics	Minimum	Maximum	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	$\infty$	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	$\infty$	ns
3	Time from master assert SPI_CSN to first clock edge	20	$\infty$	ns
4	Setup time for MOSI data lines	8	$\frac{1}{2}$ SCK	ns
5	Hold time for MOSI data lines	8	$\frac{1}{2}$ SCK	ns
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	$\infty$	ns
8	Idle time between subsequent SPI transactions	1 SCK	$\infty$	ns

**Figure 10: SPI Timing, Mode 0 and 2**

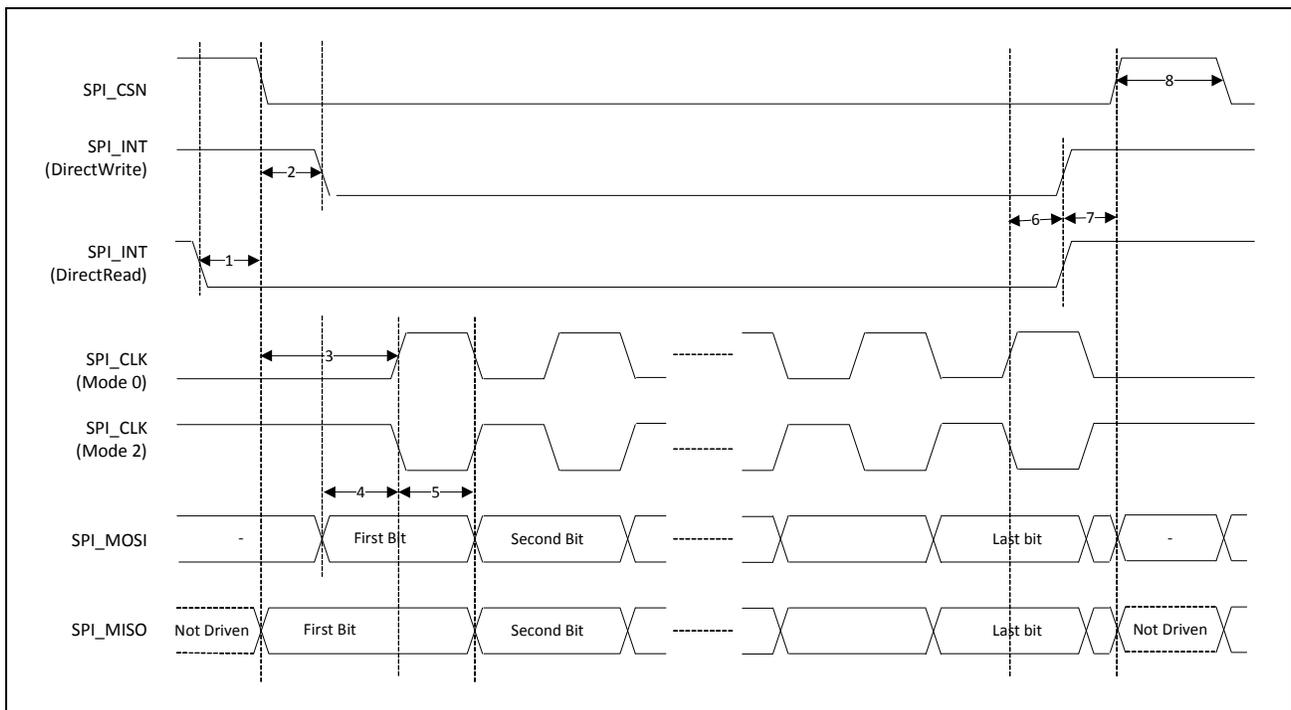
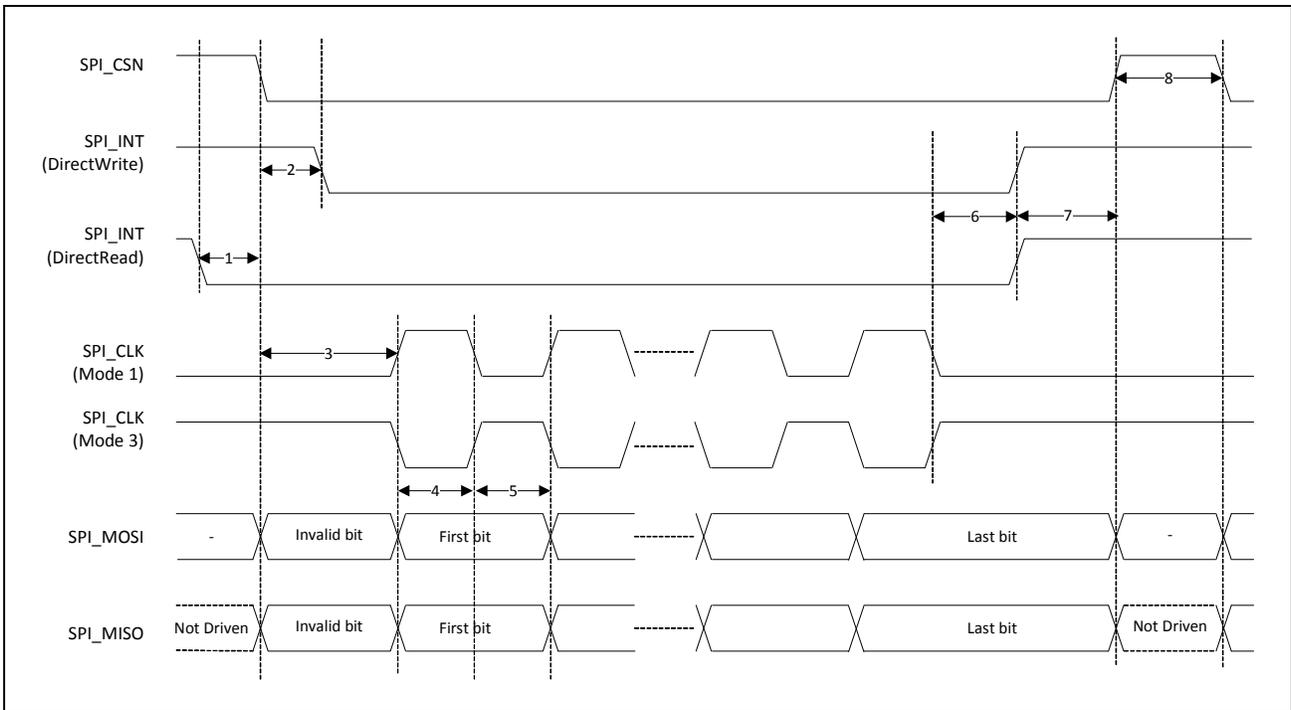


Table 21 and Figure 11 show the timing requirements when operating in SPI Mode 0 and 2.

**Table 21: SPI Mode 1 and 3**

Reference	Characteristics	Minimum	Maximum	Unit
1	Time from slave assert SPI_INT to master assert SPI_CSN (DirectRead)	0	$\infty$	ns
2	Time from master assert SPI_CSN to slave assert SPI_INT (DirectWrite)	0	$\infty$	ns
3	Time from master assert SPI_CSN to first clock edge	20	$\infty$	ns
4	Setup time for MOSI data lines	8	$\frac{1}{2}$ SCK	ns
5	Hold time for MOSI data lines	8	$\frac{1}{2}$ SCK	ns
6	Time from last sample on MOSI/MISO to slave deassert SPI_INT	0	100	ns
7	Time from slave deassert SPI_INT to master deassert SPI_CSN	0	$\infty$	ns
8	Idle time between subsequent SPI transactions	1 SCK	$\infty$	ns

**Figure 11: SPI Timing, Mode 1 and 3**



## BSC Interface Timing

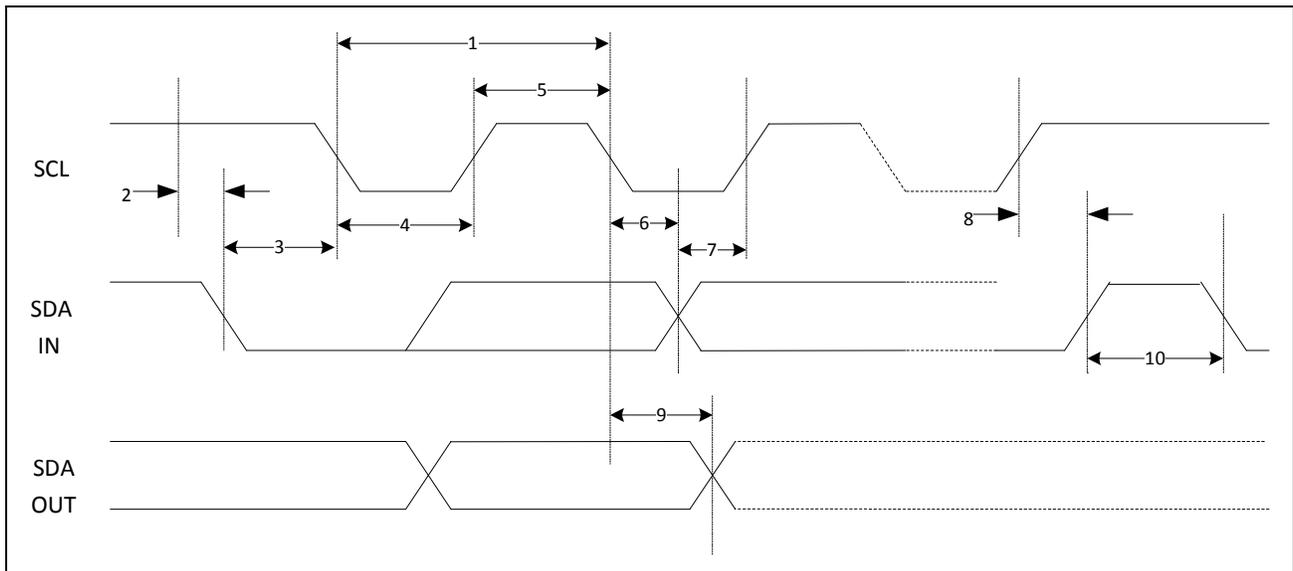
The specifications in [Table 22](#) references [Figure 12](#).

**Table 22: BSC Interface Timing Specifications (up to 1 MHz)**

Reference	Characteristics	Minimum	Maximum	Unit
1	Clock frequency		100 400 800 1000	kHz
2	START condition setup time	650	–	ns
3	START condition hold time	280	–	ns
4	Clock low time	650	–	ns
5	Clock high time	280	–	ns
6	Data input hold time <sup>a</sup>	0	–	ns
7	Data input setup time	100	–	ns
8	STOP condition setup time	280	–	ns
9	Output valid from clock	–	400	ns
10	Bus free time <sup>b</sup>	650	–	ns

- a. As a transmitter, 125 ns of delay is provided to bridge the undefined region of the falling edge of SCL to avoid unintended generation of START or STOP conditions.
- b. Time that the CBUS must be free before a new transaction can start.

**Figure 12: BSC Interface Timing Diagram**



# PCM Interface Timing

## Short Frame Sync, Master Mode

Figure 13: PCM Timing Diagram (Short Frame Sync, Master Mode)

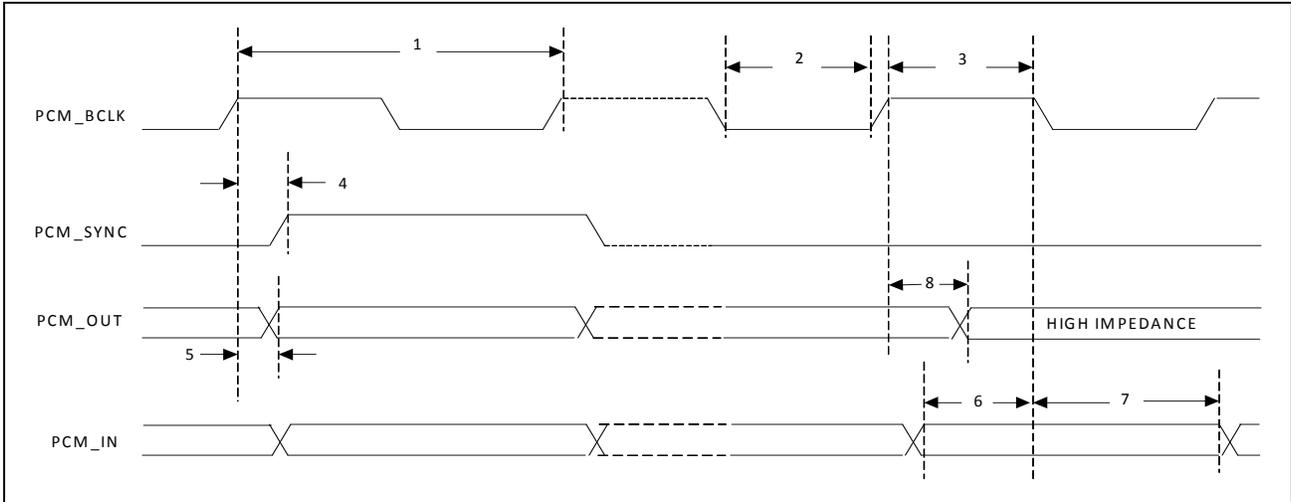


Table 23: PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	20.0	MHz
2	PCM bit clock LOW	20.0	–	–	ns
3	PCM bit clock HIGH	20.0	–	–	ns
4	PCM_SYNC delay	0	–	5.7	ns
5	PCM_OUT delay	–0.4	–	5.6	ns
6	PCM_IN setup	16.9	–	–	ns
7	PCM_IN hold	25.0	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	–0.4	–	5.6	ns

## Short Frame Sync, Slave Mode

Figure 14: PCM Timing Diagram (Short Frame Sync, Slave Mode)

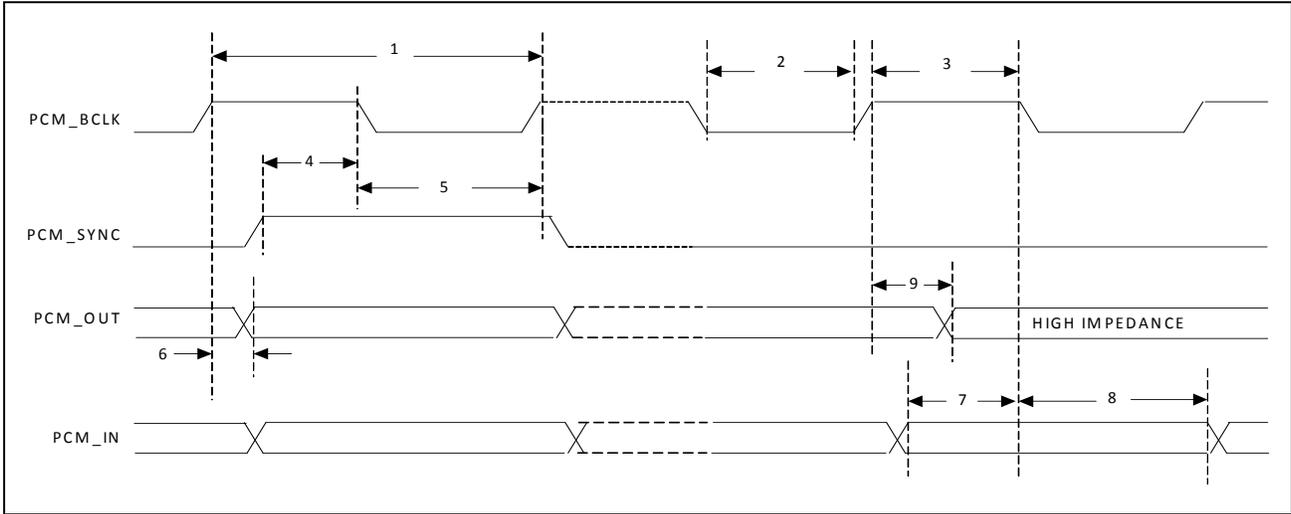


Table 24: PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	TBD	MHz
2	PCM bit clock LOW	TBD	–	–	ns
3	PCM bit clock HIGH	TBD	–	–	ns
4	PCM_SYNC setup	TBD	–	–	ns
5	PCM_SYNC hold	TBD	–	–	ns
6	PCM_OUT delay	TBD	–	TBD	ns
7	PCM_IN setup	TBD	–	–	ns
8	PCM_IN hold	TBD	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	TBD	–	TBD	ns

## Long Frame Sync, Master Mode

Figure 15: PCM Timing Diagram (Long Frame Sync, Master Mode)

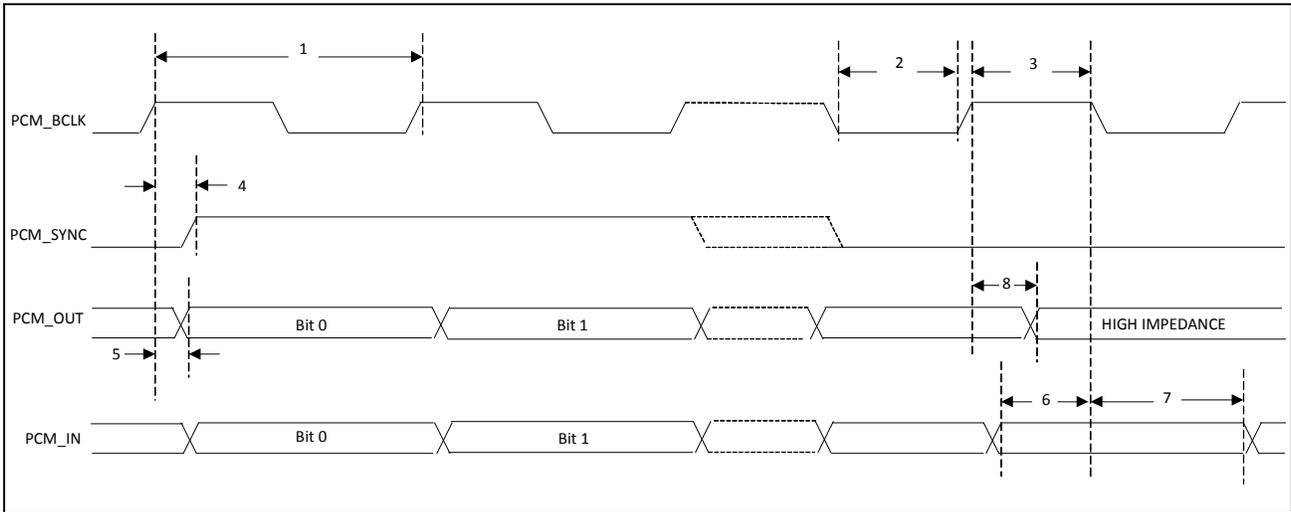


Table 25: PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	TBD	MHz
2	PCM bit clock LOW	TBD	–	–	ns
3	PCM bit clock HIGH	TBD	–	–	ns
4	PCM_SYNC delay	TBD	–	TBD	ns
5	PCM_OUT delay	TBD	–	TBD	ns
6	PCM_IN setup	TBD	–	–	ns
7	PCM_IN hold	TBD	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	TBD	–	TBD	ns

## Long Frame Sync, Slave Mode

Figure 16: PCM Timing Diagram (Long Frame Sync, Slave Mode)

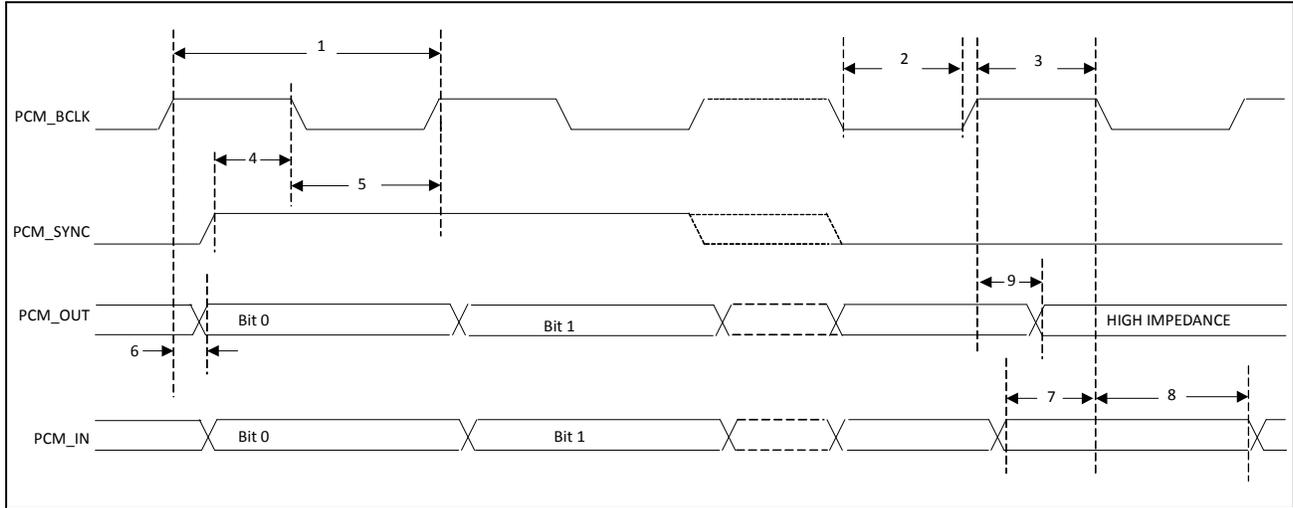


Table 26: PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	TBD	MHz
2	PCM bit clock LOW	TBD	–	–	ns
3	PCM bit clock HIGH	TBD	–	–	ns
4	PCM_SYNC setup	TBD	–	–	ns
5	PCM_SYNC hold	TBD	–	–	ns
6	PCM_OUT delay	TBD	–	TBD	ns
7	PCM_IN setup	TBD	–	–	ns
8	PCM_IN hold	TBD	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	TBD	–	TBD	ns

## I<sup>2</sup>S Timing

The BCM20734 supports two independent I<sup>2</sup>S digital audio ports. The I<sup>2</sup>S interface supports both master and slave modes. The I<sup>2</sup>S signals are:

- I<sup>2</sup>S clock: I<sup>2</sup>S SCK
- I<sup>2</sup>S Word Select: I<sup>2</sup>S WS
- I<sup>2</sup>S Data Out: I<sup>2</sup>S SDO
- I<sup>2</sup>S Data In: I<sup>2</sup>S SDI

I<sup>2</sup>S SCK and I<sup>2</sup>S WS become outputs in master mode and inputs in slave mode, while I<sup>2</sup>S SDO always stays as an output. The channel word length is 16 bits and the data is justified so that the MSB of the left-channel data is aligned with the MSB of the I<sup>2</sup>S bus, per the I<sup>2</sup>S specification. The MSB of each data word is transmitted one bit clock cycle after the I<sup>2</sup>S WS transition, synchronous with the falling edge of bit clock. Left-channel data is transmitted when I<sup>2</sup>S WS is low, and right-channel data is transmitted when I<sup>2</sup>S WS is high. Data bits sent by the BCM20734 are synchronized with the falling edge of I2S\_SCK and should be sampled by the receiver on the rising edge of I2S\_SSCK.

The clock rate in master mode is either of the following:

$$48 \text{ kHz} \times 32 \text{ bits per frame} = 1.536 \text{ MHz}$$

$$48 \text{ kHz} \times 50 \text{ bits per frame} = 2.400 \text{ MHz}$$

The master clock is generated from the input reference clock using a N/M clock divider.

In the slave mode, any clock rate is supported to a maximum of 3.072 MHz.



**Note:** Timing values specified in [Table 27](#) are relative to high and low threshold levels.

**Table 27: Timing for  $\hat{P}$ S Transmitters and Receivers**

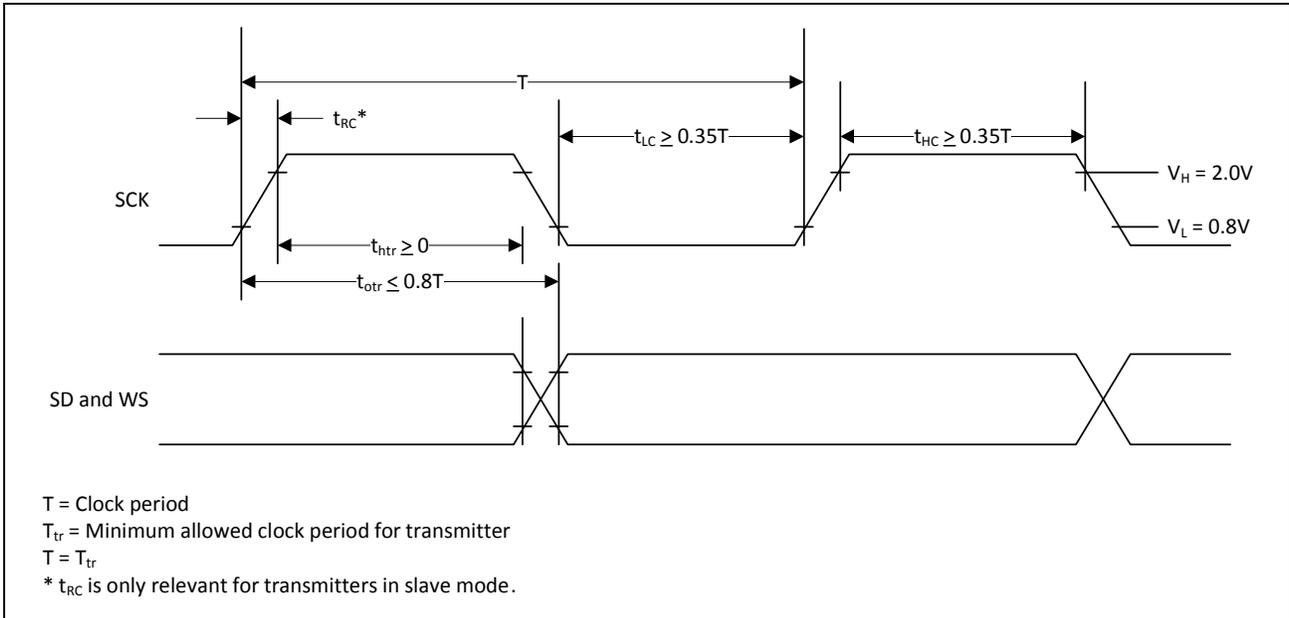
	<i>Transmitter</i>				<i>Receiver</i>				<i>Notes</i>
	<i>Lower Limit</i>		<i>Upper Limit</i>		<i>Lower Limit</i>		<i>Upper Limit</i>		
	<i>Min</i>	<i>Max</i>	<i>Min</i>	<i>Max</i>	<i>Min</i>	<i>Max</i>	<i>Min</i>	<i>Max</i>	
Clock Period T	$T_{tr}$	–	–	–	$T_r$	–	–	–	a
<b>Master Mode: Clock generated by transmitter or receiver</b>									
HIGH $t_{HC}$	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
LOW $t_{LC}$	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	–	b
<b>Slave Mode: Clock accepted by transmitter or receiver</b>									
HIGH $t_{HC}$	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
LOW $t_{LC}$	–	$0.35T_{tr}$	–	–	–	$0.35T_{tr}$	–	–	c
Rise time $t_{RC}$	–	–	$0.15T_{tr}$	–	–	–	–	–	d
<b>Transmitter</b>									
Delay $t_{dtr}$	–	–	–	$0.8T$	–	–	–	–	e
Hold time $t_{htr}$	0	–	–	–	–	–	–	–	d
<b>Receiver</b>									
Setup time $t_{sr}$	–	–	–	–	–	$0.2T_r$	–	–	f
Hold time $t_{hr}$	–	–	–	–	–	0	–	–	f

- a. The system clock period T must be greater than  $T_{tr}$  and  $T_r$  because both the transmitter and receiver have to be able to handle the data transfer rate.
- b. At all data rates in master mode, the transmitter or receiver generates a clock signal with a fixed mark/space ratio. For this reason,  $t_{HC}$  and  $t_{LC}$  are specified with respect to T.
- c. In slave mode, the transmitter and receiver need a clock signal with minimum HIGH and LOW periods so that they can detect the signal. So long as the minimum periods are greater than  $0.35T_r$ , any clock that meets the requirements can be used.
- d. Because the delay ( $t_{dtr}$ ) and the maximum transmitter speed (defined by  $T_{tr}$ ) are related, a fast transmitter driven by a slow clock edge can result in  $t_{dtr}$  not exceeding  $t_{RC}$  which means  $t_{htr}$  becomes zero or negative. Therefore, the transmitter has to guarantee that  $t_{htr}$  is greater than or equal to zero, so long as the clock rise-time  $t_{RC}$  is not more than  $t_{RCmax}$ , where  $t_{RCmax}$  is not less than  $0.15T_{tr}$ .
- e. To allow data to be clocked out on a falling edge, the delay is specified with respect to the rising edge of the clock signal and T, always giving the receiver sufficient setup time.
- f. The data setup and hold time must not be less than the specified receiver setup and hold time.

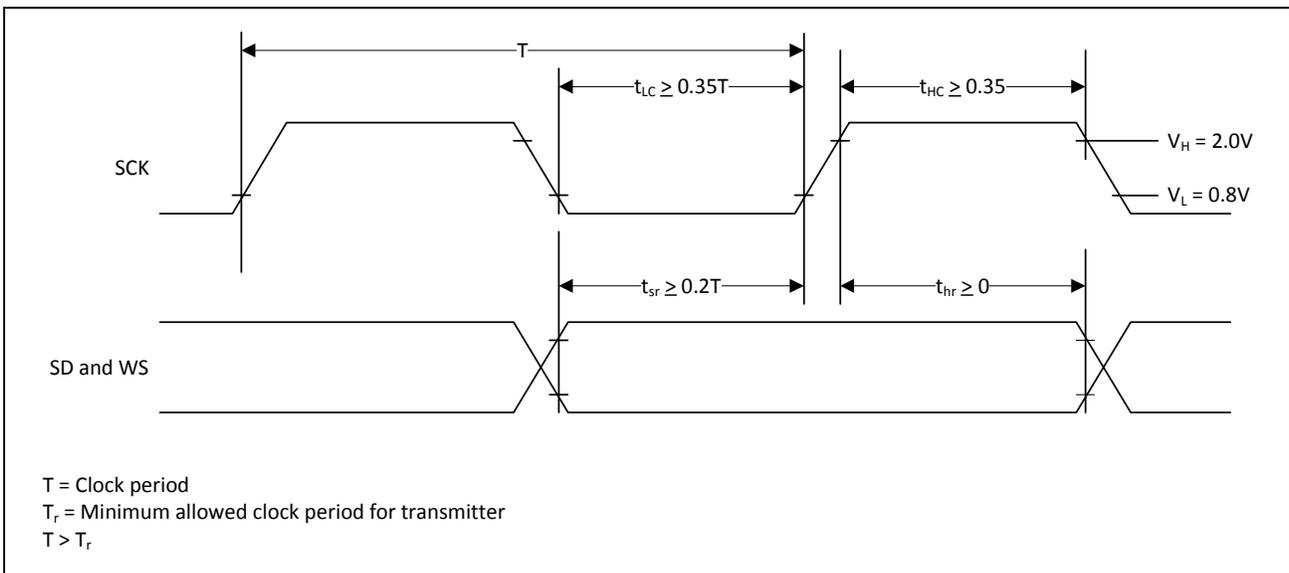


**Note:** The time periods specified in Figure 17 and Figure 18 are defined by the transmitter speed. The receiver specifications must match transmitter performance.

**Figure 17: I<sup>2</sup>S Transmitter Timing**



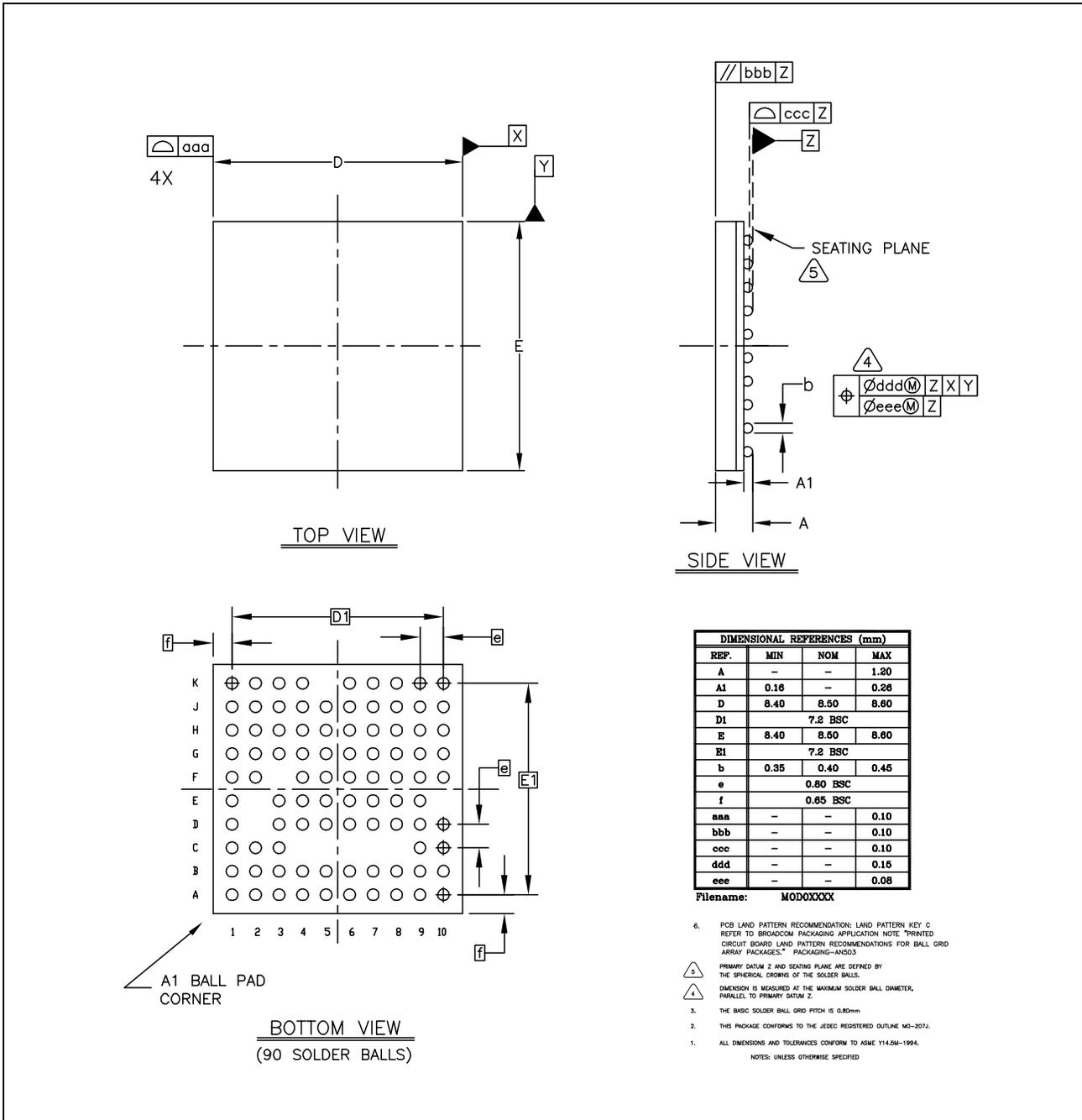
**Figure 18: I<sup>2</sup>S Receiver Timing**



# Section 4: Mechanical Information

## Package Diagram

Figure 19: BCM20734 8.5 mm x 8.5 mm 90-Pin FBGA Package



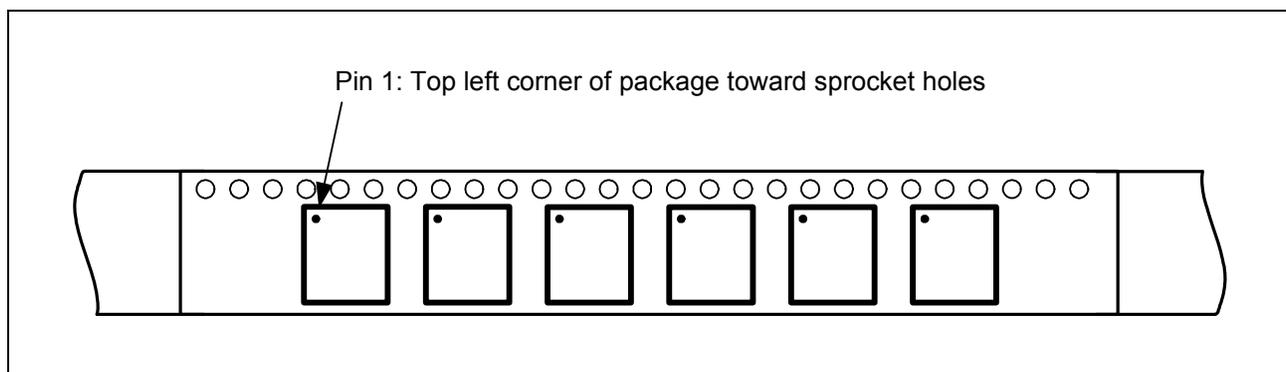
# Tape Reel and Packaging Specifications

**Table 28: BCM20734 Tape Reel Specifications**

<b>Parameter</b>	<b>Value</b>
Quantity per reel	2500
Reel diameter	13 inches
Hub diameter	4 inches
Tape width	16 mm
Tape pitch	12 mm

The top-left corner of the BCM20734 package is situated near the sprocket holes, as shown in [Figure 20](#).

**Figure 20: Pin 1 Orientation**



## Section 5: Ordering Information

*Table 29: Ordering Information*

<i>Part Number</i>	<i>Package</i>	<i>Ambient Operating Temperature</i>
BCM20734UA1KFFB3G	90-pin FBGA	0°C to 70°C

# Appendix A: Acronyms and Abbreviations

The following list of acronyms and abbreviations may appear in this document.

<b>Term</b>	<b>Description</b>
ADC	analog-to-digital converter
AFH	adaptive frequency hopping
AHB	advanced high-performance bus
APB	advanced peripheral bus
APU	audio processing unit
ARM7TDMI-S™	Acorn RISC Machine 7 Thumb instruction, Debugger, Multiplier, Ice, Synthesizable
BSC	Broadcom Serial Control
BTC	Bluetooth controller
COEX	coexistence
DFU	device firmware update
DMA	direct memory access
EBI	external bus interface
HCI	Host Control Interface
HV	high voltage
IDC	initial digital calibration
IF	intermediate frequency
IRQ	interrupt request
JTAG	Joint Test Action Group
LCU	link control unit
LDO	low drop-out
LHL	lean high land
LPO	low power oscillator
LV	LogicVision™
MIA	multiple interface agent
PCM	pulse code modulation
PLL	phase locked loop
PMU	power management unit
POR	power-on reset
PWM	pulse width modulation
QD	quadrature decoder
RAM	random access memory
RC oscillator	A resistor-capacitor oscillator is a circuit composed of an amplifier, which provides the output signal, and a resistor-capacitor network, which controls the frequency of the signal.
RF	radio frequency
ROM	read-only memory

<b><i>Term</i></b>	<b><i>Description</i></b>
RX/TX	receive, transmit
SPI	serial peripheral interface
SW	software
UART	universal asynchronous receiver/transmitter
UPI	μ-processor interface
WD	watchdog

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[RFPIC12F675H-I/SS](#) [JN5169001Z](#) [CYBL11171-56LQXI](#) [CYBL11573-56LQXI](#) [CYBL10161-56LQXI](#) [EZR32LG230F64R63G-C0](#)  
[ATSAMR21E18A-MU](#) [SI4010-C2-GSR](#) [EZR32WG330F256R69G-B0](#) [EZR32WG230F128R55G-B0](#) [EZR32WG230F256R55G-B0](#)  
[EZR32WG330F64R55G-B0](#) [Si1063-A-GM](#) [Si1081-A-GM](#) [Si1082-A-GM](#) [Si1084-A-GM](#) [Si1085-A-GM](#)