

60V N-Channel Trench MOSFET

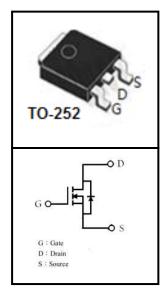
FEATURES

- Super Low Gate Charge
- 100% EAS Guaranteed
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply (UPS)
- Hard switched and high frequency circuits





Device Marking and Package Information				
Device	Package	Marking		
CTD06N017	TO-252	CTD06N017		

Absolute Maximum Ratings at T _j = 25°C unless otherwise noted				
Parameter		Symbol	Value	Unit
Drain-Source Voltage (V _{GS} = 0V)		V _{DSS}	60	V
Drain Current-Continuous(Tc=25°C)	(note1)	,	55	_
Drain Current-Continuous(Tc =100°C)	(note1)	I _D	35	Α
Pulsed Drain Current	(note2)	I _{DM}	200	А
Gate Source Voltage		V _{GSS}	±20	V
Power Dissipation $T_C = 25^{\circ}C$	(note4)	P _D	100	W
Single Pulse Avalanche Energy	(note3)	E _{AS}	64	mJ
Operating Junction and Storage Temperature Range		T_J,T_stg	-55~+175	°C

Thermal Characteristics				
Parameter		Symbol	Value	Unit
Thermal Resistance Junction-Case	(note1)	$R_{\theta Jc}$	1.5	°C/W



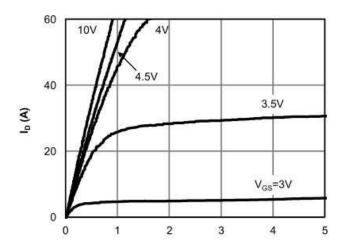
Electrical Characteristics T _j = 25°C unless otherwise specified							
Barranatar	Ob-al	Tool Conditions	Value			11.24	
Parameter	Symbol Test Conditions -		Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_{D} = 250\mu A$	60	-		V	
Zero Gate Voltage Drain Current		$V_{DS} = 60V, V_{GS} = 0V, T_{J} = 25^{\circ}C$			1	uA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 60V, V_{GS} = 0V, T_{J} = 55^{\circ}C$			5	uA	
Gate-Source Leakage	I _{GSS}	$V_{GS} = \pm 20V$			±100	nA	
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	1.0	1.6	2.5	V	
Drain-Source On-Resistance (note2)	D	$V_{GS} = 10V, I_D = 30A$		12	17	mΩ	
Diam-Source Off-Resistance (flotez)	R _{DS(on)}	$V_{GS} = 4.5V, I_{D} = 20A$		16	25	mΩ	
Dynamic							
Input Capacitance	C _{iss}	$V_{GS} = 0V$,		2890			
Output Capacitance	C_{oss}	$V_{DS} = 0.00$, $V_{DS} = 15V$, f = 1.0MHz		140		pF	
Reverse Transfer Capacitance	C_{rss}	T = T.UIVINZ		124			
Total Gate Charge (4.5V)	Q_g			50			
Gate-Source Charge	Q_gs	$V_{DS} = 30V, I_{D} = 30A,$ $V_{GS} = 10V$		6		пC	
Gate-Drain Charge	Q_{gd}	50		15			
Turn-on Delay Time	t _{d(on)}			7.4			
Turn-on Rise Time	t _r	$V_{DS} = 25V, I_{D} = 30A$		5.1		ns	
Turn-off Delay Time	$t_{d(off)}$	$V_{GS} = 10V, R_G = 24\Omega$		28.2			
Turn-off Fall Time	t _f			5.5			
Body Diode Characteristics							
Continuous Body Diode Current	Is	T _C = 25 °C			55	Α	
Body Diode Voltage	V _{SD}	$T_J = 25^{\circ}\text{C}, I_{SD} = 20\text{A}, V_{GS} = 0\text{V}$			1.2	V	
Reverse Recovery Time	trr	TJ=25°C IF= 60A,		28		nS	
Reverse Recovery Charge	Qrr	di/dt=100A/μs		40		NC	

Notes

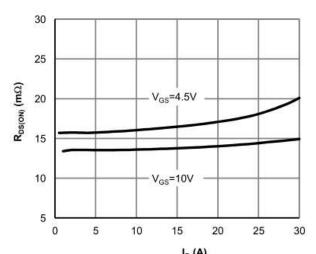
- 1. The data tested by surface mounted on a 1 inch2 FR-4 board with 2OZ copper.
- 2. The data tested by pulsed , pulse width $\!\!\! \leq \!\! 300 us$, duty cycle $\!\!\! \leq \!\! 2\%$
- 3. The EAS data shows Max. rating . The test condition is VDD =25V,VGS =10V,L=0.1mH
- 4. The power dissipation is limited by 175°C junction temperature
- 5. The data is theoretically the same as ID and IDM, in real applications, should be limited by total power dissipation.



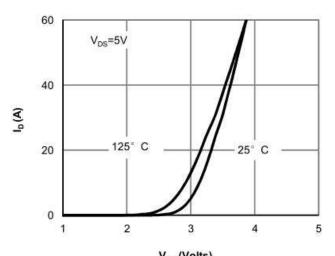
Typical Characteristics $T_J = 25^{\circ}C$, unless otherwise noted



 $V_{DS} \, (Volts) \\$ Figure 1: On-Region Characteristics (Note E)



I_D (A) Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)



V_{GS} (Volts) Figure 2: Transfer Characteristics (Note E)

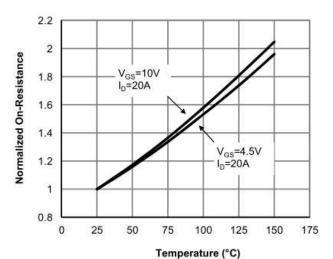
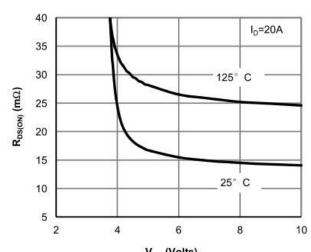
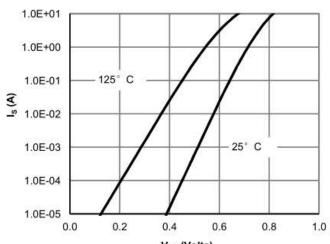


Figure 4: On-Resistance vs. Junction Temperature (Note E)



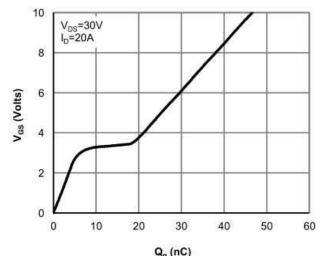
V_{GS} (Volts)
Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)



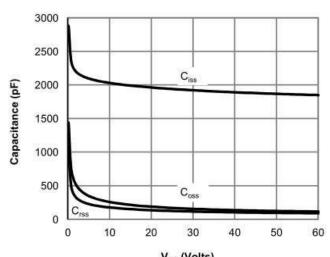
V_{SD} (Volts) Figure 6: Body-Diode Characteristics (Note E)



Typical Characteristics $T_J = 25$ °C, unless otherwise noted



 $\label{eq:Qg} \mathbf{Q_g} \, (\mathbf{nC})$ Figure 7: Gate-Charge Characteristics



V_{DS} (Volts)
Figure 8: Capacitance Characteristics

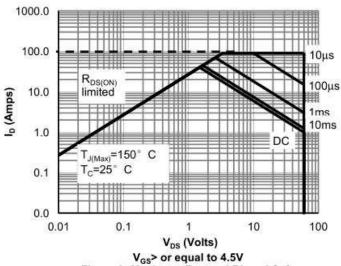


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

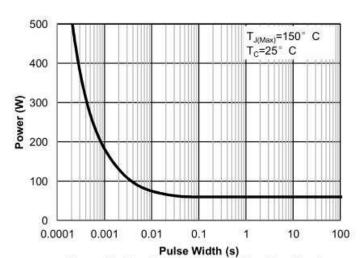


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

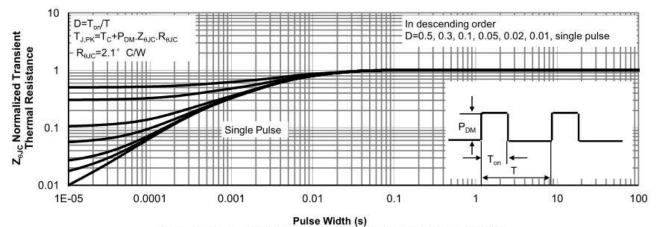


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



Figure A: Gate Charge Test Circuit and Waveform

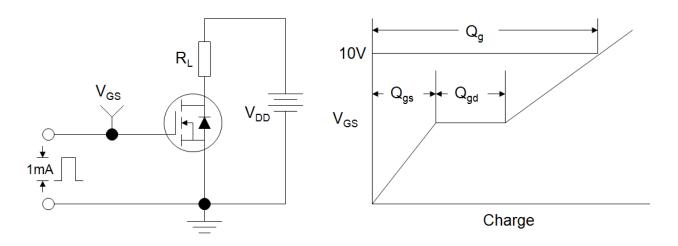


Figure B: Resistive Switching Test Circuit and Waveform

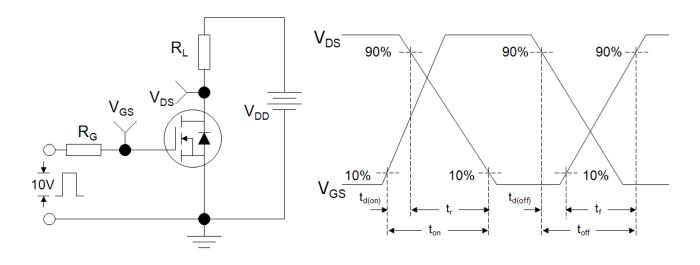
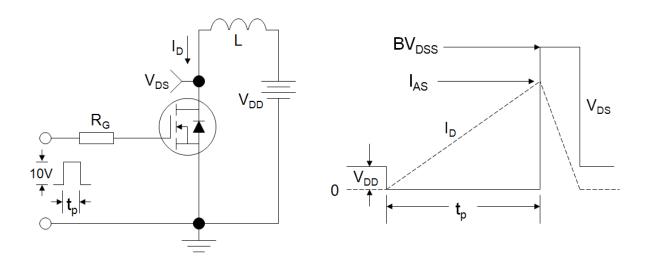
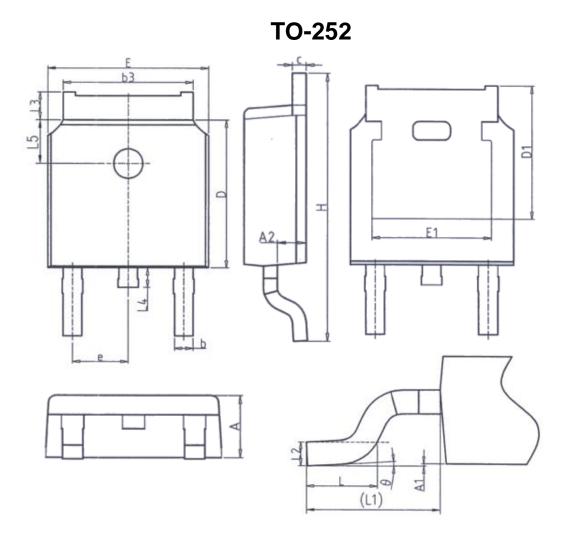


Figure C: Unclamped Inductive Switching Test Circuit and Waveform







Unit: mm			
Symbol	Min.	Max.	
Α	2. 20	2. 40	
A1	0.00	0. 20	
A2	0. 97	1. 17	
b	0. 68	0. 90	
b3	5. 20	5. 50	
С	0. 43	0. 63	
D	5. 98	6. 22	
D1	D1 5. 30REF		
E	6. 40	6. 80	
E1	4. 63	_	

Unit: mm				
Symbol	Min. Max.			
е	2. 286BSC			
Н	9. 40	10.50		
L	1. 38	1. 75		
L1	2. 90REF			
L2	0. 51BSC			
L3	0.88	1. 28		
L4	_	1.00		
L5	1. 65	1. 95		
θ	0°	8°		



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