

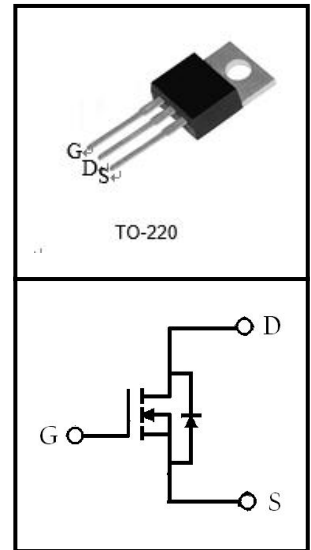
100V N-Channel Split Gate MOSFET

FEATURES

- Super Low Gate Charge
- 100% EAS Guaranteed
- RoHS compliant
- Green Device Available
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology

APPLICATIONS

- DC/DC Converter
- Ideal for high-frequency switching and synchronous rectification



Device Marking and Package Information

Device	Package	Marking
CSP10N4P2	TO-220	CSP10N4P2

Absolute Maximum Ratings at $T_J = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Value	Unit
Drain-Source Voltage ($V_{GS} = 0V$)	V_{DSS}	100	V
Continuous Drain Current $T_C = 25^\circ\text{C}$ (note1)	I_D	180	A
Continuous Drain Current $T_C = 100^\circ\text{C}$ (note1)		110	A
Pulsed Drain Current (note2)	I_{DM}	450	A
Gate Source Voltage	V_{GSS}	± 20	V
Single Pulse Avalanche Energy (note3)	E_{AS}	665	mJ
Power Dissipation $T_C = 25^\circ\text{C}$ (note4)	P_D	284	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	$-55 \sim +150$	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	0.4	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient (note1)	$R_{\theta JA}$	50	

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0V, I _D = 250μA	100	--	--	V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 100V, V _{GS} = 0V, T _J = 25°C	--	--	1	uA
		V _{DS} = 100V, V _{GS} = 0V, T _J = 55°C	--	--	5	uA
Gate-Source Leakage	I _{GSS}	V _{GS} = ±20V	--	--	±100	nA
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250μA	2	--	4	V
Drain-Source On-Resistance (note2)	R _{DS(on)}	V _{GS} = 10V, I _D = 60A	--	3.5	4.2	mΩ
Dynamic						
Input Capacitance	C _{iss}	V _{GS} = 0V, V _{DS} = 25V, f = 1.0MHz	--	5505	--	pF
Output Capacitance	C _{oss}		--	1656	--	
Reverse Transfer Capacitance	C _{rss}		--	90	--	
Total Gate Charge (10V)	Q _g	V _{DS} = 80V, I _D = 40A, V _{GS} = 10V	--	83	--	nC
Gate-Source Charge	Q _{gs}		--	24	--	
Gate-Drain Charge	Q _{gd}		--	19	--	
Turn-on Delay Time	t _{d(on)}	V _{DS} = 50V, I _D = 30A V _{GS} = 10V,R _G = 4.7Ω	--	25	--	ns
Turn-on Rise Time	t _r		--	33	--	
Turn-off Delay Time	t _{d(off)}		--	45	--	
Turn-off Fall Time	t _f		--	19	--	
Body Diode Characteristics						
Continuous Body Diode Current	I _{SD}		--	--	180	A
Pulsed Diode Forward Current	I _{SDM}		--	--	450	A
Body Diode Voltage	V _{SD}	T _J = 25°C, I _{SD} = 60A, V _{GS} = 0V	--	--	1.2	V
Reverse Recovery Time	t _{rr}	T _J = 25°C , I _F = 30A di _F /dt = 100A/μs	--	71	--	ns
Reverse Recovery Charge	Q _{rr}		--	144	--	nC

Notes

1. The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
3. The EAS data shows Max. rating . The test condition is $V_{DD} = 25V, V_{GS} = 10V, L = 0.5mH$
4. The power dissipation is limited by 150°C junction temperature
5. The data is theoretically the same as I_D and IDM , in real applications , should be limited by total power dissipation.

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

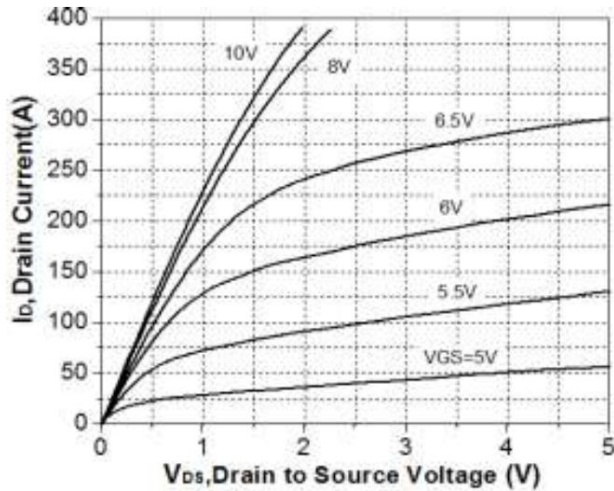


Figure 1. On-Region Characteristics

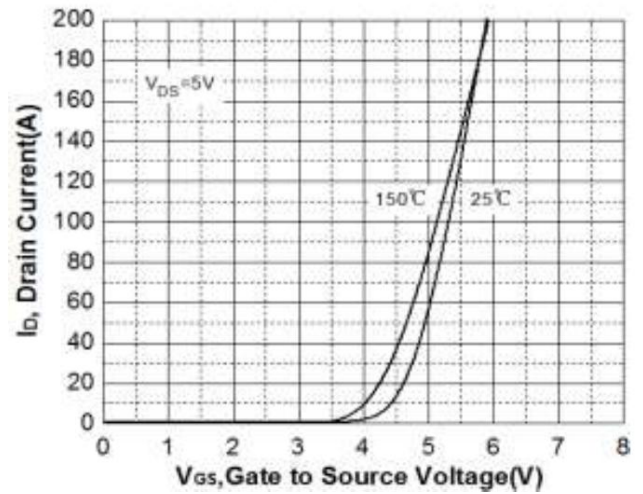


Figure 2. Transfer Characteristics

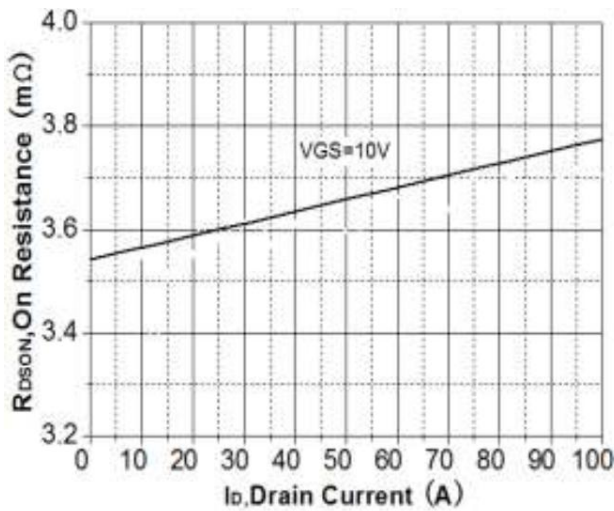


Figure 3. On-Resistance Variation vs Drain Current

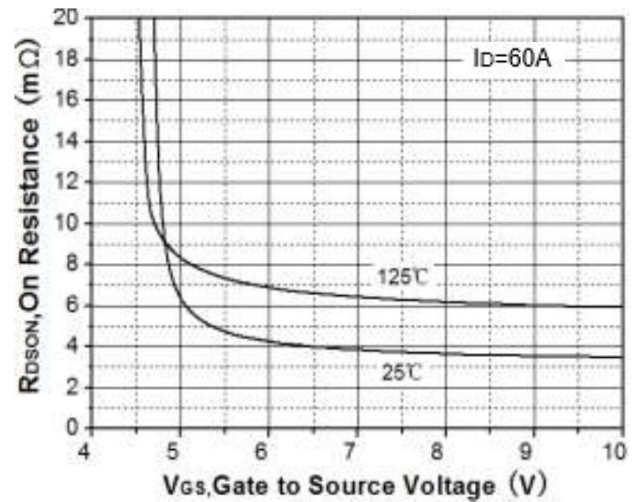


Figure 4. On-Resistance Vs Gate to Source Voltage

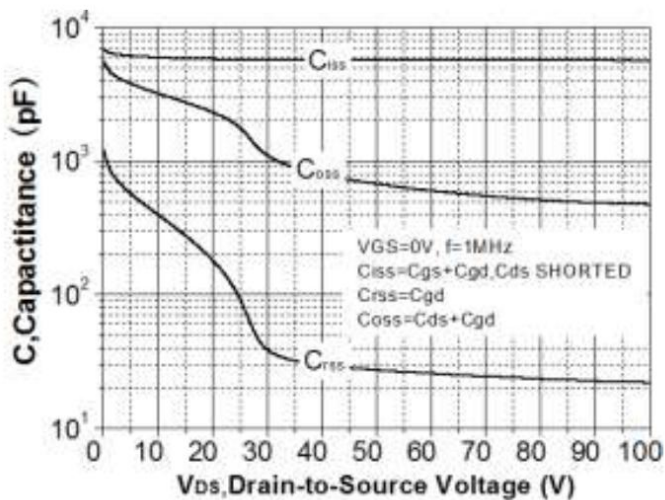


Figure 5. Capacitance Characteristics

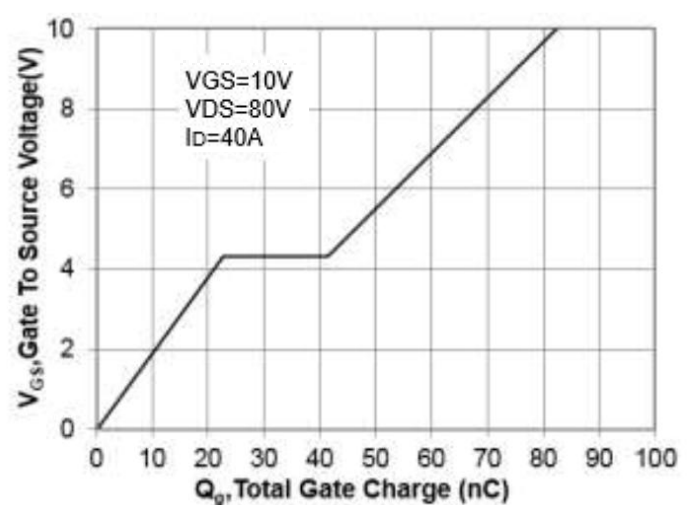


Figure 6. Gate Charge Characteristics

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

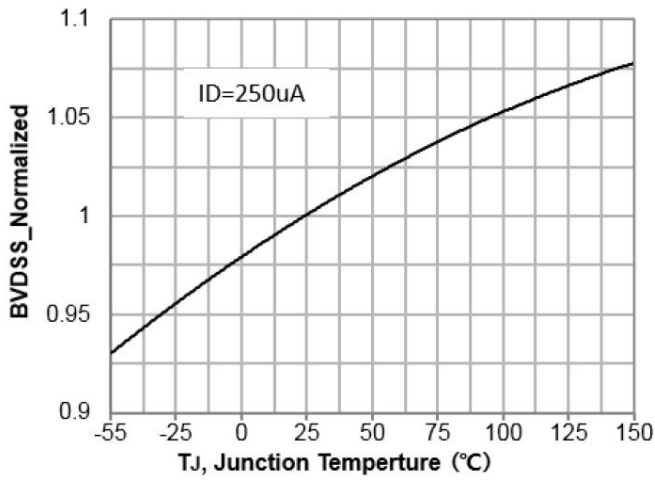


Figure 7. Breakdown Voltage Variation vs Temperature

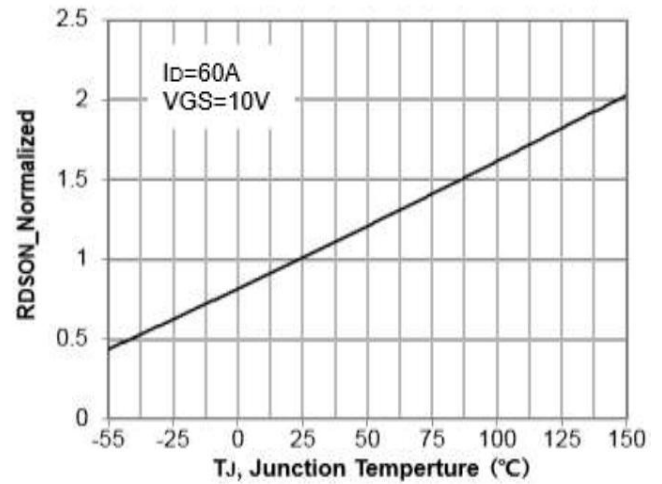


Figure 8. On-Resistance Variation vs Temperature

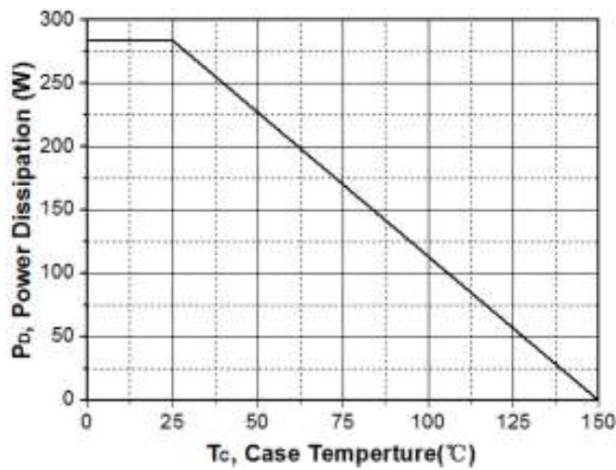


Figure 9. Power Dissipation

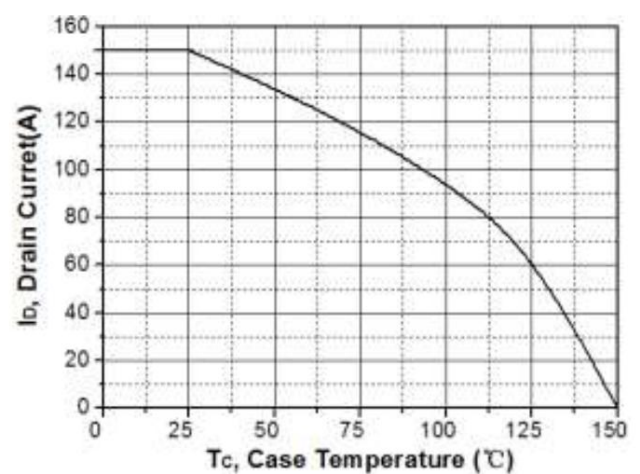


Figure 10. Drain Current Derating

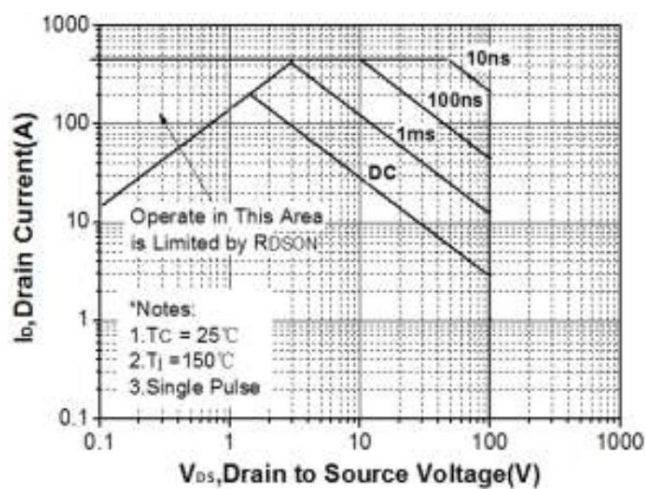


Figure 11. Maximum Safe Operating Area

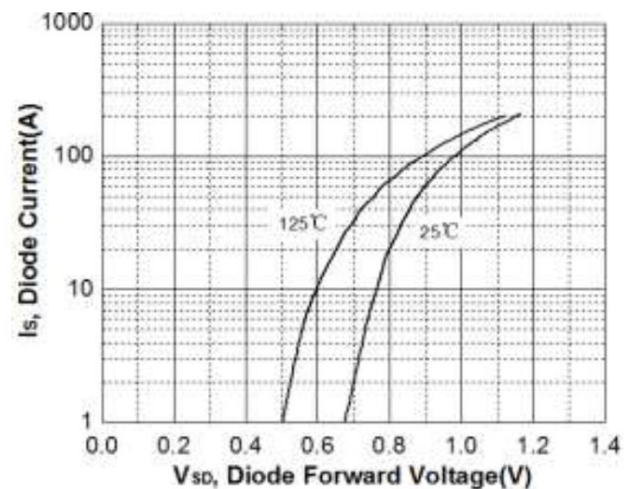


Figure 12. Body-diode Forward Characteristics

Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

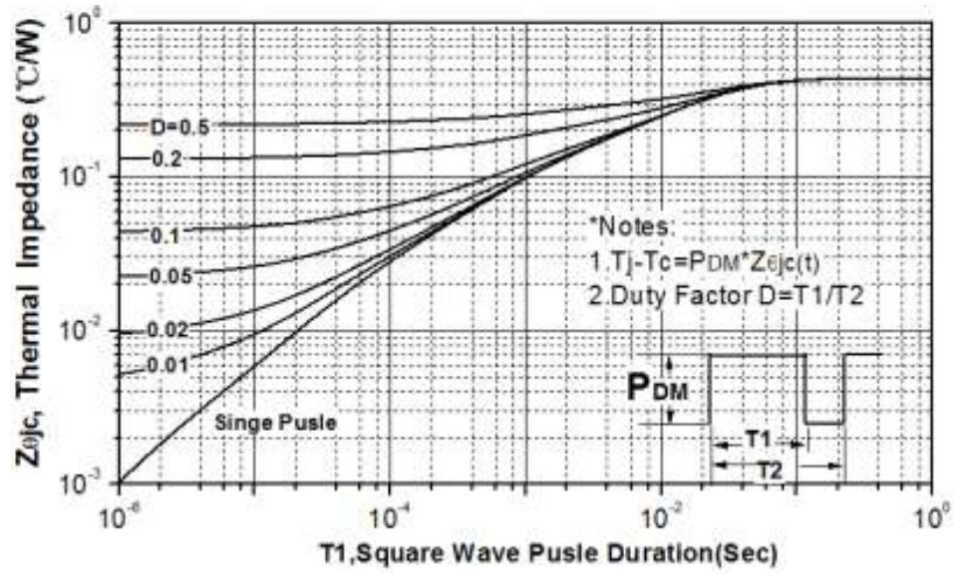
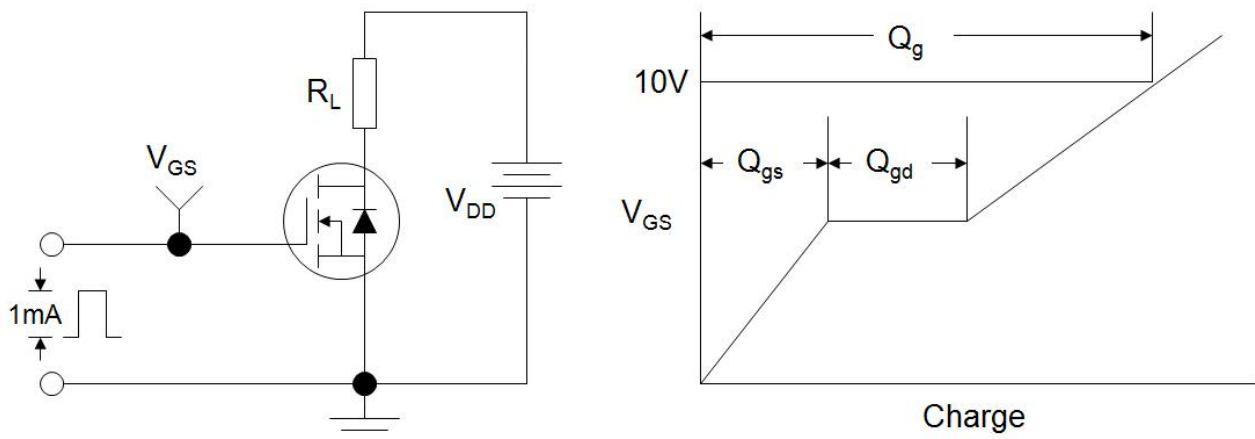
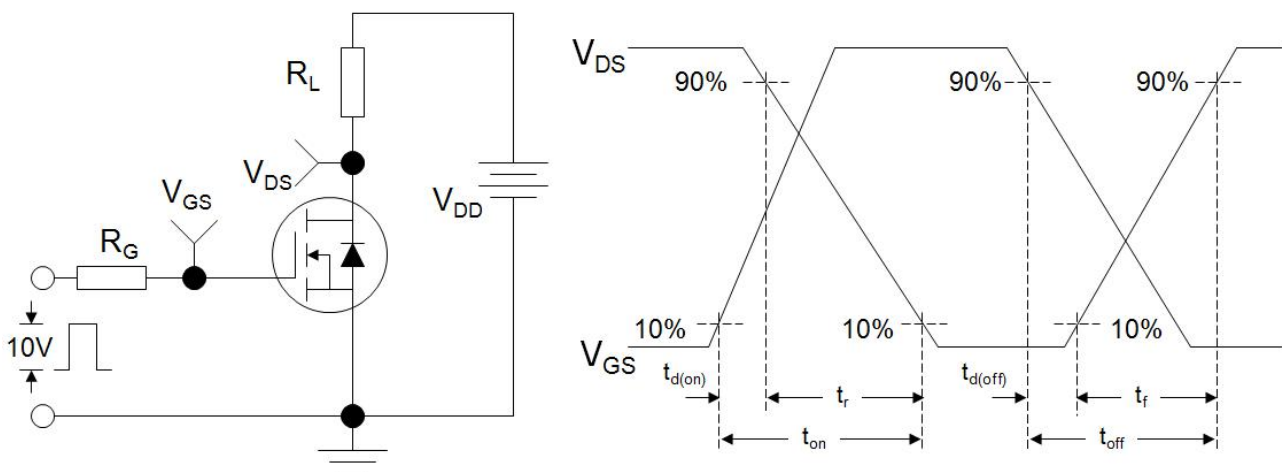
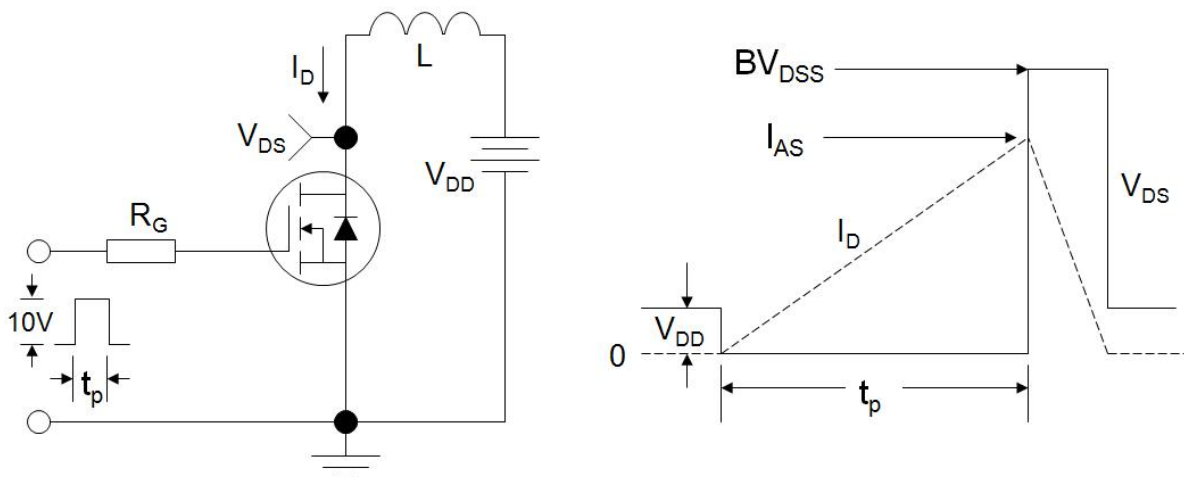
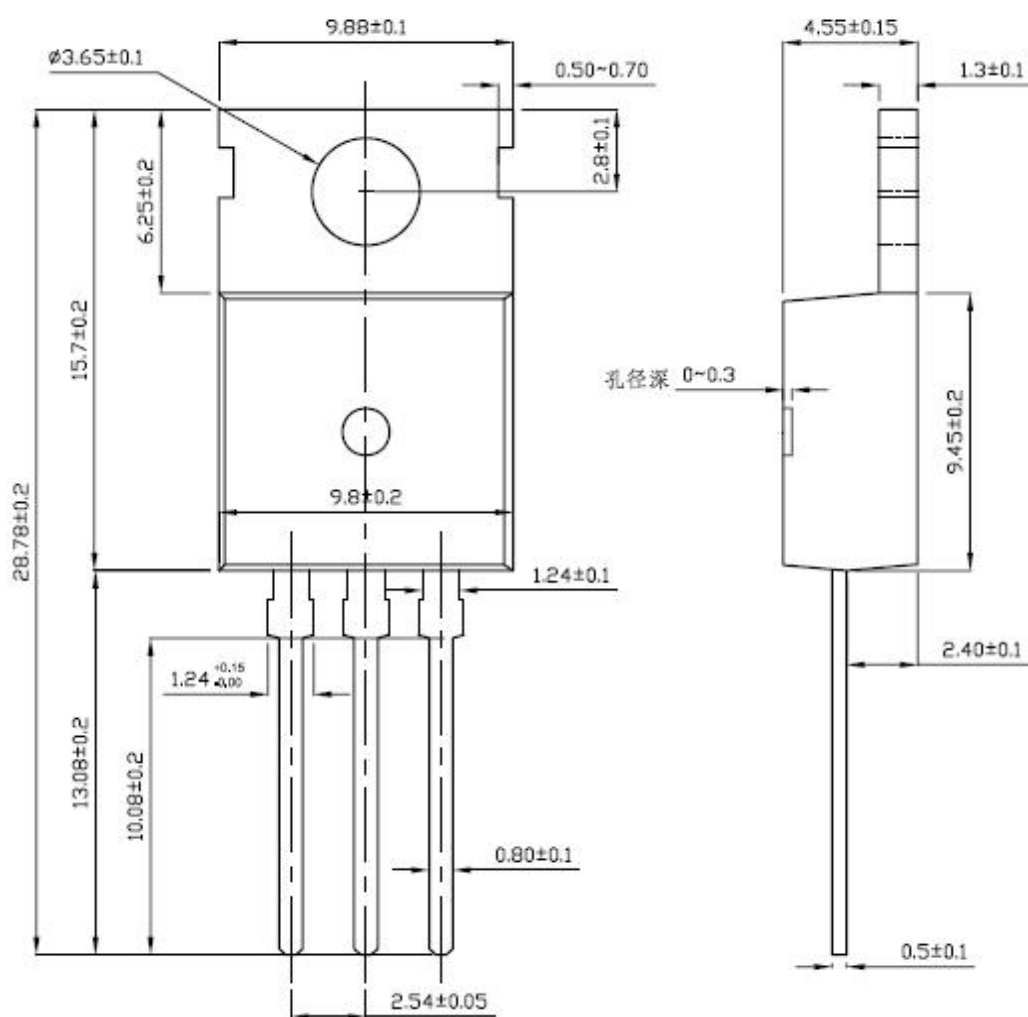


Figure 13. Transient Thermal Response Curve

Figure A: Gate Charge Test Circuit and Waveform

Figure B: Resistive Switching Test Circuit and Waveform

Figure C: Unclamped Inductive Switching Test Circuit and Waveform


TO-220



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