

20V N+P-Channel Enhancement Mode MOSFET

Description

The AP25G02NF uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 2.5V. This device is suitable for use as a Battery protection or in other Switching application.

General Features

$V_{DS} = 20V$ $I_D = 32A$

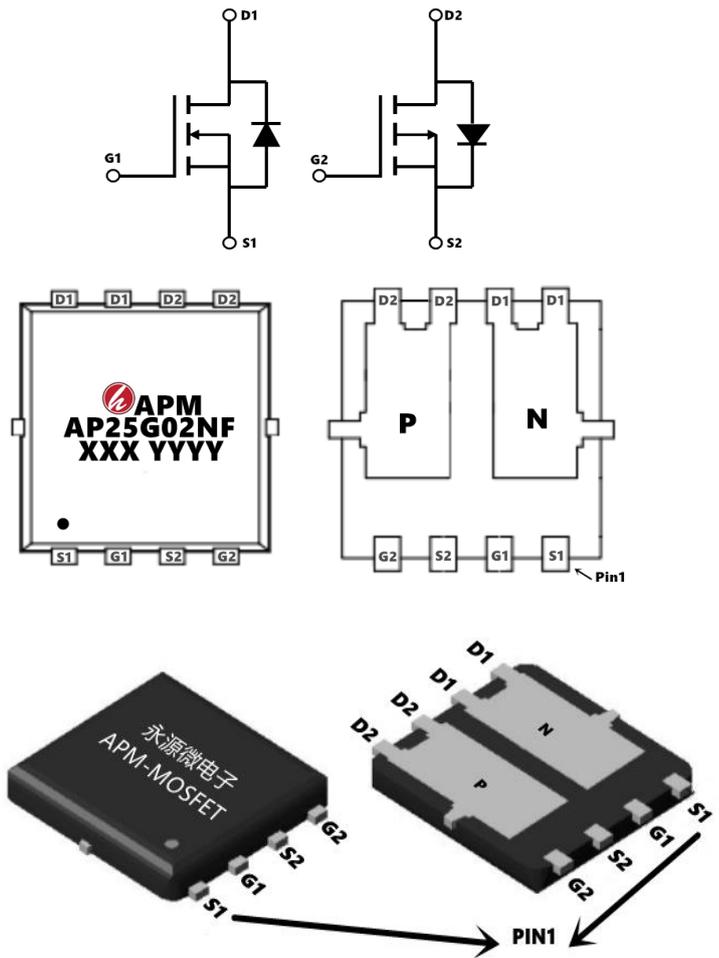
$R_{DS(ON)} < 10m\Omega$ @ $V_{GS}=4.5V$ (Type: 7.7m Ω)

$V_{DS} = -20V$ $I_D = -26.8A$

$R_{DS(ON)} < 20m\Omega$ @ $V_{GS}=-4.5V$ (Type: 16.8m Ω)

Application

- Wireless charging
- Boost driver
- Brushless motor



Package Marking and Ordering Information

Product ID	Pack	Marking	Qty(PCS)
AP25G02NF	PDFN5*6-8L	AP25G02NF XXX YYYY	5000

Absolute Maximum Ratings ($T_C=25^\circ C$ unless otherwise noted)

Symbol	Parameter	N-Ch	P-Ch	Units
V_{DS}	Drain-Source Voltage	20	-20	V
V_{GS}	Gate-Source Voltage	± 12	± 12	V
$I_D@T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	32	26.8	A
$I_D@T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V^1$	27.4	-22.5	A
I_{DM}	Pulsed Drain Current ²	78	-69.1	A
EAS	Single Pulse Avalanche Energy ³	150	135	mJ
I_{AS}	Avalanche Current	72	68	A
$P_D@T_C=25^\circ C$	Total Power Dissipation ⁴	46	41.3	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	-55 to 150	$^\circ C$
$R_{\theta JA}$	Thermal Resistance Junction-Ambient ¹	62		$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance Junction-Case ¹	5		$^\circ C/W$

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Electrical Characteristics (T_c=25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250μA	20	23	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} =20V, V _{GS} =0V,	-	-	1.0	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} =±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	0.58	0.65	1.2	V
RDS(on)	Static Drain-Source on-Resistance note3	V _{GS} =4.5V, I _D =25A	-	7.7	10	mΩ
		V _{GS} =2.5V, I _D =10A	-	10	13	
C _{iss}	Input Capacitance	V _{DS} =10V, V _{GS} =0V, f=1.0MHz	-	1458	-	pF
C _{oss}	Output Capacitance		-	238	-	pF
C _{rss}	Reverse Transfer Capacitance		-	212	-	pF
Q _g	Total Gate Charge	V _{DS} =10V, I _D =25A, V _{GS} =4.5V	-	19	-	nC
Q _{gs}	Gate-Source Charge		-	3	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	6.4	-	nC
td(on)	Turn-on Delay Time	V _{DS} =10V, I _D =10A, R _{GEN} =3Ω, V _{GS} =4.5V	-	10	-	ns
t _r	Turn-on Rise Time		-	21	-	ns
td(off)	Turn-off Delay Time		-	39	-	ns
t _f	Turn-off Fall Time		-	19	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	50	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	200	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S =30A	-	-	1.2	V
trr	Body Diode Reverse Recovery Time	IF=20A, dI/dt=100A/μs	-	25	-	ns
Qrr	Body Diode Reverse Recovery Charge		-	20	-	nC

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The EAS data shows Max. rating . The test condition is V_{DD}=16V, V_{GS}=10V, L=0.1mH, I_{AS}=21A
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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Electrical Characteristics (T_c=25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V(BR)DSS	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250μA	-20	-22	-	V
IDSS	Zero Gate Voltage Drain Current	V _{DS} = -20V, V _{GS} =0V,	-	-	-1	μA
IGSS	Gate to Body Leakage Current	V _{DS} =0V, V _{GS} = ±12V	-	-	±100	nA
VGS(th)	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250μA	-0.58	-0.7	-1.2	V
RDS(on)	Static Drain-Source on-Resistance note2	V _{GS} = -4.5V, I _D = -10A	-	16.8	20	mΩ
		V _{GS} = -2.5V, I _D = -5A	-	21.5	25	
C _{iss}	Input Capacitance	V _{DS} = -10V, V _{GS} =0V, f=1.0MHz	-	2000	-	pF
C _{oss}	Output Capacitance		-	242	-	pF
C _{rss}	Reverse Transfer Capacitance		-	231	-	pF
Q _g	Total Gate Charge	V _{DS} = -10V, I _D = -6A, V _{GS} = -4.5V	-	15.3	-	nC
Q _{gs}	Gate-Source Charge		-	2.2	-	nC
Q _{gd}	Gate-Drain("Miller") Charge		-	4.4	-	nC
td(on)	Turn-on Delay Time	V _{DD} = -10V, I _D = -12A, V _{GS} = -4.5V, R _{GEN} =2.5Ω	-	10	-	ns
t _r	Turn-on Rise Time		-	31	-	ns
td(off)	Turn-off Delay Time		-	28	-	ns
t _f	Turn-off Fall Time		-	8	-	ns
IS	Maximum Continuous Drain to Source Diode Forward Current		-	-	-12	A
ISM	Maximum Pulsed Drain to Source Diode Forward Current		-	-	-48	A
VSD	Drain to Source Diode Forward Voltage	V _{GS} =0V, I _S = -12A	-	-0.8	-1.2	V

Note :

- 1、 The data tested by surface mounted on a 1 inch² FR-4 board with 20Z copper.
- 2、 The data tested by pulsed , pulse width ≅ 300us , duty cycle ≅ 2%
- 3、 The EAS data shows Max. rating . The test condition is V^{DD}=-16V,V^{GS}=-10V,L=0.1mH,I^{AS}=-21A
- 4、 The power dissipation is limited by 150°C junction temperature
- 5、 The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

N-Typical Characteristics

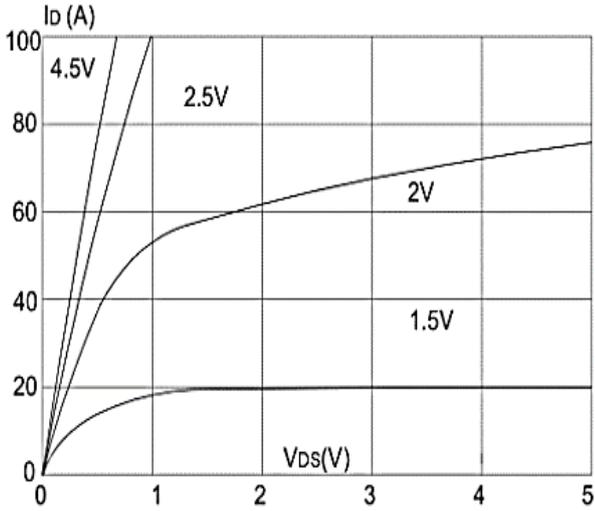


Figure 1: Output Characteristics

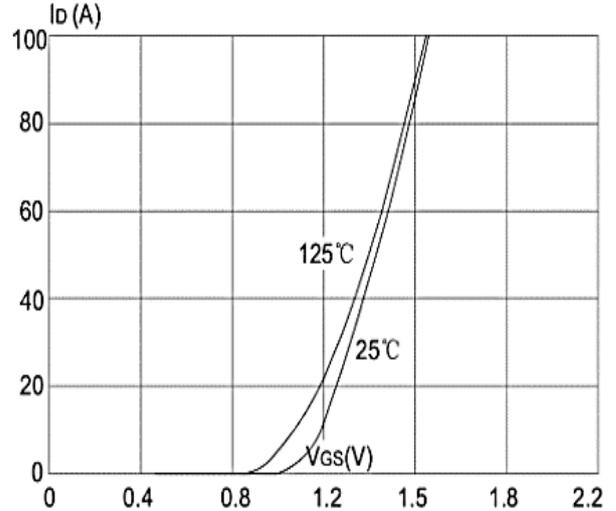


Figure 2: Typical Transfer Characteristics

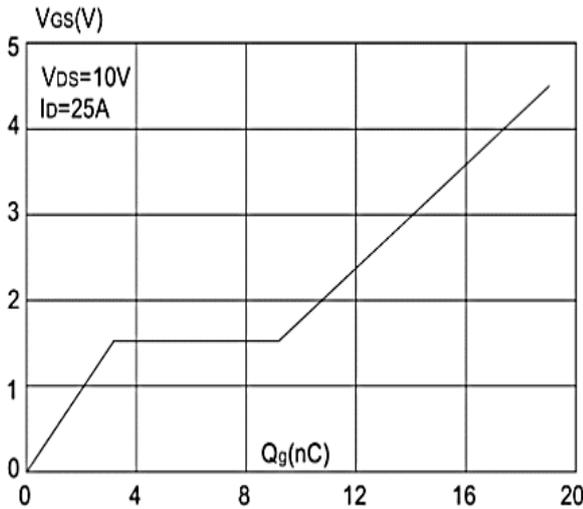


Figure 3: On-resistance vs. Drain Current

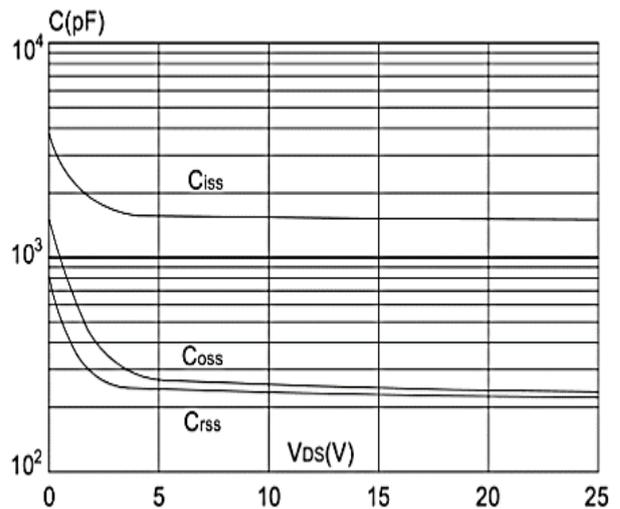


Figure 4: Body Diode Characteristics

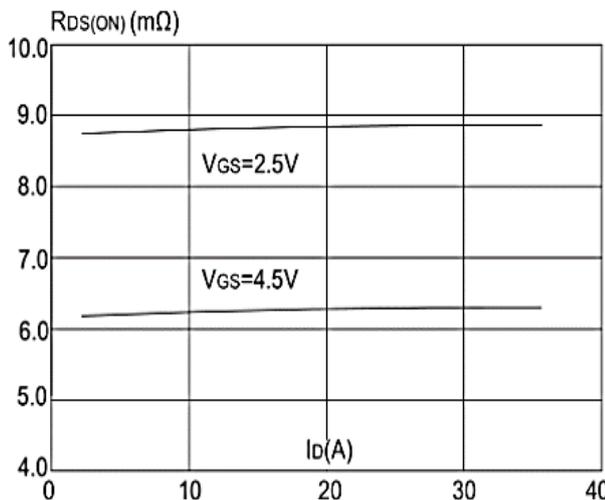


Figure 5: Gate Charge Characteristics

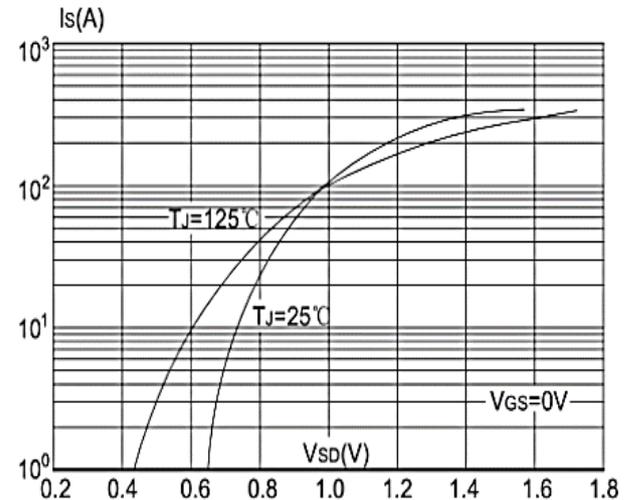


Figure 6: Capacitance Characteristics



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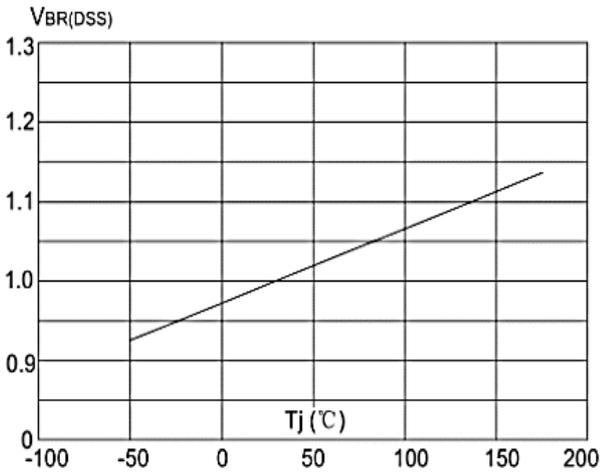


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

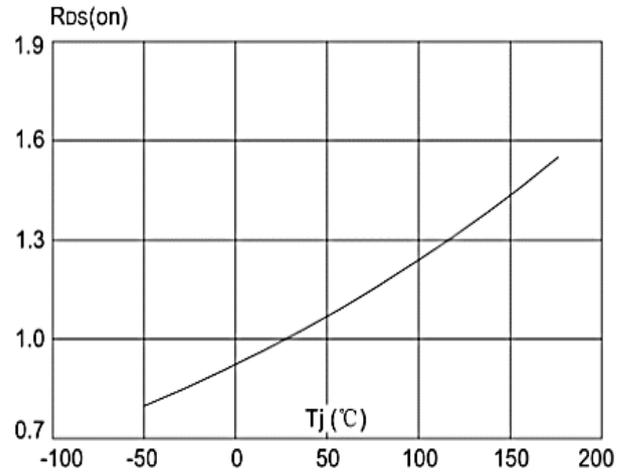


Figure 8: Normalized on Resistance vs. Junction Temperature

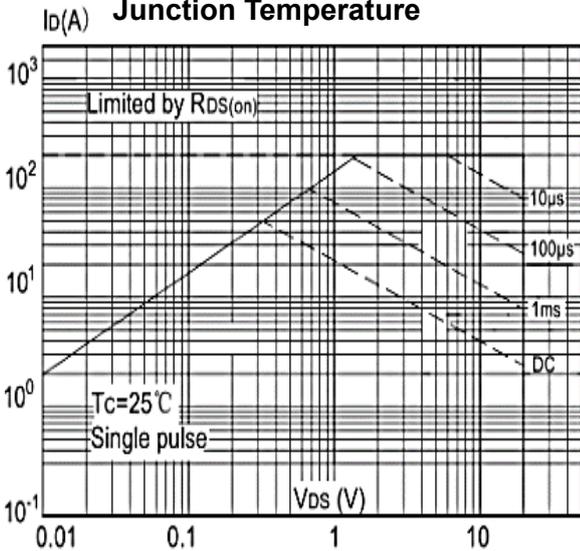


Figure 9: Maximum Safe Operating Area

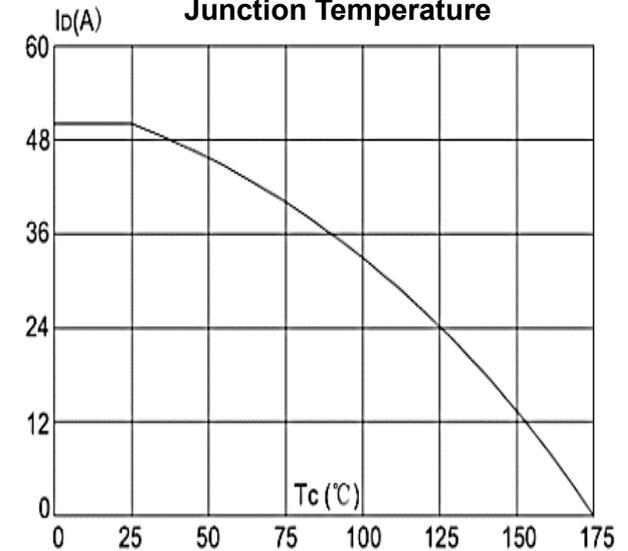


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

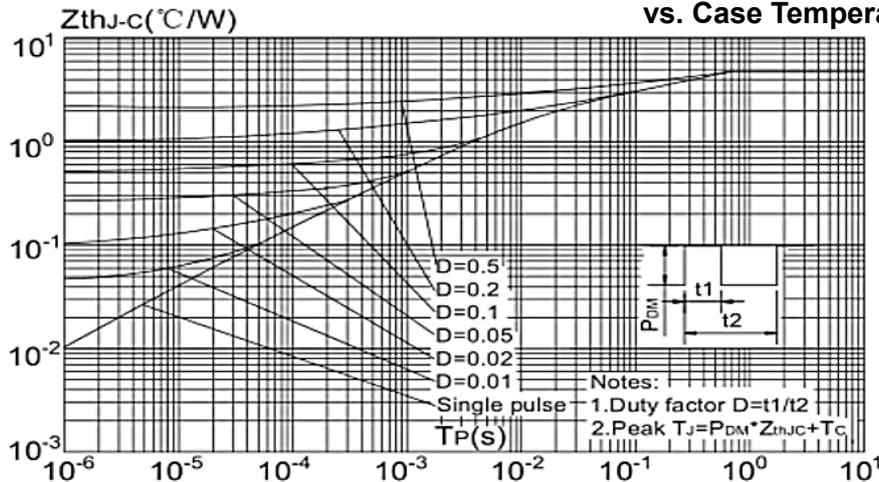


Figure 11: Maximum Effective Transient Thermal Impedance, Junction-to-Case

P-Typical Characteristics

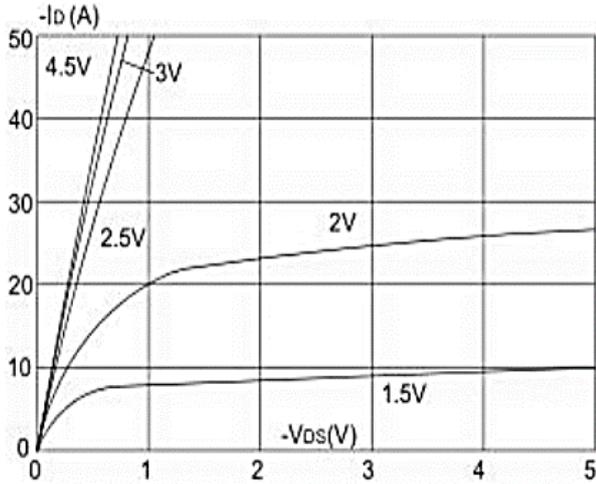


Figure 1: Output Characteristics

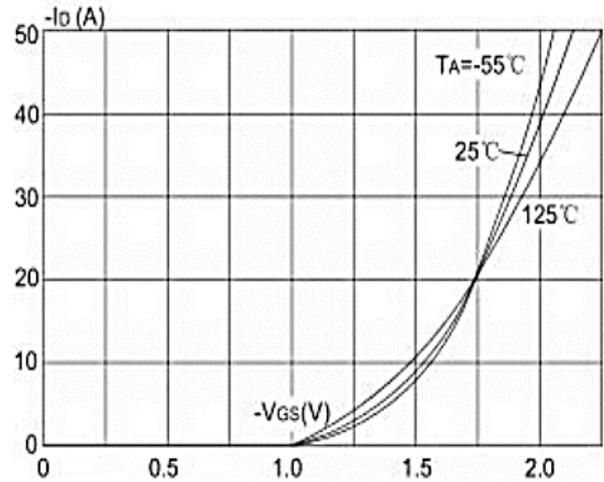


Figure 2: Typical Transfer Characteristics

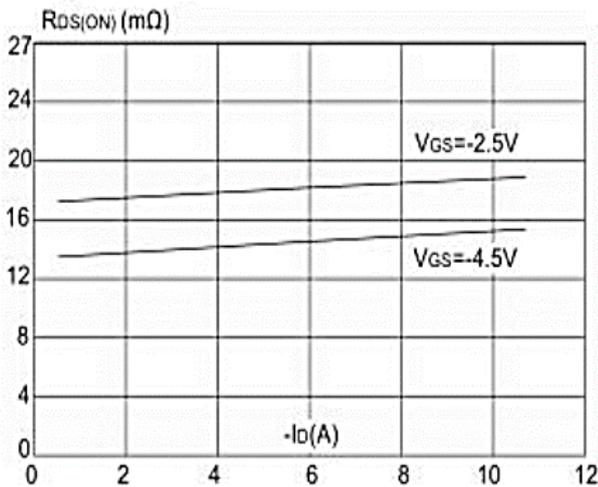


Figure 3: On-resistance vs. Drain Current

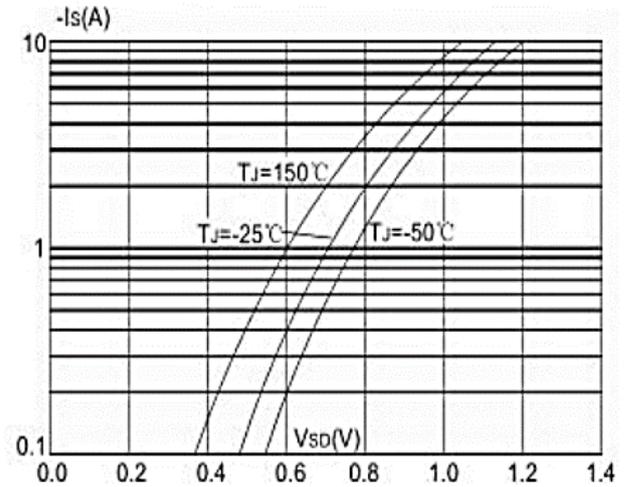


Figure 4: Body Diode Characteristics

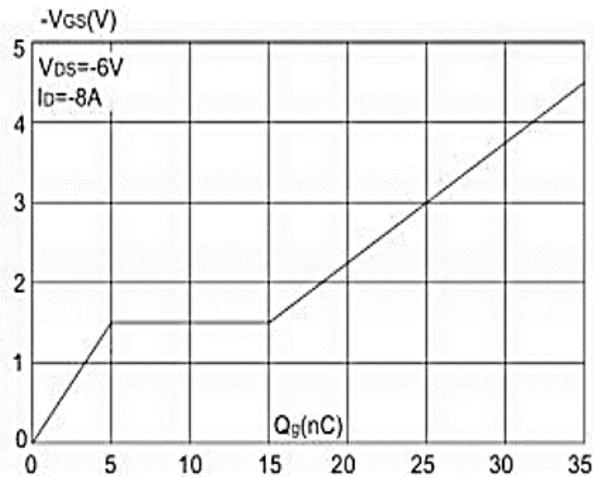


Figure 5: Gate Charge Characteristics

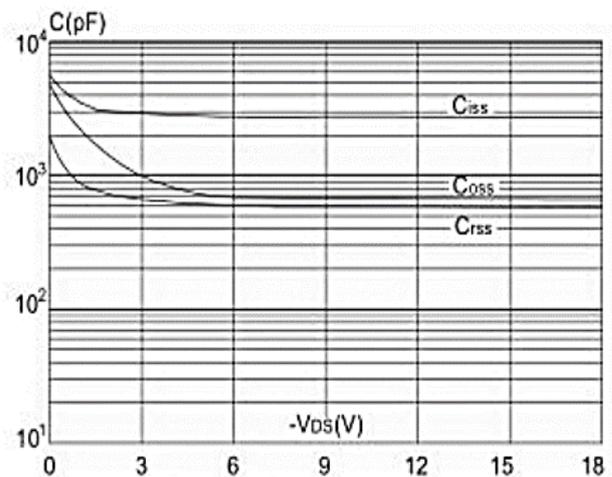


Figure 6: Capacitance Characteristics



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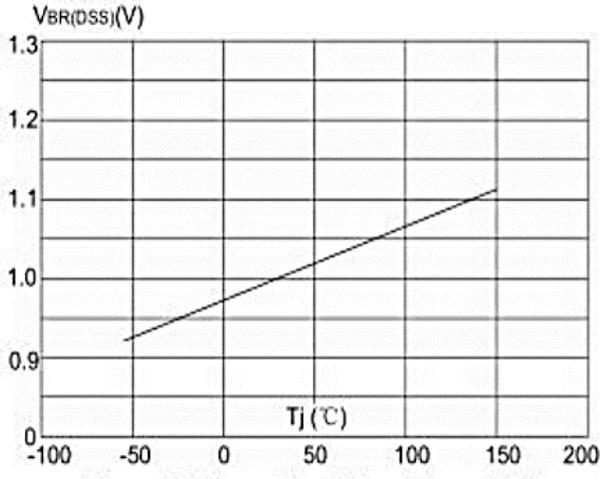


Figure 7: Normalized Breakdown Voltage vs. Junction Temperature

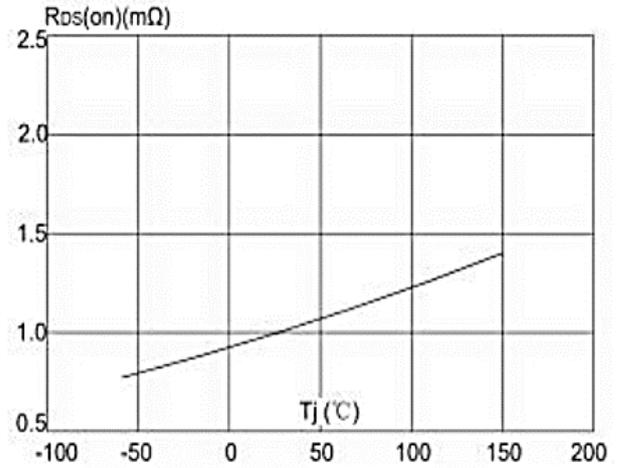


Figure 8: Normalized on Resistance vs. Junction Temperature

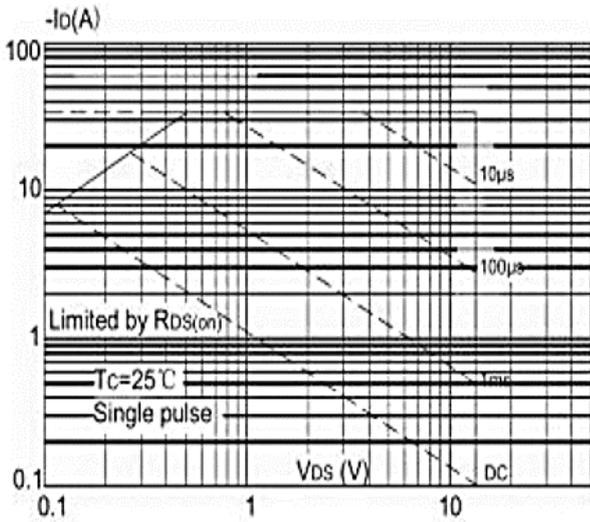


Figure 9: Maximum Safe Operating Area

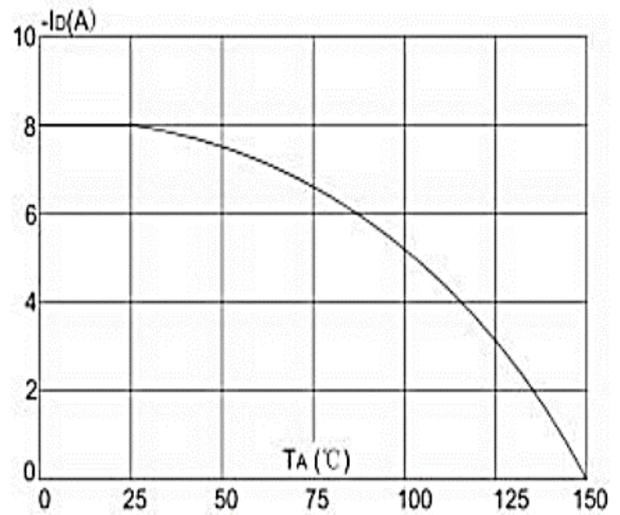


Figure 10: Maximum Continuous Drain Current vs. Case Temperature

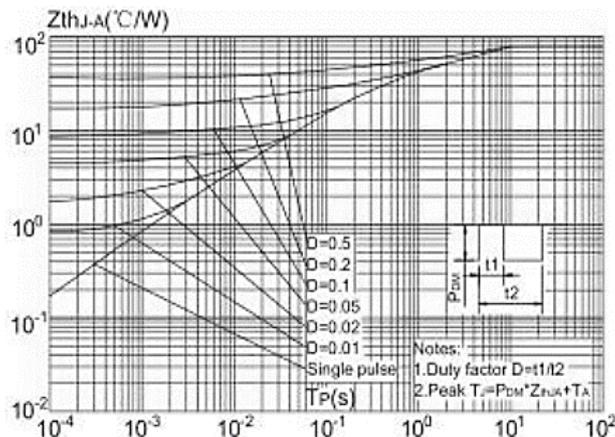
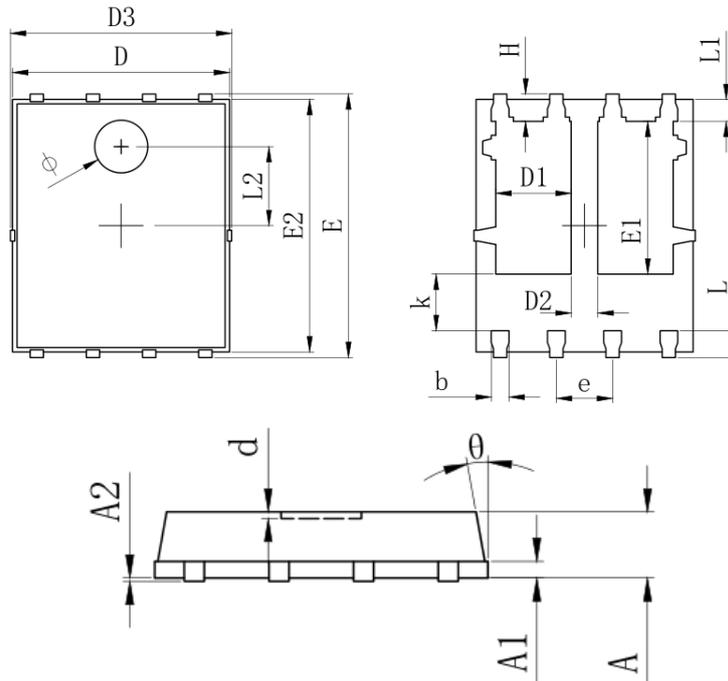


Figure.11: Maximum Effective Transient Thermal Impedance, Junction-to-Case



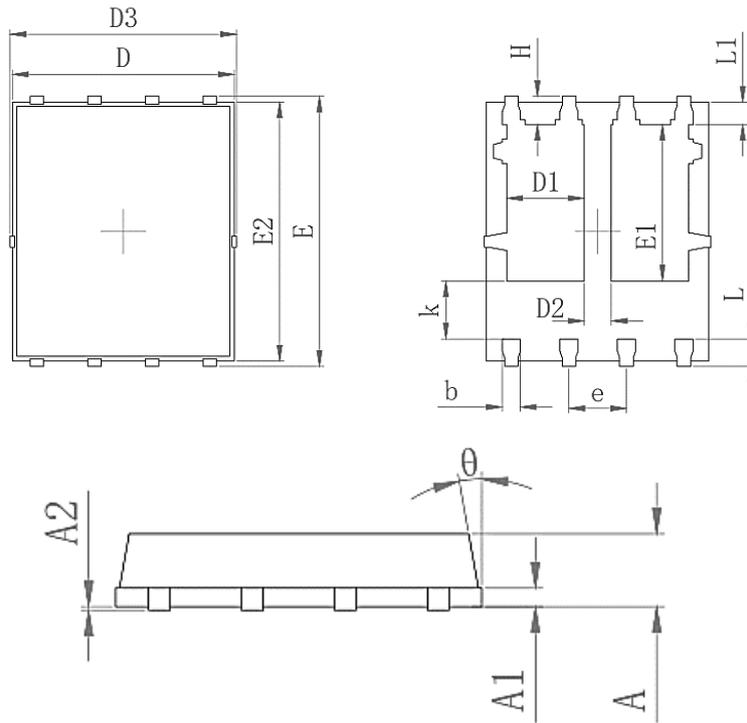
20V N+P-Channel Enhancement Mode MOSFET

Package Mechanical Data-PDFN5*6-8L-XZT Double (New)



Symbol	Common		
	mm		
	Mim	Typ	Max
A	0.900	1.000	1.100
A1	0.254		
A2	0-0.05		
D	4.824	4.900	4.976
D1	1.605	1.05	1.805
D2	0.500	0.600	0.700
D3	4.924	5.000	5.076
E	5.924	6.000	6.076
E1	3.375	3.475	3.575
E2	5.674	5.750	5.826
b	0.350	0.400	0.450
e	1.270		
L	0.534	0.610	0.686
L1	0.424	0.500	0.576
L2	1.800 REF		
K	1.190	1.29	1.390
H	0.549	0.625	0.701
θ	8°	10°	12°
d	0.100		

Package Mechanical Data-PDFN5*6-8L-XZT Double (Old)



Symbol	Common	
	mm	
	Mim	Max
A	0.900	1.100
A1	0.254	
A2	0-0.05	
D	4.824	4.976
D1	1.605	1.805
D2	0.500	0.700
D3	4.924	5.076
E	5.924	6.076
E1	3.375	3.575
E2	5.674	5.826
b	0.350	0.450
e	1.270	
L	0.534	0.686
L1	0.424	0.576
K	1.190	1.390
H	0.549	0.701
θ	8°	12°

20V N+P-Channel Enhancement Mode MOSFET**Attention**

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Edition	Date	Change
Rve1.0	2020/2/30	Initial release
Rve1.1	2022/2/30	Modified pack format

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