AIC1513

8-Channel Parallel High Voltage Driver

RoHS COMPLIANT

FEATURES

- High Voltage Driver with 8 Parallel Push-Pull Outputs
- Wide Supply Voltage Range (30V to 300V)
- Output Current per Channel is 40mA
- Output Rise Time Control by External Resistance
- Serial or Parallel Input
- N-channel MOSFET Outputs for Reduced Power Consumption

APPLICATIONS

- Drive of Capacitive Actuators
- Piezo Transducer Excitation
- Electro-Luminescent Displays

DESCRIPTION

The AIC1513 is a rigid, low-cost, general-purpose high-voltage driver IC with 8 high-voltage push-pull outputs. The device has been designed for harsh industrial requirements, allowing for a wide range of applications. The outputs can drive capacitive and resistive loads, such as piezoelectric transducers, electroluminescent devices, and micro-mechanical actuators. The maximum operating voltage is 300 V, and each output can handle currents of up to 40 mA.

External output resistors can be used to limit the maximum power dissipation of the device, allowing the outputs to be run in parallel. The IC allows for the use of an external resistor to set the switch-on time of the outputs as well as provides protected direct transistor gate inputs. The high-voltage push-pull outputs are well protected against possible latch-up by utilizing the bulk-drain diodes of the output MOSFETs and their full dielectric isolation.

The AIC1513's inputs can be configured to operate in either parallel or serial mode. In parallel mode, each high-voltage output is controlled by a dedicated input pin. In serial mode, internal shift registers and latches convert data provided by a clocked serial input stream to the high-voltage output. Additionally, several AIC1513 devices can be daisy-chained in serial mode if more than 8 parallel outputs are required.

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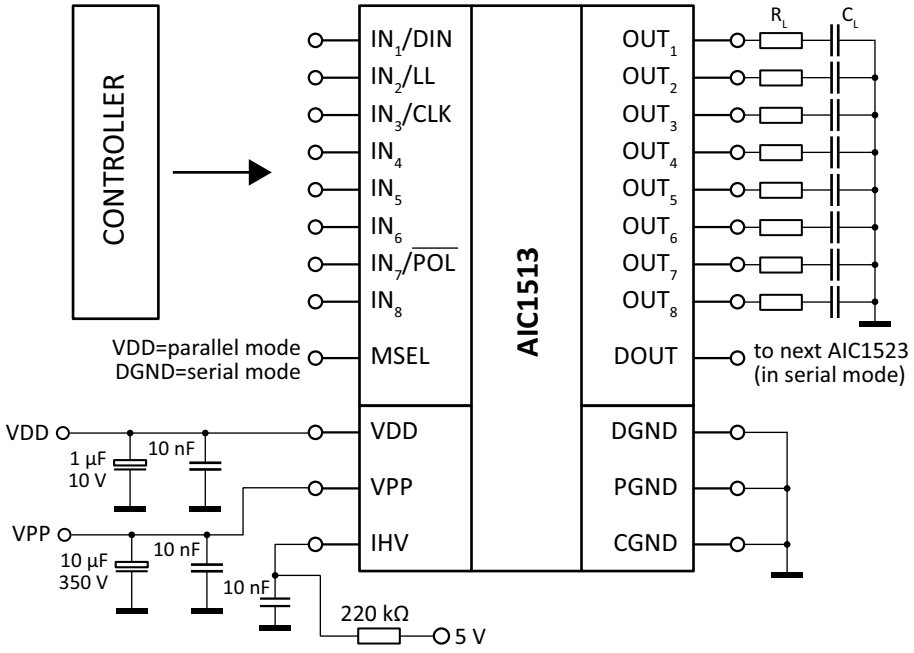
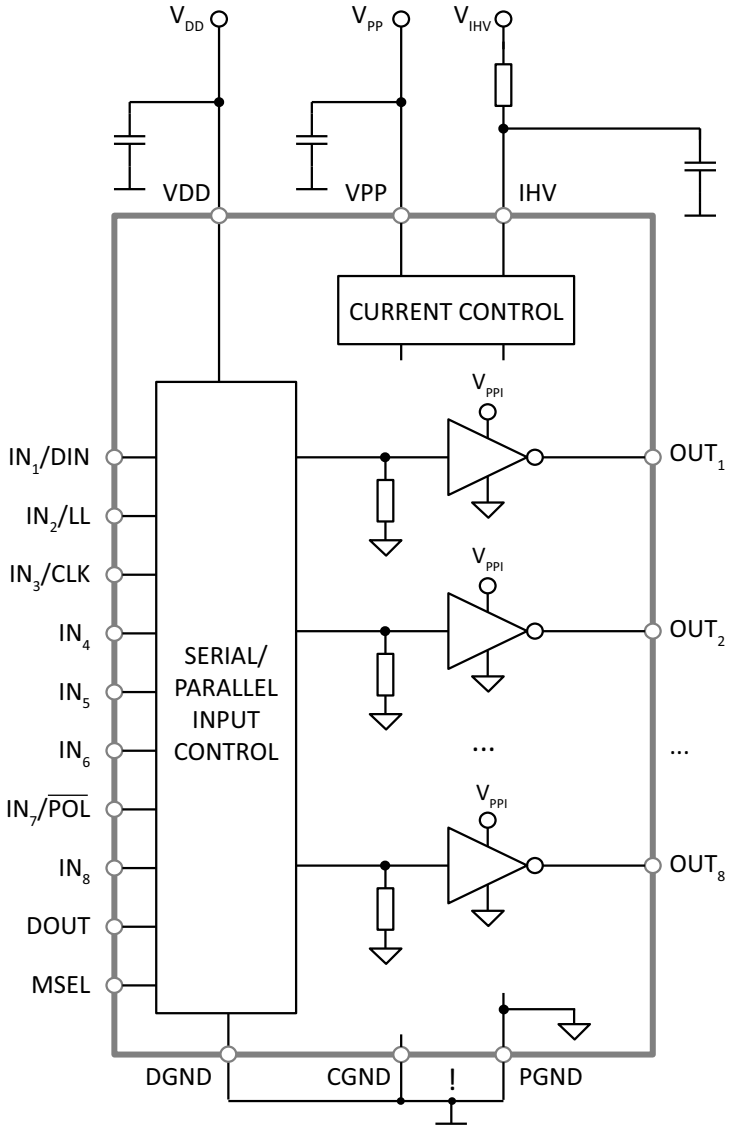
Figure 1: Common Application Circuit



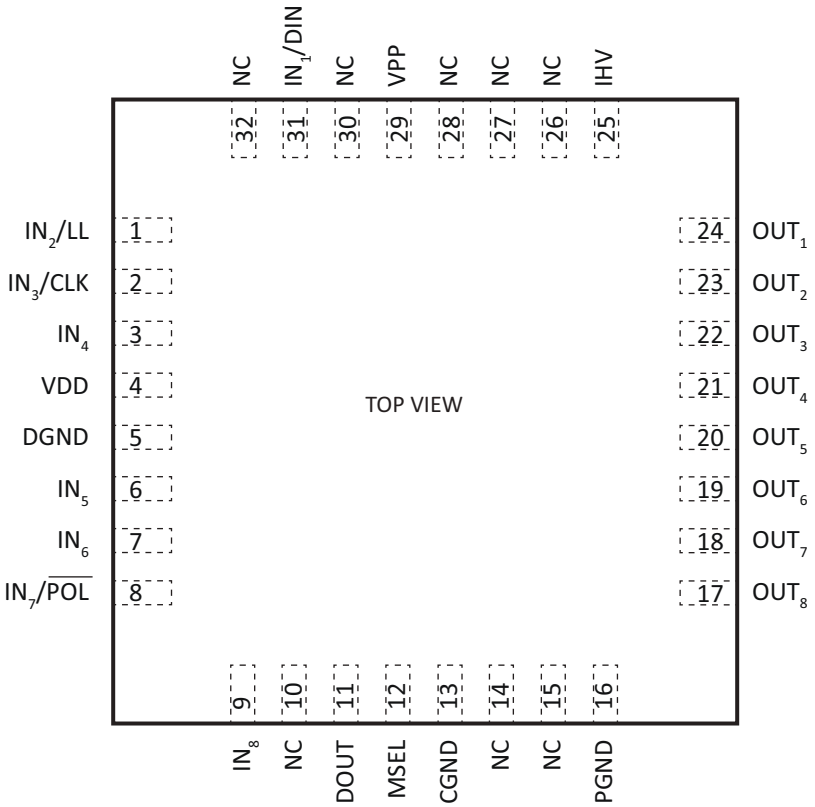
BLOCK DIAGRAM

Figure 2: Block Diagram



PINOUT AND PIN DESCRIPTION TABLE (32-PIN QFN)

Figure 3: Pinout (32-Pin QFN)



Pin Number	Name	Internal Pull Resistor	Description
1	IN_2/LL	Up	Parallel mode: Input 2 Serial mode: latch lock
2	IN_3/CLK	Down	Parallel mode: Input 3 Serial mode: serial data clock
3	IN_4	Down	Parallel mode: Input 4 Serial mode: no function
4	VDD		Supply voltage for digital input circuit
5	DGND		Ground for digital input circuit. Must be connected externally to PGND
6	IN_5	Down	Parallel mode: Input 5 Serial mode: no function
7	IN_6	Down	Parallel mode: Input 6 Serial mode: no function
8	$IN_7/\overline{POL}$	Up	Parallel mode: Input 7 Serial mode: output polarity inversion (active low)

Pin Number	Name	Internal Pull Resistor	Description
9	IN_8	Down	Parallel mode: Input 8 Serial mode: no function
10	NC		not connected
11	DOUT		Parallel mode: no function Serial mode: clocked data output (for daisy-chaining several devices)
12	MSEL	Down	Mode selection for input signals. Connect to VDD for parallel mode or DGND for serial mode.
13	CGND		Capacitive ground. Must be connected externally to PGND
14, 15	NC		not connected
16	PGND		Power ground of the 8 high voltage push-pull outputs
17	OUT_8		High voltage push-pull output 8
18	OUT_7		High voltage push-pull output 7
19	OUT_6		High voltage push-pull output 6
20	OUT_5		High voltage push-pull output 5
21	OUT_4		High voltage push-pull output 4
22	OUT_3		High voltage push-pull output 3
23	OUT_2		High voltage push-pull output 2
24	OUT_1		High voltage push-pull output 1
25	IHV		Input to connect an external resistor to adjust the switching speed of the high voltage push-pull outputs (if not necessary this pin can be left open)
26-28	NC		not connected
29	VPP		High voltage Supply
30	NC		not connected
31	IN_1/DIN	Down	Parallel mode: Input 1 Serial mode: clocked data input
32	NC		not connected

SPECIFICATIONS

Unless otherwise noted: T_A = 25°C, high voltage supply V_{PP} = 200 V, V_{DD}= 5 V, IHV connected to PGND.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Unit
High voltage supply	V_{PP}	0	320	V
Voltage supply digital input circuitry	V_{DD}		6	V
Output voltages	V_{OUT}	-0.3	V_{PP}	V
Slew rate of V_{PP}	W_{VPP}		160	V/ms
Input levels	V_{IN}	-0.3	V_{DD}	V
IHV input level	I_{IHV}	-100	300	µA
Continuous total power dissipation	P_{TOT}		600	mW
Storage temperature range	T_{stg}	-55	150	°C
Junction temperature range	T_J	-40	150	°C
Thermal resistance, junction to ambient	R_{thja}		35	°C/W

NORMAL OPERATING RANGE

Parameter	Symbol	Test Condition	Min	Typ	Max	Units
High voltage supply	V_{PP}		30		300	V
Output voltages	V_{OUT}		0		300	V
Voltage supply digital input circuitry	V_{DD}		3.0		5.5	V
High level input voltage[1]	V_{INH}	V_{DD}=3.3V	2.3		3.3	V
		V_{DD}=5.0V	3.5		5.0	V
Low level input voltage[1]	V_{INL}	V_{DD}=3.3V	0		0.6	V
		V_{DD}=5.0V	0		1.5	V
IHV input current	I_{IHV}	V_{DD}=3.3V	-0.1	25	50	µA
		V_{DD}=5.0V	-0.1	25	100	µA
Operating junction temperature	T_J		-40		125	°C
Operating temperature	T_A		-40		70	°C

1. The input voltage area between 30% and 70% of V_{DD} is forbidden with respect to total power dissipation

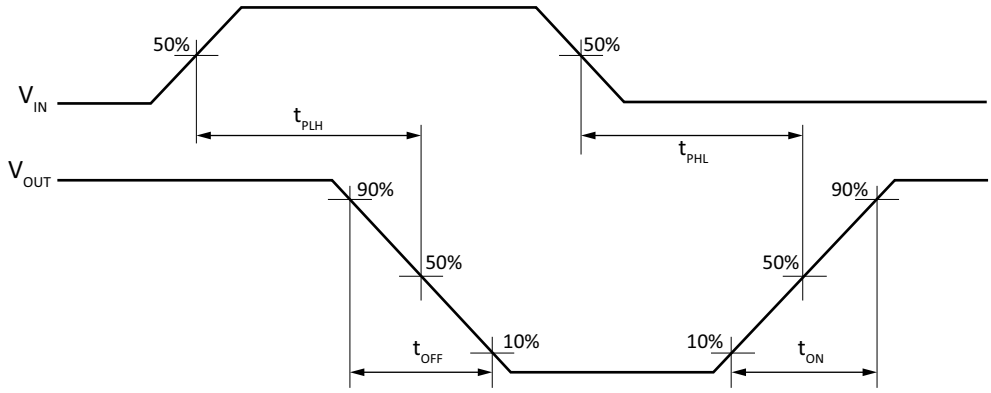
DC CHARACTERISTICS

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Input current for pins with pull-up or pull-down resistors when driven externally to the alternative logic level	$\|I_{PR}\|$	V_{DD}=3.3V		25	32	µA
		V_{DD}=5.0V		40	60	µA
Maximum current in digital input pins	I_{IN}	V_{IN} = 5.0V	-100		100	µA
ON resistance of sinking path	RDS(ON)L	I_{OUT}=-10 mA, V_{DD}=5.0V		250	1000	Ω
		I_{OUT}=-10 mA, V_{DD}=3.3V				Ω

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
ON resistance of sourcing path	RDS(ON)H	I_{OUT}=10 mA		350	1200	Ω
Minimum sink current of one output	$I_{OUTL,MIN}$	V_{PP}=30.0V, V_{DD}=5.0V	20			mA
		V_{PP}=30.0V, V_{DD}=3.3V	8			mA
Minimum source current of one output	$I_{OUTL,MIN}$	V_{PP}=30.0V	40			mA

AC CHARACTERISTICS

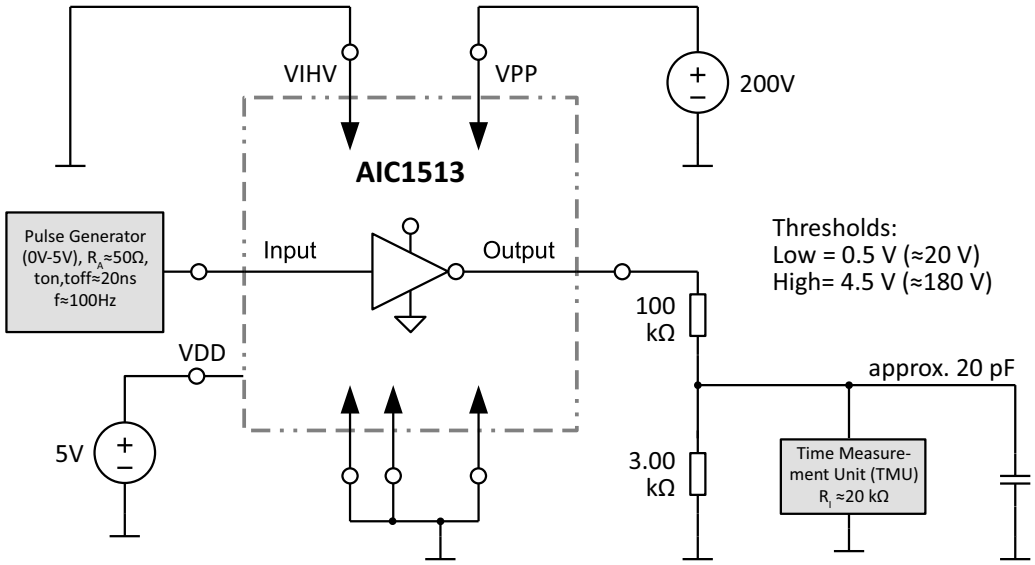
Figure 4: Switching Wave Forms



Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Propagation delay time, V_{IN} → low to high	t_{PLH}	V_{IN} = 0.0V - 5.0V C_L = 20pF		1		µs
Propagation delay time, V_{IN} → high to low	t_{PHL}	V_{IN} = 5.0V – 0.0V C_L = 20pF		15		µs
Output Fall time	t_{OFF}	V_{IN} = 0.0V – 3.3V C_L = 20pF V_{DD} = 3.3 V, IHV = 0 µA		0.5[1]		µs
		V_{IN} = 0.0V – 5.0V C_L = 20pF V_{DD} = 5.0 V, IHV = 0 µA		0.2		µs
Output Rise time	t_{ON}	V_{IN} = 5.0V – 0.0V C_L = 20pF	See Figure 10			µs

1. The output fall time increases for V_{DD}=3.3V once IHV is greater than 100 µA. See Figure 11 for details.

Figure 5: AC Characteristics Test Circuit



INPUT INTERFACE

AIC1513 can be configured for parallel or serial input based on voltage level at the MSEL pin. In parallel mode(MSEL=1), each high voltage output is controlled by a dedicated input pin. In serial mode (MSEL=0), internal latches convert data provided by a clocked serial input stream to the high voltage output. In serial mode, several AIC1513 can be daisy chained if more than 8 parallel outputs are required.

Figure 6: Digital Input Interface Block Diagram

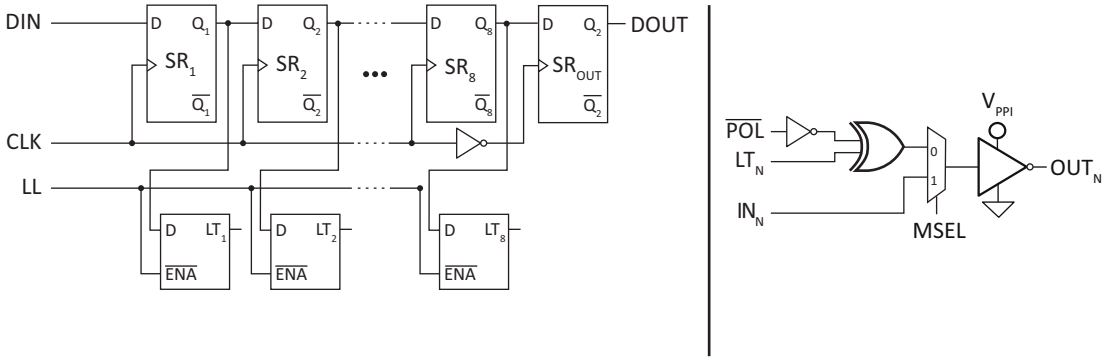
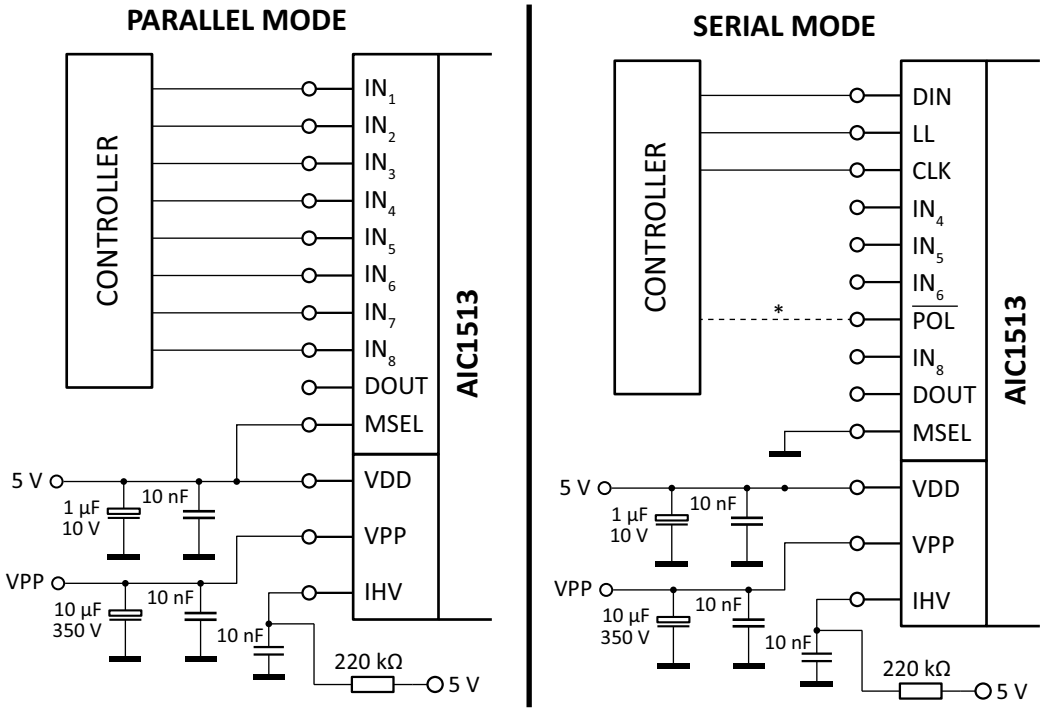


Figure 7: External connections when operating in parallel or serial mode



* can be directly connected to VDD or DGND if polarity control is not needed.

SERIAL MODE OPERATION (MSEL=0)

When operating in serial mode, data is stored in the shift register on the rising edge of the clock (CLK) signal. For daisy chaining, the output data will become valid half a clock cycle later, meaning at the falling edge of the CLK signal. The CLK signal is always edge sensitive.

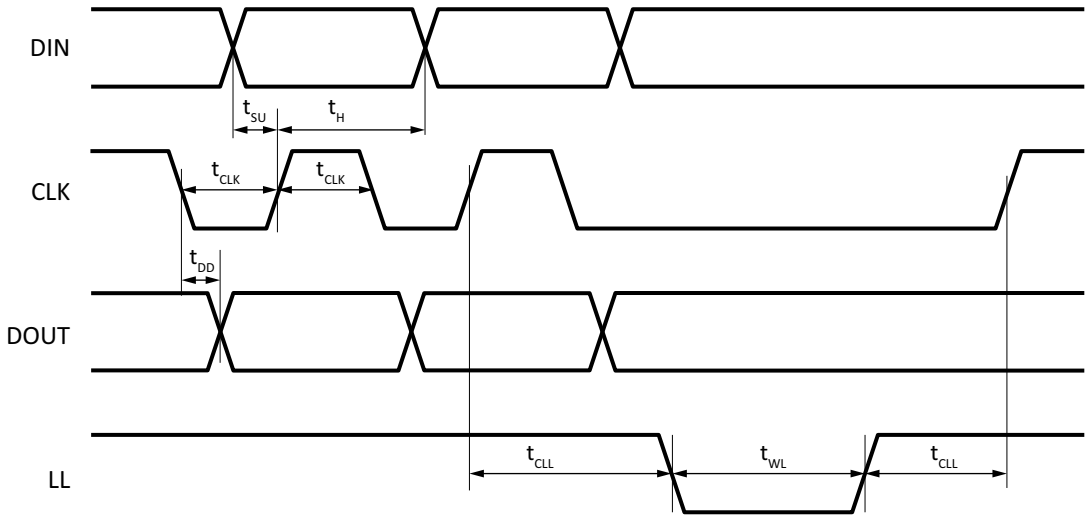
The output of the AIC1513 is controlled by the data stored in the latch registers. Data is copied from the input shift registers to the latch registers while the latch lock signal (LL) is pulled low. Please note that the LL signal is level sensitive. Thus, the AIC1513 can operate in both transparent and non-transparent serial modes. In non-transparent mode, data is shifted in on the rising edge of the clock signal while the latches are locked (with the latch lock signal LL set high). The output of the AIC1513 will not change during the shifting of the data. Once all data has been shifted in, the system can update the output of the AIC1513 by holding the clock signal at a steady level before unlocking the latches (by pulling the latch lock signal low). New data can then be provided to the device after the latches are locked again (LL is set back to high).

In transparent mode, the latches remain unlocked (with the signal LL set to low) while data is shifted in. Whenever new data is shifted in on the rising edge of the clock signal (CLK), it is also copied to the corresponding latch, updating the output of the AIC1513.

Mode	Function	DIN	CLK	LL	Shift Register (SR N)	Latch Register (LT N)
Non-Transparent	Load Shift Register	L/H	↗	H	N=1: $SR_{1,NEW}$ = DIN N>1: $SR_{N,NEW}$ = $SR_{N-1,PREV}$	no change
	Load Latch	X	H or L	↘ [1]	no change	LT_N = SR_N
Transparent	Load Shift and Latch Registers	L/H	↗	L	N=1: $SR_{1,NEW}$ = DIN N>1: $SR_{N,NEW}$ = $SR_{N-1,PREV}$	N=1: LT_1 = $SR_{1,NEW}$ (DIN) N>1: LT_N = $SR_{N,NEW}$

1. The data is loaded in the latch once the signal reaches the L level, as it is level sensitive.

Figure 8: Serial Input Mode Input Timing



Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Clock frequency	f_{CLK}			10		MHz
Clock width (high and low)	t_{CLK}			50		ns
Data setup time before clock rising edge	t_{SU}			25		ns
Data hold time after clock rising edge	t_H			30		ns
Latch lock to CLK setup time	t_{CLL}			100		ns
Latch write time	t_{WL}			50		ns
Clock falling edge to DOUT	t_{DD}			30		ns

PERFORMANCE GRAPHS

Figure 9: One Low Output Transistor with Respect to Input Voltage and Power Dissipation

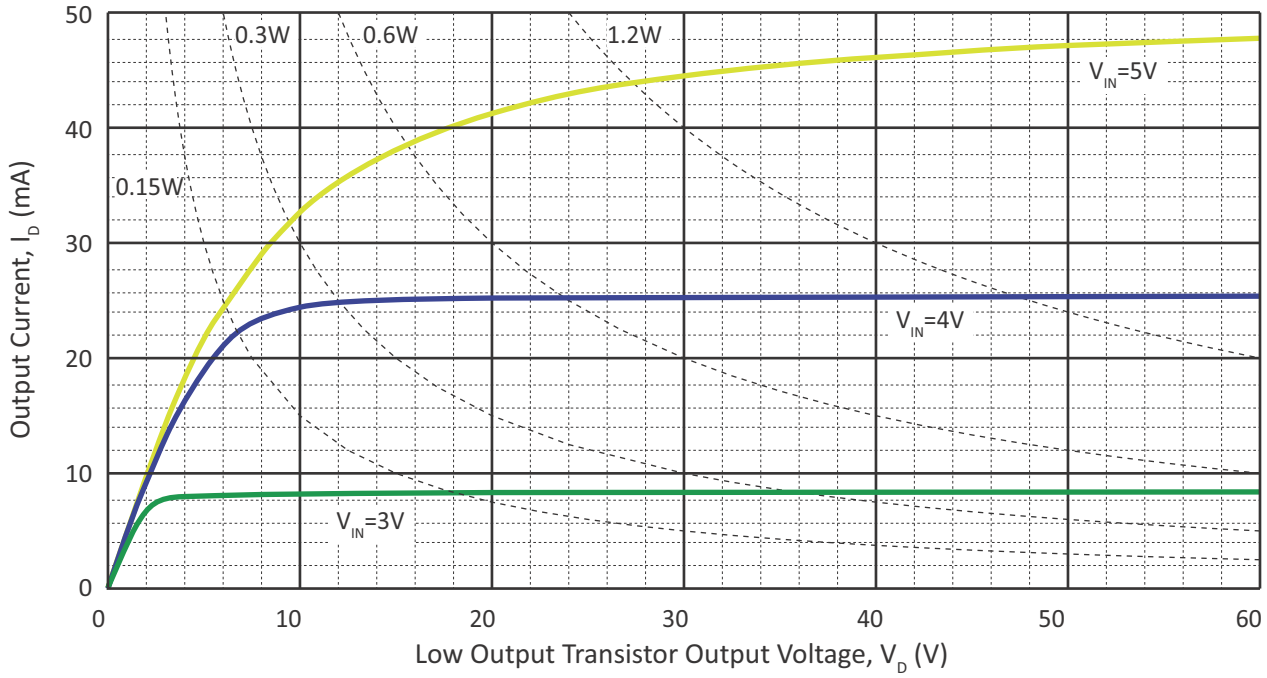


Figure 10: Rise Time vs IHV Current

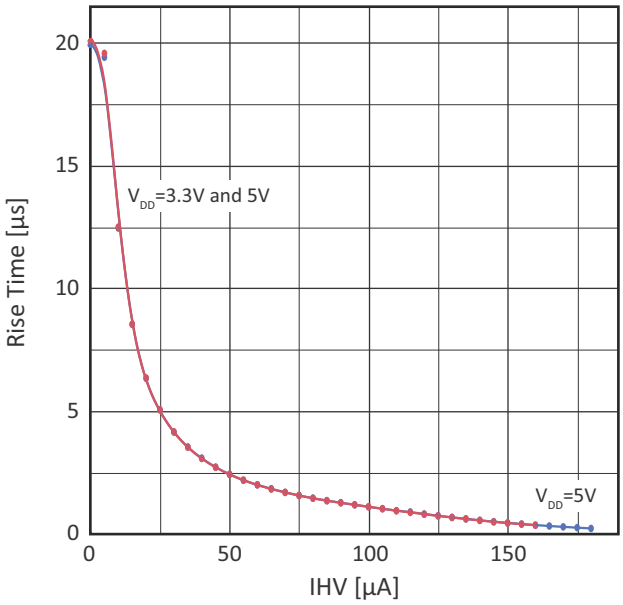
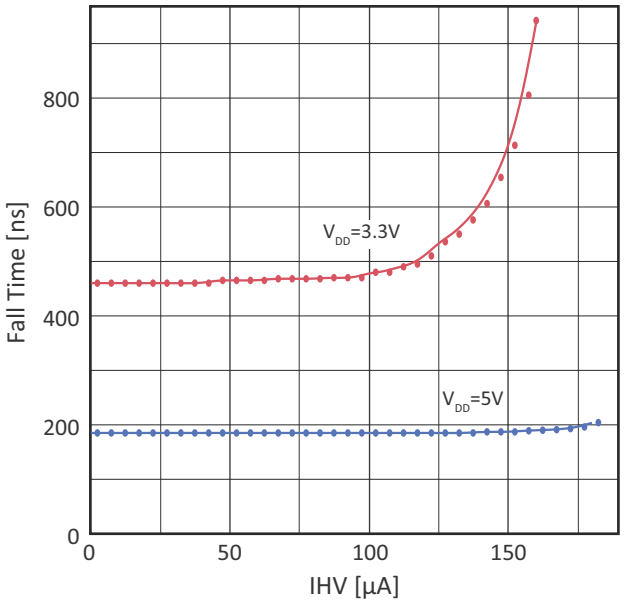


Figure 11: Fall Time vs IHV Current



APPLICATION

Figure 12: Example application with full bridge (basic circuit)

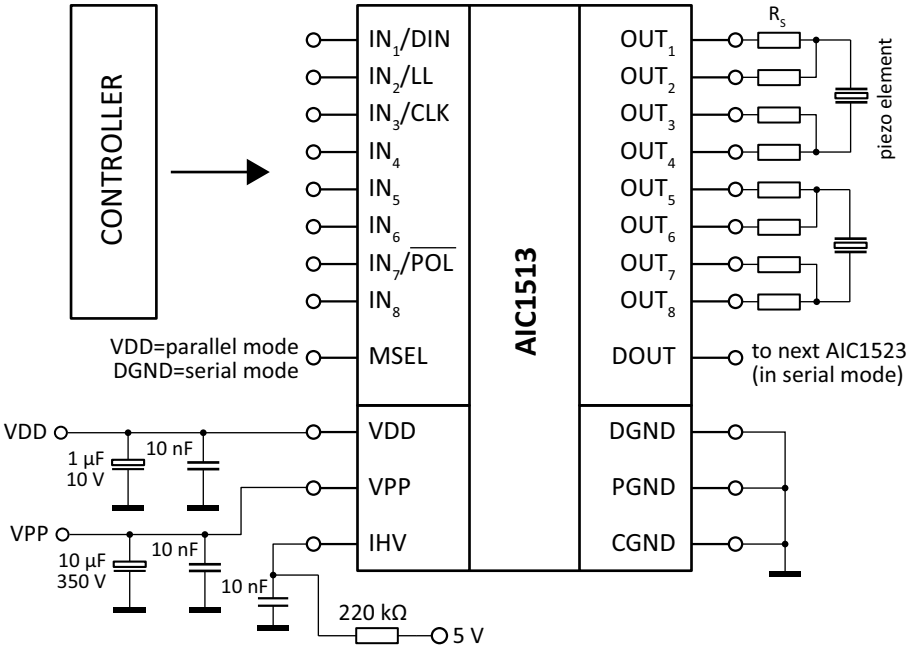
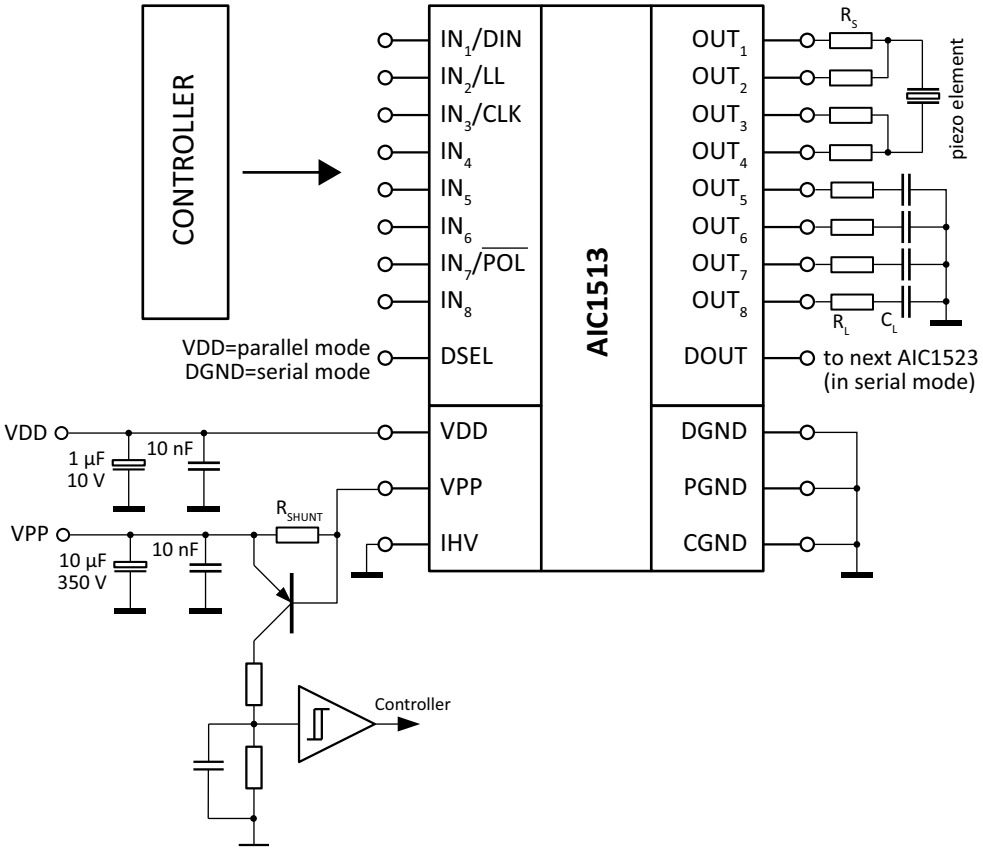


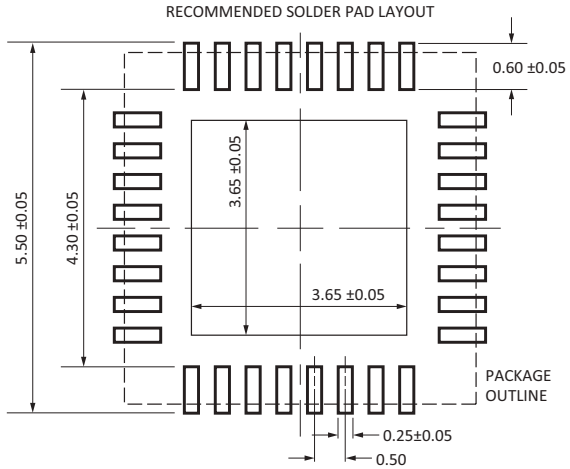
Figure 13: Example application with over current protection (basic circuit)



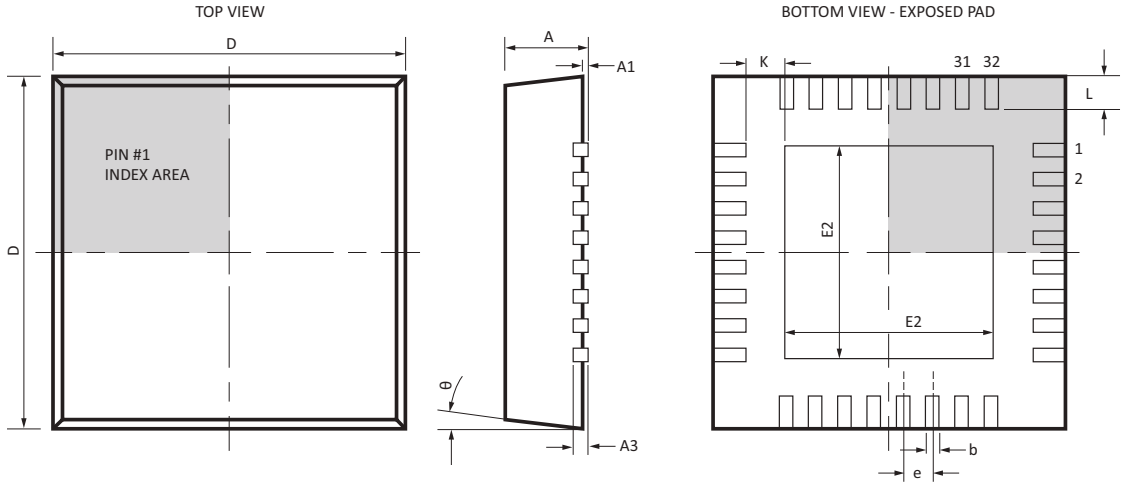
PACKAGE OPTIONS

Part Number	Apex Package Style	Description
AIC1513	ZK	32-pin VQFN package

32-PIN VQFN PACKAGE STYLE



NOTES:
1. DRAWING MO-220 (VHHD-4)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS IN MM
4. EXPOSED PAD SHALL BE SOLDER PLATED
5. SHADED AREA FOR ILLUSTRATION ONLY



Symbol	A	A1	A3	D	E2	e	b	L	K	θ
min	0.80	0			3.50		0.18	0.35	0.20	0°
nom	0.90	0.02	0.2	5.0	3.65	0.50	0.25	0.40		
max	1.00	0.05			3.80		0.30	0.45		14°

ESD PROTECTION

The Requirements for Handling Electrostatic Discharge Sensitive Devices are described in the JEDEC standard JESD625-A. Please note the following recommendations:

- When handling the device, operators must be grounded by wearing a for the purpose designed grounded wrist strap with at least 1MΩ resistance and direct skin contact.
- Operators must at all times wear ESD protective shoes or the area should be surrounded by for ESD protection intended floor mats.
- Opening of the protective ESD package that the device is delivered in must only occur at a properly equipped ESD workbench. The tape with which the package is held together must be cut with a sharp cutting tool, never pulled or ripped off.
- Any unnecessary contact with the device or any unprotected conductive points should be avoided.
- Work only with qualified and grounded tools, measuring equipment, casing and workbenches.
- Outside properly protected ESD-areas the device or any electronic assembly that it may be part of should always be transported in EGB/ESD shielded packaging.

STORAGE CONDITIONS

The AIC1513 corresponds to moisture sensitivity classification MSL3, according to JEDEC standard J-STD-020, and should be handled and stored according to J-STD-033.

NEED TECHNICAL HELP? CONTACT APEX SUPPORT!

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