*Click **here** to ask an associate for production status of specific part numbers.*

# MAX20499C/MAX20499D

# Automotive Single 16A/12A Step-Down Converter

## General Description

The MAX20499C/MAX20499D is a high-efficiency, synchronous step-down converter that operates with a 3.0V to 5.5V input voltage range and supplies a 0.5V to 1.275V output voltage range. The wide input/output voltage range and the ability to provide up to 16A peak output current make this device ideal for on-board point-of-load and post-regulation applications. The MAX20499C/MAX20499D achieves ±1.5% output error over load, line, and temperature ranges.

The MAX20499C/MAX20499D features a 2.2MHz fixed-frequency PWM mode for better noise immunity and load-transient response. The 2.2MHz frequency operation allows for the use of all ceramic capacitors and minimizes external components. The spread-spectrum frequency modulation option minimizes radiated electromagnetic emissions. Integrated low $R_{DS(ON)}$ switches improve efficiency at heavy loads and make layout simpler than discrete solutions.

The MAX20499C/MAX20499D is offered with factory-preset output voltage. The $I^2C$ interface supports dynamic voltage adjustment with programmable slew rates. Other features include programmable soft start, overcurrent, and overtemperature protections.

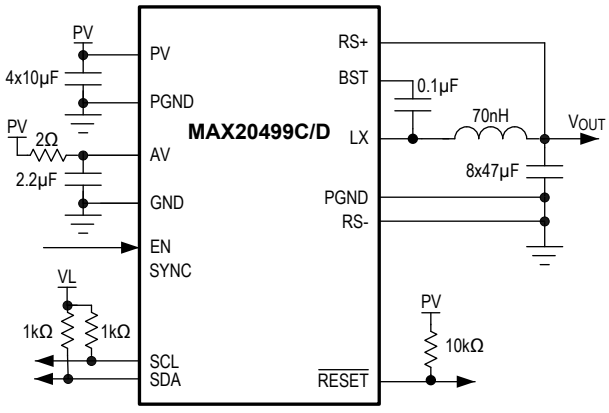
## Applications

- Automotive Entertainment Systems
- SoC Core Power

## Benefits and Features

- High-Efficiency DC-DC Converter
- Up to 16A Peak Output Current
  - MAX20499C: 16A
  - MAX20499D: 12A
- Differential Remote Voltage Sensing
- 3.0V to 5.5V Operating Supply Voltage
- $I^2C$-Controlled Output Voltage: 0.5V to 1.275V in 6.25mV Steps
- Excellent Load-Transient Performance
- Programmable Compensation
- 2.2MHz or 1.1MHz Operation
- ±1.5% Output Voltage Accuracy
- $\overline{\text{RESET}}$ Output
- Current-Mode, Forced-PWM Operation
- Overtemperature and Short-Circuit Protection
- 3.5mm x 4mm, 17-Pin, Side-Wettable FC2QFN
- -40°C to +125°C Grade 1 Automotive Temperature Range

## Simplified Block Diagram




*Ordering Information appears at end of data sheet.*

19-100981; Rev 5; 9/23

## TABLE OF CONTENTS

## TABLE OF CONTENTS (CONTINUED)

## LIST OF FIGURES

## LIST OF TABLES

## Absolute Maximum Ratings

PV, AV, EN, $\overline{\text{RESET}}$ to GND ..... -0.3V to +6V
SYNC, RS+, RS- to GND ..... -0.3V to AV+0.3V
SDA, SCL to GND ..... -0.3V to +6V
GND to PGND ..... -0.3V to +0.3V
BST to LX ..... -0.3V to +6V
LX to PGND ..... -0.3V to PV+0.3V
Output Short-Circuit Duration ..... Continuous

Continuous Power Dissipation ($T_A$ = +70°C)
17-FC2QFN (derate 28.26mW/°C > +70°C) .....2260.5mW
Operating Junction Temperature (Note 4) .....-40°C to +150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s).....+300°C
Soldering Temperature (reflow) .....+260°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Recommended Operating Conditions

| PARAMETER | SYMBOL | CONDITION | TYPICAL RANGE | UNIT |
|---|---|---|---|---|
| Ambient Temperature Range | | | -40 to +125 | °C |

**Note:** These limits are not guaranteed.

## Package Information

### 17 FC2QFN

| PACKAGE CODE | F173A4FY+1 |
|---|---|
| Outline Number | 21-100418 |
| Land Pattern Number | 90-100150 |
| **Thermal Resistance (Four-Layer Board):** | |
| Junction to Ambient ($\theta_{JA}$) | 35.4°C/W |
| Junction to Case ($\theta_{JC}$) | 7.8°C/W |
| **Thermal Resistance, EV Kit (Eight-Layer Board):** | |
| Junction to Ambient ($\theta_{JA}$) | 26°C/W |
| Junction to Case ($\theta_{JC}$) | 6°C/W |

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the EV kit, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

## Electrical Characteristics

($V_{PV}$ = $V_{AV}$ = 5V, $T_J$ = -40°C to +150°C, unless otherwise noted, typical values are at $T_A$ = +25°C under normal conditions, unless otherwise noted. (*Note 2*))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **SUPPLY VOLTAGE** | | | | | | |
| PV Supply Voltage | $V_{PV}$ | | 3.0 | | 5.5 | V |
| AV Supply Voltage | $V_{AV}$ | Fully operational | 3.0 | | 5.5 | V |

## Electrical Characteristics (continued)

($V_{PV}$ = $V_{AV}$ = 5V, $T_J$ = -40°C to +150°C, unless otherwise noted, typical values are at $T_A$ = +25°C under normal conditions, unless otherwise noted. (Note 2))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| UVLO | | Rising | | 2.7 | 2.9 | V |
| | | Falling | 2.45 | 2.6 | | |
| Supply Current | $I_{IN}$ | EN = high, $I_{OUT}$ = 0mA, no switching | | 2.5 | | mA |
| Shutdown Supply Current | $I_{IN}$ | EN = low, $T_A$ ≤ +125°C | | 3 | 30 | µA |
| **PWM FREQUENCY** | | | | | | |
| PWM Switching Frequency | $f_{SW}$ | Internally generated, CONFIG.FSW = 0 | 2.0 | 2.2 | 2.4 | MHz |
| | | Internally generated, CONFIG.FSW = 1 | 1.0 | 1.1 | 1.2 | |
| Spread Spectrum | | CONFIG.SS = 1 | | +3 | | % |
| **OUTPUT VOLTAGE** | | | | | | |
| Voltage Accuracy | $V_{OUT}$ | $I_{LOAD}$ = 0A to IMAX, $V_{PV}$ = 3.3V, $V_{OUT}$ = 1.0V | -1 | | +1 | % |
| | | $I_{LOAD}$ = 0A to IMAX, 3.0V ≤ $V_{PV}$ ≤ 5.5V, 0.80V to 1.275V | -1.5 | | +1.5 | |
| | | $I_{LOAD}$ = 0A to IMAX, 3.0V ≤ $V_{PV}$ ≤ 5.5V, 0.50V to 0.79V | -15 | | 15 | mV |
| OV Threshold | | | 106 | 108 | 110 | % |
| UV Threshold | | | 90 | 92 | 94 | % |
| UV/OV Propagation Delay | | $V_{OUT}$ = $V_{SET}$ | | 15 | | µs |
| Active Timeout Period | | Option 1 (32768 Clocks) | | 14.9 | | ms |
| | | Option 2 (16384 Clocks) | | 7.4 | | |
| | | Option 3 (8192 Clocks) (default) | | 3.7 | | |
| | | Option 4 (1024 Clocks) | | 0.5 | | |
| **POWER FET** | | | | | | |
| HS NMOS On-Resistance | | $V_{PV}$ = $V_{AV}$ = 5V, $I_{LX}$ = 1A | | 6.8 | | mΩ |
| LS NMOS On-Resistance | | $V_{PV}$ = $V_{AV}$ = 5V, $I_{LX}$ = 1A | | 4 | | mΩ |
| HS NMOS Current-Limit Threshold | | MAX20499D (12A) (Note 3) | 15 | 18 | 22 | A |
| | | MAX20499C (16A) (Note 3) | 20 | 24 | 28 | |
| LX Leakage Current | | $V_{PV}$ = $V_{AV}$ = 5V, LX = PGND or PV, $T_A$ = 25ºC | | 1 | | µA |
| LX Discharge Resistance | | $V_{EN}$ = 0V, $I_{LOAD}$ = 10mA | | 11 | | Ω |
| **THERMAL OVERLOAD** | | | | | | |
| Thermal Shutdown Temperature | | $T_J$ rising | | 165 | | °C |
| Hysteresis | | | | 15 | | °C |
| **DIGITAL OUTPUT ($\overline{\text{RESET}}$, SYNC, SDA)** | | | | | | |
| $\overline{\text{RESET}}$ Output Low Level | | 3.0V ≤ $V_{PV}$ ≤ 5.5V, 3.0V ≤ $V_{AV}$ ≤ 5.5V, $I_{SINK}$ = 2mA | | | 0.4 | V |

## Electrical Characteristics (continued)

($V_{PV}$ = $V_{AV}$ = 5V, $T_J$ = -40°C to +150°C, unless otherwise noted, typical values are at $T_A$ = +25°C under normal conditions, unless otherwise noted. (*Note 2*))

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $\overline{RESET}$ High Leakage current | | | | 1 | | µA |
| SYNC Output High Level | $V_{OH}$ | $I_{SOURCE}$ = 3mA | 4.2 | | | V |
| SYNC Output Low Level | $V_{OL}$ | $I_{SINK}$ = 3mA | | | 0.4 | V |
| SDA Ouput Low Level | $V_{OL\_SDA}$ | $I_{SINK}$ = 4mA | | | 0.4 | V |
| **I²C INTERFACE** | | | | | | |
| Clock Frequency | | | | | 1.0 | MHz |
| Setup Time (Repeated) START | $t_{SU:STA}$ | | 260 | | | ns |
| HOLD Time (Repeated) START | $t_{HD:STA}$ | | 260 | | | ns |
| SCL Low Time | $t_{LOW}$ | | 500 | | | ns |
| SCL High Time | $t_{HIGH}$ | | 260 | | | ns |
| DATA Setup Time | $t_{SU:DAT}$ | | 50 | | | ns |
| DATA Hold Time | $t_{HD:DAT}$ | | 0 | | | ns |
| Setup Time for STOP Condition | $t_{SU:STO}$ | | 260 | | | ns |
| Spike Suppression | | | | 20 | | ns |
| **DIGITAL INPUT (SYNC)** | | | | | | |
| Input High Level | $V_{IH}$ | | 1.8 | | | V |
| Input Low Level | $V_{IL}$ | | | | 0.4 | V |
| SYNC Input Pulldown | | | | 100 | | kΩ |
| SYNC Input Frequency Range | | $f_{OSC}$ = 2.2MHz | 1.8 | | 2.6 | MHz |
| | | $f_{OSC}$ = 1.1MHz | 0.9 | | 1.3 | |
| **DIGITAL INPUT (EN, SDA, SCL)** | | | | | | |
| Input High Level | | | 1.3 | | | V |
| Input Low Level | | | | | 0.5 | V |
| Input Hysteresis | | | | 50 | | mV |
| Input Leakage Current | | | | 1 | | µA |

**Note 1:** All units are 100% production tested at +25°C. All temperature limits are guaranteed by design and characterization.

**Note 2:** The device is designed to operate under in cabin automotive temperature profiles similar to *Typical Operating Characteristics* 1.

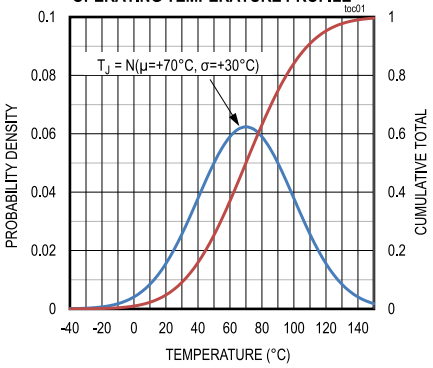
**Note 3:** Based on ATE measurements using scaled currents.

**Note 4:** The device is designed for continuous operation up to $T_J$ = 125°C for 95,000 hours and $T_J$ = 150°C for 5,000 hours.

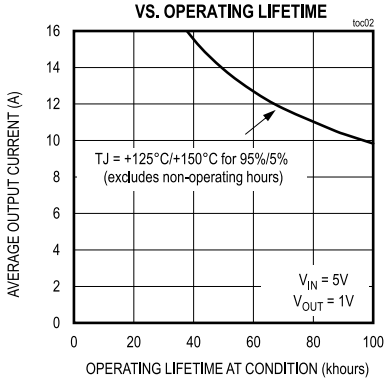
## Typical Operating Characteristics

($V_{PV}$ = $V_{AV}$ = 5V; $T_A$= +25°C unless otherwise noted)

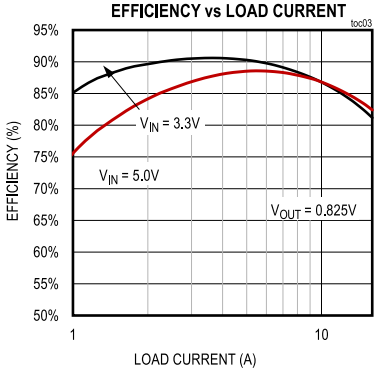
OPERATING TEMPERATURE PROFILE



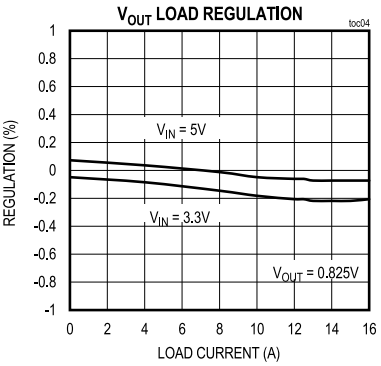

AVERAGE OUTPUT CURRENT VS. OPERATING LIFETIME



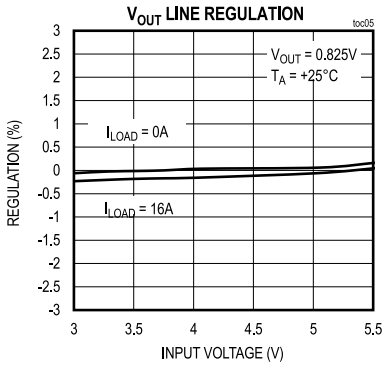

EFFICIENCY vs LOAD CURRENT



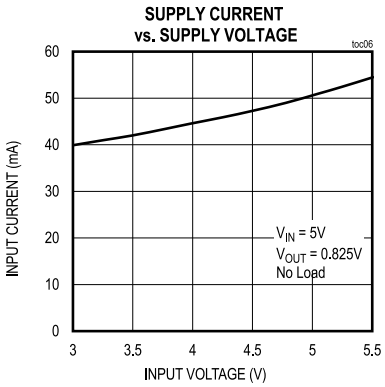

$V_{OUT}$ LOAD REGULATION



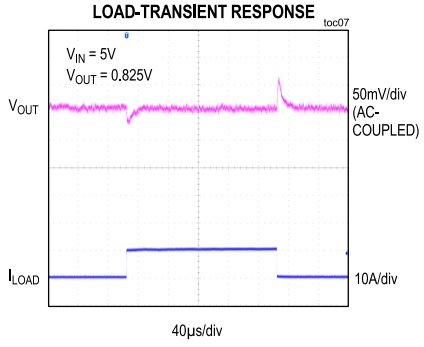

$V_{OUT}$ LINE REGULATION



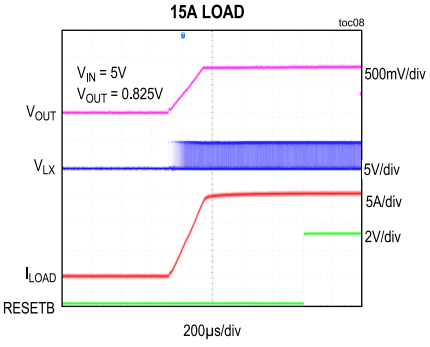

SUPPLY CURRENT vs. SUPPLY VOLTAGE



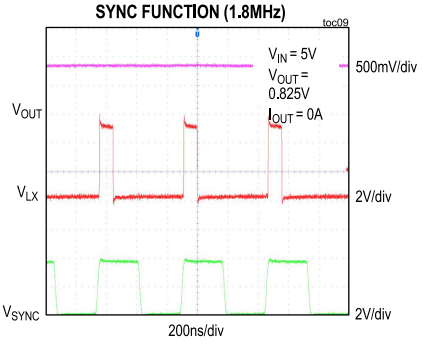

LOAD-TRANSIENT RESPONSE




START-UP BEHAVIOR 15A LOAD

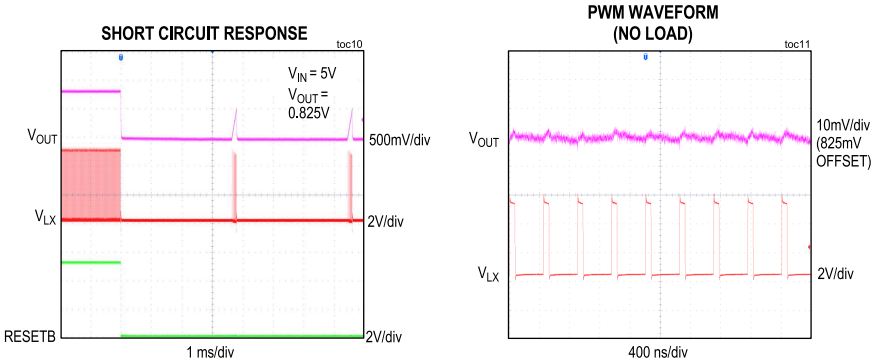



SYNC FUNCTION (1.8MHz)



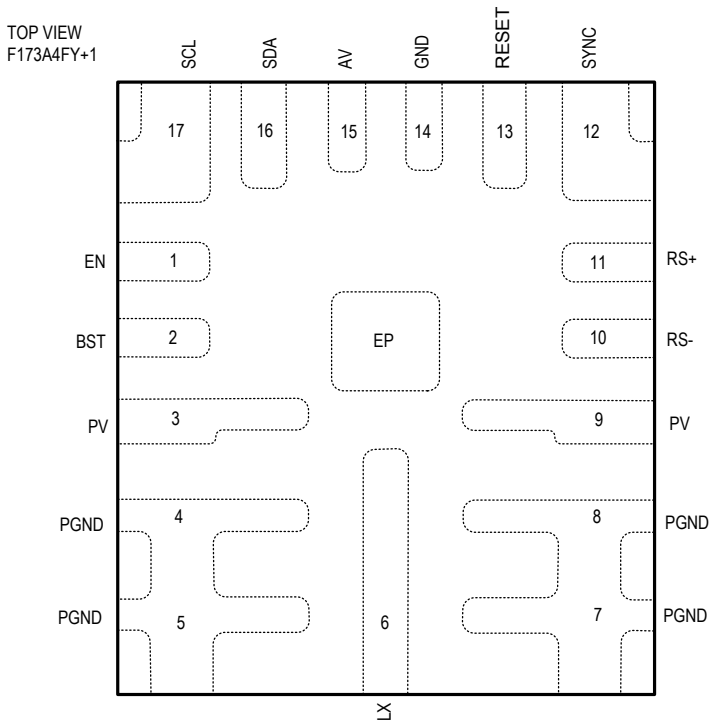
## Typical Operating Characteristics (continued)

($V_{PV}$ = $V_{AV}$ = 5V; $T_A$= +25°C unless otherwise noted)




## Pin Configuration

### Top View

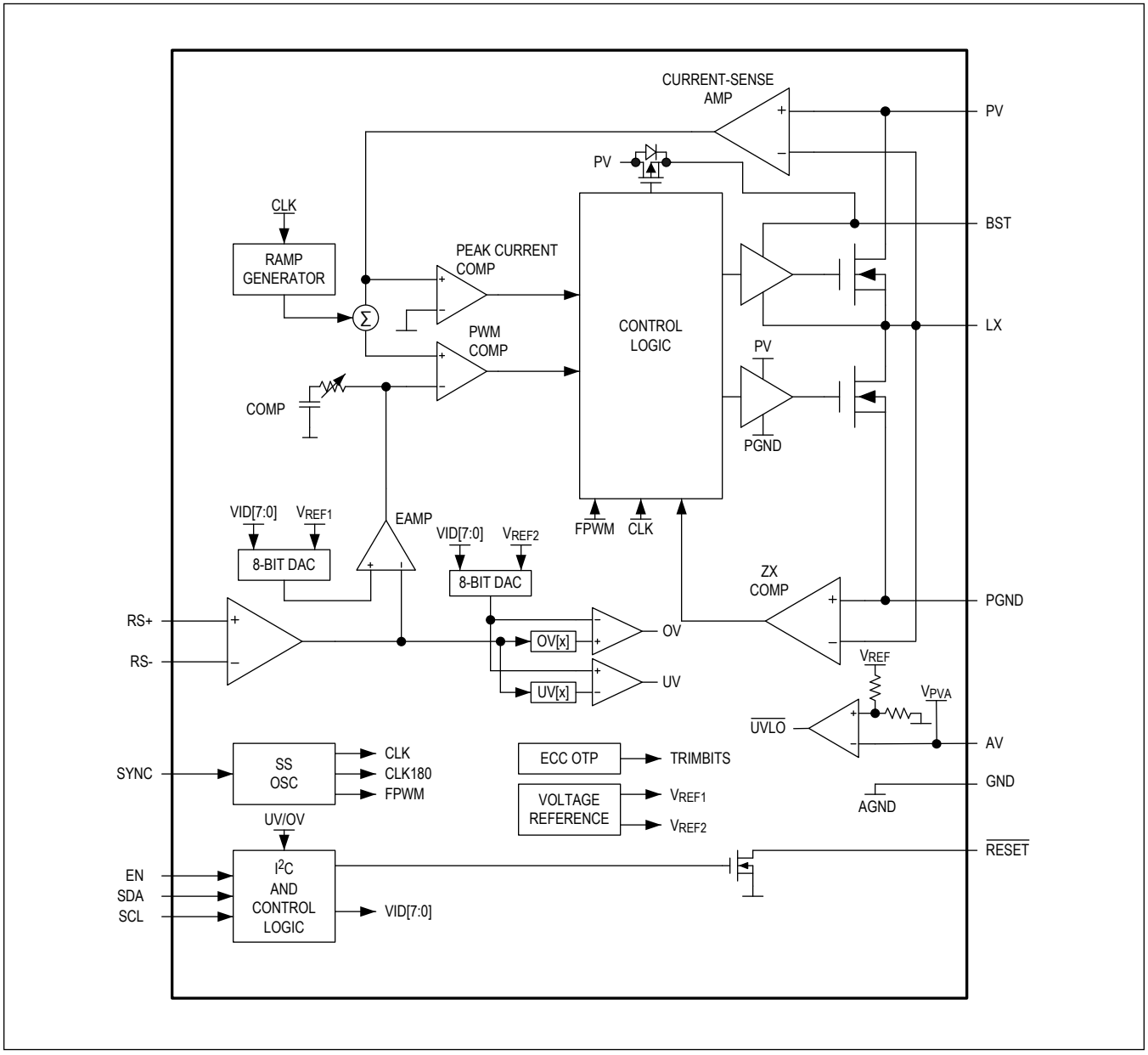


## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | EN | Active-High Enable Input. Drive EN high for normal operation. On the rising edge, the device enters soft-start. On the falling edge, the device enters soft-shutdown. |
| 2 | BST | Boost Supply |
| 3,9 | PV | Power Input Supply. Connect two 10µF or larger ceramic capacitor from PV to PGND. Connect all PV pins together. |
| 4,5,7,8 | PGND | Power Ground. Connect all PGND pins together. |
| 6 | LX | Inductor Connection. Connect LX to the switched side of the inductor. Connect all LX pins together. |
| 10 | RS- | Buck regulator remote voltage sense negative input. The common-mode range of this input is ±0.3V. |
| 11 | RS+ | Buck regulator remote voltage sense positive input. The resistance from RS+ to the remote sense connection should be kept to 2Ω or less to prevent the input current from affecting the output accuracy. The input current is +100µA (typ). |
| 12 | SYNC | SYNC I/O. Connect SYNC to AV/GND or an external clock to enable fixed-frequency forced-PWM-mode operation. When configured as an output (*CONFIG.SO[1:0]* = 2'b10), connect SYNC to other devices' SYNC inputs. |
| 13 | $\overline{\text{RESET}}$ | Open-Drain $\overline{\text{RESET}}$ Output. This output remains low for the programmed hold time after the output has reached its regulation level (see the *Electrical Characteristics* table). To obtain a logic signal, pull up RESET with an external resistor. |
| 14 | GND | Analog Ground |
| 15 | AV | Analog Input Supply |
| 16 | SDA | $I^2C$ Data I/O |
| 17 | SCL | $I^2C$ Clock Input |
| — | EP | Exposed Pad. Internally connected to PV. |

## Functional Diagrams

### Internal Block Diagram



## Detailed Description

The MAX20499C/MAX20499D is a high-efficiency, synchronous step-down converter that operates with a 3.0V to 5.5V input voltage range and provides a 0.50V to 1.275V output voltage range. The device delivers up to 16A of load current and regulates the output voltage over load, line, and temperature ranges.

Optional spread-spectrum frequency modulation minimizes radiated electromagnetic emissions due to the switching frequency. The I²C-programmable I/O (SYNC) enables system synchronization.

Integrated low $R_{DS(ON)}$ switches help improve efficiency at heavy loads and make the layout a much simpler task with respect to discrete solutions. The device is offered with a factory-preset output voltage that is dynamically adjustable through the I²C interface. The output voltage can be set to any desired values between 0.5V to 1.275V in 6.25mV steps.

Additional features include adjustable soft start, power-good delay, DVS rate, overcurrent, and overtemperature protections. Consult the factory for detailed register set information. See the *Internal Block Diagram*.

### I²C Interface

The MAX20499C/MAX20499D features an I²C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the MAX20499C/MAX20499D and the master at clock rates up to 1MHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 1 shows the 2-wire interface timing diagram.

A master device communicates to the MAX20499C/MAX20499D by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX20499C/MAX20499D SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA bus. The MAX20499C/MAX20499D SCL line operates as an input only. A pullup resistor greater than 500Ω is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation even on a noisy bus.

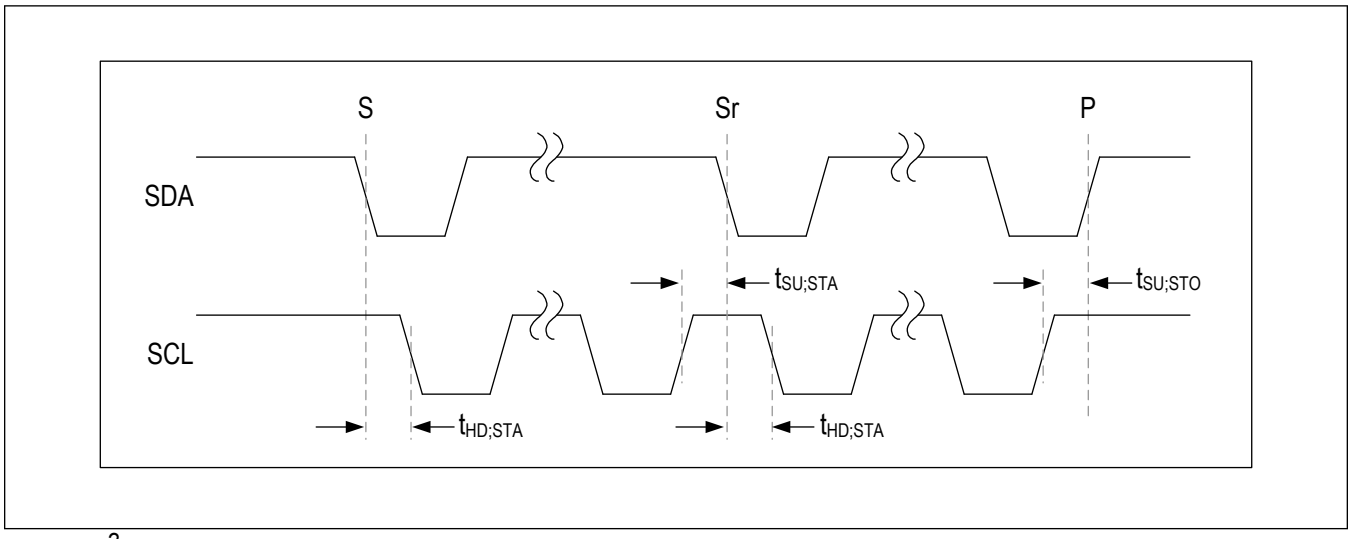



*Figure 1. I²C Timing Diagram*

#### Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals. SDA and SCL idle high when the I²C bus is not busy.

### STOP and START Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 1). A START (S) condition from the master signals the beginning of a transmission to the MAX20499C/MAX20499D. The master terminates transmission and frees the bus by issuing a STOP (P) condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

### Early STOP condition

The MAX20499C/MAX20499D recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

### Clock Stretching

In general, the clock signal generation for the $I^2C$ bus is the responsibility of the master device. The $I^2C$ specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX20499C/MAX20499D does not use any form of clock stretching to hold down the clock line.

### $I^2C$ General Call Address

The MAX20499C/MAX20499D does not implement the $I^2C$ specifications general call address. If the MAX20499C/MAX20499D detects the general call address (0b0000_0000), it will not issue an acknowledgment.

### Slave Address

The address is defined as the 7 most significant bits (MSBs) followed by the R/W bit. Set the R/W bit to 1 to configure the devices to read mode. Set the R/W bit to 0 to configure the device to write mode. The address is the first byte of information sent to the devices after the START condition. The slave address is factory preset. See the *Ordering Information* table for the 7-bit address for each version. The factory-programmable $I^2C$ addresses are 0x38 through 0x3F.

### Acknowledge

The acknowledge bit (ACK) is a clocked 9th bit that the device uses to handshake receipt each byte of data (Figure 2). The device pulls down SDA during the master-generated 9th clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication.

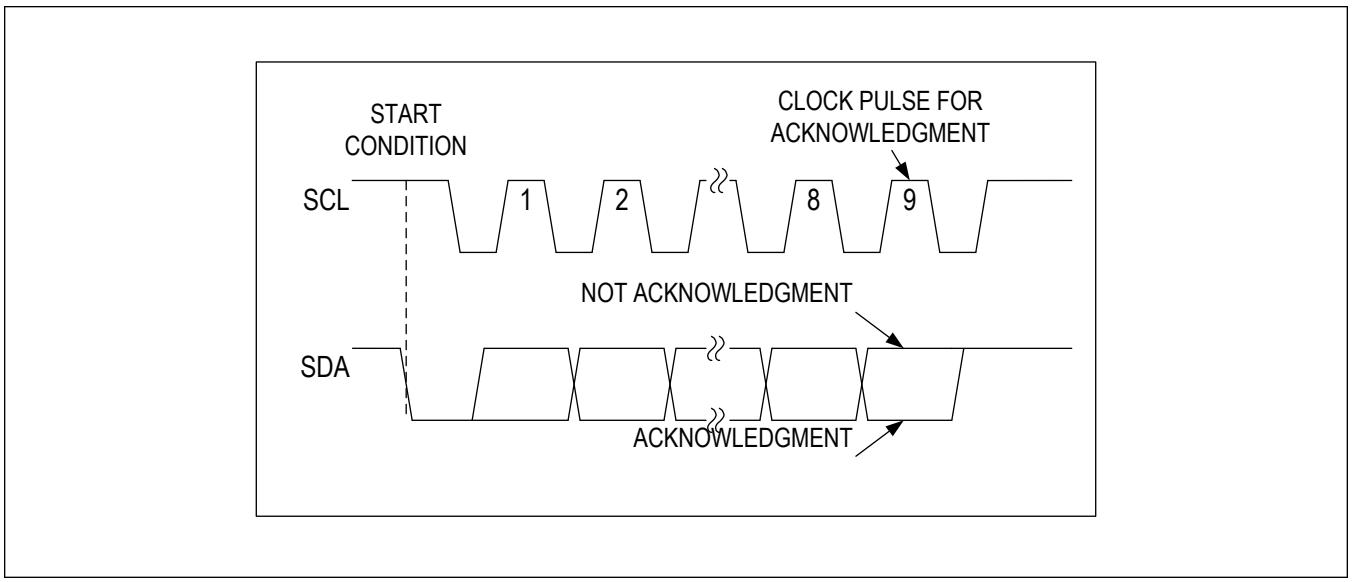



*Figure 2. Acknowledge Condition*

### Write Data Format

A write to the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to the register address, one byte of data to the command register, and a STOP condition. Figure 3 illustrates the proper format for one frame.

### Read Data Format

A read from the device includes transmission of a START condition, the slave address with the write bit set to 0, one byte of data to the register address, restart condition, the slave address with read bit set to 1, one byte of data to the command register, and a STOP condition. Figure 3 illustrates the proper format for one frame.

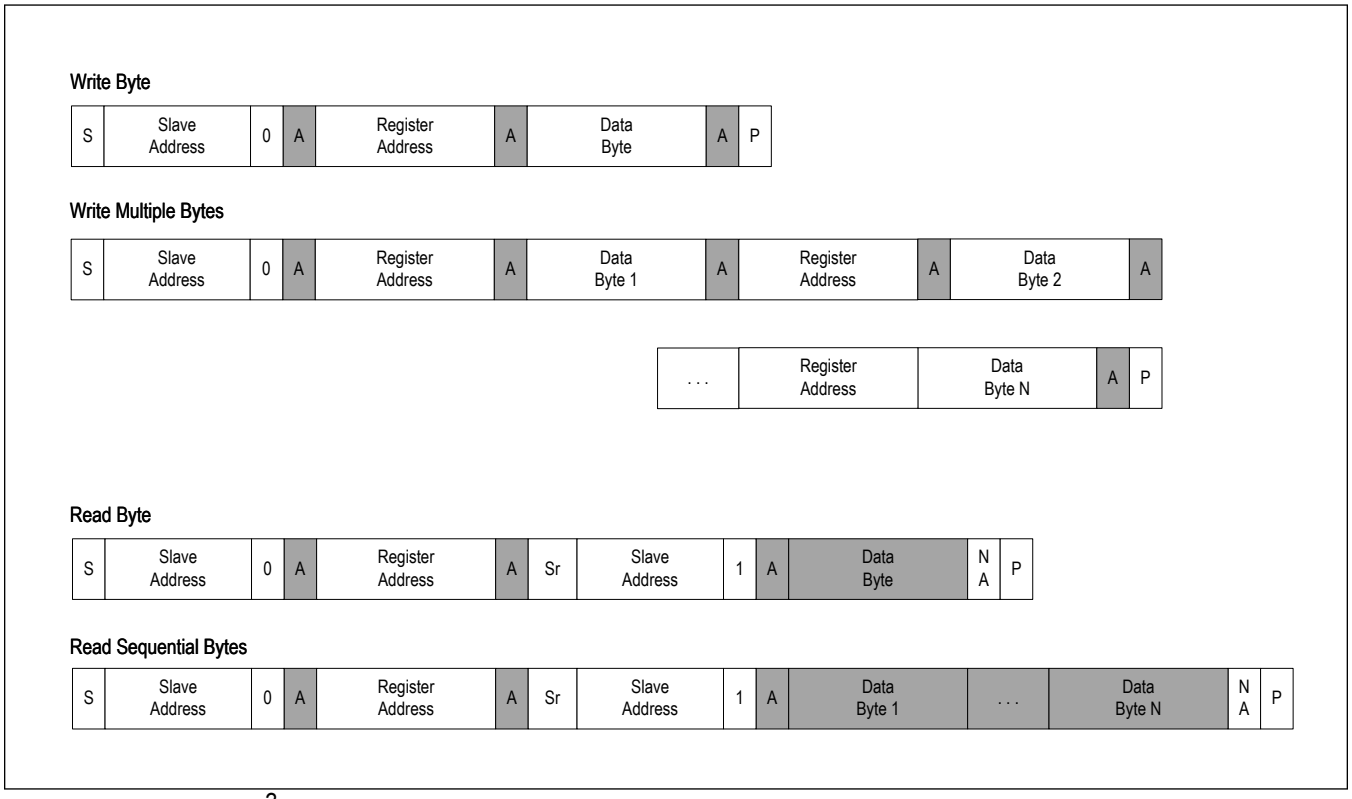



*Figure 3. Data Format of I²C Interface*

### Writing to a Single Register

Figure 4 shows the protocol for the I²C master device to write one byte of data to the MAX20499C/MAX20499D. This protocol is the same as the SMBus specification's write byte protocol.

The write byte protocol is as follows:

1. The master sends a start (S) command.
2. The master sends the 7-bit slave address followed by a write bit (R/nW = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave updates with the new data.
8. The slave does or does not acknowledge the data byte. The next rising edge on SDA loads the data byte into its target register, and the data becomes active.
9. The master sends a stop condition (P) or a repeated start condition (Sr).

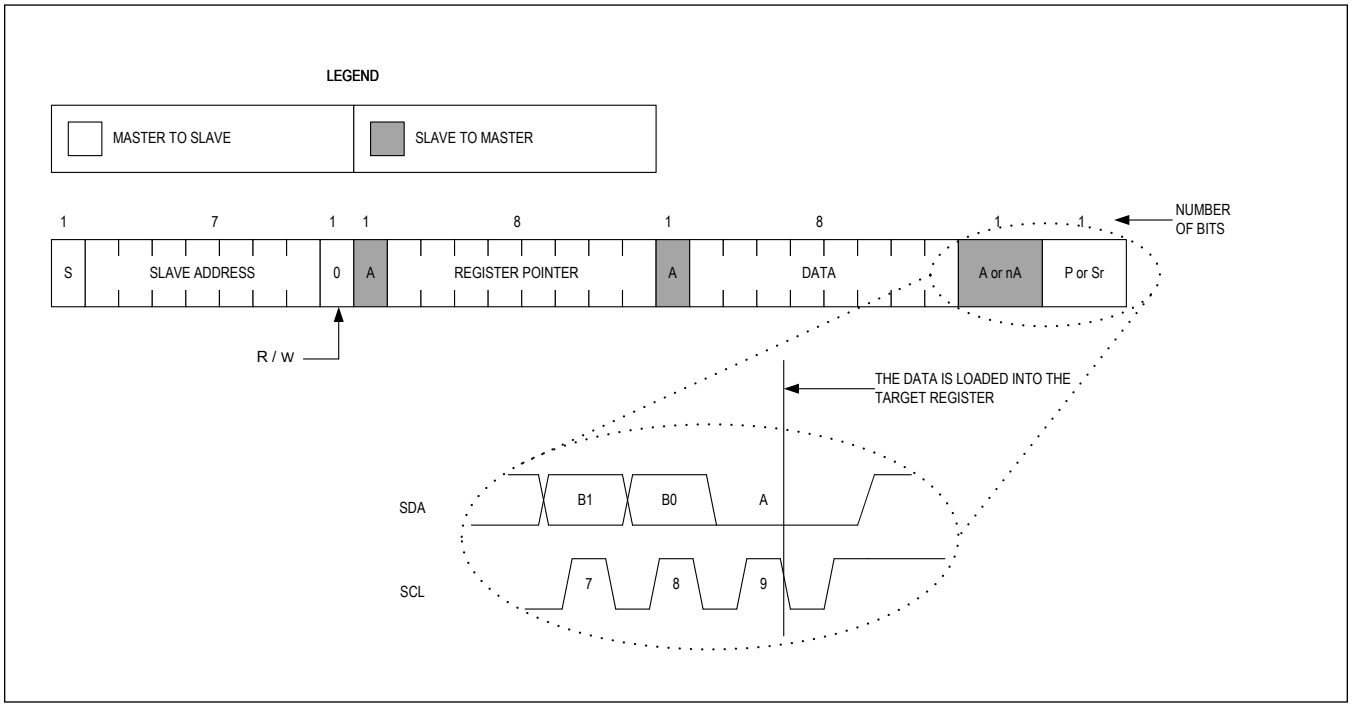



*Figure 4. Write Byte Format*

### Writing Multiple Bytes Using Register-Data Pairs

Figure 5 shows the protocol for the I²C master device to write multiple bytes to the MAX20499C/MAX20499D using register-data pairs. This protocol allows the I²C master device to address the slave only once and then send data to multiple registers in a random order. Registers may be written continuously until the master issues a stop condition.

The multiple byte register-data pair protocol is as follows:

1. The master sends a start (S) command.
2. The master sends the 7-bit slave address followed by a write bit.
3. The addressed slave asserts an acknowledge by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register, and the data becomes active.
8. Steps 5 to 7 are repeated as many times as the master requires.
9. The master sends a stop condition. During the rising edge of the stop related SDA edge, the data byte that was previously written is loaded into the target register and becomes active.

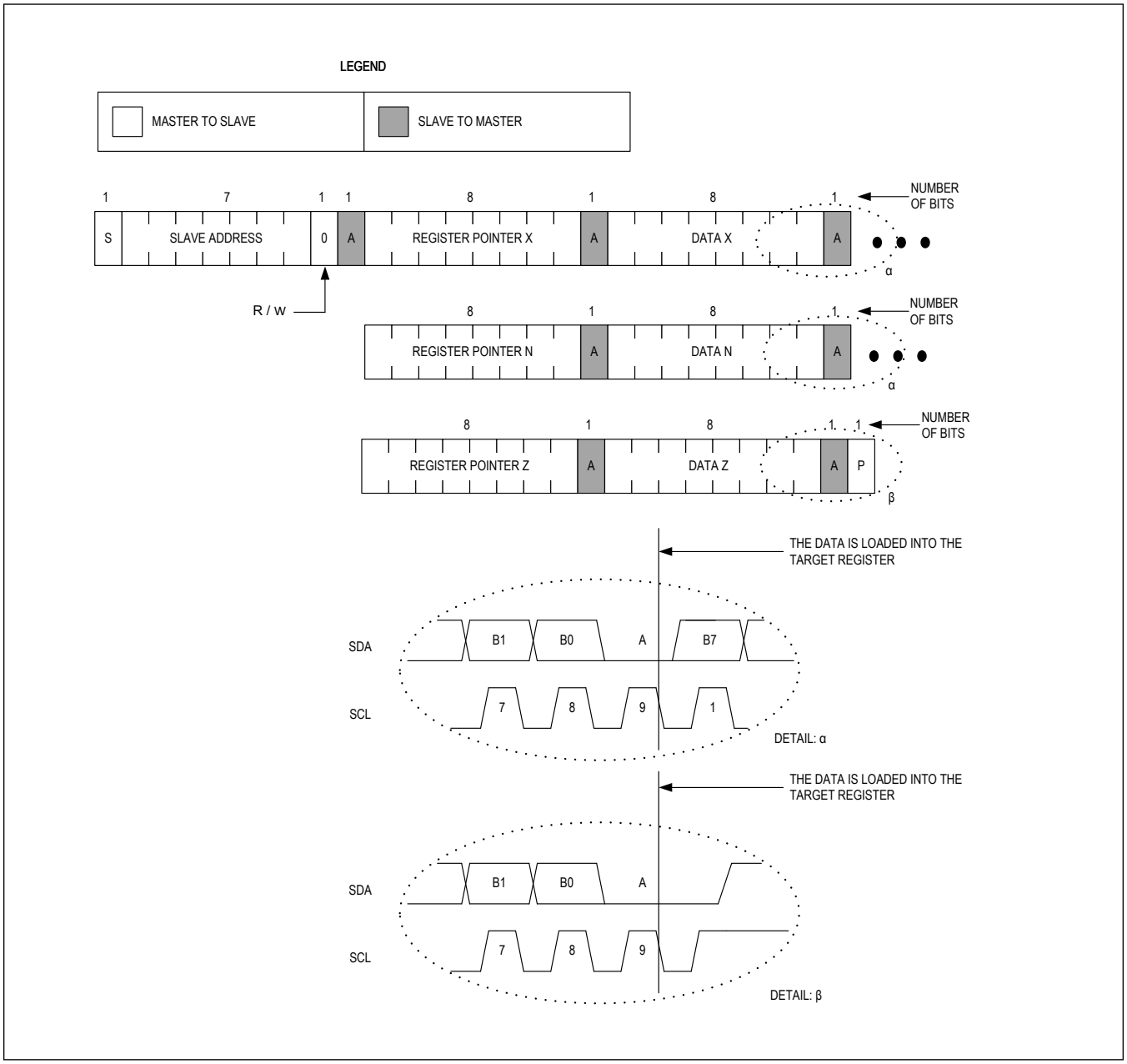



*Figure 5. Write Register-Data Pair Format*

### Reading a Single Register

Figure 6 shows the protocol for the I²C master device to read one byte of data from the MAX20499C/MAX20499D.

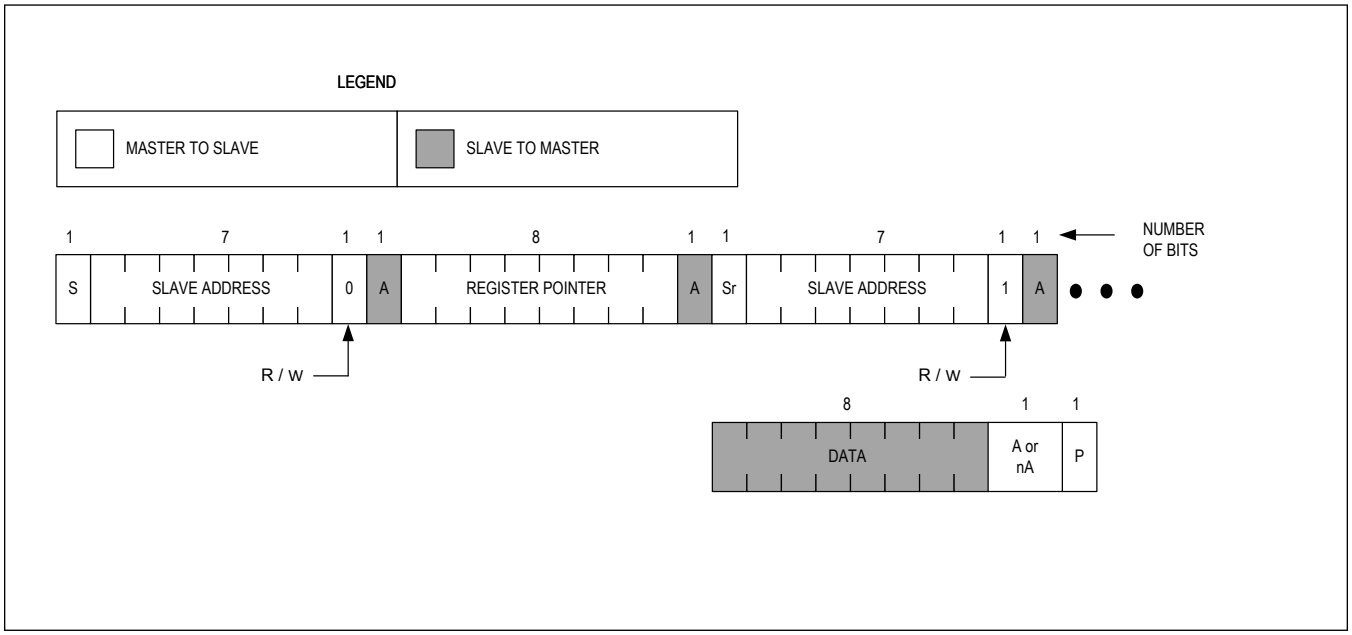



*Figure 6. Read Byte Format*

### Reading Multiple Bytes

Figure 7 shows the protocol for the I2C master device to read multiple bytes sequentially from the MAX20499C/MAX20499D.

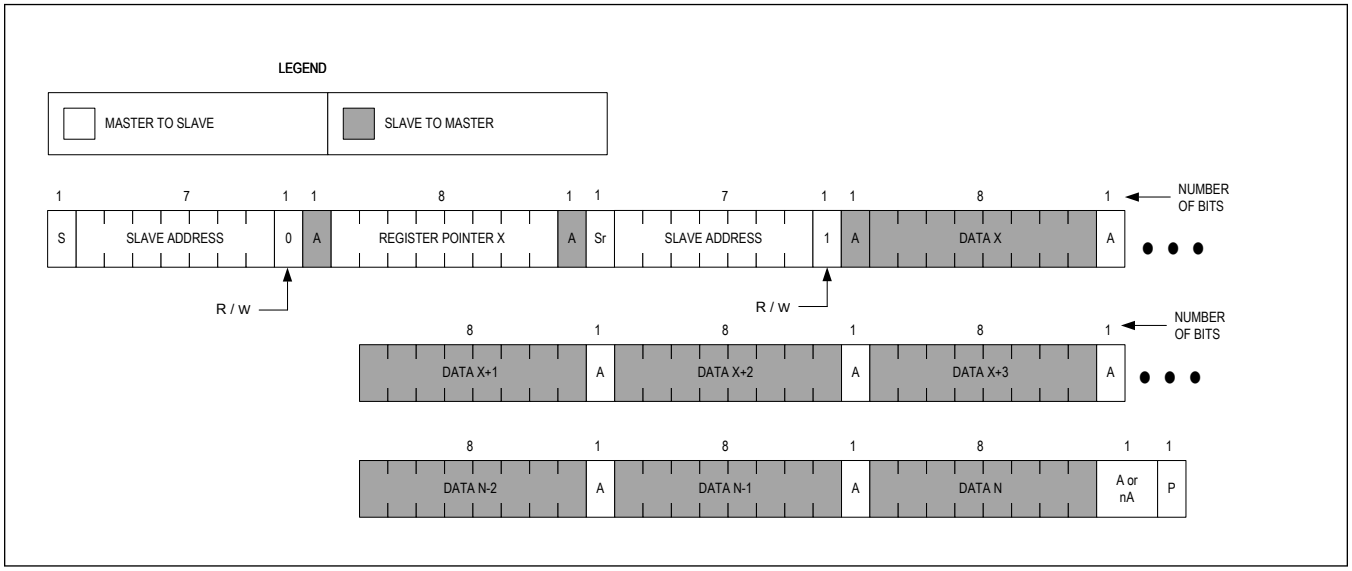



*Figure 7. Sequential Read Format*

## $\overline{\text{RESET}}$ Output

The MAX20499C/MAX20499D features an open-drain $\overline{\text{RESET}}$ output that asserts when the output voltage deviates from

the target regulated voltage by a programmed amount. $\overline{\text{RESET}}$ remains asserted for a fixed timeout period after the output is within the programmed regulation window. Connect $\overline{\text{RESET}}$ to a pullup resistor.

### Soft-Start

The MAX20499C/MAX20499D includes a programmable soft-start feature to limit startup inrush current by forcing the output voltage to slowly ramp up towards its regulation point. The soft-start slew rate is set in the SLEW register.

### Dynamic Voltage Scaling

The step-down regulator features dynamic voltage scaling (DVS) to allow loads to margin their supply voltage. The output voltage is set with VID[7:0]. The slew rate during DVS is adjustable with SR[3:0] in the SLEW register. The OV/UV comparators are masked to prevent false $\overline{\text{RESET}}$ assertions during the DVS period.

### Shutdown

During shutdown, the output voltage is ramped down at the programmed soft-start slew rate. After the soft shutdown is complete, an 11Ω pulldown resistor is enabled to discharge the remaining output voltage.

### Spread-Spectrum Option

The MAX20499C/MAX20499D featuring spread-spectrum (SS) operation varies the internal operating frequency by +3% relative to the internally generated operating frequency of 2.2MHz or 1.1MHz (typ). This function does not apply to externally applied oscillation frequency.

### Synchronization (SYNC)

SYNC is a factory-programmable I/O. When SYNC is configured as an input, a logic-high on PWM enables SYNC to accept a signal frequency in the range of 1.8MHz < $f_{SYNC}$ < 2.6MHz (CONFIG.FSW = 0) or 0.9MHz < $f_{SYNC}$ < 1.3MHz (CONFIG.FSW = 1). When SYNC is configured as an output, SYNC outputs the internal PWM switching frequency.

### Current Limit/Short-Circuit Protection

The device features current limit that protects the device against short-circuit and overload conditions at the output. In the event of a short-circuit or overload condition, the high-side MOSFET reaches the high-side MOSFET's current-limit threshold and turns off. The converter then turns on the low-side MOSFET to allow the inductor current to ramp down. Once the inductor current falls below the low-side MOSFET valley current-limit threshold, the converter allows the high-side MOSFET to turn on again. This cycle repeats until the short or overload condition is removed.

### Boost Refresh

When the device is enabled, the boost capacitor must be charged by turning on the low-side FET before initiating soft-start.

### Overtemperature Protection

Thermal overload protection limits the total power dissipation in the MAX20499C/MAX20499D. When the junction temperature exceeds +165°C (typ), an internal thermal sensor shuts down the internal bias regulator and the step-down controller, allowing the IC to cool. The thermal sensor turns on the IC again after the junction temperature cools by +15°C.

## Applications Information

### Input Capacitor

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by the circuit's switching.

The input capacitor RMS current requirement ($I_{RMS}$) is defined by the following equation:

$$I_{RMS} = I_{LOAD(MAX)} \frac{\sqrt{V_{OUT}\left(V_{PV} - V_{OUT}\right)}}{V_{PV}}$$

$I_{RMS}$ has a maximum value when the input voltage equals twice the output voltage ($V_{PV} = 2V_{OUT}$), so $I_{RMS(MAX)} = I_{LOAD(MAX)} / 2$

Choose an input capacitor that exhibits less than +10°C self-heating temperature rise at the RMS input current for optimal long-term reliability.

The input voltage ripple consists of $\Delta V_Q$ (caused by the capacitor discharge) and $\Delta V_{ESR}$ (caused by the ESR of the capacitor). Use low-ESR ceramic capacitors with high ripple-current capability at the input. Assume the contribution from the ESR and capacitor discharge equal to 50%. Calculate the input capacitance and ESR required for a specified input voltage ripple using the following equations:

$$ESR_{IN} = \frac{\Delta V_{ESR}}{I_{OUT} + \frac{\Delta I_L}{2}}$$

Where,

$$\Delta I_L = \frac{\left(V_{PV} - V_{OUT}\right) \times V_{OUT}}{V_{PV} \times f_{SW} \times L}$$

And

$$C_{IN} = \frac{I_{OUT} \times D(1 - D)}{\Delta V_Q \times f_{SW}} \text{ and } D = \frac{V_{OUT}}{V_{PV}}$$

$I_{OUT}$ is the maximum output current. D is the duty cycle.

### Inductor Selection

Three key inductor parameters must be specified for operation with the MAX20499C/MAX20499D: inductance value (L), peak inductor current ($I_{PEAK}$), and inductor saturation current ($I_{SAT}$). The minimum required inductance is a function of operating frequency, input-to-output voltage differential, and the maximum output current capability of the output. A lower inductor value minimizes size and cost, improves large-signal and transient response, but reduces efficiency due to higher peak currents and higher peak-to-peak output-voltage ripple for the same output capacitor. On the other hand, higher inductance increases efficiency by reducing the ripple current. Resistive losses due to extra wire turns can exceed the benefit gained from lower ripple current levels, especially when the inductance is increased without also allowing for larger inductor dimensions. The MAX20499C/MAX20499D is designed for $\Delta I_{P-P}$ equal to 20% to 40% of the full load current. Use the following equation to calculate the inductance:

$$L_{MIN1} = \frac{\left(V_{IN} - V_{OUT}\right) \cdot V_{OUT}}{V_{IN} \cdot f_{SW} \cdot I_{MAX} \cdot 40\,\%}$$

$V_{IN}$ and $V_{OUT}$ are typical values so that efficiency is optimum for typical conditions. The switching frequency is typically 2.2MHz or 1.1MHz. See the *Output Capacitor* section to verify the worst-case output ripple is acceptable. The inductor saturation current is also important to avoid runaway current during continuous output short circuit.

## Table 1. Inductor Selection Parameters

| PARAMETER | DESCRIPTION |
|---|---|

## Table 1. Inductor Selection Parameters (continued)

| | |
|---|---|
| $V_{IN}$ | Nominal input voltage (typically 3.3V or 5V) |
| $V_{OUT}$ | Nominal output voltage |
| $L_{TOL}$ | Inductor tolerance (typically ±20%) |
| $I_{MAX}$ | 16A |
| $f_{SW}$ | Operating frequency (2.2MHz or 1.1MHz, unless externally synchronized to a different frequency) |

$L_{MIN} = (1 + L_{TOL}) \times L_{MIN1}$

The maximum inductor value recommended is 1.75 times the chosen value from the above formula.

$L_{MAX} = 2.0 \times L_{MIN}$

Select a nominal inductor value based on the following formula. For optimal load-transient performance, select the first standard inductor value greater than $L_{MIN}$:

$L_{MIN} < L_{NOM} < L_{MAX}$

## Table 2. Recommended Inductor Values

| $V_{IN}$ | $V_{OUT}$ | $I_{MAX}$ | $L_{MIN}$ | $L_{MAX}$ | RECOMMENDED |
|---|---|---|---|---|---|
| 3.3V | 1V | 16A | 50nH | 100nH | 60nH, 70nH, 80nH |

Inductors are rated for maximum saturation current. The maximum inductor current equals the maximum load current in addition to half of the peak-to-peak ripple current:

$$I_{PEAK} = I_{LOAD(MAX)} + \frac{\Delta I_{INDUCTOR}}{2}$$

The actual peak-to-peak inductor ripple current is calculated in the $\Delta I_L$ equation above.

The saturation current should be larger than $I_{PEAK}$ or at least in a range where the inductance does not degrade significantly.

### Output Capacitor

The compensation is programmable to allow application-specific optimization between output capacitance and AC performance. The typical output capacitor range is 150µF (typ) to 700µF (typ). Using the default COMP value of 0xE2, the following equation provides a good starting point.

$$C_{OUTNOM} = 15 \times I_{OUTMAX} \times \frac{R_{COMP}}{70K\Omega} \times \frac{\mu sec}{V}$$

Where,

$I_{OUTMAX}$ is 16A

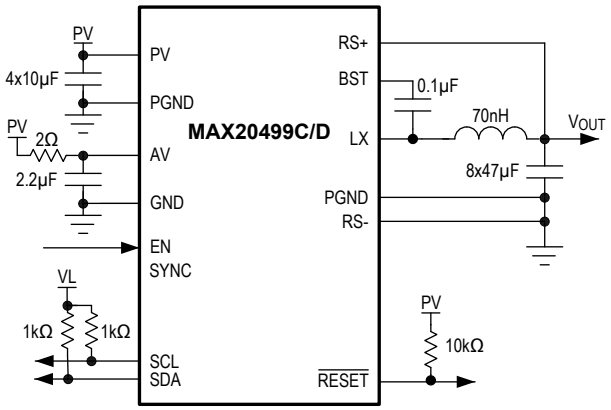
This will place the unity gain bandwidth at approximately 200kHz, which is at the peak of the phase boost and results in the best phase margin. It is possible to trade phase margin for a lower output capacitor from this point. To ensure stability, always measure the phase margin with the fully derated output capacitance.

### Programmable Compensation

The device has a programmable zero along with a programmable compensation resistor. In most cases, the zero should be enabled with the $g_m$ set to 113µS and resistance set to 300kΩ. This provides the largest phase boost possible and allows the highest cross-over frequency. This is done by setting the upper nibble of the COMP register to 0xE. The compensation resistor is set based on the application requirements. A higher value resistance results in increased AC performance and an increased output capacitor requirement, while a lower compensation resistance results in a decrease in AC performance with a lower output capacitance requirement.

It is recommended that the compensation optimization be completed on the application PCB to account for PCB parasitics when trying to maximize AC performance and/or minimize the output capacitance.

## Typical Application Circuits




## Ordering Information

| PART | $I_{OUT}$ | $V_{OUT}$ | $V_{MAX}$ | SLEW | COMP | CONFIG | CONFIG2 | OV/UV | RESET HOLD | $I^2C$ |
|---|---|---|---|---|---|---|---|---|---|---|
| MAX20499CAFOA/VY+ | 16A | 0.85V | 1V | 0x09 | 0xE4 | 0x0C | 0x00 | 0xBB | 0.5ms | 0x38 |
| MAX20499CAFOB/VY+ | 16A | 0.75625V | 1V | 0x09 | 0xE4 | 0x08 | 0x00 | 0xBB | 0.5ms | 0x38 |
| MAX20499CAFOC/VY+ | 16A | 1V | 1.1V | 0x09 | 0xEB | 0x0C | 0x00 | 0x55 | 0.5ms | 0x38 |
| MAX20499DAFOA/VY+ | 12A | 0.85V | 1V | 0x09 | 0xE4 | 0x0C | 0x00 | 0xBB | 0.5ms | 0x38 |
| MAX20499DAFOB/VY+ | 12A | 1.05V | 1.05V | 0x09 | 0xE4 | 0x0C | 0x00 | 0xBB | 0.5ms | 0x3A |

*/VY Denotes side-wettable automotive-qualified parts.*

*+ Indicates a lead(Pb)-free/RoHS compliant package.*

*Contact factory for additional part options and custom configurations. Refer to $I^2C$ register map for factory-selectable customer configurations.*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 6/21 | Initial release | — |
| 1 | 8/21 | Updated *Ordering Information* | 23 |
| 2 | 9/21 | Updated CONFIG values in *Ordering Information* | 23 |
| 3 | 12/21 | Updated *Ordering Information* | 23 |
| 4 | 6/22 | Updated *Ordering Information* | 23 |
| 5 | 9/23 | Updated *Ordering Information* | 23 |

# X-ON Electronics

Largest Supplier of Electrical and Electronic Components

***Click to view similar products for*** Switching Voltage Regulators ***category:***

***Click to view products by*** Analog Devices ***manufacturer:***

Other Similar products are found below :

LV5695P-E FAN53610AUC33X EN6310QA NCP81108MNTXG NCP81109BMNTXG 160215 R3 FAN53611AUC12X MAX809TTR AST1S31PUR NCP81203PMNTXG NCP81208MNTXG NCP81109GMNTXG NCP3235MNTXG NCP81109JMNTXG MP2161AGJ-Z NCP81241MNTXG NTE7223 NTE7222 NTE7224 L6986FTR MPQ4481GU-AEC1-P MP8756GD-P MPQ2171GJ-P MPQ2171GJ-AEC1-P NJW4153U2-A-TE2 MP28160GC-Z MPM3509GQVE-AEC1-P XDPE132G5CG000XUMA1 LM60440AQRPKRQ1 LT8653SEV#PBF MP5461GC-P NCV896530MWATXG MPQ4409GQBE-AEC1-P S-19903DA-A8T1U7 S-19903CA-A6T8U7 S-19903CA-S8T1U7 S-19902BA-A6T8U7 S-19902CA-A6T8U7 S-19932BA-A6T8U7 S-19932BA-A8T1U7 S-19902AA-A6T8U7 S-19903AA-A6T8U7 S-19902AA-S8T1U7 S-19902BA-A8T1U7 LMR23615QDRRRQ1 XC9110C301MR-G XC9141A50CMR-G XCL206F083CR-G XCL210A111GR-G