*Click **here** to ask an associate for production status of specific part numbers.*

# MAX17643

# 4.5V–60V, 2A, High-Efficiency, Synchronous Step-Down DC-DC Converter with Internal Compensation

## General Description

The Himalaya series of voltage regulator ICs, power modules, and chargers enable cooler, smaller, and simpler power-supply solutions. The MAX17643 high-efficiency, high-voltage, Himalaya synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input. The converter can deliver up to 2A and generates output voltages from 0.9V up to (0.9 x $V_{IN}$)V. The feedback (FB) voltage is accurate to within ±1.4% over -40°C to +125°C. Built-in compensation across the output-voltage range eliminates the need for external components. The MAX17643 features peak-current-mode control architecture and operates in fixed frequency forced PWM mode. The current-limit settings of the MAX17643 allow the device to supply load-current peaks up to 2A. This allows the device to support pulsed load applications such as communication modules with minimal output-voltage droop. The MAX17643 offers a low minimum on-time that allows high switching frequencies and a smaller solution size.

The device is available in a 12-pin (3mm × 3mm) TDFN package. Simulation models are available.

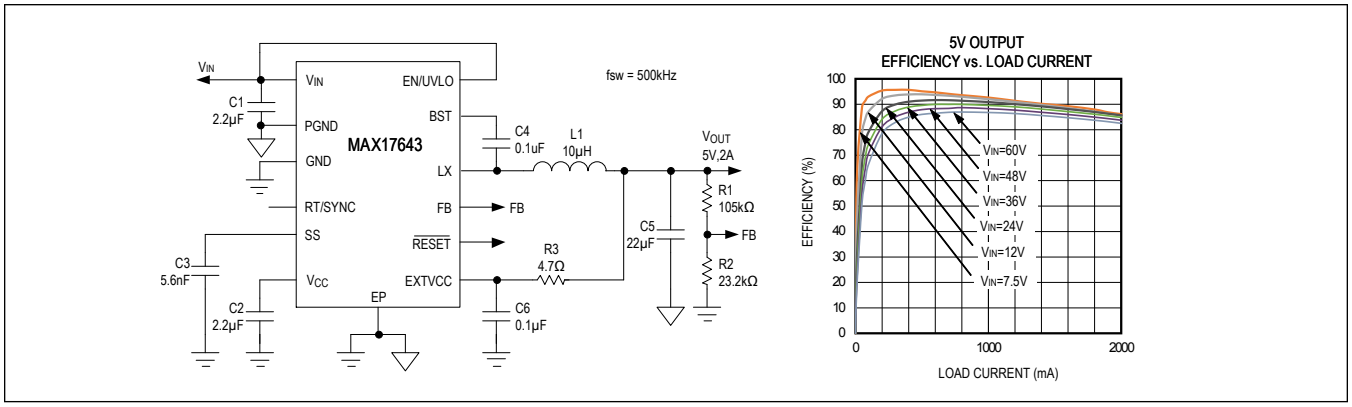
## Applications

- Industrial-Control Power Supplies
- General-Purpose Point-of-Load
- Distributed Supply Regulation
- Base-Station Power Supplies
- Wall Transformer Regulation
- High-Voltage, Single-Board Systems
- Pulsed-Load Applications
- Communication Modules

## Benefits and Features

- Reduces External Components and Total Cost
  - No Schottky-Synchronous Operation
  - Internal Compensation for Any Output Voltage
  - All-Ceramic Capacitors, Compact Layout
- Reduces Number of DC-DC Regulators to Stock
  - Wide 4.5V to 60V Input
  - Adjustable 0.9V to (0.9 × $V_{IN}$) Output
  - Up to 2A Peak-Load Current
  - 400kHz to 2.2MHz Adjustable Switching Frequency with External Synchronization
- Reduces Power Dissipation
  - Peak Efficiency of 91.6%
  - Auxiliary Bootstrap LDO for Improved Efficiency
  - 4.65µA Shutdown Current
- Operates Reliably in Adverse Industrial Environments
  - Hiccup-Mode Overload Protection
  - Adjustable Soft-Start
  - Built-In Output-Voltage Monitoring with $\overline{\text{RESET}}$
  - Programmable EN/UVLO Threshold
  - Monotonic Startup into Prebiased Load
  - Overtemperature Protection
  - Wide Industrial -40°C to +125°C Ambient Operating Temperature Range/ -40°C to +150°C Junction Temperature Range
  - Complies with CISPR32 (EN55032) Class B Conducted and Radiated Emissions

## 5V Output: Typical Application Circuit and Efficiency vs. Load Current




***Ordering Information** appears at end of datasheet.*

*19-100954; Rev 1; 9/21*

## Absolute Maximum Ratings

$V_{IN}$ to PGND ..... -0.3V to +65V
EN/UVLO to GND ..... -0.3V to ($V_{IN}$ + 0.3V)
EXTVCC to GND ..... -0.3V to +26V
BST to PGND ..... -0.3V to +70V
LX to PGND ..... -0.3V to ($V_{IN}$ + 0.3V)
BST to LX ..... -0.3V to +6.5V
BST to $V_{CC}$ ..... -0.3V to +65V
RESET, SS, RT/SYNC to GND ..... -0.3V to +6.5V
PGND to GND ..... -0.3V to +0.3V
FB to GND. ..... -0.3V to +1.5V
$V_{CC}$ to GND ..... -0.3V to +6.5V
LX Total RMS Current ..... ±2.1A
Continuous Power Dissipation ($T_A$ = +70°C Derate 24.4mW/°C above +70°C; Multilayer Board) ..... 1951mW
Output Short-Circuit Duration ..... Continuous
Junction Temperature (Note 1) ..... +150°C
Storage Temperature Range ..... -65°C to +160°C
Lead Temperature (soldering, 10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

**Note 1:** Junction temperature greater than +125°C degrades operating lifetimes.

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

## Package Information

### 12 PIN TDFN

| | |
|---|---|
| Package Code | TD1233+1C |
| Outline Number | 21-0664 |
| Land Pattern Number | 90-0397 |
| **Thermal Resistance, Four-Layer Board:** | |
| Junction to Ambient ($\theta_{JA}$) | 41°C/W |
| Junction to Case ($\theta_{JC}$) | 8.5°C/W |

For the latest package outline information and land patterns (footprints), go to ***www.maximintegrated.com/packages***. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to ***www.maximintegrated.com/thermal-tutorial***.

## Electrical Characteristics

($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $R_{RT/SYNC}$ = 40.2k, $C_{VCC}$ = 2.2µF, $V_{PGND}$ = $V_{GND}$ = EXTVCC = 0, LX = SS = $\overline{RESET}$ = OPEN, $V_{BST}$ to $V_{LX}$ = 5V, $V_{FB}$ = 1V, $T_A$ = -40°C to 125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| **INPUT SUPPLY ($V_{IN}$)** | | | | | | |
| Input-Voltage Range | $V_{IN}$ | | 4.5 | | 60 | V |
| Input-Shutdown Current | $I_{IN-SH}$ | $V_{EN/UVLO}$ = 0V (shutdown mode) | | 4.65 | 7.25 | µA |
| Input-Quiescent Current | $I_{Q\_PWM}$ | Normal switching mode, $f_{SW}$ = 500kHz, $V_{FB}$ = 0.8, EXTVCC = GND | | 5.65 | | mA |
| **ENABLE/UVLO (EN/UVLO)** | | | | | | |
| EN/UVLO Threshold | $V_{ENR}$ | $V_{EN/UVLO}$ rising | 1.19 | 1.215 | 1.26 | V |
| | VENF | VEN/UVLO falling | 1.068 | 1.09 | 1.131 | |
| EN/UVLO Input-Leakage Current | $I_{ENLKG}$ | $V_{EN/UVLO}$ = 1.25V, $T_A$ = 25°C | -50 | | +50 | nA |
| **$V_{CC}$ LDO** | | | | | | |
| $V_{CC}$ Output-Voltage Range | $V_{CC}$ | 1mA ≤ $I_{VCC}$ ≤ 15mA | 4.75 | 5 | 5.25 | V |
| | | 6V ≤ $V_{IN}$ ≤ 60V; $I_{VCC}$ = 1mA | 4.75 | 5 | 5.25 | |

## Electrical Characteristics (continued)

($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $R_{RT/SYNC}$ = 40.2k, $C_{VCC}$ = 2.2µF, $V_{PGND}$ = $V_{GND}$ = EXTVCC = 0, LX = SS = $\overline{RESET}$ = OPEN, $V_{BST}$ to $V_{LX}$ = 5V, $V_{FB}$ = 1V, $T_A$ = -40°C to 125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| $V_{CC}$ Current Limit | $I_{VCC-MAX}$ | $V_{CC}$ = 4.3V, $V_{IN}$ = 6.5V | 25 | 54 | 100 | mA |
| $V_{CC}$ Dropout | $V_{CC-DO}$ | $V_{IN}$ = 4.5V , $I_{VCC}$ = 15mA | 4.15 | | | V |
| $V_{CC}$ UVLO | $V_{CC-UVR}$ | Rising | 4.05 | 4.2 | 4.3 | V |
| | $V_{CC-UVF}$ | Falling | 3.65 | 3.8 | 3.9 | |
| **EXTVCC LDO** | | | | | | |
| EXTVCC Switchover Voltage | | EXTVCC rising | 4.56 | 4.7 | 4.84 | V |
| | | EXTVCC falling | 4.3 | 4.45 | 4.6 | |
| EXTVCC Dropout | $EXTVCC_{DO}$ | EXTVCC = 4.75V , $I_{EXTVCC}$ = 15mA | | | 0.3 | V |
| EXTVCC Current Limit | $EXTVCC_{ILIM}$ | $V_{CC}$ = 4.3V, EXTVCC = 5V | 26.5 | 60 | 100 | mA |
| **HIGH-SIDE MOSFET AND LOW-SIDE MOSFET DRIVER** | | | | | | |
| High-Side nMOS On-Resistance | $R_{DS-ONH}$ | $I_{LX}$ = 0.3A | | 330 | 620 | mΩ |
| Low-Side nMOS On-Resistance | $R_{DS-ONL}$ | $I_{LX}$ = 0.3A | | 170 | 320 | mΩ |
| LX Leakage Current (LX to PGND_) | $I_{LXLKG}$ | $V_{LX}$ = $V_{IN}$ - 1V; $V_{LX}$ = $V_{PGND}$ + 1V; $T_A$ = 25°C | -2 | | +2 | µA |
| **SOFT-START** | | | | | | |
| Soft-Start Current | $I_{SS}$ | $V_{SS}$ = 0.5 V | 4.7 | 5 | 5.3 | µA |
| **FEEDBACK** | | | | | | |
| FB Regulation Voltage | $V_{FB\_REG}$ | PWM version | 0.887 | 0.9 | 0.913 | V |
| FB Input-Bias Current | $I_{FB}$ | 0 ≤ $V_{FB}$ ≤ 1V, $T_A$ = 25°C | -50 | | +50 | nA |
| **CURRENT LIMIT** | | | | | | |
| Peak Current-Limit Threshold | $I_{PEAK-LIMIT}$ | | 2.69 | 3.25 | 3.63 | A |
| Runaway-Peak Current-Limit Threshold | $I_{RUNAWAY-LIMIT}$ | | 3.2 | 3.6 | 4 | A |
| Negative Current-Limit Threshold | | | | 1 | | A |
| **RT** | | | | | | |
| Switching Frequency | $f_{SW}$ | $R_{RT}$ = 52kΩ | 370 | 400 | 430 | kHz |
| | | $R_{RT}$ = 40.2kΩ | 475 | 500 | 525 | |
| | | $R_{RT}$ = 8.06kΩ | 1950 | 2200 | 2450 | |
| | | $R_{RT}$ = OPEN | 430 | 490 | 550 | |
| $V_{OUT}$ Undervoltage Trip-Level to Cause HICCUP | $V_{OUT-HICF}$ | | 0.56 | 0.58 | 0.65 | V |
| HICCUP Timeout | | | | 32768 | | Cycles |
| Minimum On-Time | $t_{ON\_MIN}$ | | | 60 | 90 | ns |
| Minimum Off-Time | $t_{OFF\_MIN}$ | | 140 | 150 | 160 | ns |

## Electrical Characteristics (continued)

($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $R_{RT/SYNC}$ = 40.2k, $C_{VCC}$ = 2.2µF, $V_{PGND}$ = $V_{GND}$ = EXTVCC = 0, LX = SS = $\overline{RESET}$ = OPEN, $V_{BST}$ to $V_{LX}$ = 5V, $V_{FB}$ = 1V, $T_A$ = -40°C to 125°C, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to GND, unless otherwise noted.) (Note 2)

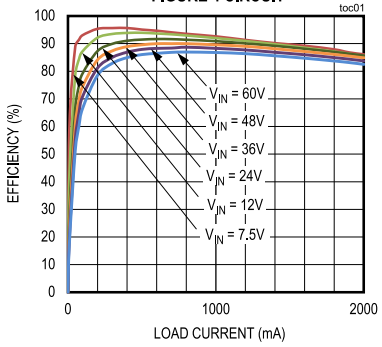
| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| SYNC Frequency Capture Range | | $f_{SW}$ set by $R_{RT}$ | 1.1 x $f_{SW}$ | | 1.4 x $f_{SW}$ | |
| SYNC Pulse-Width | | | 50 | | | ns |
| SYNC Threshold | $V_{IH}$ | | 2.1 | | | V |
| | $V_{IL}$ | | | | 0.8 | |
| LX Dead Time | | | | 5 | | ns |
| **$\overline{RESET}$** | | | | | | |
| $\overline{RESET}$ Output Level Low | | $I_{\overline{RESET}}$ = 10mA | | | 400 | mV |
| $\overline{RESET}$ Output-Leakage Current High | | $T_A$ = $T_J$ = 25°C, $V_{\overline{RESET}}$ = 5.5V | -100 | | +100 | nA |
| $V_{OUT}$ Threshold for $\overline{RESET}$ Assertion | $V_{OUT-OKF}$ | $V_{FB}$ Falling | 90.5 | 92 | 94.6 | % |
| $V_{OUT}$ Threshold for $\overline{RESET}$ Deassertion | $V_{OUT-OKR}$ | $V_{FB}$ Falling | 93.8 | 95 | 97.8 | % |
| $\overline{RESET}$ Delay after FB Reaches 95% Regulation | | | | 1024 | | Cycles |
| **THERMAL SHUTDOWN** | | | | | | |
| Thermal-Shutdown Threshold | $T_{SHDNR}$ | Temperature rising | | 165 | | °C |
| Thermal-Shutdown Hysteresis | $T_{SHDNHY}$ | | | 15 | | °C |

**Note 2:** All limits are 100% tested at $T_A$ = +25°C. Limits over the operating temperature range and relevant supply-voltage range are guaranteed by design and characterization

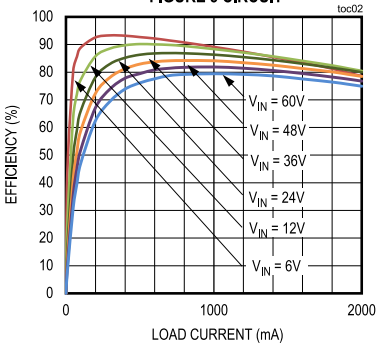
## Typical Operating Characteristics

($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{GND}$ = $V_{PGND}$ = 0V, $C_{VCC}$ = 2.2µF, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to GND.)

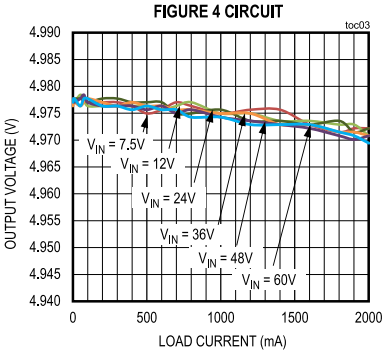
5V OUTPUT
EFFICIENCY vs. LOAD CURRENT
FIGURE 4 CIRCUIT



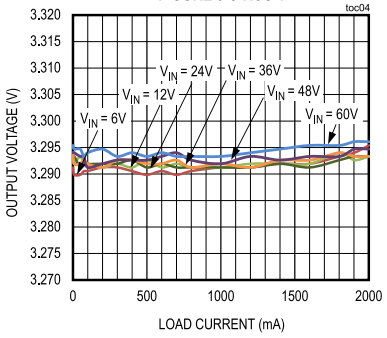

3.3V OUTPUT
EFFICIENCY vs. LOAD CURRENT
FIGURE 5 CIRCUIT



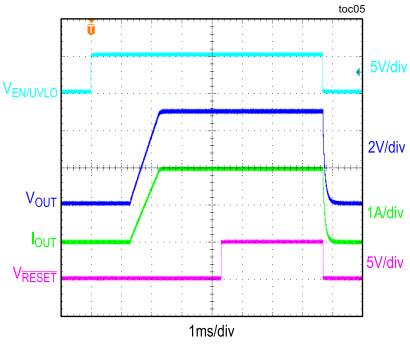

5V OUTPUT
OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 4 CIRCUIT




3.3V OUTPUT
OUTPUT VOLTAGE vs. LOAD CURRENT
FIGURE 5 CIRCUIT

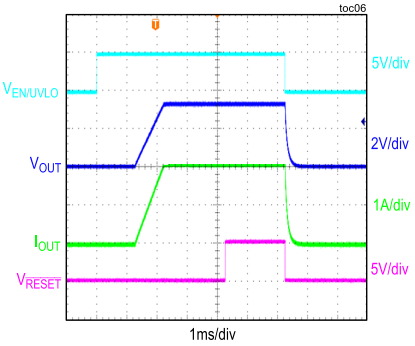



STARTUP/SHUTDOWN THROUGH EN/UVLO
2.5Ω RESISTIVE LOAD
FIGURE 4 CIRCUIT



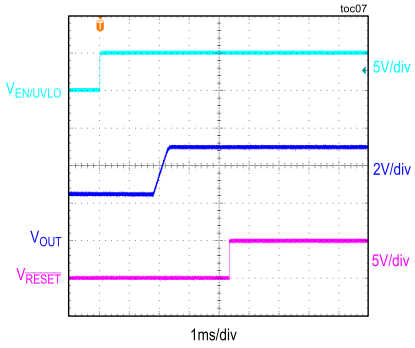

CONDITION: $\overline{RESET}$ IS PULLED UP TO $V_{CC}$ WITH A 10kΩ RESISTOR

STARTUP/SHUTDOWN THROUGH EN/UVLO
1.65Ω RESISTIVE LOAD
FIGURE 5 CIRCUIT



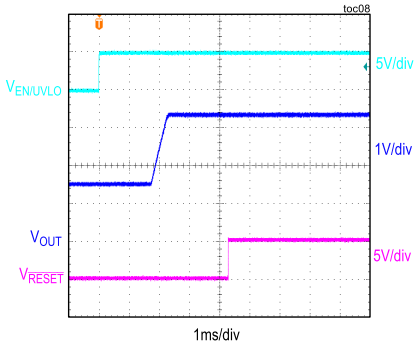

CONDITION: $\overline{RESET}$ IS PULLED UP TO $V_{CC}$ WITH A 10kΩ RESISTOR

SOFT-START WITH 2.5V PREBIAS
5V OUTPUT
FIGURE 4 CIRCUIT



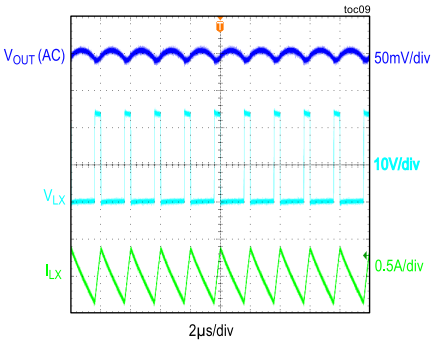

CONDITION: $\overline{RESET}$ IS PULLED UP TO $V_{CC}$ WITH A 10kΩ RESISTOR

SOFT-START WITH 1.5V PREBIAS
3.3V OUTPUT
FIGURE 5 CIRCUIT




CONDITION: $\overline{RESET}$ IS PULLED UP TO $V_{CC}$ WITH A 10kΩ RESISTOR

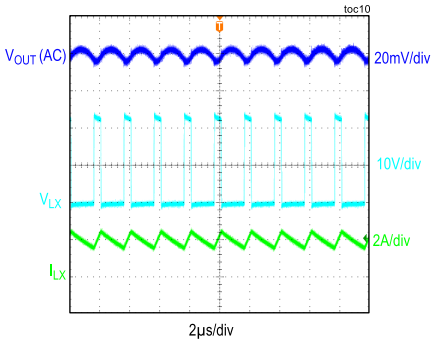
STEADY-STATE SWITCHING WAVEFORMS
5V OUTPUT, NO LOAD
FIGURE 4 CIRCUIT



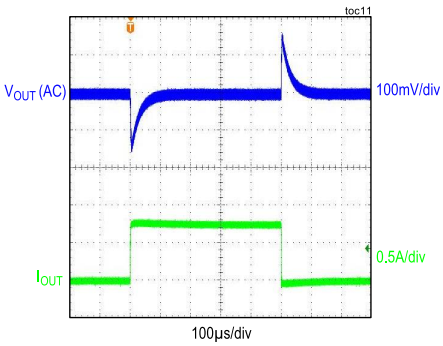
## Typical Operating Characteristics (continued)

($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{GND}$ = $V_{PGND}$ = 0V, $C_{VCC}$ = 2.2µF, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to GND.)

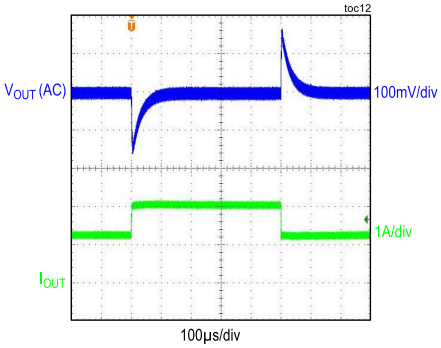
STEADY-STATE SWITCHING WAVEFORMS
5V OUTPUT, 2A LOAD CURRENT
FIGURE 4 CIRCUIT



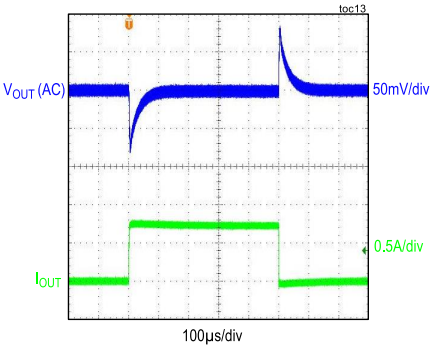

5V OUTPUT
LOAD CURRENT STEPPED FROM NO LOAD TO 0.75A
FIGURE 4 CIRCUIT



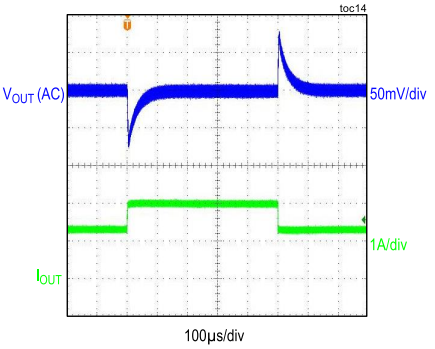

5V OUTPUT
LOAD CURRENT STEPPED FROM 1.25A TO 2A
FIGURE 4 CIRCUIT



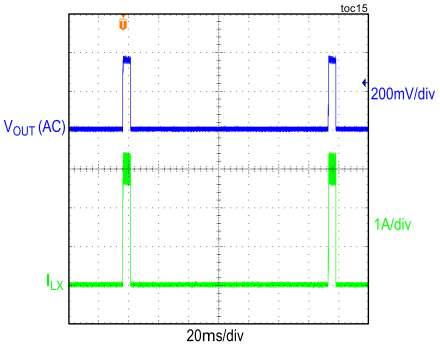

3.3V OUTPUT
LOAD CURRENT STEPPED FROM NO LOAD TO 0.75A
FIGURE 5 CIRCUIT



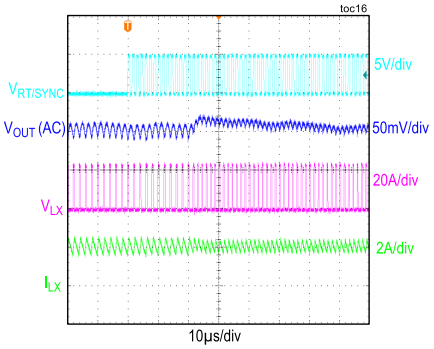

3.3V OUTPUT
LOAD CURRENT STEPPED FROM 1.25A TO 2A
FIGURE 5 CIRCUIT




OVERLOAD PROTECTION
5V OUTPUT
FIGURE 4 CIRCUIT

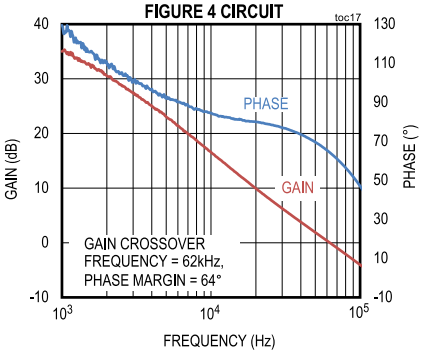



EXTERNAL-CLOCK SYNCHRONIZATION
FIGURE 4 CIRCUIT

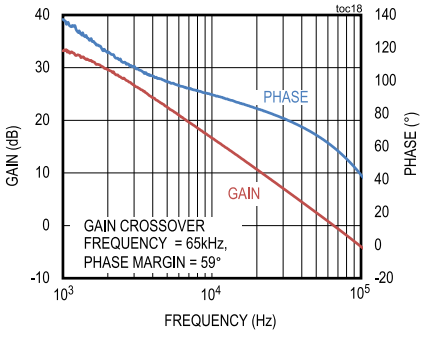



CONDITIONS: 5V OUTPUT, 2A LOAD CURRENT, $f_{SW}$ = 500kHz, EXTERNAL-CLOCK FREQUENCY = 700kHz

BODE PLOT, 5V OUTPUT
2.5Ω RESISTIVE LOAD
FIGURE 4 CIRCUIT

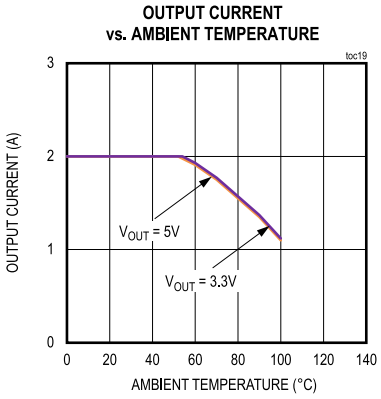


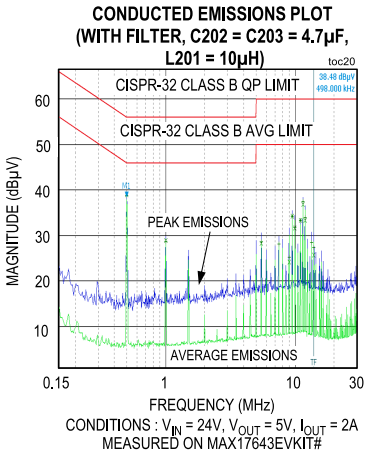

BODE PLOT, 3.3V OUTPUT
1.65Ω RESISTIVE LOAD

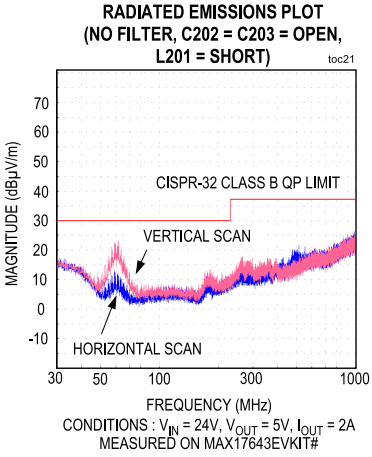


## Typical Operating Characteristics (continued)

($V_{IN}$ = $V_{EN/UVLO}$ = 24V, $V_{GND}$ = $V_{PGND}$ = 0V, $C_{VCC}$ = 2.2µF, unless otherwise noted. Typical values are at $T_A$ = +25°C. All voltages are referenced to GND.)

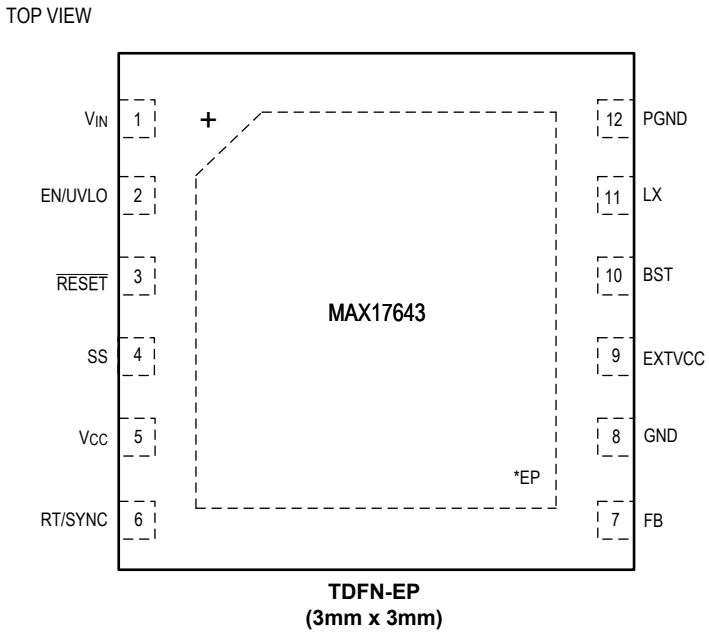



## Pin Configuration

### MAX17643

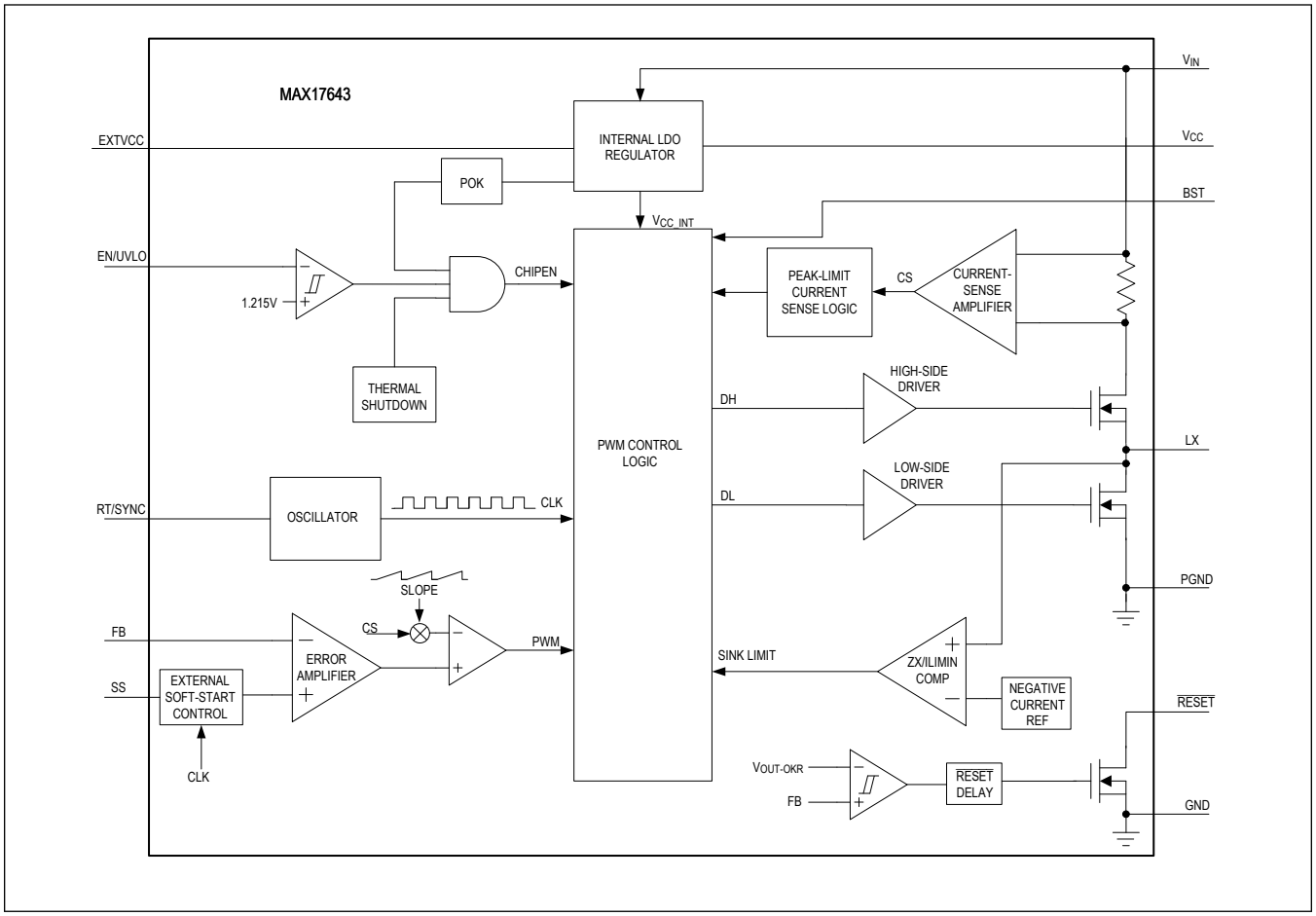



**TDFN-EP**
**(3mm x 3mm)**

## Pin Description

| PIN | NAME | FUNCTION |
|---|---|---|
| 1 | $V_{IN}$ | Power Supply Input. The input supply range is from 4.5V to 60V. |
| 2 | EN/UVLO | Enable/Undervoltage Lockout Input. Drive EN/UVLO high to enable the output voltage. Connect to the centre of the resistive divider between $V_{IN}$ and GND to set the input voltage (undervoltage threshold) at which the device turns on. Pull up to $V_{IN}$ for always-on. |
| 3 | $\overline{RESET}$ | Open-Drain $\overline{RESET}$ Output. The $\overline{RESET}$ output is driven low if FB drops below 92% of its set value. $\overline{RESET}$ goes high 1024 clock cycles after FB rises above 95% of its set value. $\overline{RESET}$ is valid when the device is enabled and $V_{IN}$ is above 4.5V. |
| 4 | SS | Soft-Start Input. Connect a capacitor from SS to GND to set the soft-start time. |
| 5 | $V_{CC}$ | 5V LDO Output. Bypass $V_{CC}$ with 2.2µF or 4.7µF ceramic capacitor to GND. |
| 6 | RT/SYNC | Oscillator Timing Resistor Input. Connect a resistor from RT/SYNC to GND to program the switching frequency from 400kHz to 2.2MHz. An external pulse can be applied to RT/SYNC through a coupling capacitor to synchronize the internal clock to the external pulse frequency. See the *Switching Frequency Selection and External Frequency Synchronization* section for details. |
| 7 | FB | Feedback Input. Connect FB to the center of the resistive divider between output voltage and GND. |
| 8 | GND | Analog Ground |
| 9 | EXTVCC | External Power-Supply Input for the Internal LDO. Applying a voltage between 4.84V and 24V at the EXTVCC pin bypasses the internal LDO and improves efficiency. |
| 10 | BST | Boost Strap Capacitor Node. Connect a 0.1µF ceramic capacitor between BST and LX. |
| 11 | LX | Switching Node. Connect LX to the switching side of the inductor. LX is high impedance when the device is in shutdown mode. |
| 12 | PGND | Power Ground. Connect PGND externally to the power ground plane. Connect GND and PGND pins together at the ground return path of the $V_{CC}$ bypass capacitor. |
| — | EP | Exposed Pad. Always connect EP to the GND pin of the IC. Also, connect EP to a large GND plane with several thermal vias for best thermal performance. Refer to the MAX17643 EV kit data sheet for an example of the correct method for EP connection and thermal vias. |

## Functional Diagram



## Detailed Description

The MAX17643 high-efficiency, high-voltage, synchronous step-down DC-DC converter with integrated MOSFETs operates over a 4.5V to 60V input. The converter can deliver up to 2A and generates output voltages from 0.9V up to (0.9 x $V_{IN}$)V. The feedback (FB) voltage is accurate to within ±1.4% over -40°C to +125°C.

The device features a peak-current-mode control architecture and operates in fixed frequency forced PWM mode. An internal transconductance error amplifier produces an integrated error voltage at an internal node that sets the duty cycle using a PWM comparator, a high-side current-sense amplifier, and a slope-compensation generator. At each rising edge of the clock, the high-side MOSFET turns on and remains on until either the appropriate or maximum duty cycle is reached, or the peak current limit is detected. During the high-side MOSFET on-time, the inductor current ramps up. During the second-half of the switching cycle, the high-side MOSFET turns off and the low-side MOSFET turns on. The inductor releases the stored energy as its current ramps down and provides current to the output.

The device features a RT/SYNC pin to program the switching frequency and to synchronize to an external clock. The device also features adjustable-input, undervoltage-lockout, adjustable soft-start, open-drain $\overline{RESET}$, and auxiliary bootstrap LDO.

### Linear Regulator ($V_{CC}$)

The device has two internal low-dropout regulators (LDOs), which power $V_{CC}$. One LDO is powered from $V_{IN}$ and the other LDO is powered from EXTVCC (EXTVCC LDO). Only one of the two LDOs is in operation at a time, depending on the voltage levels present at EXTVCC. If EXTVCC voltage is greater than 4.7V (typ), $V_{CC}$ is powered from EXTVCC. If EXTVCC is lower than 4.7V (typ), $V_{CC}$ is powered from $V_{IN}$. Powering $V_{CC}$ from EXTVCC increases efficiency at higher input voltages. EXTVCC voltage should not exceed 24V.

Typical $V_{CC}$ output voltage is 5V. Bypass $V_{CC}$ to GND with either a 2.2µF or a 4.7µF ceramic capacitor. $V_{CC}$ powers the internal blocks and the low-side MOSFET driver and recharges the external bootstrap capacitor. Both LDO can source up to 60mA (typ). The MAX17643 employs an undervoltage-lockout circuit that forces the converter off when $V_{CC}$ falls below 3.8V (typ). The converter is enabled again when $V_{CC}$ is higher than 4.2V. The 400mV UVLO hysteresis prevents chattering on power-up and power-down.

In applications where the buck converter output is connected to the EXTVCC pin, if the output is shorted to ground, then transfer from EXTVCC LDO to the internal LDO happens seamlessly without any impact on the normal functionality

### Switching Frequency Selection and External Frequency Synchronization

The switching frequency of the MAX17643 can be programmed from 400kHz to 2.2MHz by using a resistor connected from the RT/SYNC pin to GND. When no resistor is used, the frequency is programmed to 490kHz. The switching frequency ($f_{SW}$) is related to the resistor connected at the RT/SYNC pin ($R_{RT/SYNC}$) by the following equation:

$$R_{RT/SYNC} = \frac{21 \times 10^3}{f_{SW}} - 1.7$$

where $R_{RT/SYNC}$ is in kΩ and $f_{SW}$ is in kHz. See Table 1 for RT/SYNC resistor values for a few common switching frequencies.

The RT/SYNC pin can be used to synchronize the device internal oscillator to an external system clock. A resistor must be connected from the RT/SYNC pin to GND to be able to synchronize the MAX17643 to an external clock. The external clock should be coupled to the RT/SYNC pin through a network as shown in Figure 1. When an external clock is applied to the RT/SYNC pin, the internal oscillator frequency changes to the external clock frequency (from original frequency based on the RT/SYNC setting) after detecting 16 external clock edges. The external clock logic-high level should be higher than 2.1V, a logic-low level lower than 0.8V, and the pulse-width of the external clock should be more than 50ns. The RT/SYNC resistor should be selected to set the switching frequency at 10% lower than the external clock frequency

## Table 1. Switching Frequency vs. RT/SYNC Resistor

| SWITCHING FREQUENCY (kHz) | RT/SYNC RESISTOR (kΩ) |
|---|---|
| 500 | OPEN |

## Table 1. Switching Frequency vs. RT/SYNC Resistor (continued)

| SWITCHING FREQUENCY (kHz) | RT/SYNC RESISTOR (kΩ) |
|---|---|
| 1000 | 19.1 |
| 2200 | 8.06 |

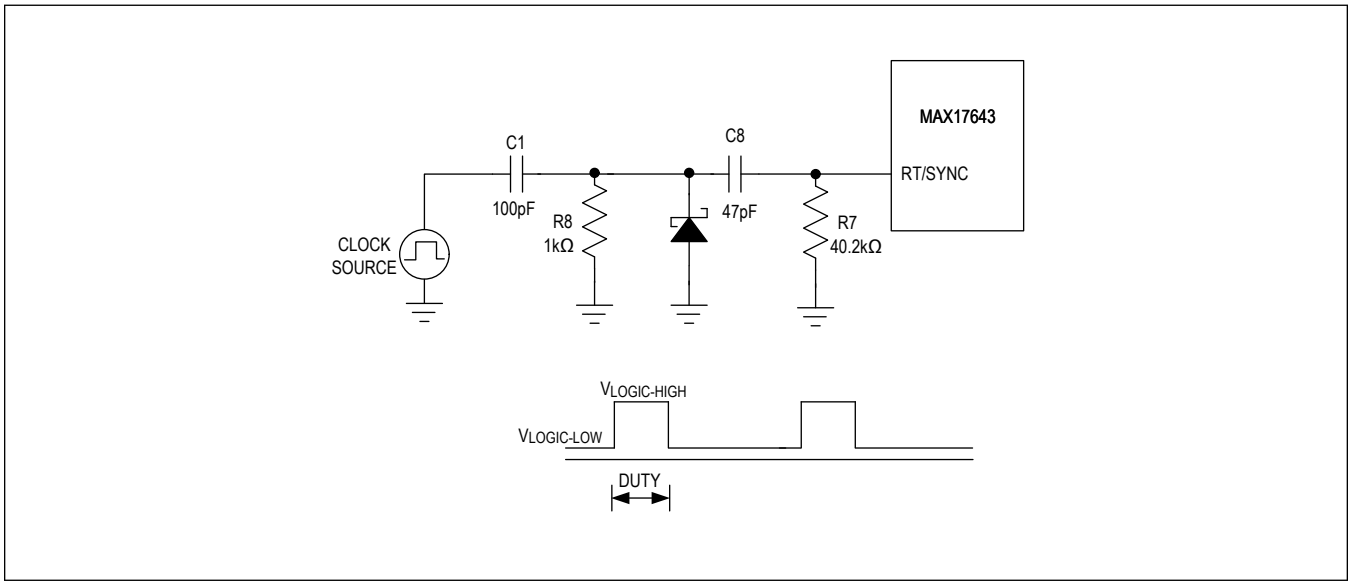



*Figure 1. External Clock Synchronization*

### Operating Input-Voltage Range

The minimum and maximum operating input voltages for a given output voltage should be calculated as follows:

$$V_{IN(MIN)} = \frac{V_{OUT} + (I_{OUT(MAX)} \times (R_{DCR(MAX)} + R_{DS\_ONL(MAX)}))}{1 - (f_{SW(MAX)} \times t_{OFF\_MIN(MAX)})} + (I_{OUT(MAX)} \times (R_{DS\_ONH(MAX)} - R_{DS\_ONL(MAX)}))$$

$$V_{IN(MAX)} = \frac{V_{OUT}}{f_{SW(MAX)} \times t_{ON\_MIN(MAX)}}$$

where:

$V_{OUT}$ = Steady-state output voltage

$I_{OUT(MAX)}$ = Maximum load current

$R_{DCR(MAX)}$ = Worst-case DC resistance of the inductor

$f_{SW(MAX)}$ = Maximum switching frequency

$t_{OFF\_MIN(MAX)}$ = Worst-case minimum switch off-time (160ns)

$t_{ON\_MIN(MAX)}$ = Worst-case minimum switch on-time (90ns)

$R_{DS\_ONH(MAX)}$ = Worst-case on-state resistances and high-side internal MOSFET

$R_{DS\_ONL(MAX)}$ = Worst-case on-state resistances and low-side external MOSFET

### Overcurrent Protection

The device is provided with a robust overcurrent protection scheme that protects the device under overload and output short-circuit conditions. A cycle-by-cycle peak current limit turns off the high-side MOSFET whenever the high-side switch

current exceeds an internal limit of 3.25A (typ). A runaway current limit on the high-side switch current at 3.6A (typ) protects the device under high input voltage, short-circuit conditions when there is insufficient output voltage available to restore the inductor current built up during the on period of the step-down converter. One occurrence of runaway current limit triggers a hiccup mode. In addition, due to any fault, if the feedback voltage drops below 0.58V any time after soft-start is completed, then hiccup mode is activated. In hiccup mode, the converter is protected by suspending switching for a hiccup timeout period of 32,768 clock cycles of half the switching frequency. Once the hiccup timeout period expires, soft-start is attempted again. Note that when soft-start is attempted under overload conditions, if feedback voltage does not exceed 0.58V, the device continues to switch at half the programmed switching frequency for the time duration of the programmed soft-start time and 1024 clock cycles. Hiccup mode of operation ensures low power dissipation under output short-circuit conditions.

### $\overline{\text{RESET}}$ Output

The device includes a $\overline{\text{RESET}}$ comparator to monitor the status of the output voltage. The open-drain $\overline{\text{RESET}}$ output requires an external pullup resistor. $\overline{\text{RESET}}$ goes high (high impedance) 1024 switching cycles after the regulator output increases above 95% of the designed nominal regulated voltage. $\overline{\text{RESET}}$ goes low when the regulator output voltage drops to below 92% of the set nominal output voltage. $\overline{\text{RESET}}$ also goes low during thermal shutdown or when the EN/UVLO pin goes below $V_{ENF}$.

### Thermal-Shutdown Protection

Thermal-shutdown protection limits total power dissipation in the device. When the junction temperature of the device exceeds +165°C, an on-chip thermal sensor shuts down the device, allowing the device to cool. The device turns on with soft-start after the junction temperature reduces by 15°C. The MAX17643 can enter thermal shutdown for load currents greater than 2A. Carefully evaluate the total power dissipation (see the *Power Dissipation* section) to avoid unwanted triggering of the thermal shutdown protection in normal operation.

## Applications Information

### Input Capacitor Selection

The input filter capacitor reduces peak currents drawn from the power source and reduces noise and voltage ripple on the input caused by circuit switching. The input capacitor RMS current ($I_{RMS}$) is defined by the following equation:

$$I_{RMS} = I_{OUT(MAX)} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{IN}}$$

where, $I_{OUT(MAX)}$ is the maximum load current. $I_{RMS}$ has a maximum value when the input voltage equals twice the output voltage ($V_{IN} = 2 \times V_{OUT}$), so $I_{RMS(MAX)} = \frac{I_{OUT(MAX)}}{2}$.

Choose an input capacitor that exhibits less than +10°C temperature rise at the RMS input current for optimal long-term reliability. Use low-ESR ceramic capacitors with high-ripple-current capability at the input. X7R capacitors are recommended in industrial applications for their temperature stability. Calculate the input capacitance using the following equation:

$$C_{IN} = \frac{I_{OUT(MAX)} \times D \times (1 - D)}{\eta \times f_{SW} \times \triangle V_{IN}}$$

where:

D = $V_{OUT}$ / $V_{IN}$ and is the duty ratio of the converter,

$f_{SW}$ = Switching frequency,

$\Delta V_{IN}$ = Allowable input voltage ripple

η = Efficiency

In applications where the source is located distant from the device input, an electrolytic capacitor should be added in parallel to the ceramic capacitor to provide necessary damping for potential oscillations caused by the inductance of the longer input power path and input ceramic capacitor.

### Inductor Selection

Three key inductor parameters must be specified for operation with the device: inductance value (L), inductor saturation current ($I_{SAT}$), and DC resistance ($R_{DCR}$). The switching frequency and output voltage determine the inductor value as follows:

$$L = \frac{1.1 \times V_{OUT}}{f_{SW}}$$

where $V_{OUT}$ and $f_{SW}$ are nominal values and $f_{SW}$ is in Hz. Select an inductor whose value is nearest to the value calculated by the previous formula.

Select a low-loss inductor closest to the calculated value with acceptable dimensions and having the lowest possible DC resistance. The saturation current rating ($I_{SAT}$) of the inductor must be high enough to ensure that saturation can occur only above the peak current-limit value.

### Output Capacitor Selection

X7R ceramic output capacitors are preferred due to their stability over temperature in industrial applications. The output capacitors are usually sized to support a step load of 50% of the maximum output current in the application, so the output voltage deviation is contained to 3% of the output-voltage change. The minimum required output capacitance can be calculated as follows: $C_{OUT} = \frac{90}{V_{OUT}}$

Where $C_{OUT}$ is in µF. Derating of ceramic capacitors with DC voltage must be considered while selecting the output capacitor. Derating curves are available from all major ceramic capacitor vendors.

## Soft-Start Capacitor Selection

The device implements adjustable soft-start operation to reduce inrush current. A capacitor connected from the SS pin to GND programs the soft-start time. The selected output capacitance ($C_{SEL}$) and the output voltage ($V_{OUT}$) determine the minimum required soft-start capacitor as follows:

$$C_{SS} \geq 56 \times 10^{-6} \times C_{SEL} \times V_{OUT}$$

The soft-start time ($t_{SS}$) is related to the capacitor connected at SS ($C_{SS}$) by the following equation:

$$t_{SS} = \frac{C_{SS}}{5.55 \times 10^{-6}}$$

For example, to program a 2ms soft-start time, a 12nF capacitor should be connected from the SS pin to GND. Note that during startup, the device operates at half the programmed switching frequency until the output voltage reaches 66.7% of the set output nominal voltage.

## Adjusting Output Voltage

Set the output voltage with a resistive voltage-divider connected from the positive terminal of the output capacitor ($V_{OUT}$) to SGND (see Figure 2). Connect the center node of the divider to the FB pin. Use the following procedure to choose the resistive voltage-divider values:

Calculate resistor R4 from the output to the FB pin as follows:

$$R4 = \frac{1635}{C_{OUT\_SEL}}$$

Where $C_{OUT\_SEL}$ (µF) is the actual derated value of the output capacitance used and R4 is in kΩ. The minimum allowable value of R4 is (5.6 x $V_{OUT}$), where R4 is in kΩ. If the value of R4 calculated using the above equation is less than (5.6 x $V_{OUT}$), increase the value of R4 to at least (5.6 x $V_{OUT}$).

$$R5 = \frac{R4 \times 0.9}{(V_{OUT} - 0.9)}$$

R5 is in kΩ.

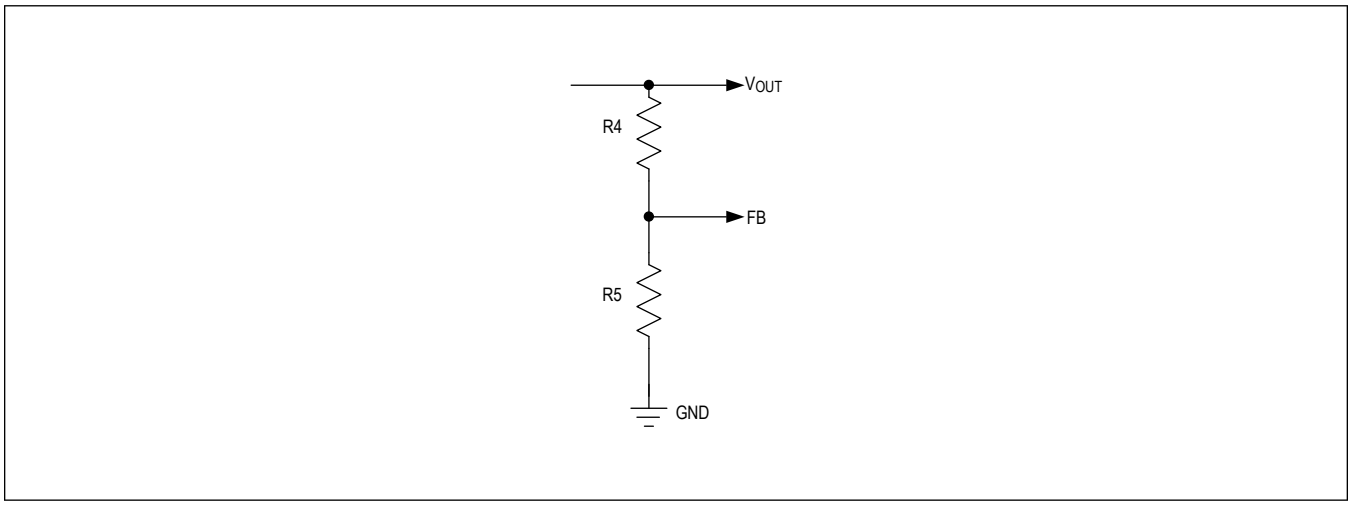



*Figure 2. Adjusting Output Voltage*

## Setting the Undervoltage Lockout Level

The device offers an adjustable input undervoltage-lockout level. Set the voltage at which the device turns on with a resistive voltage-divider connected from $V_{IN}$ to SGND (Figure 3). Connect the center node of the divider to EN/UVLO.

Choose R1 to be 3.32MΩ and then calculate R2 as follows:

$$R2 = \frac{1.215 \times R1}{(V_{INU} - 1.215)}$$

where $V_{INU}$ is the voltage at which the device is required to turn on. Ensure that $V_{INU}$ is higher than 0.8 x $V_{OUT}$. To avoid hiccup during slow power-up (slower than soft-start) or power-down.

If the EN/UVLO pin is driven from an external signal source, it is recommended that a series resistance of minimum 1kΩ is placed between the signal source output and the EN/UVLO pin to reduce voltage ringing on the line.

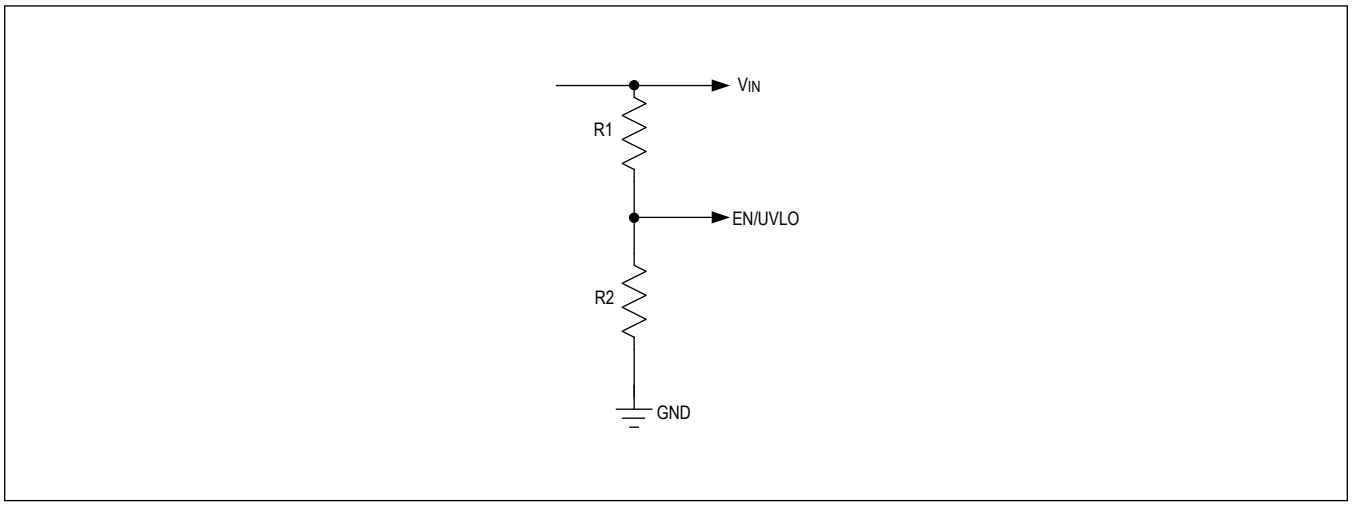



*Figure 3. Setting the Input Undervoltage Lockout*

## Power Dissipation

At a particular operating condition, the power losses that lead to temperature rise of the part are estimated as follows:

$$P_{LOSS} = (P_{OUT} \times (\frac{1}{\eta} - 1)) - (I_{OUT}^2 \times R_{DCR})$$

$$P_{OUT} = V_{OUT} \times I_{OUT}$$

where:

$P_{OUT}$ = Output power

$\eta$ = Efficiency of the converter

$R_{DCR}$ = DC resistance of the inductor (see the *Typical Operating Characteristics* for more information on efficiency at typical operating conditions).

For a typical multilayer board, the thermal performance metrics for the package are given below:

$\theta_{JA} = 41\ ^\circ C/W$

$\theta_{JC} = 8.5\ ^\circ C/W$

The junction temperature of the device can be estimated at any given maximum ambient temperature ($T_{A(MAX)}$) from the following equation:

$$T_{J(MAX)} = T_{A(MAX)} + (\theta_{JA} \times P_{LOSS})$$

If the application has a thermal-management system that ensures that the exposed pad of the device is maintained at a given temperature ($T_{EP(MAX)}$) by using proper heat sinks, the junction temperature of the device can be estimated at any given maximum ambient temperature as:

$T_{J(MAX)} = T_{EP(MAX)} + (\theta_{JC} \times P_{LOSS})$

Junction temperatures greater than +125°C degrades operating lifetimes.

## PCB Layout Guidelines

Careful PCB layout is critical to achieving a clean and stable operation. The switching power stage requires particular attention. Follow the guidelines below for a good PCB layout.

- Place the input ceramic capacitor as close as possible to the $V_{IN}$ and GND pins.
- Place the output capacitor as close as possible to the OUT pin.
- Place the GND terminals of the input capacitor, output capacitor, and the inductor as close as possible and connect them to the GND plane.
- Connect the negative terminal of the $V_{CC}$ bypass capacitor to the GND pin with shortest possible trace or ground plane.
- Minimize the area formed by the LX pin and the inductor connection to reduce the radiated EMI.
- Place the $V_{CC}$ decoupling capacitor as close as possible to the $V_{CC}$ pin.
- Place the BST capacitor close to the BST and LX pins.
- Place the RT/SYNC resistor and the feedback resistor divider as close as possible to their respective pins.
- Keep all the power connections and load connections short.
- Ensure that all feedback connections are short and direct.
- Route the high-speed switching node (LX) away from the FB/$V_{OUT}$, $\overline{\text{RESET}}$, and MODE pins.

For a sample layout that ensures first pass success, refer to the MAX17643 evaluation kit layout available at www.maximintegrated.com.

## Typical Application Circuits

### 5V Output with 500kHz Switching Frequency

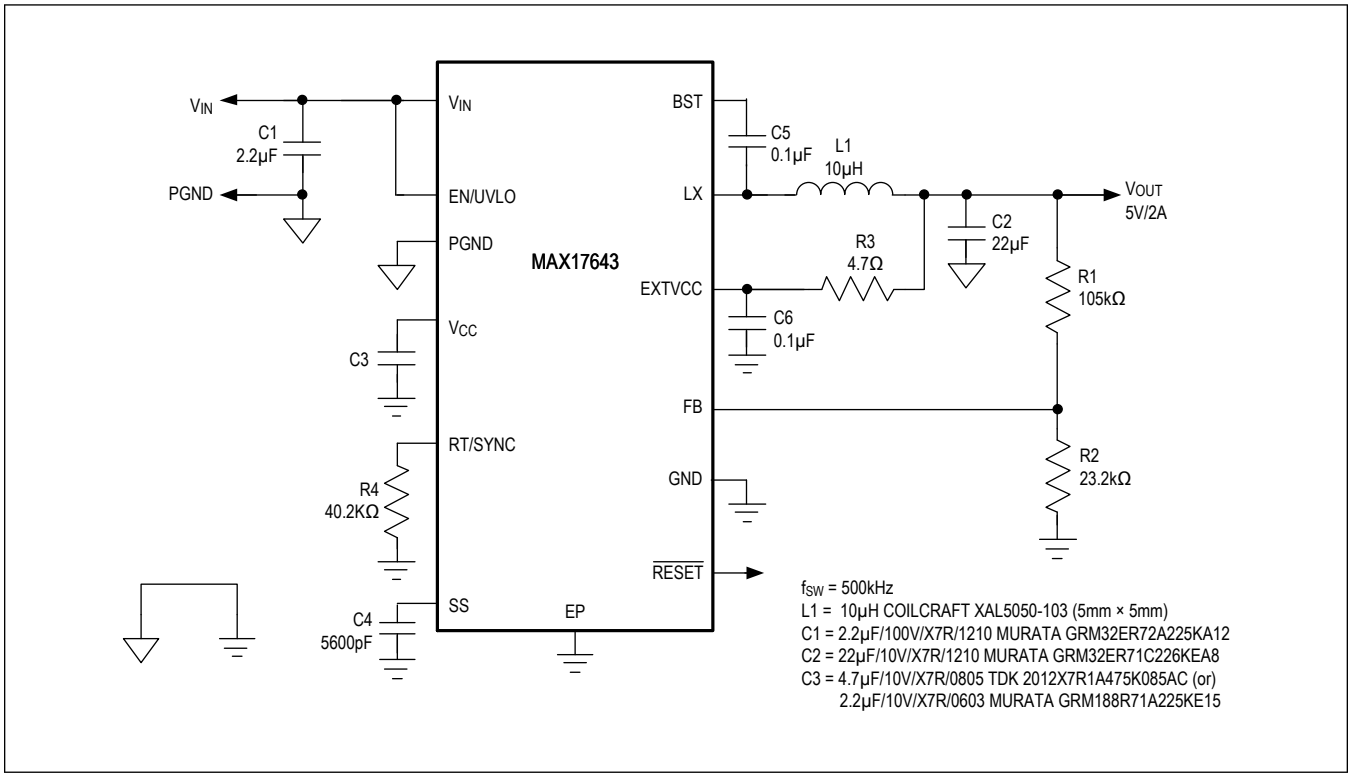



*Figure 4. Typical Application Circuit for 5V Output with 500kHz Switching Frequency*

## Typical Application Circuits (continued)

### 3.3V Output with 500kHz Switching Frequency

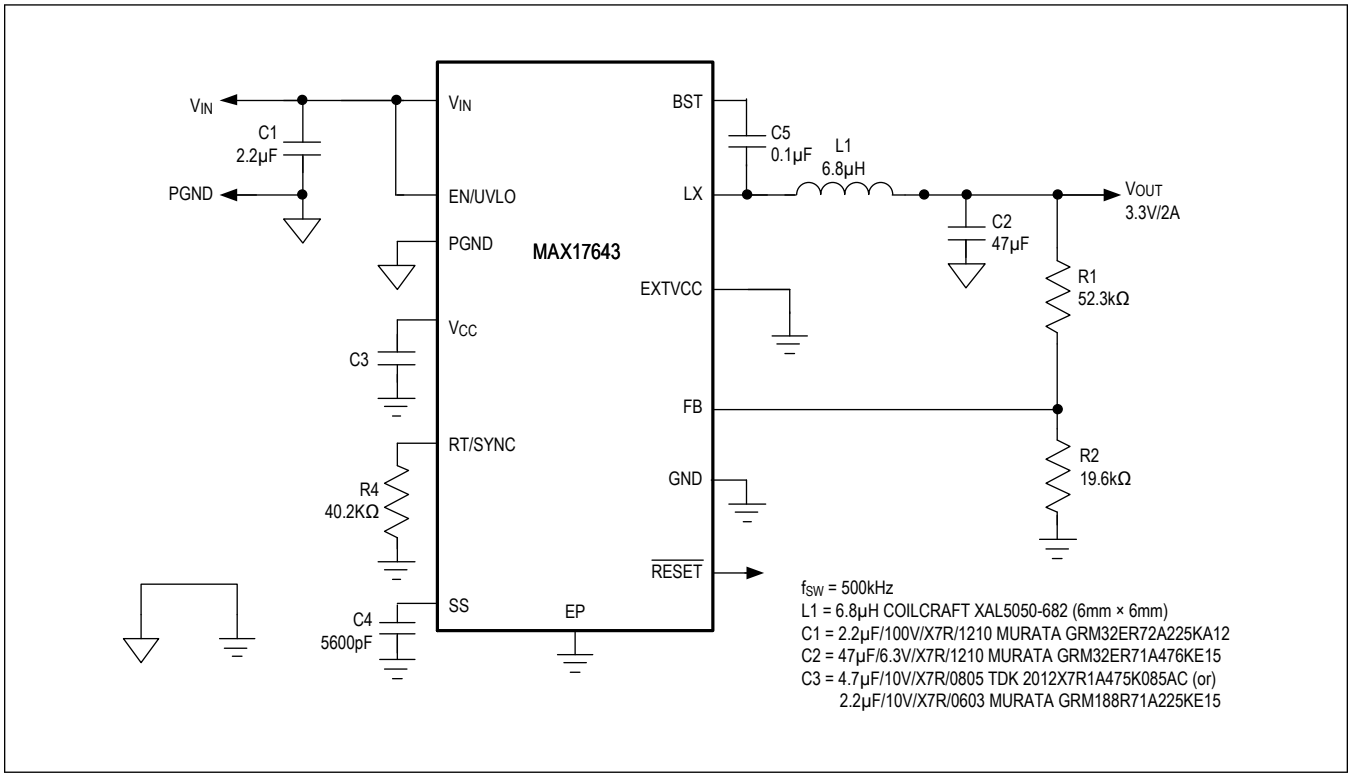



*Figure 5. Typical Application Circuit for 3.3V Output with 500kHz Switching Frequency*

## Ordering Information

| PART | PIN-PACKAGE | PACKAGE SIZE |
|---|---|---|
| MAX17643ATC+ | 12-TDFN EP* | 3mm x 3mm |
| MAX17643ATC+T | 12-TDFN EP* | 3mm x 3mm |

*+Denotes a lead(Pb)-free/RoHS-compliant package.*

*T = Tape and reel.*

**EP = Exposed pad.*

## Revision History

| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|---|---|---|---|
| 0 | 10/20 | Release for Market Intro | — |
| 1 | 9/21 | Updated the *Benefits and Features*, added TOC 20 and 21 | 1, 7 |

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