5.5V, 3A Ultralow Noise, High PSRR, 45mV Dropout Linear Regulator with PMBus

FEATURES

- Ultralow RMS Noise: 1.2µV_{RMS} (10Hz to 100kHz)
- Ultralow Spot Noise: 3.5nV/√Hz at 10kHz
- Ultralow 1/f Noise: 7µVP-P (0.1Hz to 10Hz)
- High PSRR at High Frequency: 52dB at 1MHz
- Ultrafast Transient Response
- Dropout Voltage: 45mV Typical
- 100µA Reference Current: ±0.5% Initial Accuracy
- Precision Current Monitor: ±3% Accuracy at 3A
- PMBus Capability Includes:
  - V_{OUT}, I_{OUT}, V_{IN}, V_{BIAS}, and Temperature Reporting
  - V_{OUT} Margining
  - I_{OUT} Overcurrent and Undercurrent Warn Limits
  - V_{OUT}, V_{IN}, and V_{BIAS} Undervoltage and Overvoltage Warn Limits
  - Overtemperature Warn Limit
- Stable with Ceramic Output Capacitors (10µF Minimum)
- Parallel Multiple Devices for Higher Current
- VIOC Pin to Control Upstream Switching Converter
- 22-Lead (3mm × 4mm) LQFN Package

APPLICATIONS

- RF Power Supplies: PLLs, VCOs, Mixers, LNAs, PAs
- High Speed/High Precision Data Converters
- Low Noise Instrumentation
- Post-Regulator for Switching Supplies
- FPGA and DSP Power Supplies
- Medical Applications

GENERAL DESCRIPTION

The LT3074 is a low voltage, ultralow noise, and ultrafast transient response linear regulator with a PMBus serial interface. The device supplies up to 3A with a typical dropout voltage of 45mV. A 4.7µF reference bypass capacitor decreases output voltage noise to 1.2µV_{RMS}. The wide bandwidth and high PSRR permit the use of small ceramic capacitors, saving bulk capacitance and cost. The LT3074 is supported by the LTPowerPlay software development tool with a graphical user interface (GUI).

The LT3074 sources a 100µA precision reference current to the LT3074's SETRES pin. Placing a resistor from this SETRES pin to GND sets the output voltage. The LT3074's unity-gain operation provides virtually constant output noise, PSRR, bandwidth and load regulation, independent of the programmed output voltage. Additionally, the LT3074 incorporates a unique tracking feature (VIOC) to control the upstream switching regulator to maintain a constant voltage across the LT3074, and hence minimize power dissipation.

The PMBus control allows to set the output current limit from 1A to 6.4A in discrete steps of 0.05A. The PMBus Telemetry feature provides information regarding the output voltage and current, input voltage, bias voltage and die temperature. The LT3074 features a CLKDIS pin to control the internal clock. Pulling this pin to BIAS disables the internal clocks to put LT3074 in the "quiet mode". The LT3074 is available in a compact 22 lead (3mm × 4mm) LQFN package (laminate package with QFN footprint).

SIMPLIFIED APPLICATION DIAGRAM

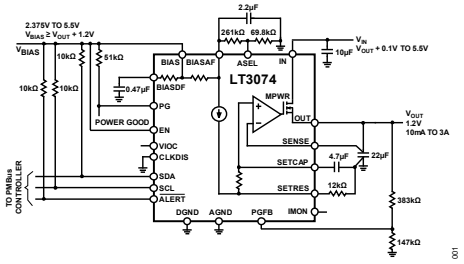

Figure 1. Simplified Application Diagram

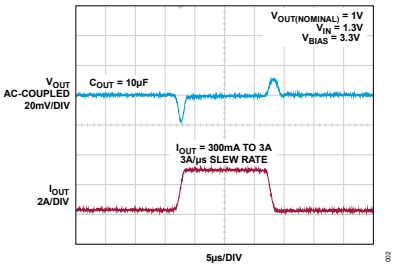

Figure 2. Transient Response

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REVISION HISTORY

10/2024 - Rev 0: Initial Release

SPECIFICATIONS

Table 1. Electrical Characteristics

(All typical specifications are at T_J (junction temperature). = 25°C and all min. and max. specifications are across the entire operating temperature range, unless otherwise noted. C_{OUT} = 22µF, C_{SETCAP} = 4.7µF, C_{BIASAF} = 2.2µF, and C_{BIASDF} = 0.47µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
IN Pin Voltage	V_{IN}					5.5	V
BIAS Pin Voltage [1]	V_{BIAS}			2.375		5.5	V
SETRES Pin Current[3]	I_{SETRES}	Max [2.375, V_{OUT} + 1.2V] ≤ V_{BIAS} ≤ 5.5V, V_{OUT} + 0.2V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ 4.2V, 50mA ≤ I_{OUT} ≤ 3A, MFR_MARGIN = 8'h00	T_J = 25°C	99.5	100	100.5	µA
SETRES Pin Current	I_{SETRES}	Max [2.375, V_{OUT} + 1.2V] ≤ V_{BIAS} ≤ 5.5V, V_{OUT} + 0.2V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ 4.2V, 50mA ≤ I_{OUT} ≤ 3A, MFR_MARGIN = 8'h00		99	100	101	µA
Output Offset Voltage	V_{OS}	V_{BIAS} = 2.375V, V_{IN} = 1.2V, V_{OUT} = 1V, I_{OUT} = 10mA		−1		1	mV
		Max [2.375V, V_{OUT} + 1.2V] ≤ V_{BIAS} ≤ 5.5V, 50mA ≤ I_{OUT} ≤ 3A, V_{OUT} + 0.2V ≤ V_{IN} ≤ 5.5V, 0.5V ≤ V_{OUT} ≤ 4.2V		−2		2	
I_{SETRES} Line Regulation to V_{IN}	ΔI_{SETRES} = $f(\Delta V_{IN})$	V_{OUT} = 0.5V, ΔV_{IN} = 0.7V to 5.5V, V_{BIAS} = 2.375V, I_{OUT} = 50mA				50	nA
		V_{OUT} = 4.2V, ΔV_{IN} = 4.4V to 5.5V, V_{BIAS} = 5.5V, I_{OUT} = 10mA				50	
V_{OUT} Line Regulation to V_{IN}	ΔV_{OUT} = $f(\Delta V_{IN})$	V_{OUT} = 0.5V, ΔV_{IN} = 0.7V to 5.5V, V_{BIAS} = 2.375V, I_{OUT} = 50mA				0.5	mV
		V_{OUT} = 4.2V, ΔV_{IN} = 4.4V to 5.5V, V_{BIAS} = 5.5V, I_{OUT} = 10mA				0.6	
I_{SETRES} Line Regulation to V_{BIAS}	ΔI_{SETRES} = $f(\Delta V_{BIAS})$	V_{OUT} = 0.5V, ΔV_{BIAS} = 2.375V to 5.5V, V_{IN} = 0.7V, I_{OUT} = 50mA				100	nA
		V_{OUT} = 3.3V, ΔV_{BIAS} = 4.5V to 5.5V, V_{IN} = 3.5V, I_{OUT} = 10mA				100	
V_{OUT} Line Regulation to V_{BIAS}		V_{OUT} = 0.5V, ΔV_{BIAS} = 2.375V to 5.5V, V_{IN} = 0.7V, I_{OUT} = 50mA				0.25	mV

(All typical specifications are at T_J (junction temperature). = 25°C and all min. and max. specifications are across the entire operating temperature range, unless otherwise noted. C_{OUT} = 22µF, C_{SETCAP} = 4.7µF, C_{BIASAF} = 2.2µF, and C_{BIASDF} = 0.47µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
	ΔV_{OUT} = $f(\Delta V_{BIAS})$	V_{OUT} = 3.3V, ΔV_{BIAS} = 4.5V to 5.5V, V_{IN} = 3.5V, I_{OUT} = 10mA				2	
I_{SETRES} Load Regulation [1]	ΔI_{SETRES} = $f(\Delta I_{OUT})$	V_{BIAS} = 2.375V, V_{SETRES} = V_{OUT} = 1V, V_{IN} = 1.2V, ΔI_{OUT} = 10mA to 3A			50		nA
						100	
V_{OUT} Load Regulation [1]	ΔV_{OUT} = $f(\Delta I_{OUT})$	ΔI_{OUT} = 50mA to 3A	V_{BIAS} = 2.375V, V_{IN} = 0.7V, V_{OUT} = 0.5V			0.6	mV
V_{OUT} Load Regulation	ΔV_{OUT} = $f(\Delta I_{OUT})$	ΔI_{OUT} = 10mA to 3A	V_{BIAS} = 2.4V, V_{IN} = 1.4V, V_{OUT} = 1.2V			1.2	mV
			V_{BIAS} = 4.5V, V_{IN} = 3.5V, V_{OUT} = 3.3V			3.3	
			V_{BIAS} = 5.4V, V_{IN} = 4.4V, V_{OUT} = 4.2V			4.2	
I_{SETRES} Common Mode Regulation	ΔI_{SETRES} = $f(\Delta V_{SETRES})$	V_{IN} = 5.5V, V_{BIAS} = 5.5V, 0.5V ≤ V_{OUT} = V_{SETRES} ≤ 0.8V, I_{OUT} = 50mA				50	nA
		V_{IN} = 5.5V, V_{BIAS} = 5.5V, 0.8V ≤ V_{OUT} = V_{SETRES} ≤ 4.2V, I_{OUT} = 10mA				200	
Output Offset Voltage Common Mode Regulation	ΔV_{OS} = $f(\Delta V_{SETRES})$	V_{IN} = 5.5V, V_{BIAS} = 5.5V, 0.5V ≤ V_{OUT} = V_{SETRES} ≤ 0.8V, I_{OUT} = 50mA				0.5	mV
		V_{IN} = 5.5V, V_{BIAS} = 5.5V, 0.8V ≤ V_{OUT} = V_{SETRES} ≤ 4.2V, I_{OUT} = 10mA				0.8	
V_{OUT} Margining Accuracy		MFR_MARGIN = 8'h33		±4	±5	±6.5	%
		MFR_MARGIN = 8'h88		±25	±30	±37.5	
Dropout Voltage [2]	V_{DO}	V_{IN} = $V_{OUT(NOMINAL)}$, V_{BIAS} ≥ V_{OUT} + 1.2V, I_{OUT} = 1A	T_J = 25°C		15	22	mV
						33	
		V_{IN} = $V_{OUT(NOMINAL)}$, V_{BIAS} ≥ V_{OUT} + 1.2V, I_{OUT} = 2A	T_J = 25°C		30	44	
						66	
		V_{IN} = $V_{OUT(NOMINAL)}$, V_{BIAS} ≥ V_{OUT} + 1.2V, I_{OUT} = 3A	T_J = 25°C		45	65	
						100	
Minimum Load Current	$I_{OUT(MIN)}$	V_{OUT} ≥ 0.8V				10	mA
		V_{OUT} < 0.8V				50	
Ground Pin Current	I_{GND}	V_{IN} = 1.4V, V_{OUT} = 1.2V, V_{BIAS} = 2.5V	I_{OUT} = 10mA		4.6	7.9	mA
			I_{OUT} = 3A		4.9	9.8	

(All typical specifications are at T_J (junction temperature). = 25°C and all min. and max. specifications are across the entire operating temperature range, unless otherwise noted. C_{OUT} = 22µF, C_{SETCAP} = 4.7µF, C_{BIASAF} = 2.2µF, and C_{BIASDF} = 0.47µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
BIAS Pin Current	I_{BIAS}	V_{IN} = 1.4V, V_{OUT} = 1.2V, V_{BIAS} = 2.5V	I_{OUT} = 10mA		4.7	9	mA
BIAS Pin Current	I_{BIAS}	V_{IN} = 1.4V, V_{OUT} = 1.2V, V_{BIAS} = 2.5V	I_{OUT} = 3A		5.7	10	mA
BIAS Pin Current in Dropout [2]	I_{BIAS_DO}	V_{BIAS} = V_{OUT} +1.2V, V_{IN} = V_{OUT}, I_{OUT} = 3A			5.2	11	mA
		V_{BIAS} = 5.5V, V_{IN} = V_{OUT}, I_{OUT} = 3A			40	60	
BIAS Pin Current in Shutdown (Nap Mode)	I_{BIAS_NAP}	V_{BIAS} = 5.5V, EN = 0V				200	µA
IMON Pin Voltage	V_{IMON}	I_{OUT} = 3A, V_{IN} – V_{OUT} = 0.2V		0.97	1	1.03	V
		I_{OUT} = 1A, V_{IN} – V_{OUT} = 0.2V		311.7	333.3	353.3	mV
Programmable Current Limit [3]	$I_{LIM(P)}$	IOUT_OC_FAULT_LIMIT = 16'h0003		2.92	3.04	3.14	A
		IOUT_OC_FAULT_LIMIT = 16'h0001		0.95	1.02	1.085	
Internal Current Limit [3]	$I_{ILIM(I)}$	V_{IN} =1.5V, ΔV_{OUT} = -5%, V_{BIAS} = 5.5V			4.5	6	A
PGFB Pin Threshold		PGFB Rising		295	300	305	mV
		Hysteresis			8		
PG Low Voltage	V_{PG_OL}	I_{PG} = 200µA, V_{PGFB} = 250mV			60	100	mV
CLKDIS Threshold		Input High Voltage		V_{BIAS} – 0.3			V
		Input Low Voltage				0.3	
CLKDIS Leakage Current		V_{CLKDIS} = 5.5V				100	nA
SETCAP Pin Current	I_{SETCAP}	V_{SETRES} – V_{SETCAP} ≥ 100mV (Fast Start Enabled)			2		mA
Fast Start-Up Threshold		Turn On (Measured as V_{SETRES} – V_{SETCAP})		10		75	mV
		Turn Off (Measured as V_{SETRES} – V_{SETCAP})		-5		15	
Temperature Output Error [4]		T_J = 25°C		−5		5	°C
		0°C ≤ T_J ≤ 125°C		−9		9	
Thermal Shutdown	TSDN	T_J Rising			168		°C
		Hysteresis			7		
BIAS Pin Undervoltage Lock Out	$V_{BIAS(UVLO)}$	EN = V_{BIAS}, V_{IN} = 0V, V_{OUT} = 0V	V_{BIAS} Rising	2.11	2.16	2.2	V
			V_{BIAS} Falling	1.96	2.02	2.06	
Input-to-Output Differential Voltage Control [5]	$VIOC_{AV}$	VIOC Amplifier Gain			1		V/V

(All typical specifications are at T_J (junction temperature). = 25°C and all min. and max. specifications are across the entire operating temperature range, unless otherwise noted. C_{OUT} = 22µF, C_{SETCAP} = 4.7µF, C_{BIASAF} = 2.2µF, and C_{BIASDF} = 0.47µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Input-to-Output Differential Voltage Control [5]	$VIOC_{VOS}$	VIOC Amplifier Offset		790	800	810	mV
	$VIOC_{ISOURCE}$	VIOC Pin Source Current: V_{BIAS} > VIOC + 1V		200			µA
	$VIOC_{ISINK}$	VIOC Pin Sink Current: V_{BIAS} > VIOC + 1V			20		
EN Pin Threshold	EN_{VTHR}	EN Trip Point Rising, V_{BIAS} = 2.375V		1.20	1.26	1.32	V
	EN_{VTHF}	EN Trip Point Hysteresis, V_{BIAS} = 2.375V			80		mV
EN Pin Current	I_{EN}	0V ≤ V_{EN} ≤ 5.5V, V_{BIAS} = 5.5V				5	µA
		V_{EN} = 5.5V, V_{BIAS} = 0V			10	20	
ASEL Pin Leakage Current	I_{ASEL}	0V ≤ V_{ASEL} ≤ 5.5V, V_{BIAS} = 0V				1	µA
BIAS Ripple Rejection	$PSRR_{BIAS}$	V_{BIAS} = 5V (Avg.), V_{IN} = 1.3V, V_{SETRES} = V_{OUT} = 1.0V	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{OUT} = 3A		114		dB
			V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 1MHz, I_{OUT} = 3A		67		
IN Ripple Rejection	$PSRR_{IN}$	V_{BIAS} = 5V, V_{IN} = 1.3V (Avg.), V_{SETRES} = V_{OUT} = 1.0V	V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 120Hz, I_{OUT} = 3A		90		dB
			V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 1MHz, I_{OUT} = 3A		52		
Output RMS Noise [6]	$V_{RMS(OUT)}$	V_{OUT} = 1V, I_{OUT} = 3A, V_{IN} = 1.3V, V_{BIAS} = 3.3V, C_{OUT} = 22µF	BW = 10Hz to 100kHz, C_{SETCAP} = 0.47µF		1.6		$µV_{RMS}$
			BW = 10Hz to 100kHz, C_{SETCAP} = 4.7µF		1.2		
Output Noise Spectral Density [6]	$V_{n(OUT)}$	V_{OUT} = 1V, I_{OUT} = 3A, V_{IN} = 1.3V, V_{BIAS} = 3.3V, C_{SETCAP} = 0.47µF	Frequency = 0.1Hz		2.4		µV/√Hz
			Frequency = 10Hz		650		nV/√Hz
			Frequency = 10kHz		3.5		
			Frequency = 100kHz		3		

(All typical specifications are at T_J (junction temperature). = 25°C and all min. and max. specifications are across the entire operating temperature range, unless otherwise noted. C_{OUT} = 22µF, C_{SETCAP} = 4.7µF, C_{BIASAF} = 2.2µF, and C_{BIASDF} = 0.47µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Output Noise Spectral Density [6]	$V_{n(OUT)}$	V_{OUT} = 1V, I_{OUT} = 3A, V_{IN} = 1.3V, V_{BIAS} = 3.3V, C_{SETCAP} = 4.7µF	Frequency = 0.1Hz		1.4		µV/√Hz
			Frequency = 10Hz		40		nV/√Hz
			Frequency = 10kHz		3.5		
			Frequency = 100kHz		3		
Output Voltage Readback		Resolution			12		Bits
	V_{OUT_FS}	Full Scale Voltage			6.25		V
		Accuracy	V_{OUT} = 4.2V	-1		1	%
		Zero Code Offset			−8		mV
	t_{CONV_VOUT}	Conversion Time	T_J = 25°C		4.096		msec
	$t_{REFRESH\_VOUT}$	Refresh Rate	T_J = 25°C		9.216		
Output Current Readback		Resolution			12		Bits
	I_{OUT_FS}	Full Scale Current			9.375		A
		Accuracy	I_{OUT} = 3A	−3		3	%
		Zero Code Offset			−12		mA
	t_{CONV_IOUT}	Conversion Time	T_J = 25°C		4.096		msec
	$t_{REFRESH\_IOUT}$	Refresh Rate	T_J = 25°C		9.216		
Input Voltage Readback		Resolution			10		Bits
	V_{IN_FS}	Full Scale Voltage			6.25		V
		Accuracy	V_{IN} = 5.5V	−1		1	%
		Zero Code Offset			−8		mV
	t_{CONV_VIN}	Conversion Time	T_J = 25°C		1.024		msec
	$t_{REFRESH\_VIN}$	Refresh Rate	T_J = 25°C		27.648		
Bias Voltage Readback		Resolution			10		Bits
	V_{BIAS_FS}	Full Scale Voltage			6.25		V
		Accuracy	V_{BIAS} = 5.5V	−1		1	%
		Zero Code Offset			-8		mV
	t_{CONV_VBIAS}	Conversion Time	T_J = 25°C		1.024		msec
	$t_{REFRESH\_VBIAS}$	Refresh Rate	T_J = 25°C		27.648		
Temperature Readback		Resolution			10		Bits
		Full Scale Temperature			312.5		°C
		Accuracy	T_J = 25°C	−5		5	
		Zero Code Offset			−0.4		
	t_{CONV_TEMP}	Conversion Time	T_J = 25°C		1.024		msec

(All typical specifications are at T_J (junction temperature). = 25°C and all min. and max. specifications are across the entire operating temperature range, unless otherwise noted. C_{OUT} = 22µF, C_{SETCAP} = 4.7µF, C_{BIASAF} = 2.2µF, and C_{BIASDF} = 0.47µF, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS/COMMENTS		MIN	TYP	MAX	UNITS
Temperature Readback	$t_{REFRESH\_TEMP}$	Refresh Rate	T_J = 25°C		46.08		msec
Digital Inputs (SCL, SDA)	V_{IH}	Input High Voltage		1.35			V
	V_{IL}	Input Low Voltage				0.8	
	V_{HYST}	Input Hysteresis	T_J = 25°C		0.235		
	C_{PIN}	Input Capacitance				10	pF
Open Drain Outputs (SCL, SDA, $\overline{ALERT}$)	V_{OL}	Output Low Voltage, I_{SINK} = 6mA				0.4	V
	I_{LEAK}	Output Leakage Current, 0V ≤ V_{PIN} ≤ 5.5V				5	µA
Serial Bus Operating Frequency	f_{SCL}			10		400	kHz
Bus Free Time Between Start and Stop	t_{BUF}			1.3			µsec
Hold Time After Start Condition (after this period, the first clock is generated).	$t_{HD(STA)}$			0.6			µsec
Repeated Start Condition Setup Time	$t_{SU(STA)}$			0.6		10000	µsec
Stop Condition Setup Time	$t_{SU(STO)}$			0.6			µsec
Data Hold Time	$t_{HD(DAT)}$	Receiving Data		0			µsec
		Sending Data		0.3		0.9	
Data Setup Time	$t_{SU(DAT)}$			0.1			µsec
Stuck PMBus Timer	$t_{TIMEOUT\_SMB}$				35		msec
Serial Clock Low Period	t_{LOW}			1.3		10000	µsec
Serial Clock High Period	t_{HIGH}			0.6			µsec

[1] To maintain proper performance and regulation, the BIAS voltage must satisfy the following conditions: 2.375V ≤ V_{BIAS} ≤ 5.5V and V_{BIAS} ≥ (V_{OUT} + 1.2V).

[2] Dropout voltage, V_{DO}, is the minimum input-to-output voltage differential at a specified output current. In dropout, the output voltage equals V_{IN} – V_{DO}.

[3] Operating conditions are limited by maximum junction temperature. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current. When operating at maximum output current, limit the input voltage range to V_{IN} ≤ V_{OUT} + 600mV.

[4] The temperature reported represents the average temperature of the LT3074's power device. Due to power dissipation, temperature gradients, and thermal time constants across the die, the reported temperature

measurement is not guaranteed to precisely track transient power excursions in the power device. The internal thermal shutdown sensor is designed to keep the LT3074 within its safe operating area.

[5] The VIOC buffer outputs a voltage equal to $V_{IN} - V_{OUT} + 800mV$. See the *Applications Information* section for further information. The VIOC pin's source current should be set between 10µA and 200µA. The minimum voltage required from BIAS to VIOC is 1V.

[6] Adding a capacitor at the SETCAP pin decreases output voltage noise. Adding this capacitor bypasses the reference resistor's thermal noise as well as the reference current's noise. The output noise then equals the error amplifier noise. Use of a SETCAP pin bypass capacitor also increases start-up time.

ABSOLUTE MAXIMUM RATINGS

Table 2. Absolute Maximum Ratings

PARAMETER	RATING
IN Pin Voltage [1]	−0.3V to 6V
OUT Pin Voltage [1]	−0.3V to 6V
SENSE Pin Voltage [1]	−0.3V to 6V
BIAS, BIASAF, BIASDF Pin Voltage [1]	−0.3V to 6V
SCL, SDA, $\overline{\text{ALERT}}$ Pin Voltage [1]	−0.3V to 5.5V
EN Pin Voltage [1]	−0.3V to 6V
VIOC Pin Voltage [1]	−0.3V to 6V
VIOC Pin Current	−1mA to 1mA
IMON Pin Voltage [1]	−0.3V to 6V
PGFB Pin Voltage [1]	−0.3V to 6V
PG Pin Voltage [1]	−0.3V to 6V
SETRES, SETCAP Pin Voltage [1]	−0.3V to 6V
ASEL Pin Voltage [1]	−0.3V to 5.5V
CLKDIS Pin Voltage [1]	−0.3V to 5.5V
AGND to DGND Differential Voltage	−0.3V to 0.3V
Output Short-Circuit Duration	Indefinite
Operating Junction Temperature [2]	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Maximum Reflow (Package Body) Temperature	+260°C

[1] Parasitic diodes exist internally between IN, OUT, SENSE, BIAS, BIASAF, BIASDF, ASEL, SCL, SDA, $\overline{\text{ALERT}}$, EN, VIOC, CLKDIS, IMON, PG, SETRES, SETCAP, and PGFB pins, and GND. Do not drive these pins more than 0.3V below the GND pin during a fault condition. These pins must remain at a voltage more positive than GND during normal operation.

[2] The LT3074A is tested and specified under pulse load conditions such that $T_J \approx T_A$ (ambient temperature). The LT3074A is tested at T_A = 25°C. Performance of the LT3074A over the full –40°C and 125°C operating temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3074A is guaranteed over the full –40°C to 125°C operating junction temperature range.

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Thermal Resistance

Thermal performance is directly linked to PCB design and operating environment. Close attention to PCB thermal design is required.

Table 3. Thermal Resistance

PACKAGE TYPE [1]	θ_{JA}	θ_{JCTOP}	θ_{JCBOT}	UNIT
22-LEAD 3mm × 4mm LQFN	33	47	3.5	°C/W

[1] θ values are determined per JESD51. θ_{JA} value is obtained with demo board.

Electrostatic Discharge (ESD)

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only Human body model (HBM) per ANSI/ESDA/JEDEC JS-001 Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings

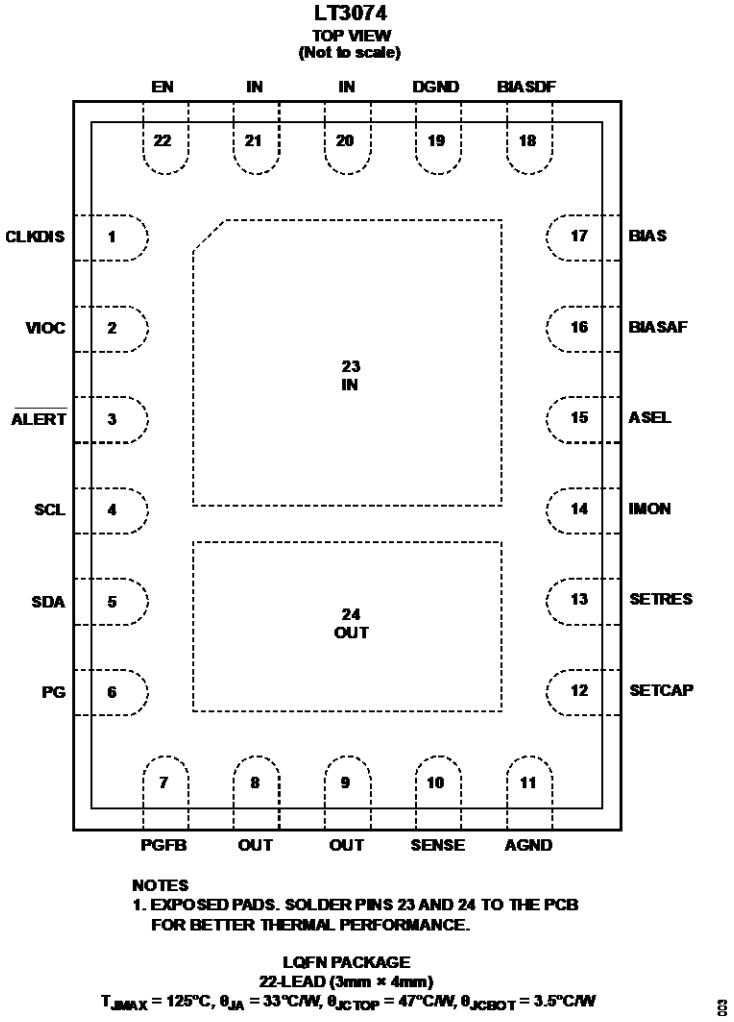
Table 4. LT3074, 22-Lead 3mm X 4mm LQFN

ESD Model	Withstand Threshold (V)	Class
HBM	3500	2
CDM	1250	C5

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high-energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



LQFN PACKAGE
22-LEAD (3mm X 4mm)
T_{JMAX} = 125°C, θ_{JA} = 33°C/W, θ_{JCTOP} = 47°C/W, θ_{JCBOT} = 3.5°C/W

Figure 3. Pin Configuration

Table 5. Pin Descriptions

PIN	NAME	DESCRIPTION
1	CLKDIS	Clock Disable. Pulling this pin high disables the internal high-frequency clocks and puts the part in a quiet mode. If not used, tie this pin to DGND. DO NOT FLOAT THIS PIN.
2	VIOC	Voltage for In-to-Out Control. The LT3074 incorporates a unique tracking feature (VIOC) to control the upstream switching regulator to maintain a constant voltage across the LT3074 and hence minimize power dissipation. See the *Applications Information* section for more information on proper control of the upstream switching regulator.

3	$\overline{\text{ALERT}}$	Open-Drain Digital Output. Connect the $\overline{\text{SMBALERT}}$ signal to this pin. A pull-up resistor to the highest supply rail is required in the application.
4	SCL	Serial Bus Clock Input. Open-Drain Output. A pull-up resistor to the highest supply rail is required in the application.
5	SDA	Serial Bus Data Input and Output. Open-Drain Output. A pull-up resistor to the highest supply rail is required in the application.
6	PG	Power Good. PG is an open-drain flag that indicates output voltage regulation. PG pulls low if PGFB is below 300mV on the PGFB rising edge. If power good functionality is not needed, float the PG pin. See the *Applications Information* section for more information.
7	PGFB	Power Good Feedback. The PG pin pulls high if the PGFB pin increases beyond 300mV on its rising edge, with 8mV hysteresis on its falling edge. Connecting an external resistor divider between OUT, PGFB, and AGND sets the programmable power good threshold with the following transfer function: 0.3V x $(1 + R_{PG2}/R_{PG1})$, where R_{PG1} is the resistor tied from PGFB to AGND and R_{PG2} is the resistor tied from OUT to PGFB. Tie PGFB to BIASAF if power good functionality is not required.
8, 9, Exposed Pad 24	OUT	Output. Pins 8, 9, and exposed pad 24 of the LQFN package are the electrical connection to OUT. These pins supply power to the load. Tie all OUT pins together for proper performance and solder pin 24 to the PCB for better thermal performance. A minimum output capacitance of 10µF is required for stability. Analog Devices recommends low ESR, X5R, or X7R dielectric ceramic capacitors for best performance. Large load transient applications require larger output capacitors to limit peak voltage transients.
10	SENSE	Kelvin Sense for OUT. The SENSE pin is the inverting input to the error amplifier. Optimum regulation is obtained when the SENSE pin is connected to the OUT pins of the regulator. In critical applications, the resistance of PCB traces between the regulator and the load causes small voltage drops, creating a load regulation error at the point of load. Connecting the SENSE pin at the load instead of directly to OUT eliminates this voltage error.
11	AGND	Analog Ground. To ensure proper electrical and thermal performance, tie all ground pins of the package to PCB ground.
12	SETCAP	Reference Filter. This pin must not be externally loaded. Bypassing the SETCAP pin to AGND with a 4.7µF capacitor decreases output voltage noise and provides a soft-start function to the reference. Analog Devices recommends the use of a high quality, low leakage capacitor.
13	SETRES	Reference. This pin sources the 100µA precision current. Placing a resistor from this pin to the AGND pin of the LT3074 sets the output regulation voltage.
14	IMON	Output Current Monitor. The IMON pin is a voltage output pin that sources a voltage proportional to the output current with a ratio of 3A/V. For best performance, minimize the external loading on this pin and do not drive the pin externally.
15	ASEL	Serial Bus Address Select. This pin allows programming the 4LSBs out of the 7-bit address space. The 3MSBs are hardwired to 110b. Connect a ±1% resistor divider between BIASAF, ASEL, and AGND to select the serial bus interface address. Optionally,

		connect the pin to AGND to set the address to 110_0000b or to BIASAF to set the address to 110_1111b. DO NOT FLOAT THIS PIN. See the *Applications Information* section for more information.
16	BIASAF	Bias Filter Pin for analog circuity. The LT3074 requires a minimum 2.2µF bypass capacitor on this pin.
17	BIAS	Bias Supply. This pin supplies current to the internal control circuitry and the output stage driving the pass transistor. This pin does not require any bypass capacitor. To ensure proper operation, the BIAS voltage must satisfy the following conditions: $2.375V \le V_{BIAS} \le 5.5V$ and $V_{BIAS} \ge 1.2 + V_{OUT}$.
18	BIASDF	Bias Filter Pin for digital circuity. The LT3074 requires a minimum 0.47µF bypass capacitor on this pin.
19	DGND	Digital Ground. To ensure proper electrical and thermal performance, tie all ground pins of the package to PCB ground.
20, 21, Exposed Pad 23	IN	Input Supply. Pins 20, 21, and exposed pad 23 of the LQFN package are the electrical connection to IN. These pins supply power to the high current pass transistor. Connect all IN pins together for proper performance and solder pin 23 to the PCB for better thermal performance. The LT3074 requires a bypass capacitor at IN to maintain stability and low input impedance over frequency. A 10µF input bypass capacitor suffices for most battery and power plane impedances. Minimizing input trace inductance optimizes performance. Applications that operate with low $V_{IN} - V_{OUT}$ differential voltage and that have large, fast load transients may require a much higher input capacitor to prevent the input supply from drooping and allowing the regulator to enter dropout.
22	EN	Device Enable. This pin enables/disables the output. Pulling the EN pin low pulls down the reference, disables the output transistor, and disables auxiliary functions. Drive the EN pin with either a digital logic port, or an open-collector NPN, or an open-drain NMOS terminated with a pull-up resistor to V_{BIAS}. The pull-up resistor must be less than 200kΩ to meet the V_{IH} condition of the EN pin. If unused, connect the EN pin to BIAS.

TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless otherwise noted.

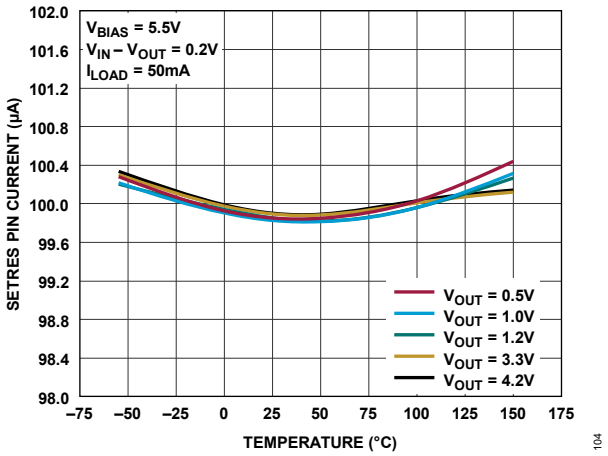


Figure 4. I_{SETRES} vs. Temperature

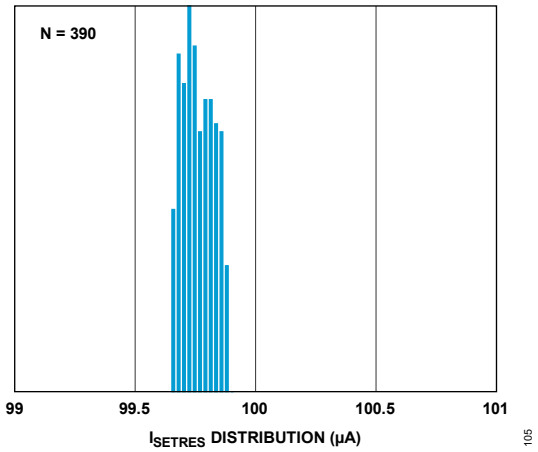


Figure 5. I_{SETRES} Distribution

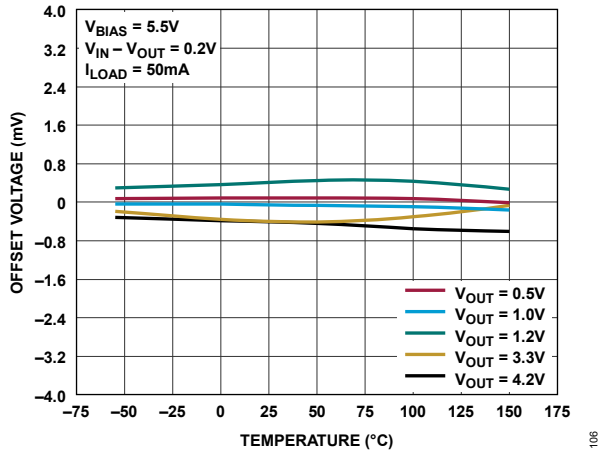


Figure 6. V_{OS} vs. Temperature

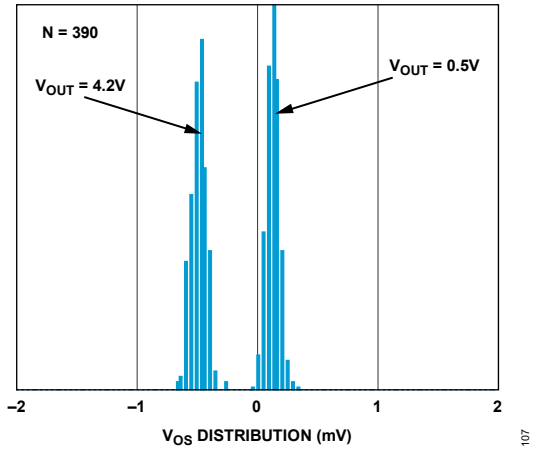


Figure 7. V_{OS} Distribution

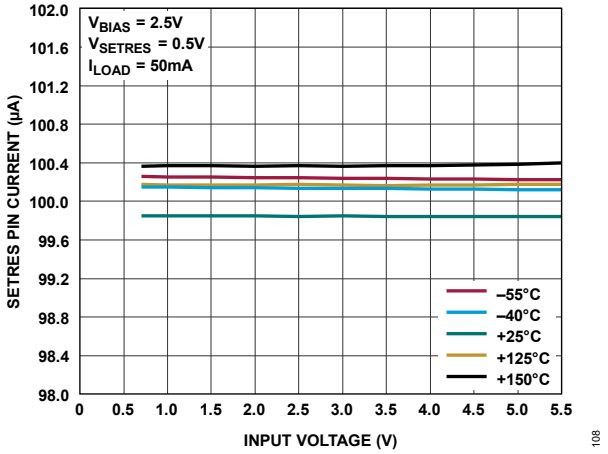


Figure 8. I_{SETRES} Regulation to V_{IN}

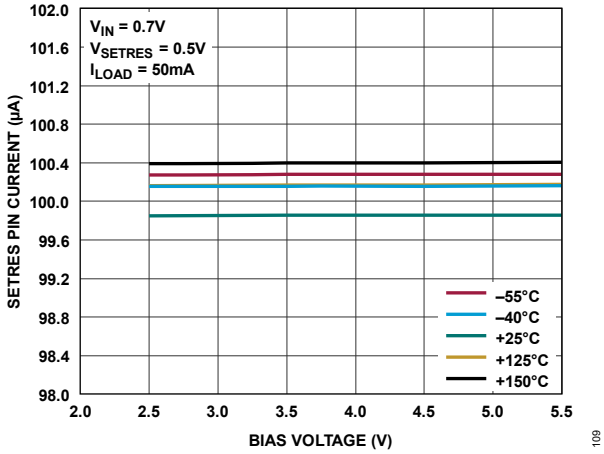


Figure 9. I_{SETRES} Line Regulation to V_{BIAS}

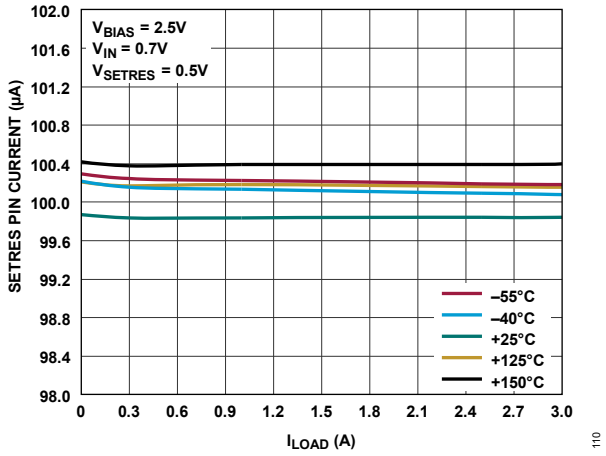


Figure 10. I_{SETRES} Load Regulation

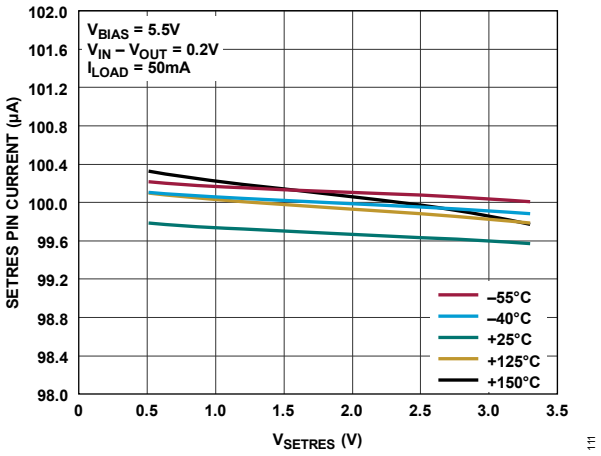


Figure 11. I_{SETRES} Common Mode Regulation

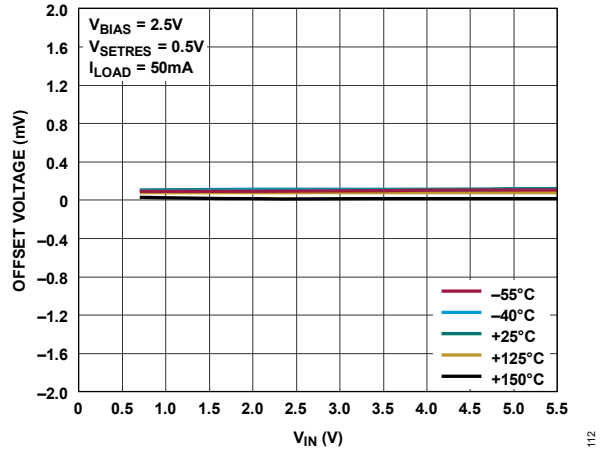


Figure 12. V_{OS} Line Regulation

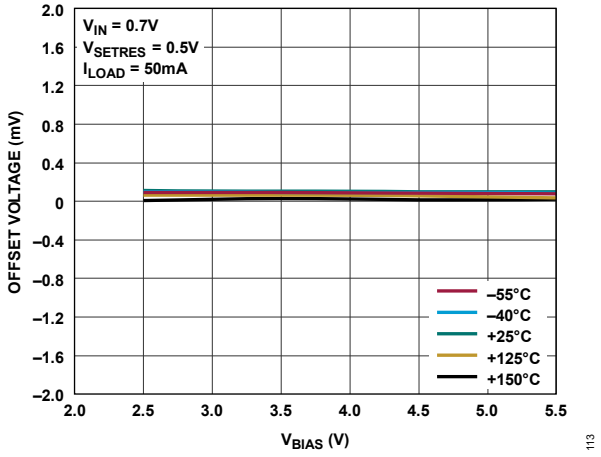


Figure 13. V_{OS} Line Regulation

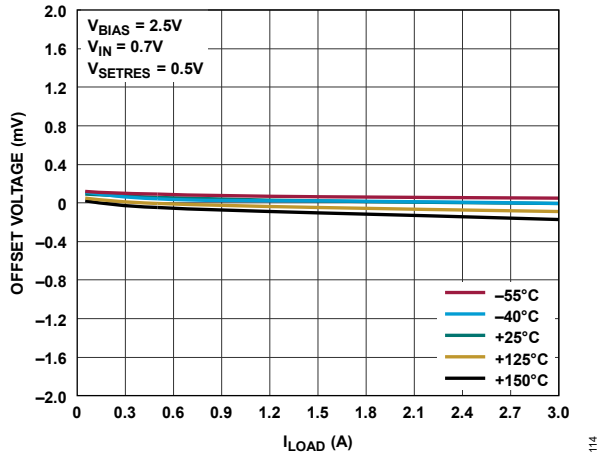


Figure 14. V_{OS} Load Regulation

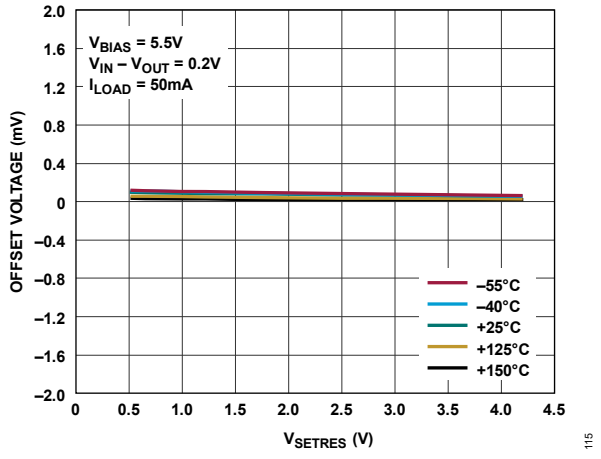


Figure 15. V_{OS} Common Mode Regulation

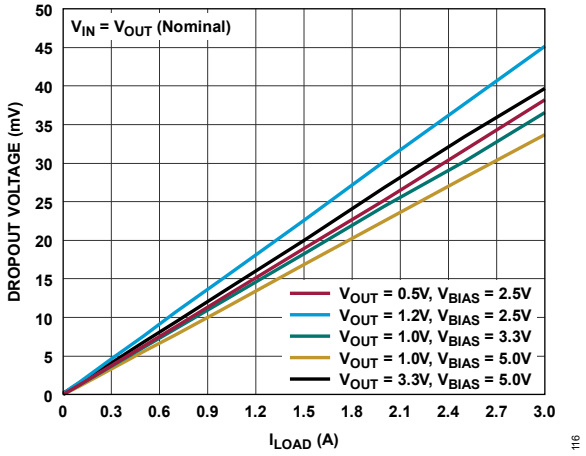


Figure 16. Dropout Voltage vs. Load

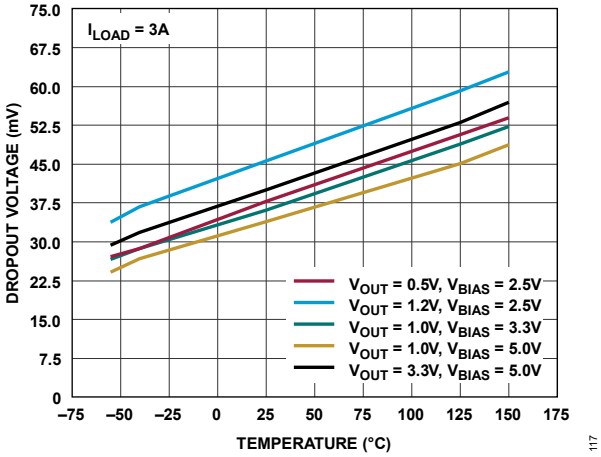


Figure 17. Dropout Voltage vs. Temperature (3A)

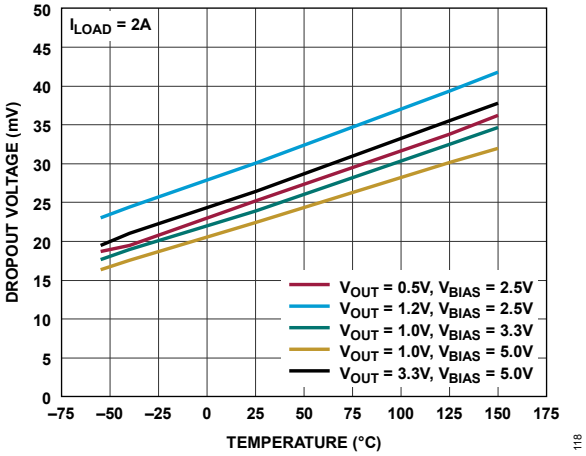


Figure 18. Dropout Voltage vs. Temperature (2A)

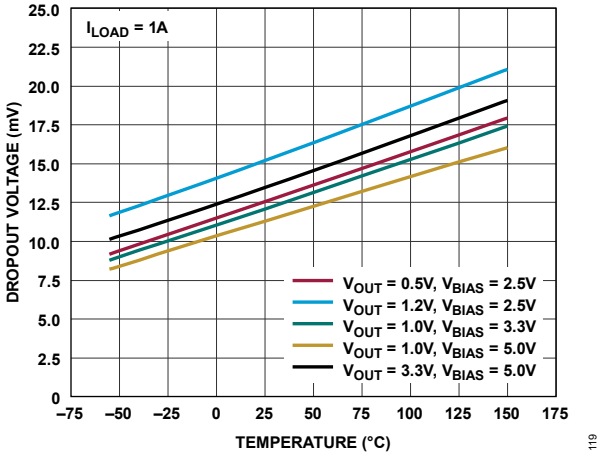


Figure 19. Dropout Voltage vs. Temperature (1A)

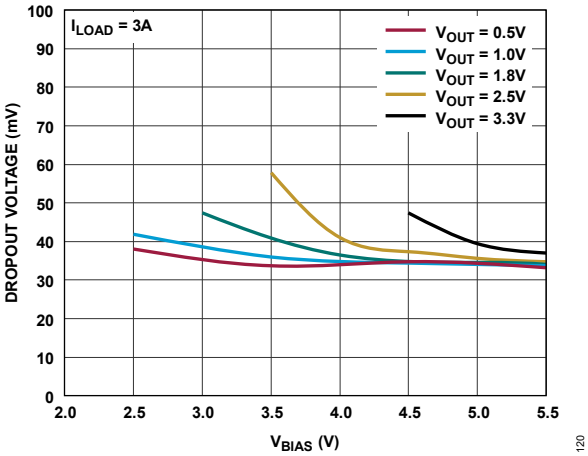


Figure 20. Dropout Voltage vs. Bias

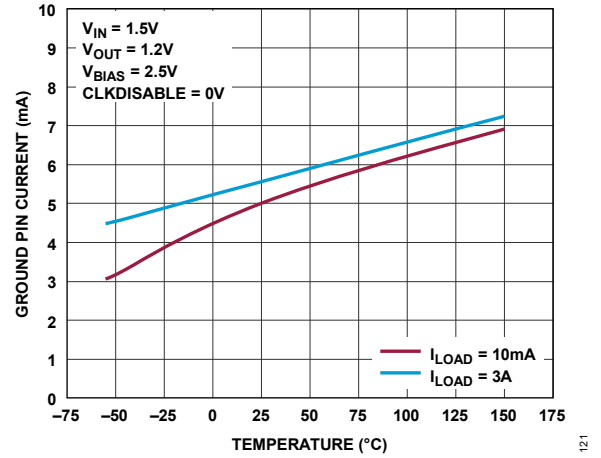


Figure 21. IGND vs. Temperature

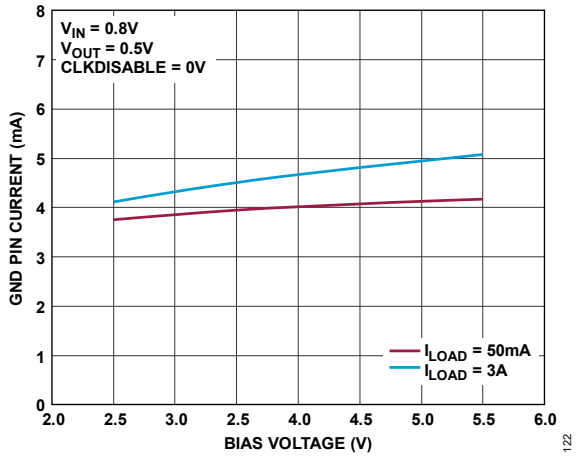


Figure 22. IGND vs. BIAS

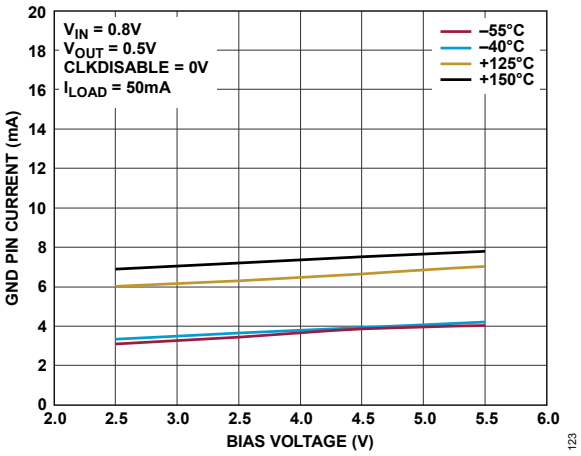


Figure 23. IGND vs. BIAS

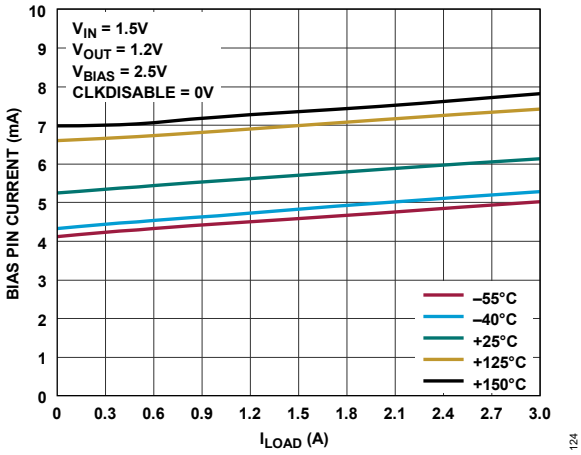


Figure 24. I_{BIAS} vs. Load

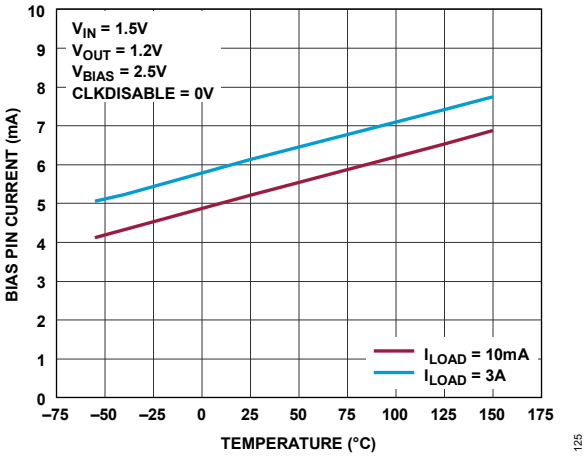


Figure 25. I_{BIAS} vs. Temperature

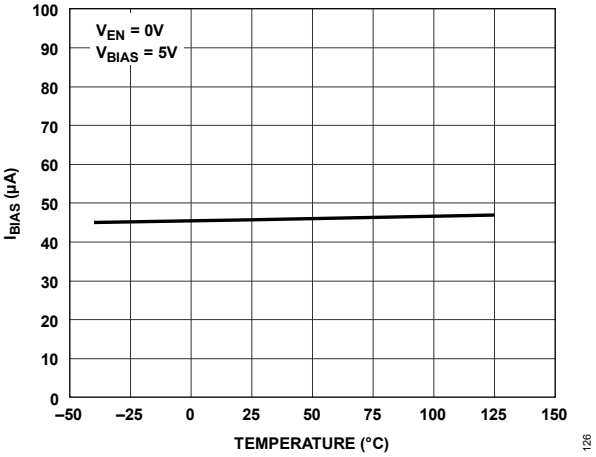


Figure 26. I_{BIAS} vs. Temperature in NAP

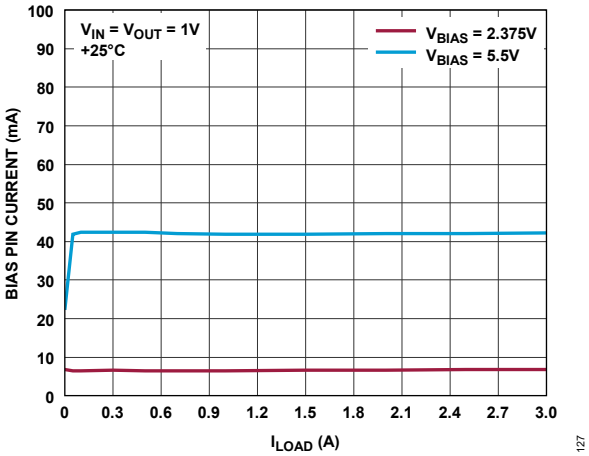


Figure 27. I_{BIAS} vs. Load in Dropout

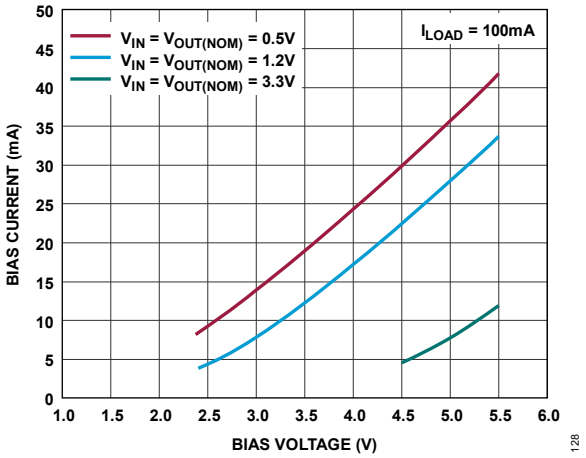


Figure 28. I_{BIAS} vs. Bias in Dropout

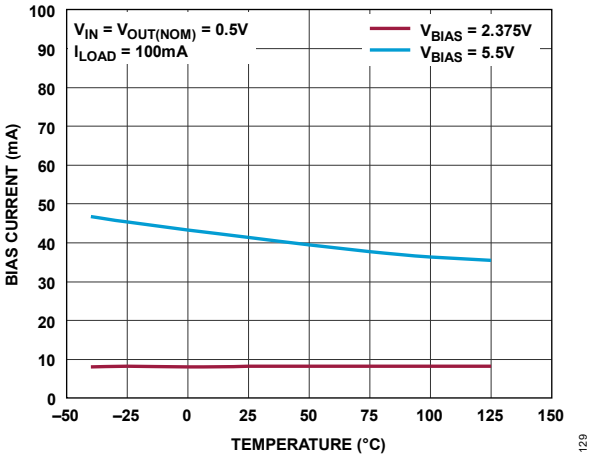


Figure 29. I_{BIAS} vs. Temperature in Dropout

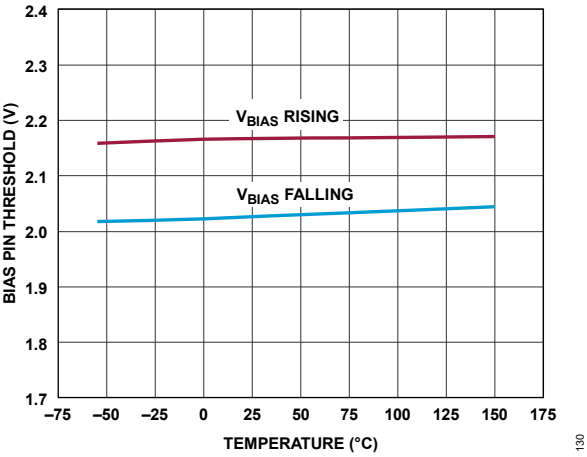


Figure 30. BIAS UVLO

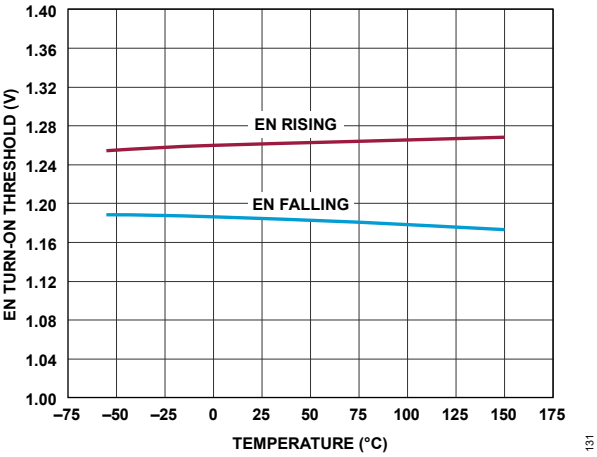


Figure 31. EN Threshold

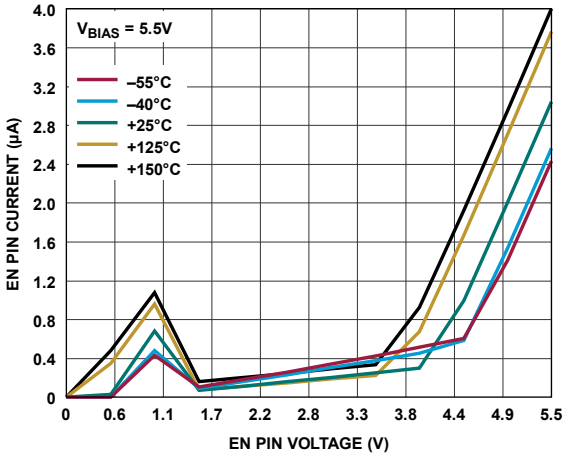


Figure 32. EN Pin Current

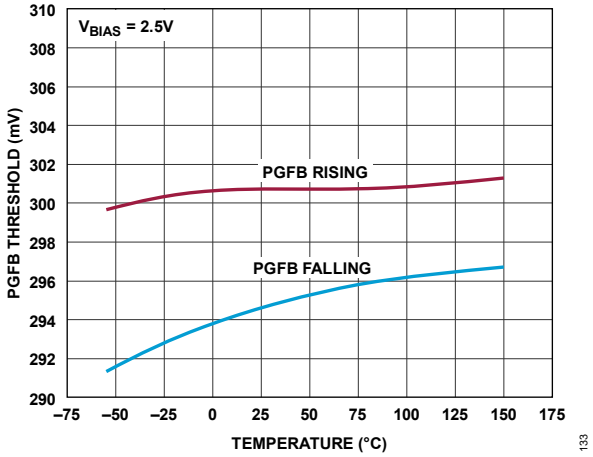


Figure 33. PGFB Threshold

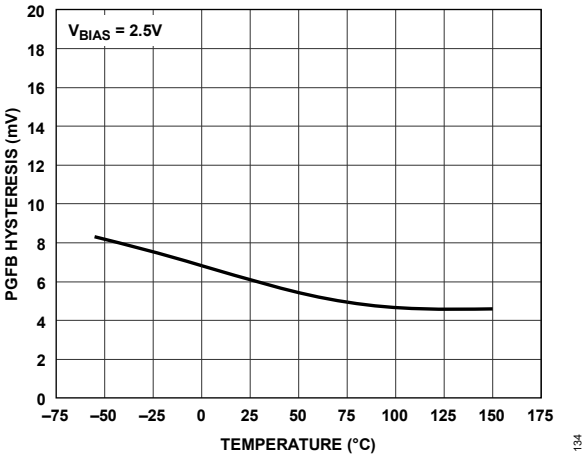


Figure 34. PGFB Hysteresis

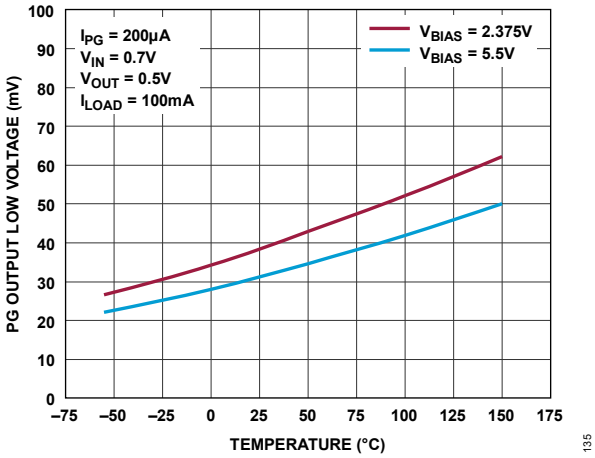


Figure 35. PG VOL

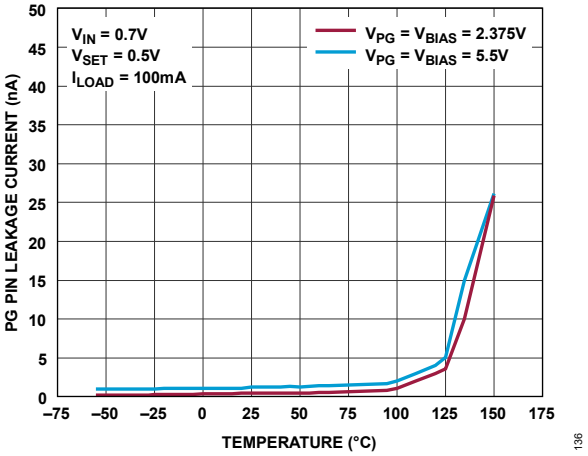


Figure 36. PG Leakage Current

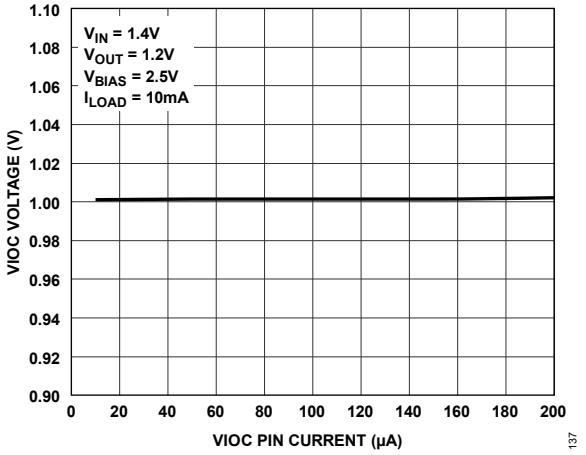


Figure 37. VIOC Pin Voltage

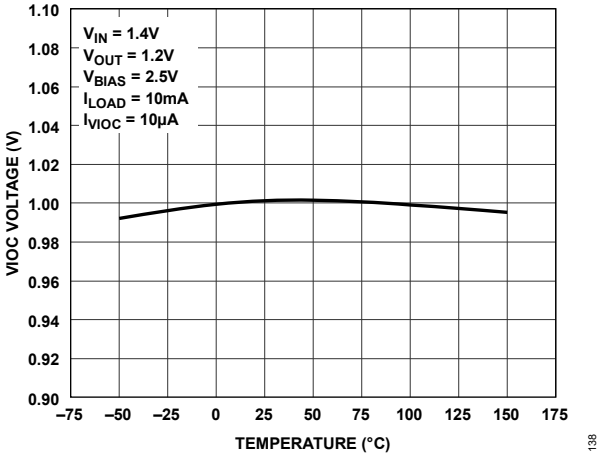


Figure 38. VIOC Pin Voltage

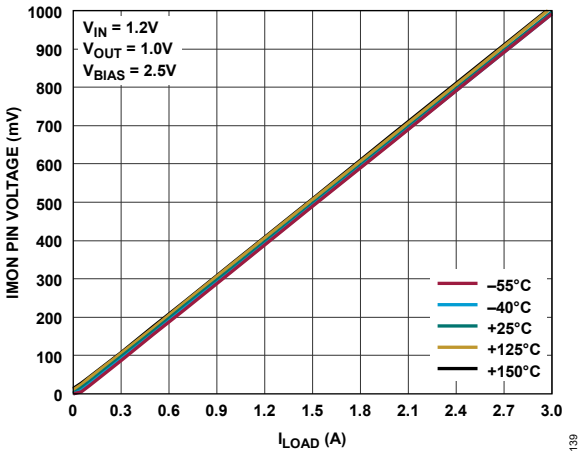


Figure 39. IMON Pin Voltage

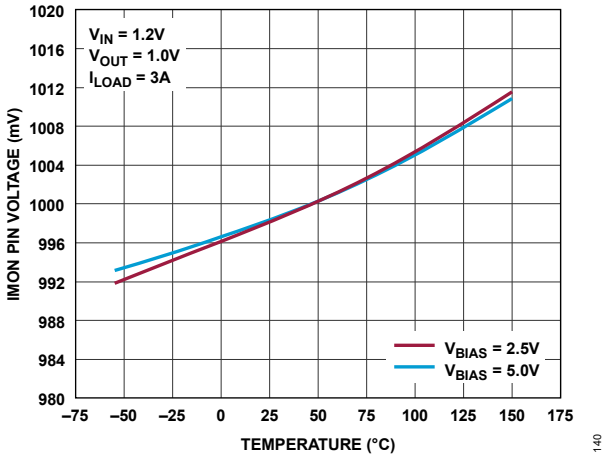


Figure 40. IMON Pin Voltage

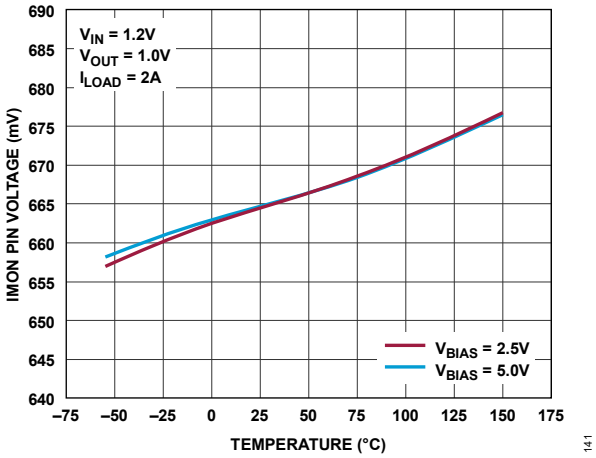


Figure 41. IMON Pin Voltage

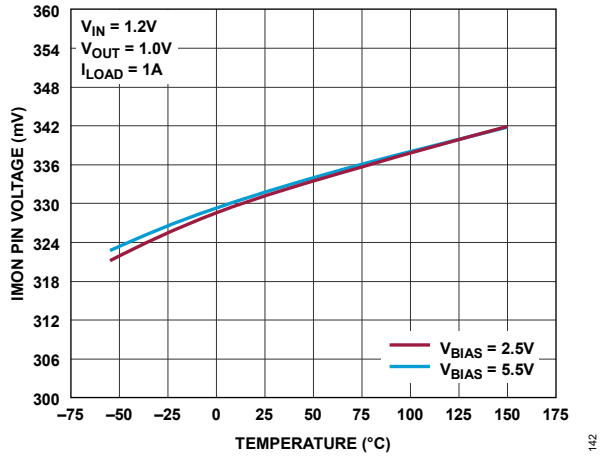


Figure 42. IMON Pin Voltage

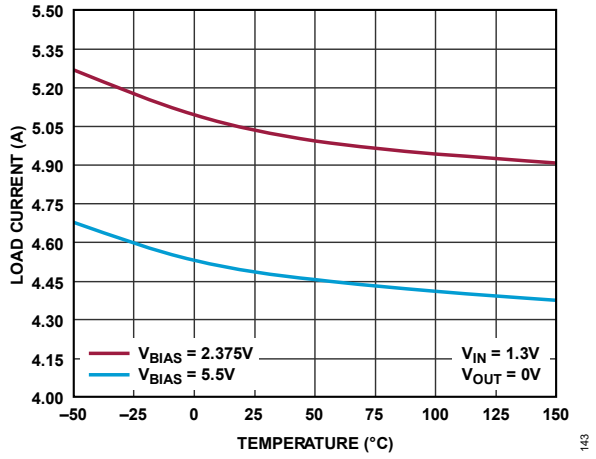


Figure 43. Internal Current Limit

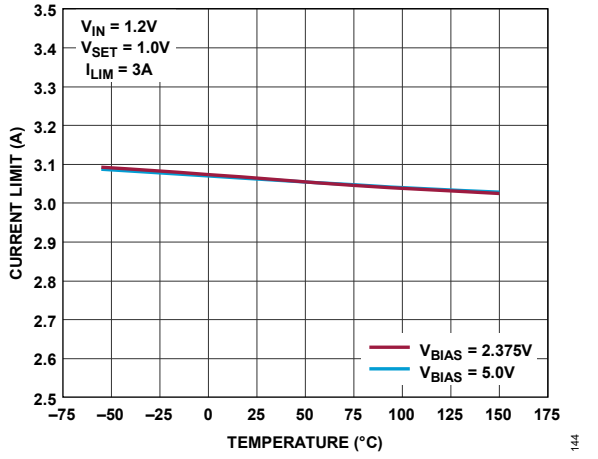


Figure 44. Programmable ILIM at 3A

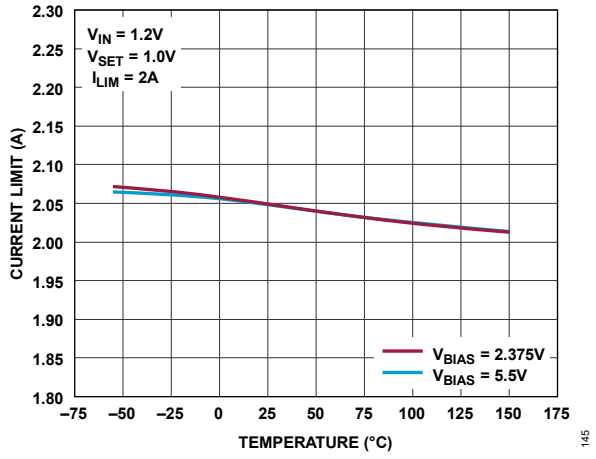


Figure 45. Programmable ILIM at 2A

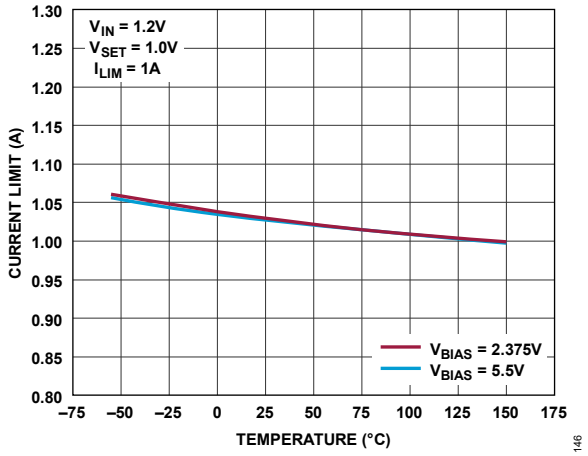


Figure 46. Programmable ILIM at 1A

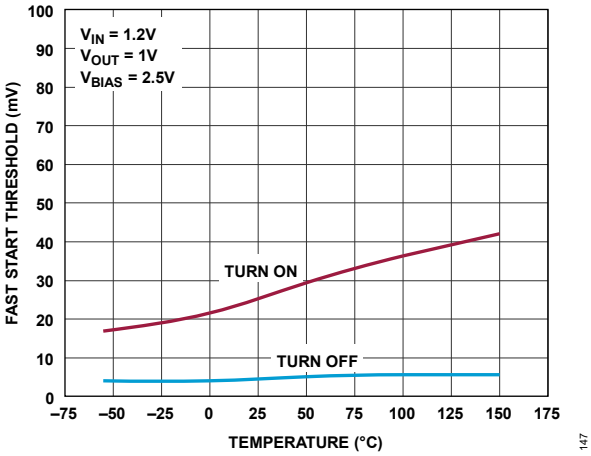


Figure 47. Fast Start Threshold

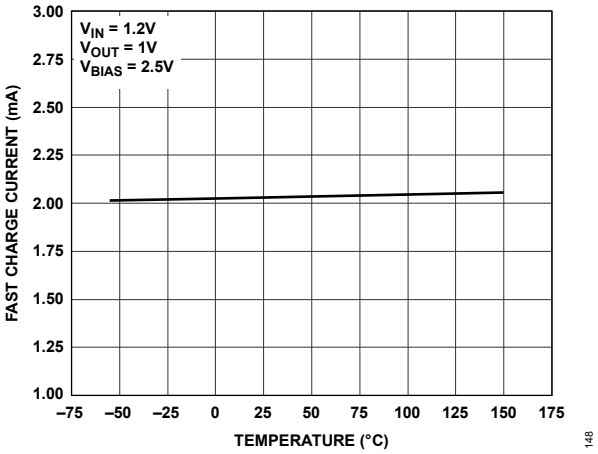


Figure 48. Fast Start Current

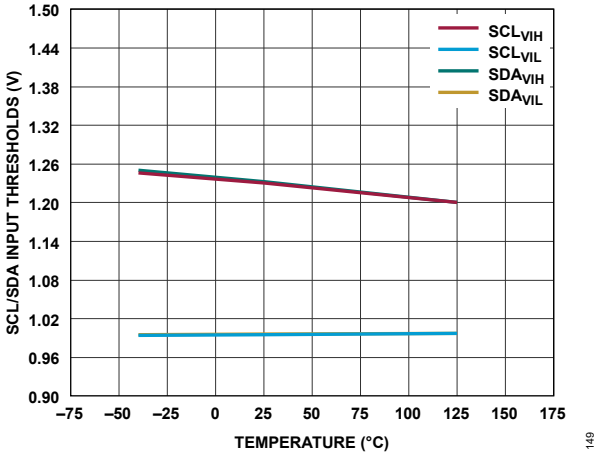


Figure 49. SCL/SDA Input Thresholds

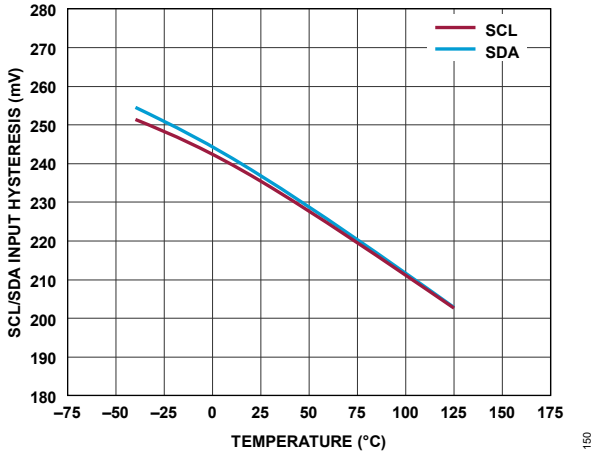


Figure 50. SCL/SDA Input Hysteresis

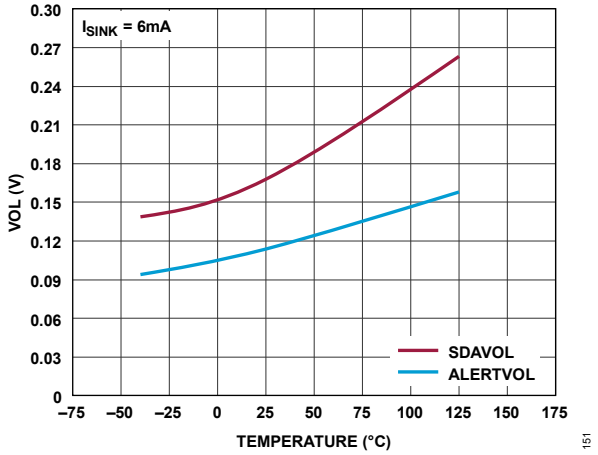


Figure 51. SDA/$\overline{ALERT}$ VOL

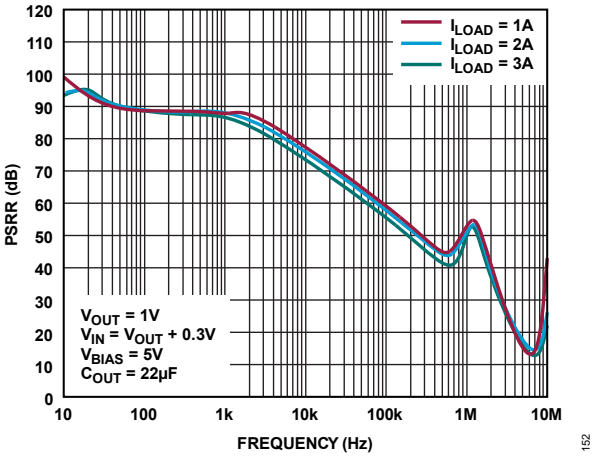


Figure 52. IN Pin PSRR

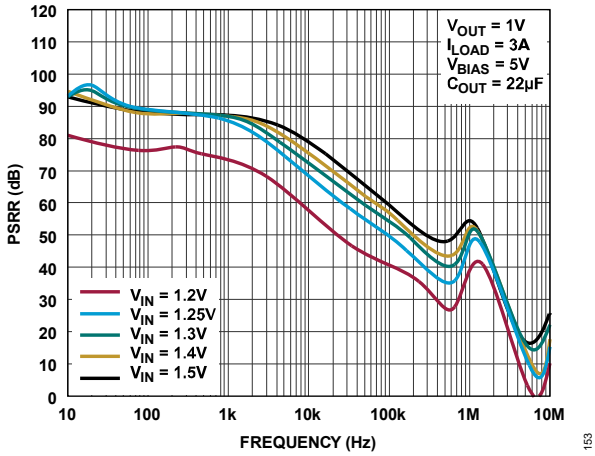


Figure 53. IN Pin PSRR

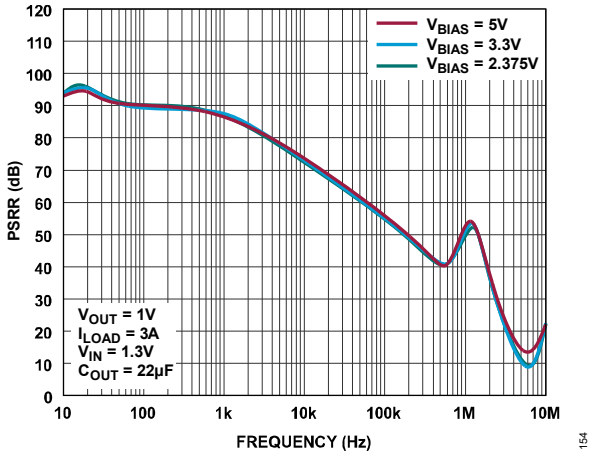


Figure 54. IN Pin PSRR

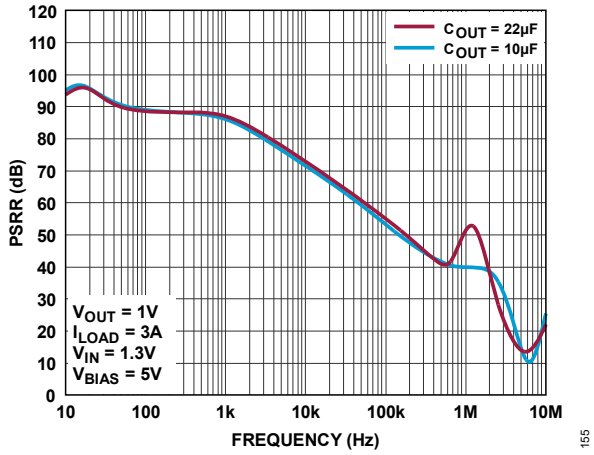


Figure 55. IN Pin PSRR

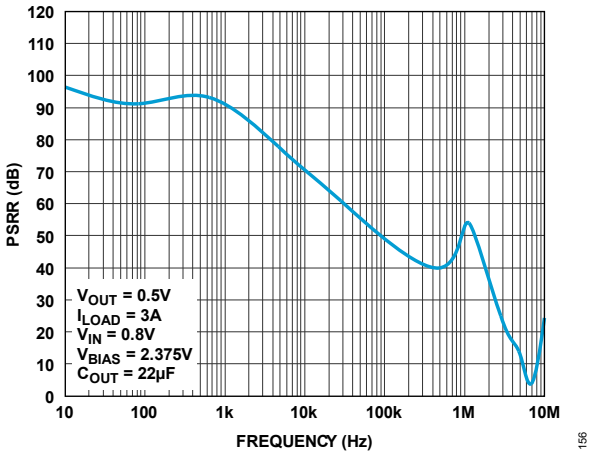


Figure 56. IN Pin PSRR

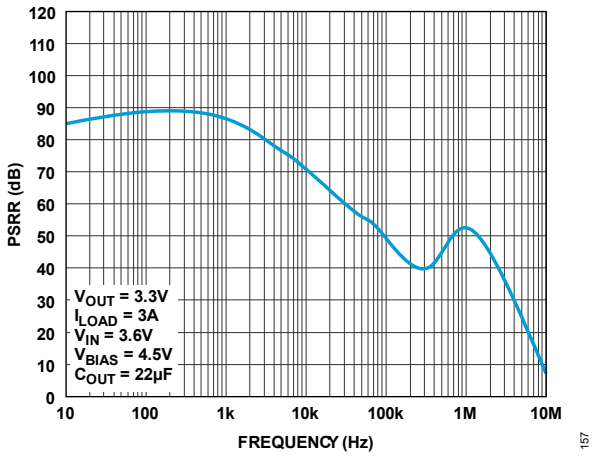


Figure 57. IN Pin PSRR

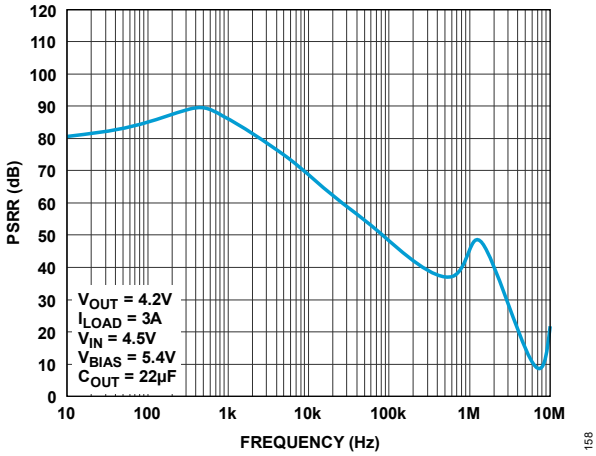


Figure 58. IN Pin PSRR

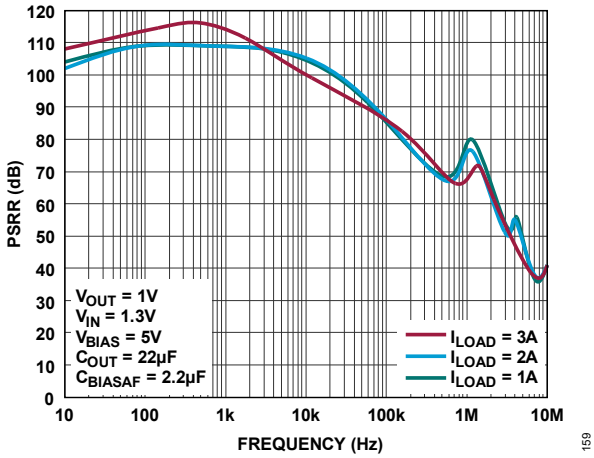


Figure 59. BIAS Pin PSRR

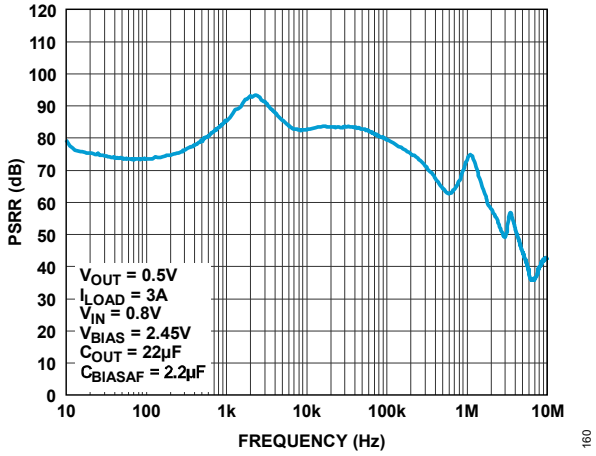


Figure 60. BIAS Pin PSRR

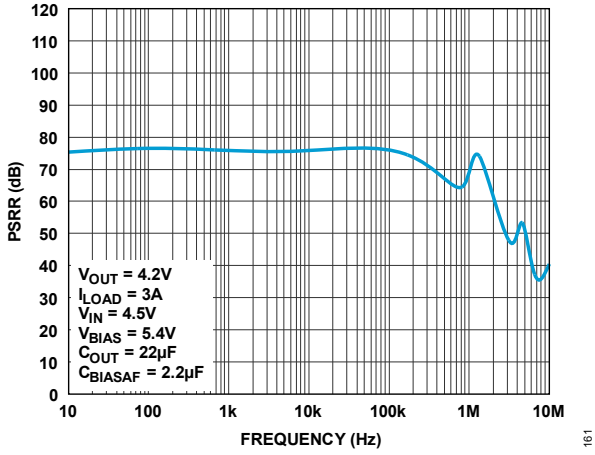


Figure 61. BIAS Pin PSRR

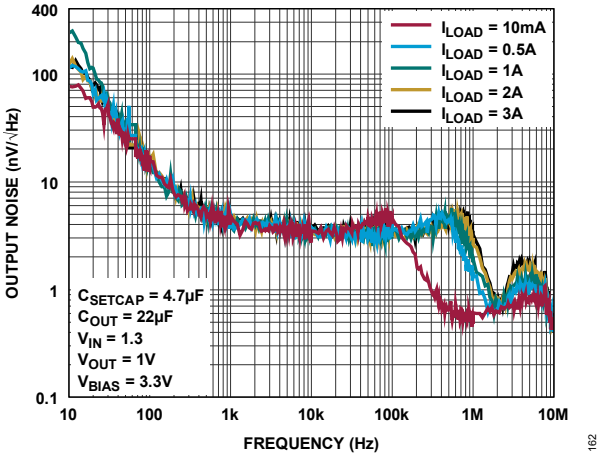


Figure 62. Noise Spectral Density

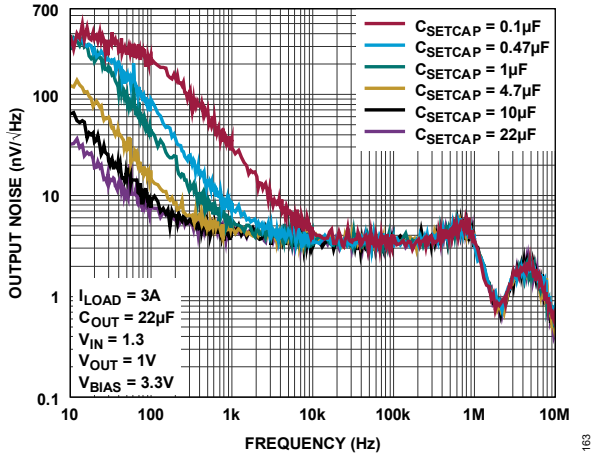


Figure 63. Noise Spectral Density

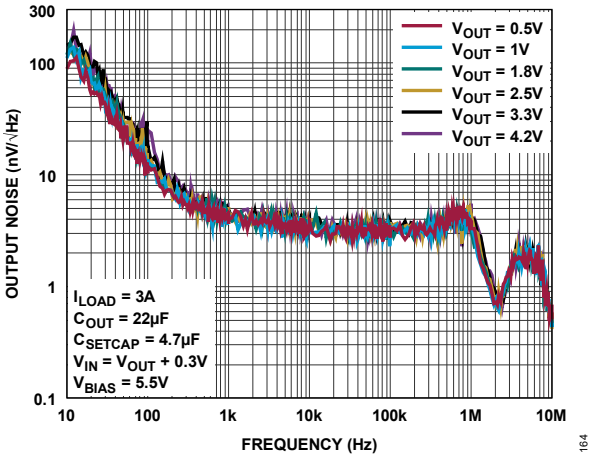


Figure 64. Noise Spectral Density

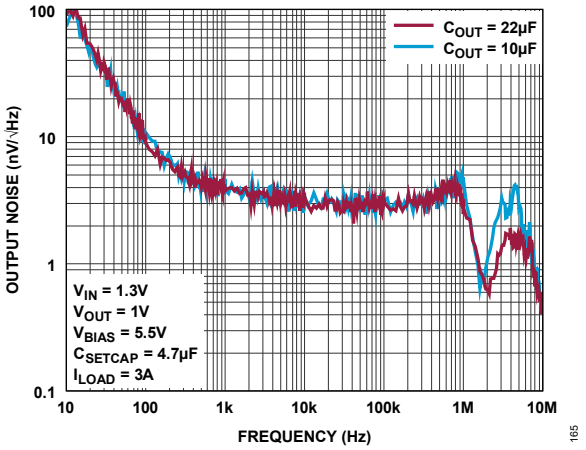


Figure 65. Noise Spectral Density

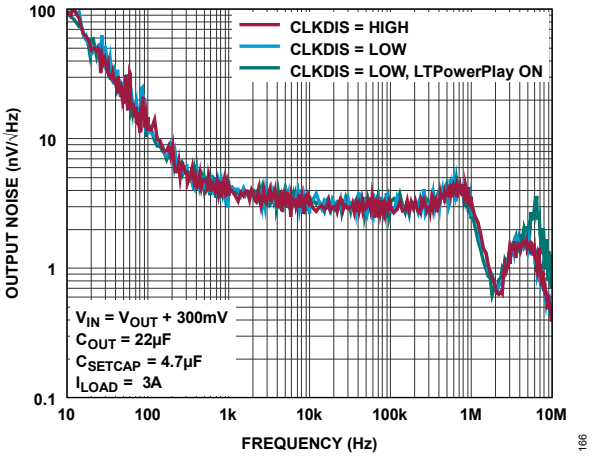


Figure 66. Noise Spectral Density

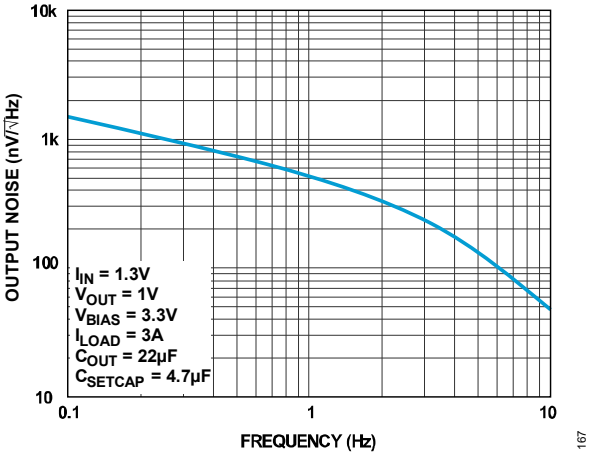


Figure 67. Noise Spectral Density

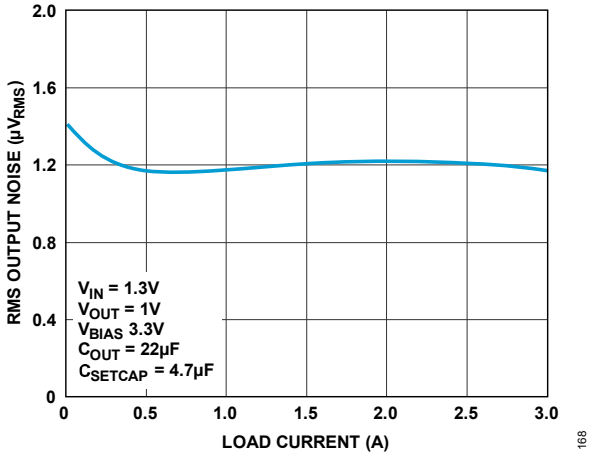


Figure 68. Integrated RMS Noise (10Hz to 100kHz)

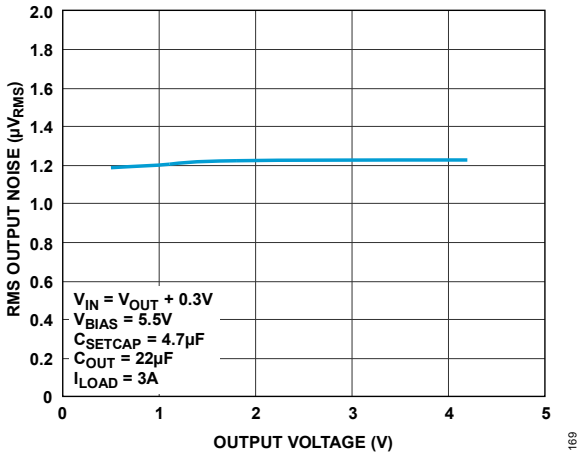


Figure 69. Integrated RMS Noise (10Hz to 100kHz)

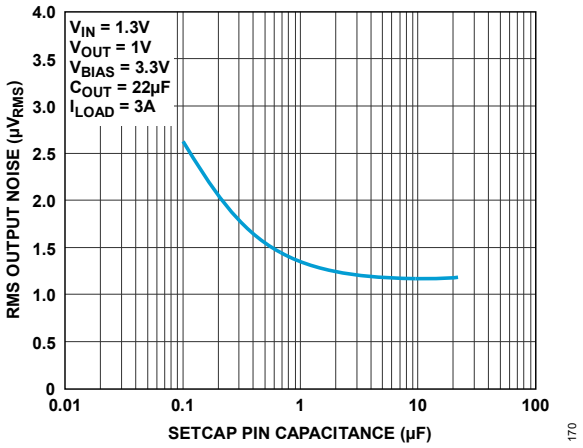


Figure 70. Integrated RMS Noise (10Hz to 100kHz)

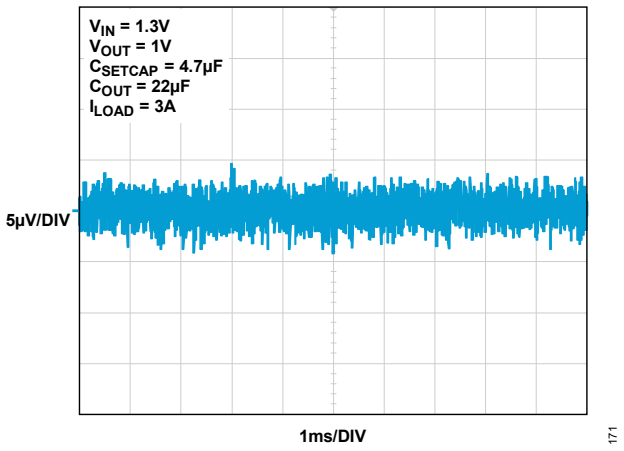


Figure 71. Output Noise (10Hz to 100kHz)

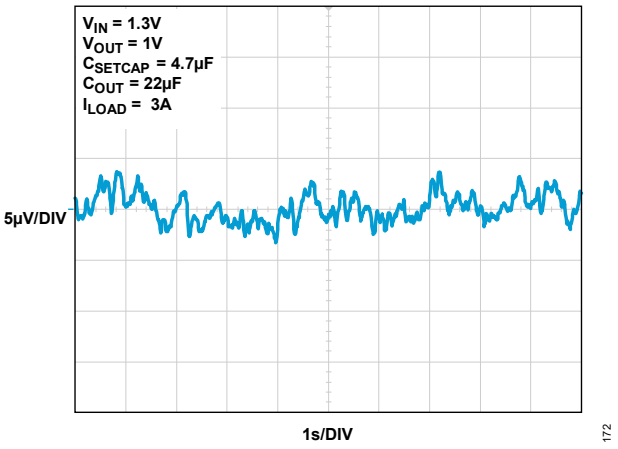


Figure 72. Output Noise (0.1Hz to 10Hz)

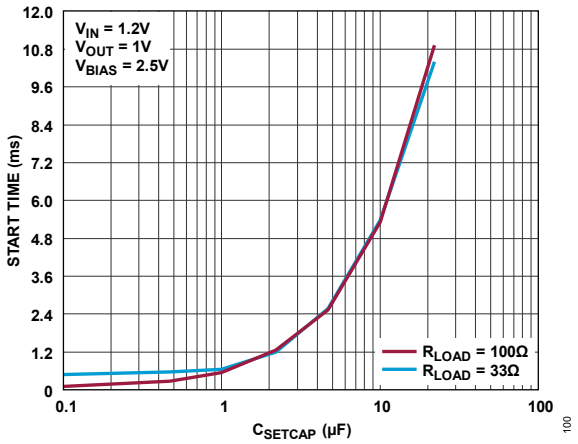


Figure 73. Startup Time

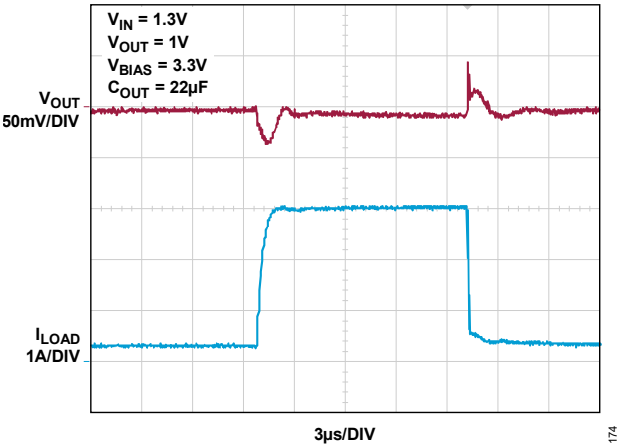


Figure 74. Load Transient Response

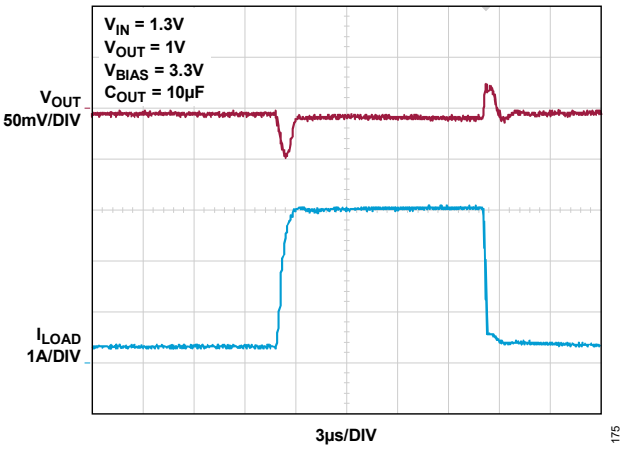


Figure 75. Load Transient Response

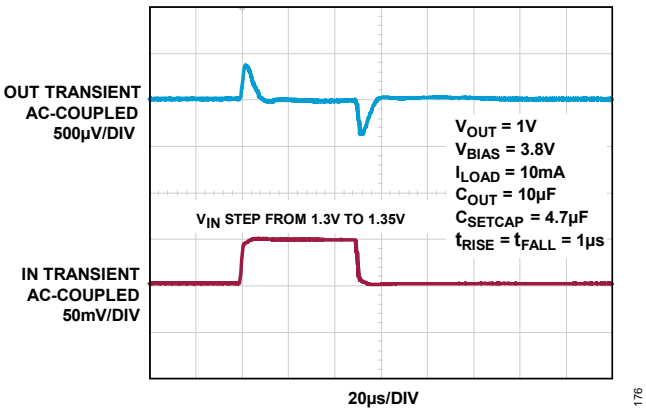


Figure 76. IN Pin Line Transient

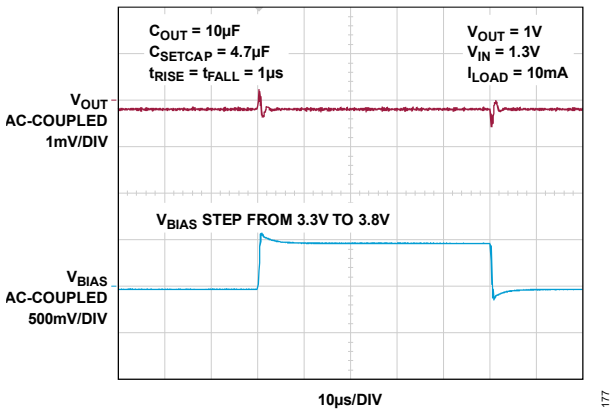


Figure 77. BIAS Line Transient Response

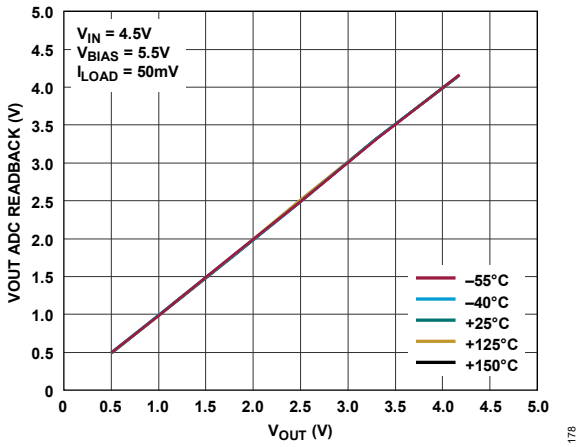


Figure 78. V_{OUT} ADC Readback

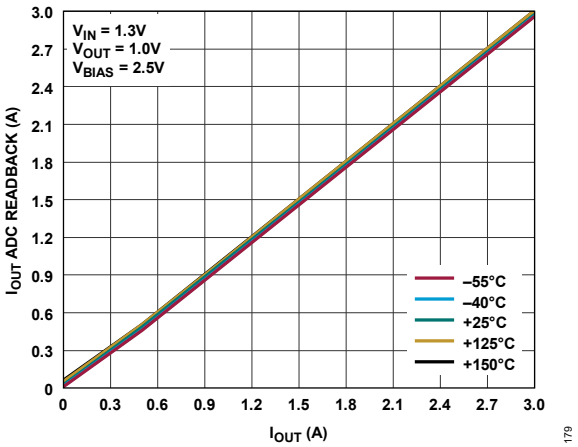


Figure 79. I_{OUT} ADC Readback

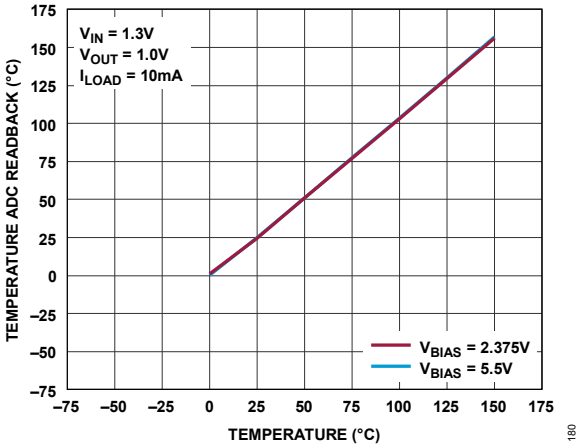


Figure 80. Temperature ADC Readback

FUNCTIONAL DIAGRAMS

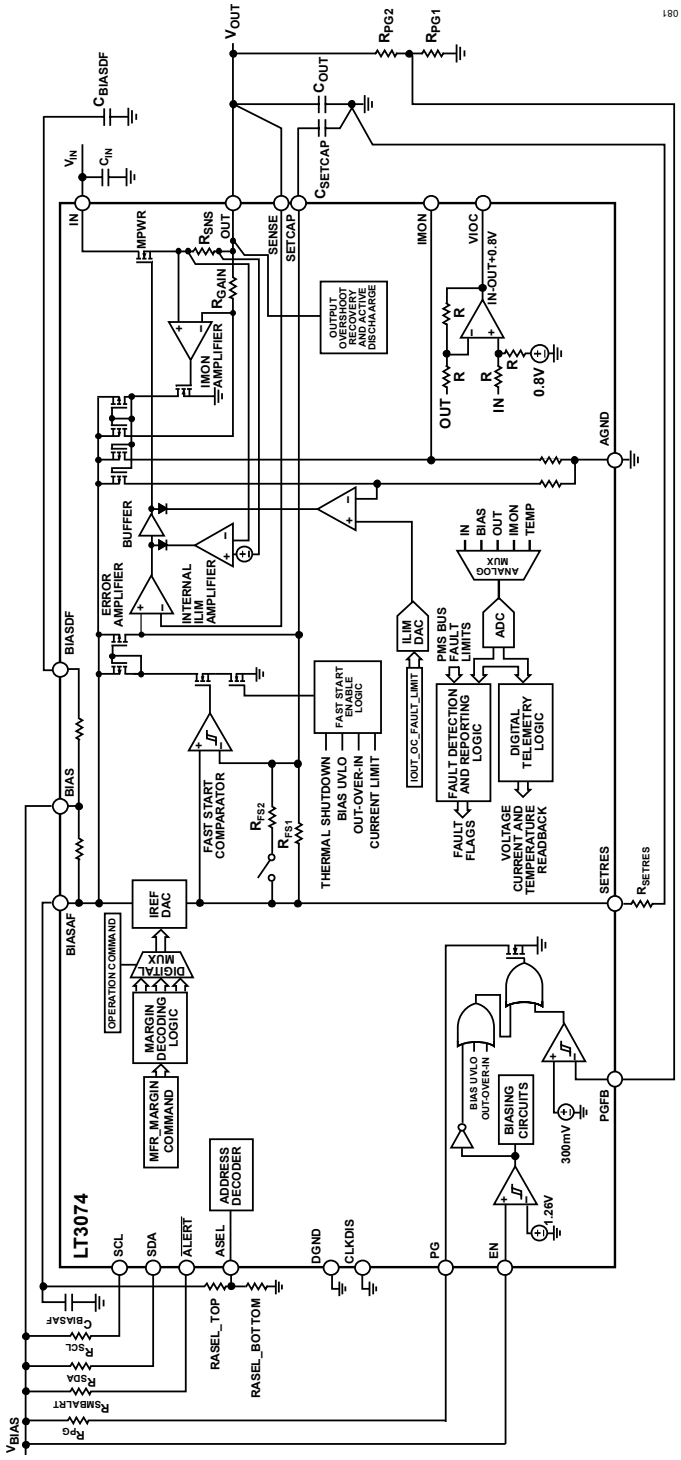


Figure 81. Block Diagram

APPLICATIONS INFORMATION

The LT3074 is a low voltage, ultralow noise, and ultrafast transient response linear regulator. The device supplies up to 3A with a typical dropout voltage of 45mV. A 4.7µF reference bypass capacitor (placed at the SETCAP pin) decreases output voltage noise to 1.2μV_{RMS}. The LDO's wide bandwidth and high power supply rejection ratio (PSRR) permit the use of small ceramic capacitors, saving bulk capacitance and cost. The LT3074 is ideal for high-performance field programmable gate arrays (FPGAs), microprocessors, radio frequency (RF) communication, and noise-sensitive supply applications.

Designed as a precision current source followed by a high-performance unity gain amplifier, the LT3074 can be easily paralleled to further reduce noise, increase output current, and spread heat on the PCB. The LT3074 also incorporates a VIOC tracking function to control an upstream switching converter to maintain constant voltage across the LT3074's power device, thus minimizing power dissipation. The LT3074 additionally features programmable current limit, fast start-up capability, and programmable power good.

The LT3074 supports PMBus compliant serial interface for control, telemetry, and fault reporting that can operate at any frequency between 10kHz and 400kHz. The serial interface supports the send byte, read byte, write byte, read word, write word, and read block communication protocols, as defined in the PMBus specification. *Table 6* gives a list of all PMBus commands supported by the LT3074. *Table 7* gives a description of the data formats.

Table 6. Supported PMBus Commands

COMMAND (CMD) NAME	CMD CODE	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE
PAGE	0x00	Provides integration with multipage PMBus devices	R/W Byte	Reg	0xFF
OPERATION	0x01	Operating mode control. On/off, margin high and margin low	R/W Byte	Reg	0x84
ON_OFF_CONFIG	0x02	PMBus on/off command configuration	R/W Byte	Reg	0x1F
CLEAR_FAULTS	0x03	Clears any fault bits that are set	Send Byte		0x00
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental writes to registers	R/W Byte	Reg	0x00
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by the device	R Byte	Reg	0xB0
VOUT_MODE	0x20	Output voltage format and exponent (2^{-13})	R Byte	Reg	0x13
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit	R/W Word	L16	0xA000 (5)
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit	R/W Word	L16	0x0000
IOUT_OC_FAULT_LIMIT	0x46	Output current limit	R/W Word	L11	0xC34D (3.3)
IOUT_OC_FAULT_RESPONSE	0x47	Action taken by the device in the event of a current limit fault	R Byte	Reg	0x00
OT_WARN_LIMIT	0x51	Overtemperature warning limit	R/W Word	L11	0xF258 (150)

COMMAND (CMD) NAME	CMD CODE	DESCRIPTION	TYPE	DATA FORMAT	DEFAULT VALUE
VIN_OV_WARN_LIMIT	0x57	Input overvoltage warning limit	R/W Word	L11	0xCAC0 (5.5)
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning limit	R/W Word	L11	0xC840 (0.5)
STATUS_BYTE	0x78	One byte summary of unit's fault condition	R/W Byte	Reg	NA
STATUS_WORD	0x79	One word summary of unit's fault condition	R/W Word	Reg	NA
STATUS_VOUT	0x7A	Output voltage fault and warning status	R/W Byte	Reg	NA
STATUS_IOUT	0x7B	Output current fault and warning status	R/W Byte	Reg	NA
STATUS_INPUT	0x7C	Input voltage fault and warning status	R/W Byte	Reg	NA
STATUS_TEMPERATURE	0x7D	Temperature fault and warning status	R/W Byte	Reg	NA
STATUS_CML	0x7E	Communication fault status	R/W Byte	Reg	NA
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and warning status	R/W Byte	Reg	NA
READ_VIN	0x88	Measured IN pin voltage	R Word	L11	NA
READ_VOUT	0x8B	Measured OUT pin voltage	R Word	L16	NA
READ_IOUT	0x8C	Measured OUT pin current	R Word	L11	NA
READ_TEMPERATURE_1	0x8D	Measured average die temperature	R Word	L11	NA
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.3	R Byte	Reg	0x33
IC_DEVICE_ID	0xAD	Device identification stored in ASCII format	R Block/R Word	ASC	LT3074
IC_DEVICE_REV	0xAE	Device revision identifier	R Block/R Word	ASC	00
MFR_MARGIN	0xC4	Configuration to set output margining value	R/W Byte	Reg	0x33
MFR_READ_VBIAS	0xC6	Measured BIAS pin voltage	R Word	L11	NA
MFR_BIAS_OV_WARN_LIMIT	0xC7	Bias overvoltage warning limit	R/W Word	L11	0xCAC0 (5.5)
MFR_BIAS_UV_WARN_LIMIT	0xC8	Bias undervoltage warning limit	R/W Word	L11	0xC91A (2.2031)
MFR_IOUT_MIN_WARN_LIMIT	0xC9	Minimum output current warning limit	R/W Word	L11	0xA19A (0.1001)
MFR_SPECIAL_ID	0xE7	Manufacturer special value used for device identification	R Word	Reg	0x1C1D
MFR_DEFAULT_CONFIG	0xF5	Indicates the status of the configuration registers	R Byte	Reg	0x01
MFR_RAIL_ADDRESS	0xFA	Common address for PolyPhase outputs to adjust common parameters	R/W Byte	Reg	0x80
MFR_RESET	0xFD	Commanded reset without requiring power down	Send Byte		NA

Table 7. Description of Data Formats

DATA FORMAT	DATA FORMAT NAME	DESCRIPTION
L11	Linear_5s_11s	PMBus Data field b[15:0] Value = Y x 2^N where, N = b[15:11] is a 5-bit 2's complement integer and Y = b[10:0] is a 11-bit 2's complement integer. Example: For b[15:0] = 0xCAC0 = 'b1100_1010_1100_0000 (Y = 010_1100_0000; N = 11001) Value = 704 x 2^{-7} = 5.5
L16	Linear_16u	PMBus Data Field b[15:0] Value = Y x 2^N where, Y = b[15:0] is an unsigned integer and N = VOUT_MODE[4:0] is a 5-bit 2's complement signed integer, hardwired to -13 decimal. Example: For b[15:0] = 0xA000 = 'b1010_0000_0000_0000 Value = 40960 x 2^{-13} = 5
Reg	Register	PMBus Data Field b[15:0] or b[7:0] Bit field meaning is defined in detail in the *PMBus Command Details* section.
ASC	Ascii Format	A variable length string of text characters conforming to ISO/IEC 9959-1 standard.

Output Voltage

The LT3074 incorporates a 100µA precision current source flowing out of the SETRES pin, which also connects to the noninverting input of the error amplifier through an RC filter network (see the *Output Noise* and *Fast Start* sections for more details). Connecting a resistor from the SETRES pin to ground generates a reference voltage for the error amplifier. This reference voltage is the product of the SETRES pin current and the SETRES pin resistance. The unity-gain configuration of the error amplifier produces a low-impedance version of this voltage at the SENSE pin, which is the inverting input of the error amplifier. The SENSE pin is externally connected to the OUT pin.

The benefit of using current reference compared to the typical voltage reference used in conventional regulators is that the regulator always operates in unity-gain configuration, independent of the programmed output voltage. This configuration allows the LT3074 to have loop gain, frequency response, and bandwidth independent of the output voltage. As a result, noise, PSRR, and transient performance do not change with the output voltage. Moreover, because none of the error amplifier gain is needed to amplify the SETRES pin voltage to a higher output voltage, output load regulation is more tightly specified in the hundreds of microvolts range and not as a fixed percentage of the output voltage.

Because the zero temperature-coefficient current source is highly accurate, the SETRES pin resistor can become a limiting factor in achieving high accuracy. Therefore, the SETRES pin resistor must be a precision resistor. *Table 8* lists many common output voltages and their corresponding 1% SETRES pin resistance values. Additionally, any leakage paths to or from the SETRES (or SETCAP) pin create errors in the output voltage. Leakages on the SETCAP

pin are worse than that on the SETRES pin as the leakage current flows through the filter resistor creating additional voltage drop. If necessary, use high-quality insulation (for example, Teflon or Kel-F). Moreover, cleaning of all insulating surfaces to remove fluxes and other residues can be required. High humidity environments can require a surface coating at the SETRES and SETCAP pins to provide moisture barrier.

Minimize board leakage by encircling the SETRES and SETCAP pins with a guard ring that operates at a potential close to itself, ideally connected to the OUT pins. Guarding both sides of the circuit board is recommended. Bulk leakage reduction depends on the guard ring width. Leakages of 100nA into or out of the SETRES creates a 0.1% or more error in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant errors in the output voltage, especially over a wide operating temperature range. *Figure 82* illustrates a typical guard ring layout.

Table 8. 1% Resistors for Common Output Voltages

V_{OUT} (V)	R_{SETRES} (kΩ)
0.5	4.99
0.8	8.06
1.0	10.0
1.2	12.1
2.5	24.9
3.3	33.2

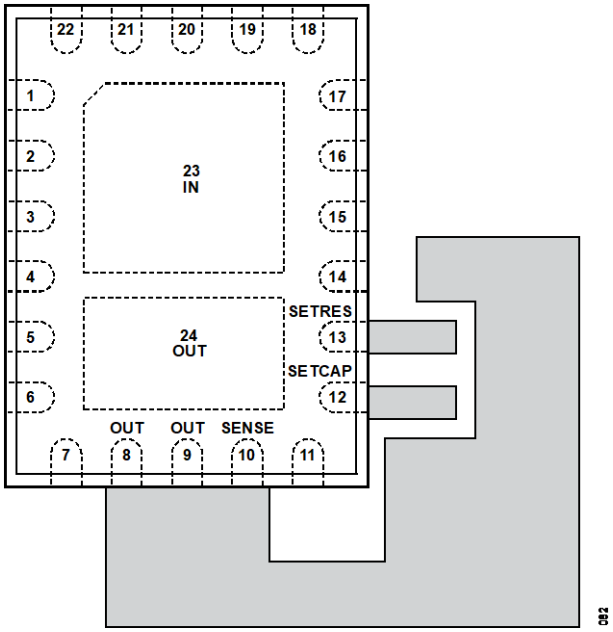


Figure 82. Guard Ring Layout

Output Sensing

The SENSE pin of the LT3074 provides a Kelvin-sense connection to the output capacitor. The GND side of the SETRES pin resistor and the SETCAP pin capacitor provide a Kelvin-sense connection to the GND side of the output capacitor (see *Figure 83*). The LT3074 corrects for the parasitic package and the PCB trace resistance drops when the SENSE pin is Kelvin connected to the output capacitor. The LT3074 handles moderate levels of output line impedance, but excessive impedance between OUT pin and the output capacitor causes an excessive phase shift in the feedback loop and adversely affects stability. This Kelvin connection also regulates the output voltage at the output capacitor, which optimizes noise, PSRR, load transient, and regulation performance. All measured at the output capacitor.

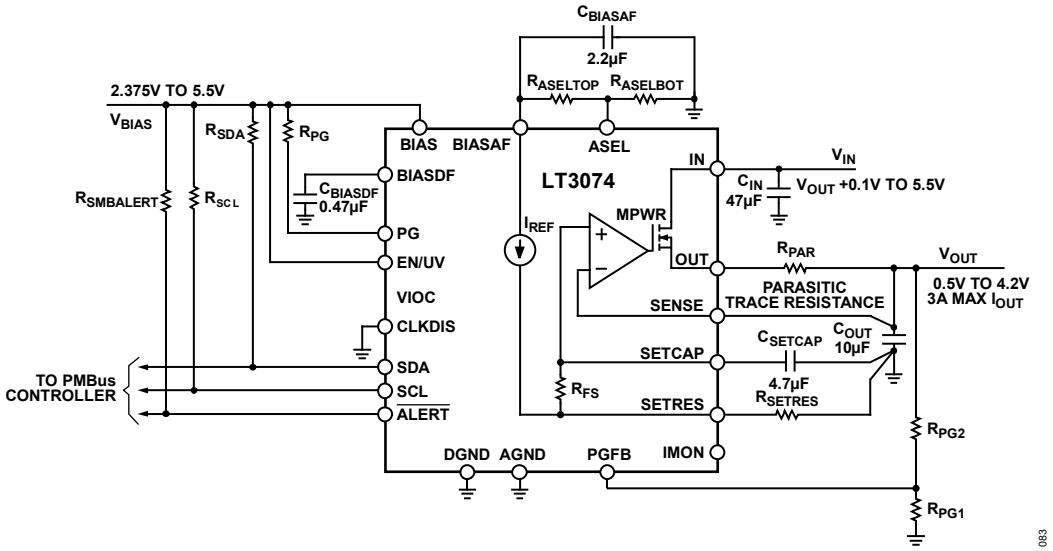


Figure 83. Output Capacitor, SETCAP Capacitor, and SETRES Resistor Connections for Best Performance

Stability and Output Capacitance

The LT3074 requires a minimum output capacitance of 10µF for stability. Analog Devices recommends the use of low ESR, X5R, or X7R ceramic capacitors near the LT3074 OUT and GND pins. Include wide routing planes for OUT and GND to minimize inductance. If possible, mount the regulator immediately adjacent to the application load to minimize distributed inductance for optimal load transient performance. Point-of-load applications present the best case layout scenario for extracting the full LT3074 performance.

Additional ceramic capacitors distributed beyond the immediate decoupling capacitors are acceptable and recommended at the point of load because the distributed PCB inductance isolates them from primary compensation capacitors.

Many of the applications in which the LT3074 excels, such as field programmable gate arrays (FPGA), application-specific integrated circuit (ASIC) processors, or digital signal processors (DSP) supplies, typically require a high-frequency decoupling capacitor network for the device being powered. This network generally consists of many low-value ceramic capacitors in parallel. In parallel, multiple low-value capacitors present a favorable frequency characteristic that reduces the parasitic inductance of the capacitors.

Given the high PSRR and low noise performance attained using a single 10µF ceramic output capacitor, larger values of output capacitors are not necessary. However, these capacitors can still improve the performance. See the *Typical Performance Characteristics* section for additional information. Moreover, larger output capacitance does decrease peak output deviations during a load transient. Note that bypass capacitors used to decouple individual components powered by the LT3074 increase the effective output capacitance.

Give extra consideration to the type of ceramic capacitors used. The capacitors are manufactured with a variety of dielectrics, each with different behaviors across temperature and applied voltage. The most common dielectrics used are specified with electronic industries alliance (EIA) temperature characteristic codes of Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitance in the small packages, but these dielectrics tend to have stronger voltage and temperature coefficients, as shown in *Figure 84* and *Figure 85*. When used with a 5V regulator, a 16V, 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 3µF for the DC bias voltage applied over the operating temperature range.

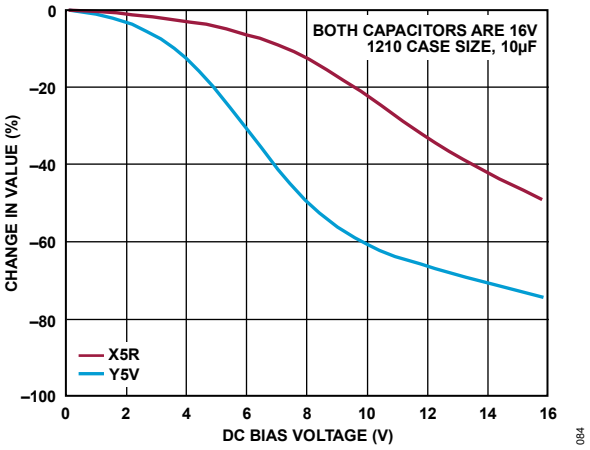


Figure 84. Ceramic Capacitor DC Bias Characteristics

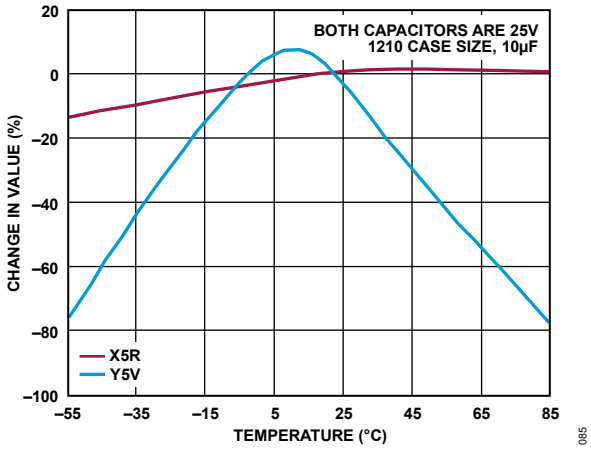


Figure 85. Ceramic Capacitor Temperature Characteristics

The X5R and X7R dielectrics result in more stable characteristics and thus are more suitable for the LT3074. The X7R dielectric has better stability across temperature, while the X5R is less expensive and is available in higher values. Nonetheless, care must still be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and the maximum capacitance change over temperature. While capacitance changes due to DC bias for X5R and X7R is better than Y5V and Z5U dielectrics, it can still be significant enough to drop the capacitance below sufficient levels. As shown in *Figure 86*, capacitor DC bias characteristics tend to improve as component case size increases. However, verification of expected capacitance at the operating voltage is highly recommended. Due to its good voltage coefficient in small case sizes, Analog Devices recommends using the Murata GCM series ceramic capacitors.

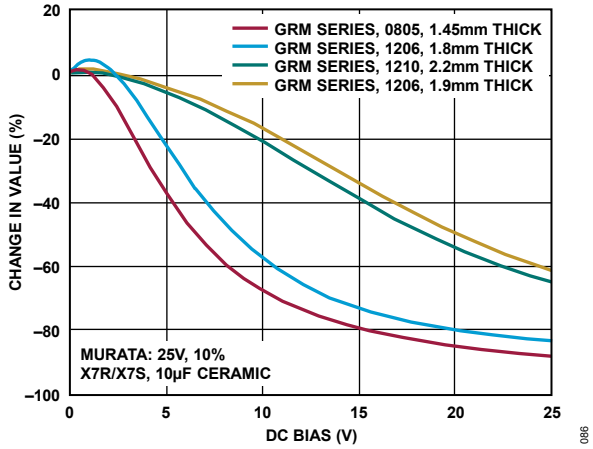


Figure 86. Capacitor Voltage Coefficient for Different Case Sizes

In addition to DC bias and temperature variation noted above, variation in effective capacitance with applied AC voltage needs to be considered as well. Ceramic capacitors are typically specified for an AC ripple of 1V. Effective capacitance decreases with lower AC ripple voltages. Effective capacitance decreases by 30% or more with the very low AC ripple at the output of the LT3074. Contact the respective ceramic capacitor vendor for more information on temperature, DC bias voltage, and AC ripple voltage effects when selecting a capacitor to meet the minimum capacitance requirements of the LT3074.

High Vibration Environments

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress, similar to how a piezoelectric microphone works. For a ceramic capacitor, this stress can be induced by mechanical vibrations within the system or due to thermal transients.

LT3074 applications in high-vibration environments have three distinct, piezoelectric noise generators; ceramic output, input, and SETCAP pin capacitors. However, due to the low output impedance over a wide frequency range for the LT3074, negligible output noise is generated using a ceramic output capacitor. Similarly, due to the high PSRR of the LT3074, negligible output noise is generated using a ceramic input capacitor.

Nonetheless, given the high SETCAP pin impedance, any piezoelectric response from the SETCAP pin capacitor generates significant output noise, peak-to-peak excursions of hundreds of mV. However, due to the high ESR and ESL tolerance of the SETCAP pin capacitor, any non-piezoelectrically responsive (tantalum, electrolytic, or film) capacitor can be used at the SETCAP pin, although electrolytic capacitors tend to have high 1/f noise. In any case, use of a surface mount capacitor is highly recommended. Due to its reduced piezoelectric response, Analog Devices recommends using the Murata GCJ series ceramic capacitors for C_{SETCAP}.

Stability and Input Capacitance

The LT3074 is stable with a minimum 10µF IN pin capacitor. Analog Devices recommends using low ESR ceramic capacitors to minimize instantaneous voltage drops under large load transient conditions. Large V_{IN} drops during large load transients may cause the regulator to enter dropout with the corresponding degradation in load transient response. Therefore, increased input and output capacitance values may be necessary depending on an application's requirements. Sufficient input capacitance is critical as the circuit is intentionally operated close to dropout to minimize power. Ideally, the output impedance of the supply that powers the IN pins should be less than 20mΩ to support a 3A load with large transients.

In cases where long wires connect the power supply to the input and ground terminals of the LT3074, the use of low value input capacitors combined with large load current can result in instability. The resonant LC tank circuit formed by the wire inductance and the input capacitor is the cause of this instability and not the LT3074. The self-inductance, or isolated inductance, of a wire is directly proportional to its length. The wire diameter, however, has less influence on its self-inductance. For example, the self-inductance of a 2-AWG isolated wire with a diameter of 0.26" is about half the inductance of a 30-AWG wire with a diameter of 0.01". One foot of 30-AWG wire has 465nH of self-inductance.

Several methods exist to reduce the self-inductance of a wire. One method divides the current flowing towards the LT3074 between two parallel conductors. In this case, placing the wires further apart reduces the inductance; up to 50% reduction when placed only a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed close to each other, their mutual inductance adds to the overall self-inductance of the wires; therefore, a 50% reduction is not possible in such cases. The second and more effective technique to reduce the overall inductance is to place the forward and return current conductors (the input and ground wires) close to each other. Two 30-AWG wires separated by 0.02" reduce the overall inductance to about one-fifth of a single wire.

If the LT3074 is powered by a battery mounted near the ground and power planes on the same circuit board, a 10µF capacitor suffices. If a distant supply powers the LT3074, use a low ESR, large value input capacitor on the order of 220µF. As power supply output impedance varies, the minimum input capacitance needed for application stability also varies.

PSRR and Input Capacitance

For applications using the LT3074 for post-regulating switching converters, placing a capacitor directly at the input of the LT3074 results in AC current (at the switching frequency) to flow near the LT3074. The relatively high frequency switching current generates a magnetic field that couples to the output of the LT3074, degrading its effective power supply rejection ratio (PSRR). While highly dependent on the PCB, the switching pre-regulator, and the input capacitance, among other factors, the PSRR degradation is present even if the LT3074 is desoldered from the board because it effectively degrades the PSRR of the PCB itself. While negligible for conventional, low PSRR, low dropout (LDO) regulators, the high PSRR of the LT3074 requires careful attention to higher order parasitics to extract the full performance offered by the regulator.

The input capacitor of the LT3074 cannot be completely removed to mitigate the flow of the high frequency switching current near the LT3074 because with no in put capacitor present, as with any regulator, the input of the LT3074 oscillates at the parasitic LC resonant frequency. In addition it is generally common (and preferred) to bypass the regulator input with some capacitance.

To that end, Analog Devices recommends using the LT3074 evaluation board layout for achieving the best possible PSRR performance. The LT3074 evaluation board layout uses magnetic field cancellation techniques to prevent PSRR degradation caused by this high frequency current flow, while using an input capacitor.

Filtering High Frequency Spikes

For applications where the LT3074 is used to post regulate a switching converter, its high PSRR effectively suppresses any noise present at the switching frequency of the switching converter, typically 100kHz to 4MHz. However, the high frequency (hundreds of MHz) spikes, beyond the bandwidth of the LT3074, associated with the power-switch transition times of the switching converter almost directly pass through the LT3074. While the output capacitor is intended to partly absorb these spikes, its ESL limits its ability at these frequencies. A ferrite bead or even the inductance associated with a short (example 0.5”) PCB trace between the output of the switching converter and the input of LT3074 can serve as an LC filter to suppress these high frequency spikes.

Output Noise

The LT3074 offers many advantages with respect to noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources for a traditional regulator are its voltage reference, error amplifier, noise from the resistor divider network used for setting the output voltage, and the noise gain created by this resistor divider. Many low noise regulators pin out their voltage reference to allow for noise reduction by bypassing the reference voltage. Unlike most linear regulators, LT3074 does not use a voltage reference. Instead, the LT3074 uses a 100µA current reference into the SETRES pin. The resultant voltage noise equals the current noise multiplied by the resistor value, which in turn, is the root mean square (RMS) summed with the noise of the error amplifier and the thermal noise of the resistor.

One problem that conventional linear regulators face is that the resistor divider setting the output voltage gains up the reference noise. In contrast, the unity-gain architecture of the LT3074 presents no gain from the SETCAP pin to the output. In addition, the SETCAP is decoupled from the SETRES pin internally with a small value filter resistor (approximately 1kΩ). This filter resistor, along with the SETCAP capacitor, creates a low-pass filter (LPF) bypassing the SETRES pin resistor noise. As a result, the output noise is independent of the programmed output voltage. The resultant output noise is then set just by the noise of the error amplifier, typically 3.5nV/√Hz from a 10kHz to 1MHz bandwidth and 1.2μV_{RMS} from a 10Hz to 100kHz bandwidth using a 4.7µF capacitor. Paralleling multiple LT3074 devices further reduces noise by a factor of √N for N parallel regulators.

SETCAP Pin Capacitance: Noise, PSRR, Transient Response, and Soft-Start

In addition to reducing output noise, using a SETCAP pin capacitor also improves PSRR and transient performance. Note that any bypass-capacitor leakage deteriorates the DC regulation of the LT3074. Leakages on the SETCAP pin capacitor shunt current away from the 100µA precision reference current and also create an offset across the filter resistor. Capacitor leakage of even 100nA is more than 0.1% DC error. Therefore, Analog Devices recommends the use of good quality, low-leakage ceramic capacitors.

Using the SETCAP pin capacitor also soft-starts the output and limits inrush current.

Fast Start

For ultralow noise applications that require low 1/f noise, a SETCAP pin capacitor with a very low frequency pole may be necessary. This significantly increases the start-up time in accordance with the RC time constant associated with the SETRES pin resistor, filter resistor, and SETCAP pin capacitor. The LT3074 incorporates fast start-up circuitry that sources the SETCAP pin with a typical current of 2mA during start-up to rapidly charge the filter capacitor, decreasing start-up time.

The 2mA current source turns on if the SETRES to SETCAP differential is greater than approximately 25mV and remains engaged until the SETCAP pin voltage catches up to the SETRES pin voltage; at which point the current turns off. If the regulator is in current limit, thermal shutdown or BIAS UVLO is detected, and the fast start function is disabled.

When fast start is enabled during start-up, if the SETCAP pin slew rate approaches the SETRES pin slew rate, the SETCAP pin voltage may catch up to the SETRES pin voltage while the SETRES pin voltage is still ramping. This shuts off the fast start circuit until the SETRES pin voltage can rise above the SETCAP pin voltage by 25mV. This is intended operation. This turn-on and turn-off cause stair stepping at the SETCAP pin voltage (and possibly in turn at the OUT voltage). Increasing the SETCAP pin capacitor smoothes the SETCAP pin start-up.

Output Voltage Margining

The LT3074 provides the capability to margin the output voltage in discrete steps from 1% to 30% using the PMBus. The margining is achieved by scaling the precision 100µA current reference supplied at the SETRES pin. Depending on the nominal output voltage and the amount of margining being used, the high side margin may enable the fast start functionality (if the SETRES to SETCAP voltage differential exceeds approximately 25mV); as a result, the output voltage rapidly settles to the margined value. For high-side margin, where the SETRES to SETCAP differential does not exceed the 25mV threshold and all low side margining, the output takes a RC delay (set by the SETRES pin resistor, approximately 1kΩ filter resistor from SETRES to SETCAP and the SETCAP pin capacitor) to settle to the margined value.

See the *OPERATION* and *MFR_MARGIN* commands in the *PMBus Command Details* section for additional information on output voltage margining.

BIAS/BIASAF/BIASDF Pin Requirements

The BIASAF and BIASDF pins are internally tied to the BIAS pin through separate filter resistors. BIASAF supplies current to all the analog functional blocks and the BIASDF supplies current to the digital circuitry. This minimizes the high frequency, digital switching noise coupling to the high performance, low noise analog circuitry. The LT3074 requires a minimum 2.2µF bypass capacitor on the BIASAF pin and 0.47µF bypass capacitor on the BIASDF pin for stability and proper operation. No bypass capacitor is needed on the BIAS pin. To ensure proper operation, the BIAS voltage must satisfy the following conditions: $2.375V \le V_{BIAS} \le 5.5V$ and $V_{BIAS} \ge V_{OUT} + 1.2V$. Do not externally load the BIASAF and/or the BIASDF pins.

BIAS Undervoltage Lockout

An internal undervoltage lockout (UVLO) comparator monitors the BIAS rail. If V_{BIAS} drops below the UVLO threshold, all functions shut down, the pass transistor is gated off, and output current falls to zero. The typical BIAS pin UVLO threshold is 2.2V on the rising edge of BIAS. The UVLO circuitry incorporates about 130mV of hysteresis on the falling edge of BIAS.

EN/UV Function (Turning the Part ON and OFF)

The EN/UV pin is used to put the regulator in a micropower shutdown state (NAP mode). In NAP mode, the BIAS pin quiescent current drops to less than 10µA.

The LT3074 has an accurate 1.26V turn-on threshold on the EN/UV pin with 80mV hysteresis. This threshold can be used with a resistor divider from the BIAS supply to define an accurate UVLO threshold for the regulator. The EN/UV pin current ($I_{EN/UV}$) at the threshold from *Table 1* must be considered when calculating the resistor divider network as follows:

$$V_{BIAS(UVLO)} = 1.26V \times \left(1 + \frac{R_{EN2}}{R_{EN1}}\right) + (I_{EN/UV} \times R_{EN2})$$

where:

R_{EN1} and R_{EN2} are the resistors from the EN/UV pin to AGND and the EN/UV pin to the BIAS pin, respectively. $I_{EN/UV}$ can be ignored if R_{EN1} is less than 100kΩ. If unused, connect the EN/UV pin to BIAS.

Power Good Indicator

The power good (PG) pin is an open-drain NMOS output that indicates the status of the output voltage. The PG pin becomes high impedance when the output is within its regulation limits and is actively pulled low when one or more of the following conditions are detected

- EN/UV pin is pulled below its turn on threshold, forcing the part in NAP mode.
- BIAS voltage is below its UVLO threshold.
- Programmable power good comparator detects an output undervoltage fault.
- OUT over IN voltage detector activates.

Programmable Power Good

In addition to programming the *VOUT_UV_WARN_LIMIT* through the PMBus, the LT3074 supports an analog method to set an output undervoltage fault. As illustrated in *Figure 81* , the power good threshold is user programmable using the ratio of two external resistors, R_{PG2} and R_{PG1}:

$$V_{OUT(PG\_THRESHOLD)} = 0.3V \times \left(1 + \frac{R_{PG2}}{R_{PG1}}\right) + (I_{PGFB} \times R_{PG2})$$

If the PGFB pin increases to more than 300mV, the open-drain PG pin deasserts and becomes high impedance. The power good comparator has 8mV of hysteresis and 10µsec of deglitch. If the power good comparator detects an output undervoltage fault, in addition to asserting the PG pin low, bit 4 of the *STATUS_VOUT* register (and as a result bit 15 of the *STATUS_WORD* register) is set and the host is notified by asserting the $\overline{\text{ALERT}}$ pin low.

If the programmable power good functionality is not needed, tie the PGFB pin to BIAS and float the PG pin. Do not float the PGFB pin.

Current Monitor and Programmable Current Limit

The IMON pin of the LT3074 serves as a voltage output proportional to the load current. The scaling factor for the reported voltage is I_{OUT}/3A such that the IMON pin voltage corresponds to 1V for the full 3A load current. The IMON

pin voltage is also measured by the on-chip analog-to-digital converter (ADC). This converted value is scaled back to the output load current and reported over the PMBus interface using the *READ_VOUT* command. Do not load the IMON pin externally. Any parasitic leakages or impedances to or from the IMON pin leads to an error in the measured output load current.

Unlike most other linear regulators that use the IMON pin, external current limit programming is decoupled from the current monitoring functionality and the IMON pin on the LT3074. External current limit on the LT3074 can only be programmed using the *IOUT_OC_FAULT_LIMIT* command over the PMBus interface. See the *IOUT_OC_FAULT_LIMIT* command for additional details on external current limit programming in the LT3074.

Output Overshoot Recovery and Active Discharge

During a load step change from full load to no load (or light load), the output voltage overshoots before the regulator responds to turn the power transistor off. Given that there is no load (or light load) present at the output, it takes a long time to discharge the output capacitor.

The LT3074 incorporates an overshoot recovery circuitry that turns on a current sink to discharge the output capacitor in the event SENSE is higher than SETCAP. This current is typically about 500mA. In addition, if the EN/UV pin is pulled low, forcing the part in NAP mode, this current sink turns on to enable an active discharge of the OUT voltage.

If SENSE is externally held more than the SETCAP pin, the current sink turns on in an attempt to restore SENSE to its programmed voltage. The current sink remains on until the external circuitry releases the SENSE pin.

Direct Paralleling for Higher Output Current

Higher output current is obtained by paralleling multiple LT3074 devices. Connect all SETRES, SETCAP, IN, and BIAS pins together. Connect the OUT pins together using small pieces of PCB trace or actual sense resistors (used as ballast resistors) beyond the feedback SENSE tap of each regulator to equalize the currents in LT3074 devices. Keep this ballast trace area free of solder to maintain a controlled resistance. *Table 9* shows the PCB trace resistance in mΩ/in.

The small worst case offset of 2mV for each paralleled LT3074 minimizes the required ballast resistor value. *Figure 92* illustrates that two LT3074 devices, each using a 2mΩ PCB trace ballast resistor, provide better than 20% accurate output current sharing at full load. The two 2mΩ external resistors only add 6mV of output regulation drop with 6A maximum current. With a 1V output, this voltage drop only adds 0.6% to the regulation accuracy. As discussed previously, connect the SENSE pin directly to the output capacitor.

Table 9. PC Board Trace Resistance

Weight (oz)	10 mil Width	20 mil Width
1	54.3	27.1
2	27.1	13.6

Trace resistance is measured in mΩ/in.

In addition, more than two LT3074 devices can be paralleled for even higher output current and lower output noise. Paralleling multiple LT3074 devices is also useful for spreading heat on the PCB.

PCB Layout Considerations

Given the high bandwidth and high PSRR of LT3074, careful PCB layout must be employed to achieve full device performance. *Figure 87* shows the evaluation board with a layout that delivers the full performance of the regulator. See the evaluation board for further details.

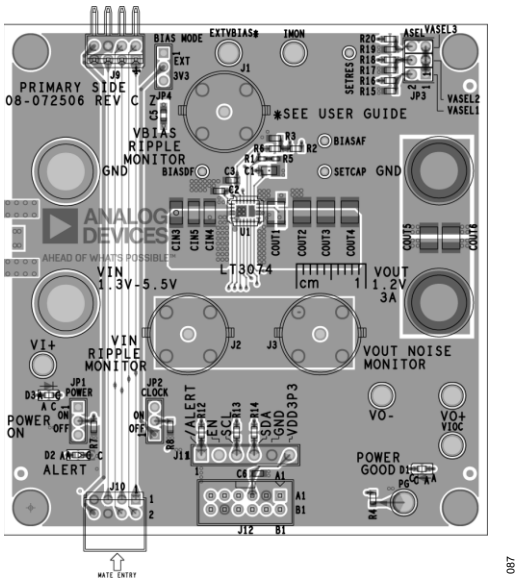


Figure 87. Evaluation Board Layout

High Efficiency Linear Regulator – Input-to-Output Voltage Control

The VIOC pin controls an upstream switching converter to maintain a constant voltage across the LT3074, regardless of the LDO's output voltage. This maximizes efficiency while maintaining PSRR performance. The VIOC pin is the output of a fast amplifier and equals (V_{IN} – V_{OUT}) + 800mV. As shown in *Figure 88*, the VIOC feature is simple to use. In the case of switching converters with feedback voltage, VFB ≥ 1V, connect the VIOC pin to the upstream switching converter's feedback (FB) pin. This regulates the LT3074 device's input-to-output differential to the switching converter's feedback voltage minus 800mV. When paralleling multiple LT3074 devices, connect the VIOC pin of one of the LT3074 device to the switching converter's FB pin and float all other VIOC pins. When LT3074 is turned off, V_{INLDO} is clamped to a voltage set by $V_{FBSWITCHER}$ × (R1 + R2)/R1.

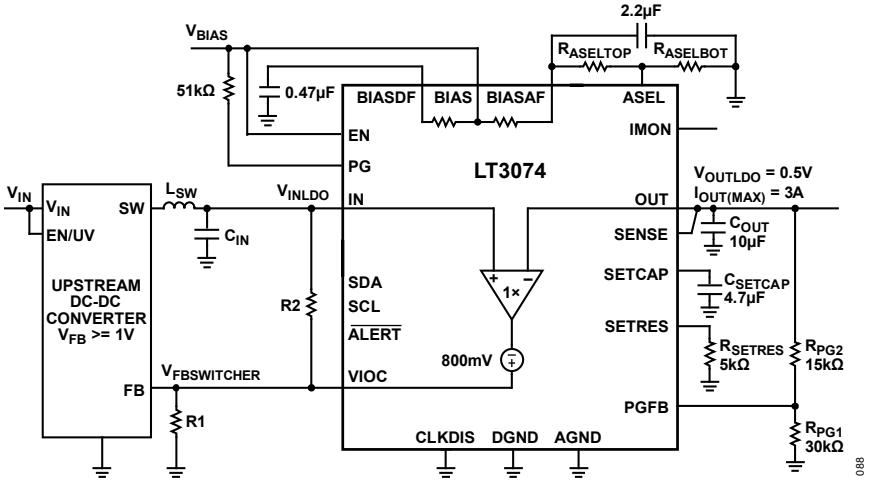


Figure 88. Basic VIOC Operation

While the VIOC buffer is inside the switching converter's feedback loop, given the VIOC buffer's high bandwidth, the switching converter's frequency compensation need not be adjusted. Phase delay through the VIOC buffer is typically less than 2° for frequencies as high as 100kHz. Hence, within the switching converter's bandwidth (usually much less than 100kHz), the VIOC buffer is transparent and acts like an ideal wire.

For example, for a switching converter with less than 100kHz bandwidth and a phase margin of 50°, using the VIOC buffer, the phase margin degrades by at most 2°. Hence, the phase margin for the switching converter (using the VIOC pin) is at least 48°. Given that the VIOC buffer is inside the switching converter's feedback loop, the total capacitance on the VIOC pin must be below 20pF.

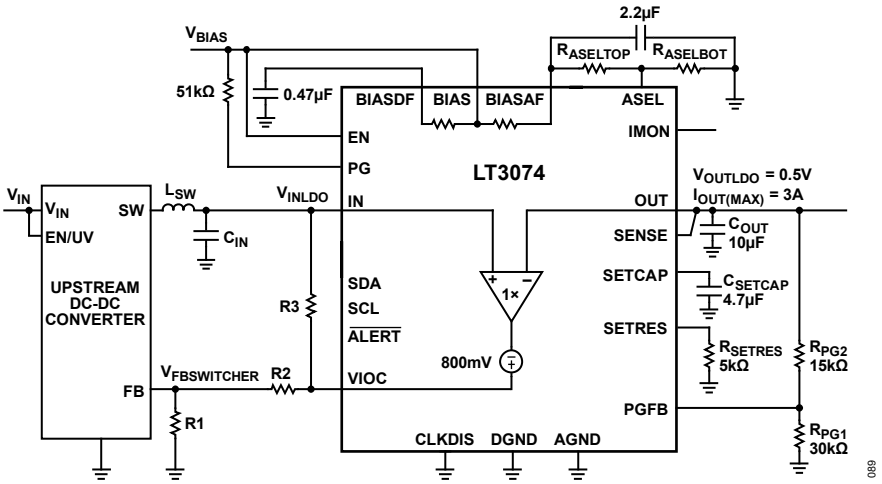


Figure 89. Programming Input-to-Output Voltage Differential

Figure 89 shows that the input-to-output differential voltage is easily programmable to support different application needs (PSRR vs. power dissipation) using the following equation:

$$V_{INLDO} - V_{OUTLDO} + 800mV = V_{VIOC} = V_{FBSWITCHER} \times \frac{R1 + R2}{R1}$$

Furthermore, if the LT3074 EN/UV pin is pulled low, the LT3074 input voltage can rise to the switching converter's input voltage and thus potentially violate the LT3074's absolute maximum rating. To prevent this, the maximum LT3074 input voltage can be set using a resistor (R3) between the VIOC and IN pins of the regulator such that:

$$V_{INLDO(MAX)} = V_{FBSWITCHER} \times \frac{R1 + R2 + R3}{R1}$$

The VIOC pin is capable of sourcing 200µA and sinking 20µA. Choose R1 and R3 values such that the VIOC pin sources at least 10µA to ensure system stability.

Figure 93 shows a typical VIOC application used to post-regulate the output of the LT8610A buck converter. The VIOC voltage is set at 1.1V (V_{INLDO} – V_{OUTLDO} is set to 300mV). The maximum LDO input voltage $V_{INLDO(MAX)}$ is set to 5.08V.

Thermal Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good hear sinking of the LT3074. The IN and OUT pins at the bottom of the package should be soldered to IN and OUT planes accordingly. In addition, the IN and OUT must be connected to large copper layers below with thermal vias; these layers spread heat dissipated by the LT3074. Placing additional vias can reduce thermal resistance further. The die temperature is calculated by multiplying the LT3074 power dissipation with the thermal resistance from the junction to ambient.

The internal overtemperature protection monitors the junction temperature of the LT3074. If the junction temperature reaches approximately 168°C, the LT3074 output is shut down until the temperature drops about 7°C.

Calculating Junction Temperature

Example: Given an output voltage of 1.2V, input voltage of 1.5V, and BIAS voltage of 5V, output ranges from 10mA to 3A, and a maximum ambient temperature of 50°C, what is the maximum junction temperature?

The LT3074's power dissipation is:

$I_{OUT(MAX)} \times (V_{IN} - V_{OUT}) + I_{GND} \times V_{BIAS}$

where: $I_{OUT(MAX)}$ = 3A; V_{BIAS} = 5V; I_{GND} (at V_{BIAS} = 5V and I_{OUT} = 3A) = 5mA

thus, P_{DISS} = 3A × (1.5V – 1.2V) + 5mA × 5V = 0.925W

When a 3mm × 4mm 4-layer LQFN package is used, the thermal resistance is in the range of 30°C/W to 36°C/W. Note that the θ_{JA} numbers vary beyond the 30°C/W to 36°C/W depending on board composition and layout. Considering a θ_{JA} value of 33°C/W, the junction temperature rise above the ambient approximately equals:

0.925W × 33°C/W = 30.525°C

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient:

T_{JMAX} = 50°C + 30.525°C = 80.525°C

Protection Features

The LT3074 incorporates internal current limit and thermal shutdown protection features. The internal current of the LT3074 typically clamps the output current to 4.5A. The die junction temperature can exceed the 125°C maximum operating temperature if the ambient temperature is high. If this occurs, the LT3074 relies on an internal thermal safety feature (thermal shutdown). Typically, at 168°C, the LT3074 thermal shutdown engages, and the output is shut down until the temperature falls below its thermal hysteresis limit.

Serial Bus Addressing

The LT3074 responds to PMBus global addresses of 7'h00 (general call address) and 7'h0C (SMBus alert response address). In addition, the ASEL pin allows the user to program 16 unique addresses for the LT3074. The three most significant bits (MSBs) of the 7-bit address are hardwired to 3'b110. A ±1% resistor divider from BIASAF, ASEL, and AGND sets the lower 4 bits of the 7-bit address. *Table 10* gives the recommended values of the resistors to be used for programming the corresponding address.

The LT3074 also supports the MFR_RAIL_ADDRESS register that allows the user to program a common address for all devices connected on a rail. The lower seven bits of the MFR_RAIL_ADDRESS register set the address to be used for communication and the MSB acts as the enable bit for this address. The rail address is enabled when the MSB of the MFR_RAIL_ADDRESS is set to 0 and disabled when the bit is set to 1. By default, the MSB of the MFR_RAIL_ADDRESS register is set to 1 and the lower 7 bits of this register are set to 7'h00. The MFR_RAIL_ADDRESS should only be used to write data to device registers connected on a shared rail. If the MFR_RAIL_ADDRESS is used to read data from the registers, data corruption is possible if all devices do not respond with the same data.

Table 10. Recommended Resistor Values for Address Programming Using ASEL pin

R_{ASEL_TOP} [1]	R_{ASEL_BOT} [1]	Address Lower Nibble	7-Bit Address
124kΩ	84.5kΩ	4'h0	7'h60 [2]
124kΩ	95.3kΩ	4'h1	7'h61 [3]
124kΩ	107kΩ	4'h2	7'h62
105kΩ	102kΩ	4'h3	7'h63
137kΩ	150kΩ	4'h4	7'h64
93.1kΩ	115kΩ	4'h5	7'h65
113kΩ	158kΩ	4'h6	7'h66
105kΩ	165kΩ	4'h7	7'h67
97.6kΩ	174kΩ	4'h8	7'h68
115kΩ	232kΩ	4'h9	7'h69
100kΩ	232kΩ	4'hA	7'h6A
90.9kΩ	243kΩ	4'hB	7'h6B
90.9kΩ	287kΩ	4'hC	7'h6C
69.8kΩ	261kΩ	4'hD	7'h6D
59kΩ	261kΩ	4'hE	7'h6E
47.5kΩ	261kΩ	4'hF	7'h6F [2]

[1] All resistors are 1% tolerance.

[2] Optionally, connecting the ASEL pin to AGND sets the 7-bit address to 7'h60 and connecting the ASEL pin to BIASAF sets the 7-bit address to 7'h6F.

[3] This is also the SM Bus device default address. If using this address, it is the responsibility of the user to ensure there is no contention on the bus.

Telemetry Readback

The LT3074 features an integrated 12-bit first order sigma-delta analog-to-digital converter (ADC) that monitors and performs conversions on the output voltage, output current, input voltage, bias voltage, and temperature. The ADC operates at a 1MHz clock frequency and is used in a round-robin fashion to monitor the physical quantities measured. The output voltage and output current are measured with a 12-bit resolution approximately every 9.216ms. The input voltage and bias voltage is measured with a 10-bit resolution approximately every 23.04ms. The die temperature is measured with a 10-bit resolution approximately every 46.08ms. *Figure 90* shows the round-robin pattern in which the voltages, current, and temperature are measured, as well as the conversion times associated with each measurement.

MEASUREMENT	V_{OUT} (12-BIT)	I_{OUT} (12-BIT)	V_{IN} (10-BIT)	V_{OUT} (12-BIT)	I_{OUT} (12-BIT)	V_{BIAS} (10-BIT)	V_{OUT} (12-BIT)	I_{OUT} (12-BIT)	V_{IN} (10-BIT)	V_{OUT} (12-BIT)	I_{OUT} (12-BIT)	V_{BIAS} (10-BIT)	V_{OUT} (12-BIT)	I_{OUT} (12-BIT)	TEMP (10-BIT)
t_{CONV}	4.096ms	4.096ms	1.024ms	4.096ms	4.096ms	1.024ms	4.096ms	4.096ms	1.024ms	4.096ms	4.096ms	1.024ms	4.096ms	4.096ms	1.024ms

090

Figure 90. ADC Round-Robin Pattern

Fault Reporting and the $\overline{\text{ALERT}}$ pin

The LT3074 supports various overvoltage, undervoltage, overcurrent, minimum current, and overtemperature faults and warnings. The $\overline{\text{ALERT}}$ pin is asserted low in response to any fault or warning that sets one or more bits of the *STATUS_BYTE* and/or *STATUS_WORD* register. *Figure 91* gives a summary of the fault bits reported by the LT3074.

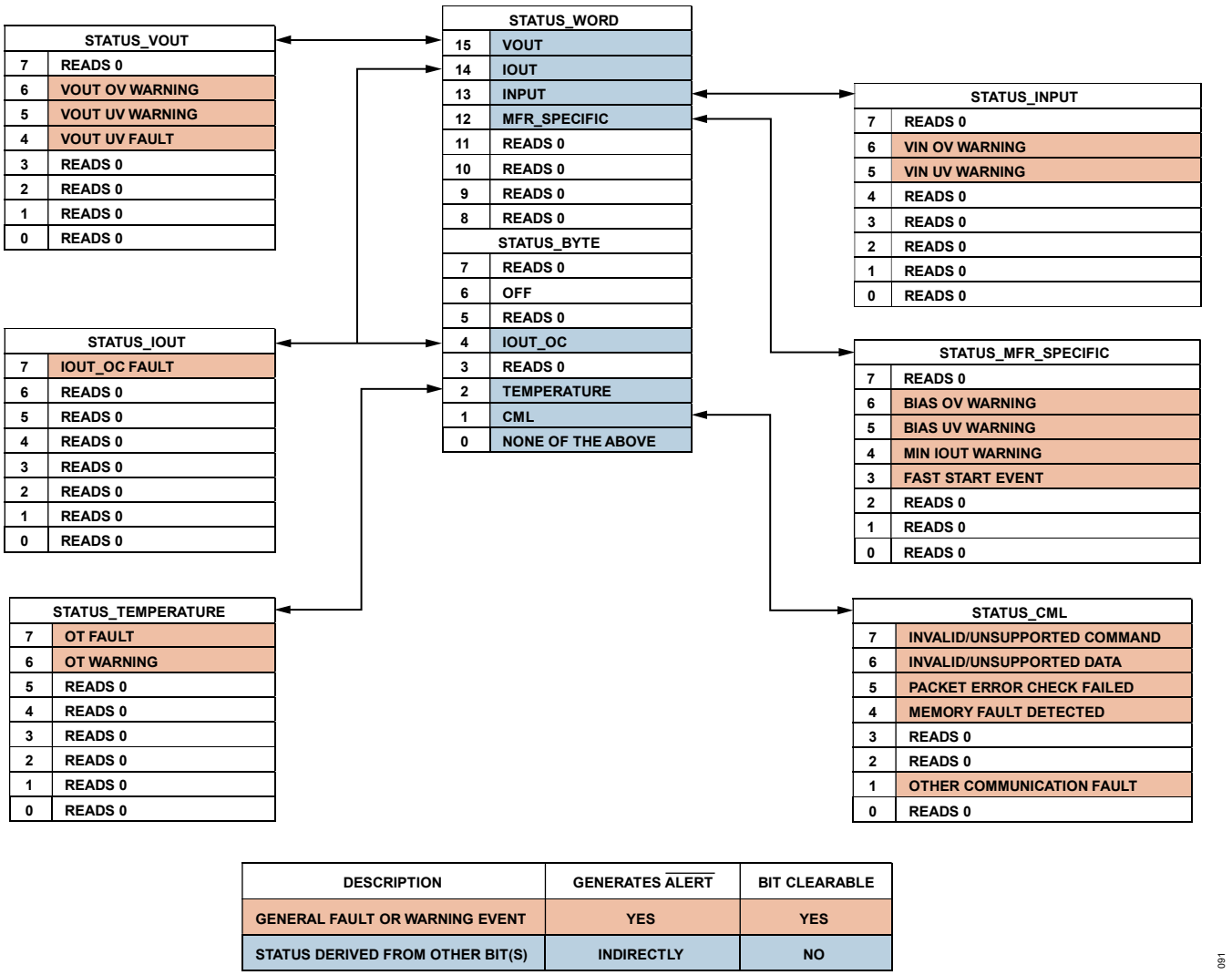


Figure 91. Summary of Faults Reported in the LT3074

Once the LT3074 pulls down the $\overline{\text{ALERT}}$ pin, the device continues to hold the pin low until one of the following occurs:

- The LT3074 is disabled and enabled again using the EN/UV pin.
- A *CLEAR_FAULTS* or *MFR_RESET* command is received (and the fault that caused the LT3074 to assert the $\overline{\text{ALERT}}$ pin low is not persistent).
- All status bits are cleared by writing a 1 to each bit (and the fault that caused the LT3074 to assert the $\overline{\text{ALERT}}$ pin low is not persistent).
- The LT3074 successfully transmits its address during a PMBus ARA.
- The BIAS power is removed from the device.

THE LT3074 does not support the masking of faults and warnings. If fault reporting for certain parameters is not needed, make sure to set the limits for the respective parameters beyond the normal operating range in the application. Regardless of the limits set, care must always be exercised to ensure the maximum operating ratings for

the LT3074 are not violated in the application setup. Faults that are detrimental to the device operation (such as thermal shutdown) are always reported and acted upon. See the *STATUS_BYTE* and *STATUS_WORD* commands and the related fault reporting commands for details on the faults supported by the LT3074.

Bus Timeout

The LT3074 implements a timeout feature to avoid hanging the serial interface. The SMBus specification includes three clock stretching specifications related to timeout conditions. The timeout conditions are described as following.

$T_{TIMEOUT}$

A timeout condition occurs if any single SCL clock pulse is held low for longer than $T_{TIMEOUT\_MIN}$ of 25ms. Upon detecting the timeout condition, the LT3074 aborts the transfer, releases the bus lines, and readies to accept a new start condition. The device initiating the timeout is required to hold the SCL clock line low for at least $T_{TIMEOUT\_MAX}$ of 35ms, guaranteeing that the LT3074 device has enough time to reset its communication protocol.

$T_{LOW:SEXT}$

The $T_{LOW:SEXT}$ of 25ms specification is defined as the cumulative time that the SCL line is held low by the target device in any one message from the start to stop condition. The LT3074 is guaranteed by design not to violate this specification.

$T_{LOW:MEXT}$

The $T_{LOW:MEXT}$ of 10ms specification is defined as the cumulative time that the SCL line is held low by the host device in any one byte of a message between the start-to-acknowledge, acknowledge-to-acknowledge, or acknowledge-to-stop. This check is not implemented in the LT3074.

PMBus Command Details

PAGE

The PAGE command is included to provide integration with multipage devices. The LT3074 accepts all data values for the PAGE register, ACKs the data, and discards it. Reading the PAGE register always returns 8'hFF.

OPERATION

The OPERATION command is used to turn the unit on or off in conjunction with the status of the EN pin. It is also used to program the output voltage to a high or low margin state. The unit stays in the commanded operating mode until a subsequent OPERATION command or a reset operation (either using the EN pin or the MRF_RESET command).

Table 11. OPERATION Command Bit Field Descriptions

Bit	Access Mode	Description
7	Read/Write	On/Off State **Value** – **Output Status** 'b0 [1] – Off 'b1 – On
6	Read Only	Turn Off Behavior (hardwired to turn off immediately)
5:4	Read/Write	Voltage Command Source **Value** – **Output Status** 'b00 – Nominal Output 'b01 – Output Margin Low (margin value set by MFR_MARGIN register)

5:4	Read/Write	‘b10	Output Margin High (margin value set by MFR_MARGIN register)
		‘b11	Not Supported
3:2	Read/Write	Margin Fault Response	
		Value	**Output Status**
		‘b00	Not Supported unless bits [5:4] are ‘b00 or bit 7 is ‘b0
		‘b01	Ignore Faults
		‘b10	Report Faults
		‘b11	Not Supported unless bits [5:4] are ‘b00 or bit 7 is ‘b0
1	Read Only	Not used	
0	Read Only	PMBus Reserved	

[1] Device does not respond to this data if bit 3 of the ON_OFF_CONFIG register is not set.

Programming unsupported data bytes to the OPERATION register generates an invalid data fault that is reported in the STATUS_CML register, and the command is ignored. The host is notified by asserting the $\overline{\text{ALERT}}$ pin. This command has one data byte.

ON_OFF_CONFIG

The ON_OFF_CONFIG command configures the combination of the EN pin input and the serial bus commands needed to turn the device on and off. This includes how the unit responds when the power is applied.

Table 12. ON_OFF_CONFIG Command Bit Field Descriptions

Bit	Access Mode	Description
7:5	Read Only	PMBus Reserved
4	Read Only	Turn On Behavior (hardwired to turn on only when commanded by the EN pin and/or OPERATION command)
3	Read/Write	OPERATION Command Control
		Value / **Output Status**
		‘b0 — Ignore On/Off State Bit (Bit 7) of OPERATION Command
		‘b1 — Turn on only when On/Off Bit (Bit 7) of OPERATION Command is ’b1
2	Read Only	EN pin control (EN pin must command the part to turn on)
1	Read Only	EN pin polarity (hardwired to be active high)
0	Read Only	Turn-off delay (hardwired to turn off immediately)

CLEAR_FAULTS

The CLEAR_FAULTS command is used to clear any fault bits that are set. This command clears all bits in all status registers simultaneously. At the same time, the device releases the $\overline{\text{ALERT}}$ pin signal output if the device is asserting the $\overline{\text{ALERT}}$ pin signal. If the fault is still present after the bits are cleared, the fault bit is set again and the host notified by asserting the $\overline{\text{ALERT}}$ pin low.

This is a write-only command with no data bytes.

WRITE_PROTECT

The WRITE_PROTECT command is used to control writing to the LT3074 registers. The intention of this command is to provide protection against accidental changes. *Table 13* gives a list of supported data bytes.

Table 13. WRITE_PROTECT Command Supported Data Bytes

Reg Byte	Description
0x80	Disable all writes except to the WRITE_PROTECT command.
0x40	Disable all writes except to the WRITE_PROTECT, PAGE and OPERATION commands.
0x20	Disable all writes except to the WRITE_PROTECT, PAGE, OPERATION and ON_OFF_CONFIG commands.
0x00	Enable all writes.

Sending a data byte that is not supported by the WRITE_PROTECT command generates an invalid data fault that is reported in the STATUS_CML register, and the command is ignored.

This command has one data byte.

CAPABILITY

This command provides a way for the host system to determine some key capabilities of a target device.

The LT3074 supports packet error checking, 400kHz bus speeds, and $\overline{\text{ALERT}}$ pin. This read-only command has one data byte.

VOUT_MODE

The VOUT_MODE command specifies the formatting for the output voltage. This includes the formatting for reporting the output voltage measured (as reported by the READ_VOUT register) as well as for setting the warning limits (set by the VOUT_OV_WARN_LIMIT and VOUT_UV_WARN_LIMIT registers). The data byte always reads 0x13 that implies a L16 (Linear 16 unsigned) format with an exponent fixed to -13.

This read-only command has one data byte.

VOUT_OV_WARN_LIMIT

The VOUT_OV_WARN_LIMIT command sets the value of the output voltage measured at the SENSE pin, in Volts, which causes an output voltage high warning. The output voltage measured and converted by the ADC (and reported using the READ_VOUT command) is used to compare the actual output voltage to the limit value. As a result, there can be up to a 10ms delay from the time the output voltage hits the limit to the time the fault is reported. Transitionary faults that last for a time period smaller than the ADC conversion time are filtered out and not reported.

In response to the VOUT_OV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register.
- Sets the VOUT bit in the STATUS_WORD register.
- Sets the VOUT_OV_WARNING bit in the STATUS_VOUT register.
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin.

This command has two data bytes and is formatted in the Linear_16u format.

VOUT_UV_WARN_LIMIT

The VOUT_UV_WARN_LIMIT command sets the value of the output voltage measured at the SENSE pin, in Volts, which causes an output voltage low warning. The output voltage measured and converted by the ADC (and reported using the READ_VOUT command) is used to compare the actual output voltage to the limit value. As a result, there

can be up to a 10ms delay from the time the output voltage hits the limit to the time the fault is reported. Transitionary faults that last for a time period smaller than the ADC conversion time are filtered out and not reported.

In response to the VOUT_UV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register.
- Sets the VOUT bit in the STATUS_WORD register.
- Sets the VOUT_UV_WARNING bit in the STATUS_VOUT register.
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin.

This command has two data bytes and is formatted in the Linear_16u format.

IOUT_OC_FAULT_LIMIT

The IOUT_OC_FAULT_LIMIT command sets the output current limit in amperes. The current limit programming range is from 1A to 6.4A with a step size of 50mA. Programmed current limit is rounded to the nearest 50mA step. For example, 1.01A is rounded to 1A and 1.04A is rounded to 1.05A. If a current limit value less than 1A is programmed, the data is accepted and stored in the IOUT_OC_FAULT_LIMIT register as received and internally the current limit value is set at 1A. For output current limit values set above 4.5A, the current limit is governed by the backup current limit of the LT3074 device.

In the event the output current hits the threshold set by the IOUT_OC_FAULT_LIMIT, the device:

- Regulates the output current set by the IOUT_OC_FAULT_LIMIT.
- Sets the IOUT_OC_FAULT bit in the STATUS_BYTE register.
- Sets the IOUT bit in the STATUS_WORD register.
- Sets the IOUT_OC_FAULT bit in the STATUS_IOUT register.
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin.

This command has two data bytes and is formatted in the Linear_5s_11s format.

IOUT_OC_FAULT_RESPONSE

The IOUT_OC_FAULT_RESPONSE notifies the host of the action of the LT3074 when an overcurrent fault is detected.

Table 14. IOUT_OC_FAULT_RESPONSE Command Bit Field Descriptions

Bit	Access Mode	Description
7:6	Read Only	Response **Value** / **Output Status** 'b00 — The LT3074 continues to operate indefinitely while maintaining the output current at a value set by the IOUT_OC_FAULT_LIMIT without regard for the output voltage (known as constant current or brickwall limiting).
5:3	Read Only	Not supported since LT3074 never shuts down (bits are hardwired to 'b000).
2:0	Read Only	Not supported since LT3074 never shuts down (bits are hard-wired to 'b000).

In addition to the response mentioned above, the device:

- Sets the IOUT_OC_FAULT bit in the STATUS_BYTE register.

- Sets the IOUT bit in the STATUS_WORD register.
- Sets the IOUT_OC_FAULT bit in the STATUS_IOUT register.
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin.

This read-only command has one data byte.

OT_WARN_LIMIT

The OT_WARN_LIMIT command sets the value of the average die temperature measured by the on-chip temperature sensor, in degrees Celsius, which causes an overtemperature warning. The die temperature measured and converted by the ADC (and reported using the READ_TEMPERATURE_1 command) is used to compare the average die temperature to the limit value. As a result, there can be up to 50ms delay from the time the average die temperature hits the limit to the time the fault is reported. Transitionary faults that last for a time period smaller than the ADC conversion time are filtered out and not reported.

In response to the OT_WARN_LIMIT being exceeded, the device:

- Sets the TEMPERATURE bit in STATUS_BYTE register.
- Sets the TEMPERATURE bit in the STATUS_WORD register.
- Sets the OVTWARNING bit in the STATUS_TEMPERATURE register.
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin.

This command has two data bytes and is formatted in the Linear_5s_1s format.

VIN_OV_WARN_LIMIT

The VIN_OV_WARN_LIMIT command sets the value of the input voltage measured at the IN pin, in Volts, which causes an input voltage high warning. The input voltage measured and converted by the ADC (and reported using the READ_VIN command) is used to compare the actual input voltage to the limit value. As a result, there can be up to a 20ms delay from the time the input voltage hits the limit to the time the fault is reported. Transitionary faults that last for a time period smaller than the ADC conversion time are filtered out and not reported.

In response to the VIN_OV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register.
- Sets the INPUT bit in the STATUS_WORD register.
- Sets the VIN_OV_WARNING bit in the STATUS_INPUT register.
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin.

This command has two data bytes and is formatted in the Linear_5s_11s format.

VIN_UV_WARN_LIMIT

The VIN_UV_WARN_LIMIT command sets the value of the input voltage measured at the IN pin, in Volts, which causes an input voltage low warning. The input voltage measured and converted by the ADC (and reported using the READ_VIN command) is used to compare the actual input voltage to the limit value. As a result, there can be up to a 20ms delay from the time the input voltage hits the limit to the time the fault is reported. Transitionary faults that last for a time period smaller than the ADC conversion time are filtered out and not reported.

In response to the VIN_UV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register.
- Sets the INPUT bit in the STATUS_WORD register.
- Sets the VIN_UV_WARNING bit in the STATUS_INPUT register.
- Notifies the host by asserting the ALERT pin.

This command has two data bytes and is formatted in the Linear_5s_11s format.

STATUS_BYTE

The STATUS_BYTE command returns a one-byte summary of the most critical faults.

Table 15. STATUS_BYTE Bit Field Descriptions

Bit	Access Mode	Bit Name	Description
7	Read Only	BUSY	Not supported (returns 0)
6	Read Only	OFF	This bit is set if the LT3074 is not providing power to the output, regardless of the reason, including simply not being turned on.
5	Read Only	VOUT_OV	Not supported (returns 0)
4	Read Only [1]	IOUT_OC	An output over current fault occurred.
3	Read Only	VIN_UV	Not supported (returns 0)
2	Read Only [2]	TEMPERATURE	A temperature fault occurred.
1	Read Only [3]	CML	A communication fault occurred.
0	Read Only	NONE OF THE ABOVE	A fault not listed by bits [7:1] occurred.

[1] Bit is cleared by clearing the IOUT_OC fault bit in the STATUS_IOUT register.
[2] Bit is cleared by clearing all bits in the STATUS_TEMPERATURE register.
[3] Bit is cleared by clearing all bits in the STATUS_CML register.

This command has one data byte.

STATUS_WORD

The STATUS_WORD command returns a two-byte summary of the device's fault condition. The low byte of the STATUS_WORD command is the same as STATUS_BYTE command. This command has two data bytes.

Table 16. STATUS_WORD High Byte Bit Field Descriptions

Bit	Access Mode	Bit Name	Description
15	Read Only [1]	VOUT	An output voltage fault or waning occurred.
14	Read Only [2]	IOUT	An output current fault or warning occurred.
13	Read Only [3]	INPUT	An input voltage warning occurred.
12	Read Only [4]	MFR_SPECIFIC	A warning specific to the LT3074 occurred.
11	Read Only	POWER_GOOD#	Not supported (returns 0)
10	Read Only	FANS	Not supported (returns 0)
9	Read Only	OTHER	Not supported (returns 0)
8	Read Only	UNKNOWN	Not supported (returns 0)

[1] Bit is cleared by clearing all bits in the STATUS_VOUT register.
[2] Bit is cleared by clearing all bits in the STATUS_IOUT register.
[3] Bit is cleared by clearing all bits in the STATUS_INPUT register.
[4] Bit is cleared by clearing all bits in the STATUS_MFR_SPECIFIC register.

STATUS_VOUT

The STATUS_VOUT command returns a one-byte summary of faults and warnings related to the output voltage.

Table 17. STATUS_VOUT Bit Field Descriptions

Bit	Access Mode	Bit Name	Description
7	Read Only	VOUT_OV_FAULT	Not supported (returns 0)
6	Read/Write 1 to Clear	VOUT_OV_WARN	An output overvoltage warning (as set by the VOUT_OV_WARN_LIMIT) occurred.
5	Read/Write 1 to Clear	VOUT_UV_WARN	An output undervoltage warning (as set by the VOUT_UV_WARN_LIMIT) occurred.
4	Read/Write 1 to Clear	VOUT_UV_FAULT	An output undervoltage fault (as set by the PGFB pin) occurred.
3	Read Only	VOUT_MAX_MIN	Not supported (returns 0)
2	Read Only	TON_MAX	Not supported (returns 0)
1	Read Only	TOFF_MAX	Not supported (returns 0)
0	Read Only	VOUT_TRACKING	Not supported (returns 0)

This command has one data byte.

STATUS_IOUT

The STATUS_IOUT command returns a one-byte summary of faults and warnings related to the output current.

Table 18. STATUS_IOUT Bit Field Descriptions

Bit	Access Mode	Bit Name	Description
7	Read/Write 1 to Clear	IOUT_OC_FAULT	An output overcurrent fault (as set by the IOUT_OC_FAULT_LIMIT) occurred.
6	Read Only	IOUT_OC_LV_FAULT	Not supported (returns 0)
5	Read Only	IOUT_OC_WARNING	Not supported (returns 0)
4	Read Only	IOUT_UC_FAULT	Not supported (returns 0)
3	Read Only	Current Share Fault	Not supported (returns 0)
2	Read Only	TON_MAX	Not supported (returns 0)
1	Read Only	TOFF_MAX	Not supported (returns 0)
0	Read Only	VOUT_TRACKING	Not supported (returns 0)

This command has one data byte.

STATUS_INPUT

The STATUS_INPUT command returns one-byte summary of warnings related to the input voltage.

Table 19. STATUS_INPUT Bit Field Descriptions

Bit	Access Mode	Bit Name	Description
7	Read Only	VIN_OV_FAULT	Not supported (returns 0)
6	Read/Write 1 to Clear	VIN_OV_WARNING	An input overvoltage warning (as set by the VIN_OV_WARN_LIMIT) occurred.
5	Read/Write 1 to Clear	VIN_UV_WARNING	An input undervoltage warning (as set by the VIN_UV_WARN_LIMIT) occurred.
4	Read Only	VIN_UV_FAULT	Not supported (returns 0)
3	Read Only	VIN_UVLO	Not supported (returns 0)

Bit	Access Mode	Bit Name	Description
2	Read Only	IIN_OC_FAULT	Not supported (returns 0)
1	Read Only	IIN_OC_WARNING	Not supported (returns 0)
0	Read Only	PIN_OP_WARNING	Not supported (returns 0)

This command has one data byte.

STATUS_TEMPERATURE

The STATUS_TEMPERATURE command returns a one-byte summary of faults and warnings related to the average die temperature.

Table 20. STATUS_TEMPERATURE Bit Field Descriptions

Bit	Access Mode	Bit Name	Description
7	Read/Write 1 to Clear	OT_FAULT	A thermal shutdown event occurred.
6	Read/Write 1 to Clear	OT_WARNING	An overtemperature warning (as set by the OT_WARN_LIMIT) occurred.
5	Read Only	UT_WARNING	Not supported (returns 0)
4	Read Only	UT_FAULT	Not supported (returns 0)
3:0	Read Only	PMBus Reserved	Returns 4'b0000

This command has one data byte.

STATUS_CML

The STATUS_CML command returns a one-byte summary of faults related to PMBus communication, memory, and logic.

Table 21. STATUS_CML Bit Field Descriptions

Bit	Access Mode	Bit Name	Description
7	Read/Write 1 to Clear	Invalid/Unsupported Command	A command not supported by the LT3074 is received.
6	Read/Write 1 to Clear	Invalid/Unsupported Data	A data value not supported by the LT3074 is received.
5	Read/Write 1 to Clear	Packet Error Check Failed	PEC data byte received is incorrect.
4	Read Only [1]	Memory Fault Detected	Uncorrectable error with the trim fuses occurred.
3	Read Only	Processor Fault Detected	Not supported (returns 0)
2	Read Only	PMBus Reserved	Returns 0
1	Read/Write 1 to Clear	Other Communication Fault	Communication fault not listed above occurred.
0	Read Only	Other Memory or Logic Fault	Not supported (returns 0)

[1] Writing 1 to this bit clears it and the bit is set again as the fault is persistent and cannot be resolved.

This command has one data byte.

STATUS_MFR_SPECIFIC

The STATUS_MFR_SPECIFIC command returns a one-byte summary of warnings specific to the LT3074.

Table 22. STATUS_MFR_SPECIFIC Bit Field Descriptions

Bit	Access Mode	Bit Name	Description
7	Read Only	Unused	Returns 0
6	Read/Write 1 to Clear	VBIAS_OV_WARNING	A bias overvoltage warning (as set by the MFR_BIAS_OV_WARN_LIMIT) occurred.
5	Read/Write 1 to Clear	VBIAS_UV_WARNING	A bias undervoltage warning (as set by the MFR_BIAS_UV_WARN_LIMIT) occurred.
4	Read/Write 1 to Clear	IOUT_MIN_WARNING	A minimum output current warning (as set by the MFR_IOUT_MIN_WARN_LIMIT) occurred.
3	Read/Write 1 to Clear	FAST_START	A fast start-up event (post initial power on) occurred.
2:0	Read Only	Unused	Returns 3'b000

This command has one data byte.

READ_VIN

The READ_VIN command returns the measured IN pin voltage, in Volts. This read-only command has two data bytes formatted in the Linear_5s_11s format.

READ_VOUT

The READ_VOUT command returns the measured SENSE pin voltage, in Volts. This read-only command has two data bytes formatted in the Linear_16u format.

READ_IOUT

The READ_IOUT command returns the measured output current, in Amperes. This read-only command has two data bytes formatted in the Linear_5s_11s format.

READ_TEMPERATURE_1

The READ_TEMPERATURE_1 command returns the measured average die temperature, in degree Celsius. This read-only command has two data bytes formatted in the Linear_5s_11s format.

PMBUS_REVISION

The PMBUS_REVISION command returns the revision of PMBus specification that the device supports. The LT3074 is compliant with the PMBus version 1.3, both part I and part II.

This read-only command has one data byte.

IC_DEVICE_ID

The IC_DEVICE_ID command indicates the manufacturer's ID of the LT3074 using ASCII characters. This read-only command is in block format.

IC_DEVICE_REV

The IC_DEVICE_REV command indicates the revision of the LT3074 using ASCII characters. This read-only command is in block format.

MFR_MARGIN

The MFR_MARGIN command is used to calculate the output voltage high and low margin values, as a percentage of the nominal output voltage. The margin value calculated using this command is applied at the output of the LT3074 based on the status of the OPERATION command.

Table 23. MFR_MARGIN Bit Field Descriptions

Bit	Access Mode	Description
7:4	Read/Write	4-bit code used to calculate the high side margin percentage. See *Table 24* for the margin percentage corresponding to each code.
3:0	Read/Write	4-bit code used to calculate the low side margin percentage. See *Table 24* for the margin percentage corresponding to each code.

Table 24. MFR_MARGIN Code to Margining Percentage Mapping

4-Bit Code	Margin Percentage
4'b0000	0
4'b0001	1
4'b0010	3
4'b0011	5
4'b0100	10
4'b0101	15
4'b0110	20
4'b0111	25
4'b1000	30

This command has one data byte.

MFR_READ_VBIAS

The MFR_READ_VBIAS command returns the measured BIAS pin voltage, in Volts. This read-only command has two data bytes formatted in the Linear_5s_11s format.

MFR_BIAS_OV_WARN_LIMIT

The MFR_BIAS_OV_WARN_LIMIT command sets the value of the bias voltage measured at the BIAS pin, in Volts, which causes a bias voltage high warning. The bias voltage measured and converted by the ADC (and reported using the MFR_READ_VBIAS command) is used to compare the actual bias voltage to the limit value. As a result, there can be up to a 20ms delay from the time the bias voltage hits the limit to the time the fault is reported. Transitionary faults that last for a time period smaller than the ADC conversion time are filtered out and not reported.

In response to the MFR_BIAS_OV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register.
- Sets the MFRSPECIFIC bit in the STATUS_WORD register.
- Sets the VBIAS_OV_WARNING bit in the STATUS_MFR_SPECIFIC register.
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin.

This command has two data bytes and is formatted in the Linear_5s_11s format.

MFR_BIAS_UV_WARN_LIMIT

The MFR_BIAS_UV_WARN_LIMIT command sets the value of the bias voltage measured at the BIAS pin, in Volts, which causes a bias voltage low warning. The bias voltage measured and converted by the ADC (and reported using the MFR_READ_VBIAS command) is used to compare the actual bias voltage to the limit value. As a result, there can be up to a 20ms delay from the time the bias voltage hits the limit to the time the fault is reported. Transitionary faults that last for a time period smaller than the ADC conversion time are filtered out and not reported.

In response to the MFR_BIAS_UV_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register.
- Sets the MFRSPECIFIC bit in the STATUS_WORD register.
- Sets the VBIAS_UV_WARNING bit in the STATUS_MFR_SPECIFIC register.
- Notifies the host by asserting the ALERT pin.

This command has two data bytes and is formatted in the Linear_5s_11s format.

MFR_IOUT_MIN_WARN_LIMIT

The MFR_IOUT_MIN_WARN_LIMIT command sets the value of the minimum output current, in Amperes, which causes an output low current warning. This command can be used to detect open connections from the output of the LT3074 to the load device. The output current measured and converted by the ADC (and reported using the READ_IOUT command) is used to compare the actual output current to the limit value. As a result, there can be up to a 14ms delay from the time the output current hits the limit to the time the fault is reported. Transitionary faults that last for a time period smaller than the ADC conversion time are filtered out and not reported.

In response to the MFR_IOUT_MIN_WARN_LIMIT being exceeded, the device:

- Sets the NONE_OF_THE_ABOVE bit in STATUS_BYTE register.
- Sets the MFRSPECIFIC bit in the STATUS_WORD register.
- Sets the IOUT_MIN_WARNING bit in the STATUS_MFR_SPECIFIC register.
- Notifies the host by asserting the $\overline{\text{ALERT}}$ pin.

This command has two data bytes and is formatted in the Linear_5s_11s format.

If the LT3074 is powered on without a preload greater than the default value set by MFR_MIN_IOUT_WARN_LIMIT register, the LT3074 asserts a fault once it completes the start-up procedure.

MFR_SPECIAL_ID

The MFR_SPECIAL_ID command is used by the LTPowerPlay GUI for device identification. This read-only command has two data bytes.

MFR_DEFAULT_CONFIG

The MFR_DEFAULT_CONFIG command is used to notify the host if any of the write-able registers of the LT3074 have been modified. A value of 0x01 indicates that all write-able registers are in their default configuration (as set upon a power on or a reset event). A value of 0x00 indicates that at least one write-able register has been modified from its default status. This command can be used to detect a BIAS UVLO event.

This command has one data byte.

MFR_RAIL_ADDRESS

The MFR_RAIL_ADDRESS command sets a direct PMBus address for the LT3074. This address should be common to all devices attached to a single power supply rail. Only perform command writes to this address. If a read is performed from this address and the rail devices do not respond with EAXCTLY the same value, this leads to bus contention and data corruption.

Setting this command to a value of 0x80 disables rail device addressing.

This command has one data byte.

MFR_RESET

The MFR_RESET command provides a means to reset the LT3074 from the serial bus. This forces the LT3074 to turn off the output power, discharge the output and the reference, reset the digital logic, clear all faults and then perform a soft start of the output.

This write-only command has no data bytes.

TYPICAL APPLICATION CIRCUITS

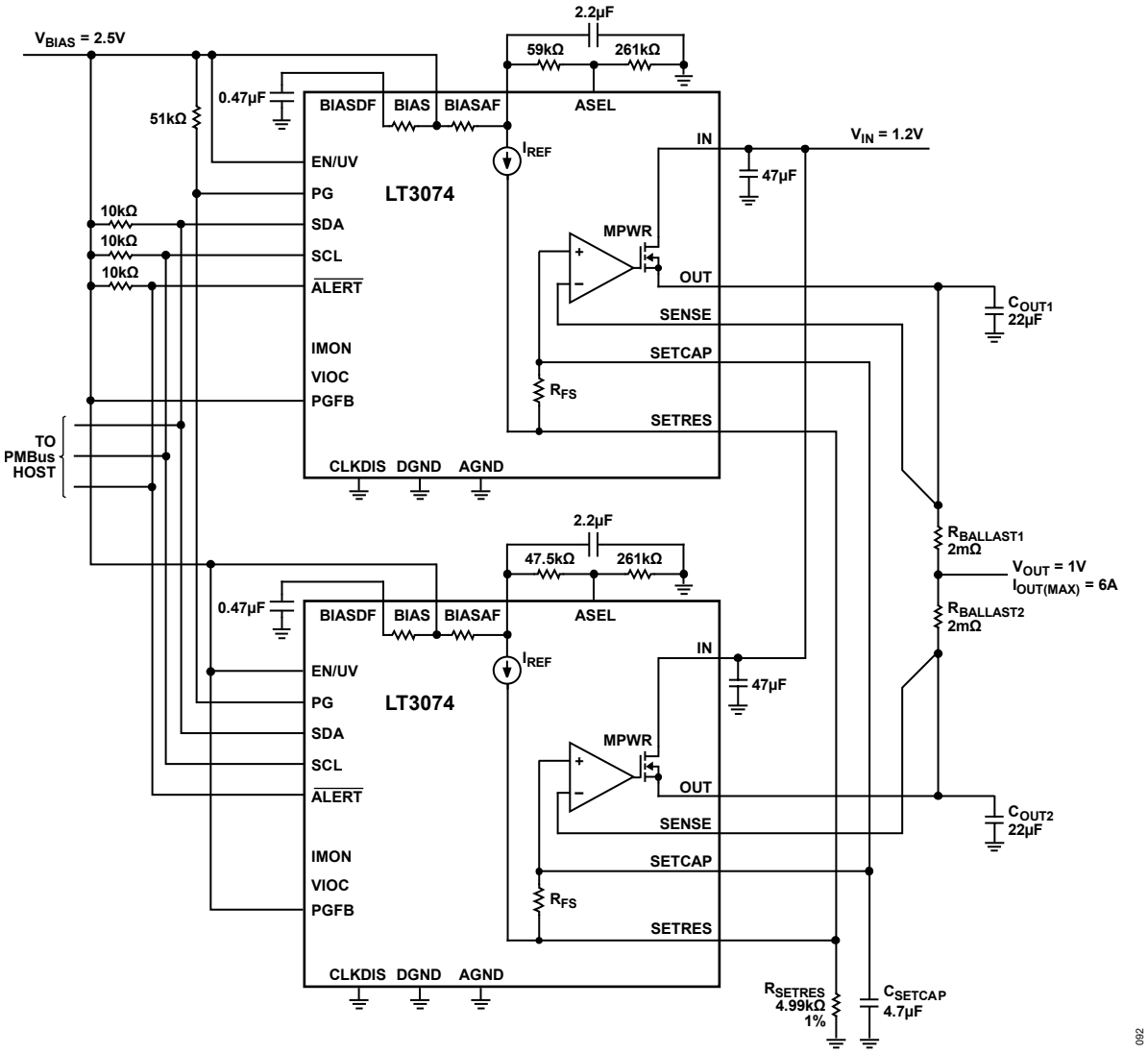


Figure 92. Paralleling Multiple LT3074s for Higher Output Current

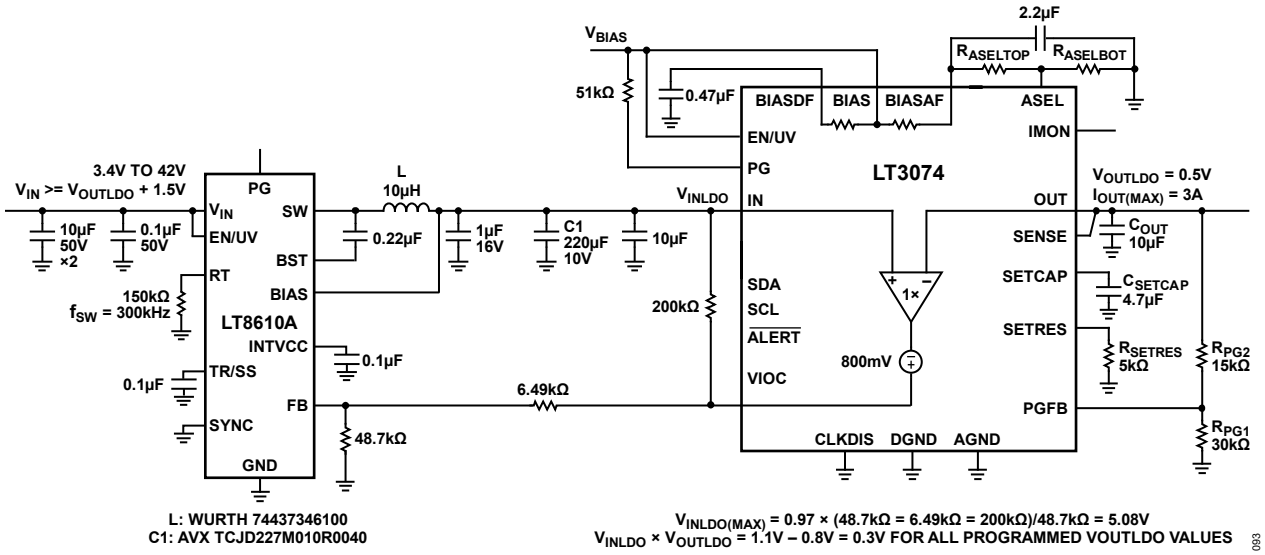
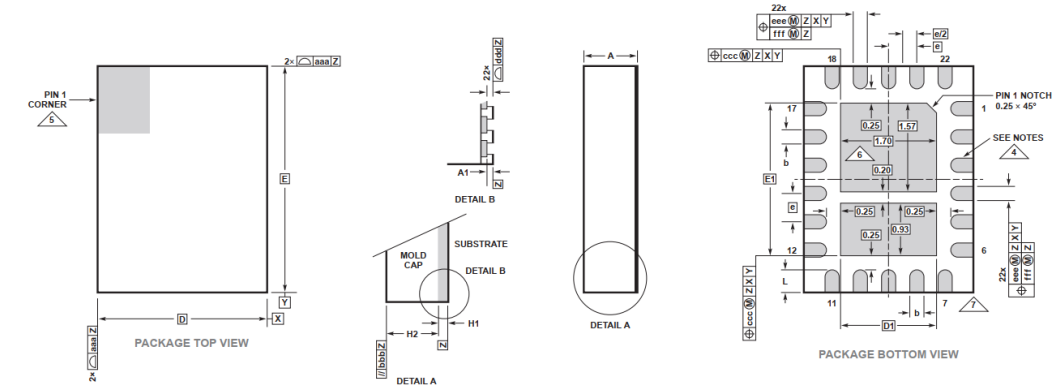


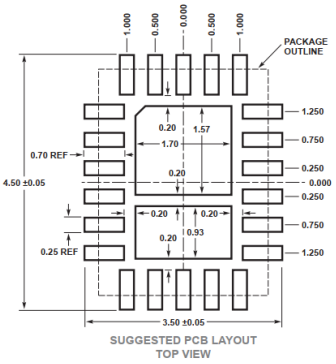
Figure 93. Regulator with VIOC Buck Control

OUTLINE DIMENSIONS

ANALOG DEVICES | ADI Power by Linear™

22-Terminal Land Grid Array [LGA]
(3mm × 4mm × 0.95mm)
(Reference DWG # CC-22-4)





DIMENSIONS				
SYMBOL	MIN	NOM	MAX	NOTES
A	0.85	0.95	1.05	
A1			0.03	
L	0.30	0.40	0.50	
b	0.22	0.25	0.28	
D		3.00		
E		4.00		
D1		1.70		
E1		2.70		
e		0.50		
H1		0.25 REF		SUBSTRATE THK
H2		0.70 REF		MOLD CAP HT
aaa			0.10	
bbb			0.10	
ccc			0.10	
ddd			0.10	
eee			0.15	
fff			0.08	

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. PRIMARY DATUM -Z- IS SEATING PLANE
4. METAL FEATURES UNDER THE SOLDER MASK OPENING NOT SHOWN SO AS NOT TO OBSCURE THESE TERMINALS AND HEAT FEATURES
5. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN 1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
6. THE EXPOSED HEAT FEATURE MAY HAVE OPTIONAL CORNER RADII
7. CORNER SUPPORT PAD CHAMFER IS OPTIONAL

ORDERING GUIDE

Table 25. Ordering Guide

Model 1	Temperature Range	Package Description	MSL Rating	Packing Quantity	Package Option
LT3074AV#PBF	-40°C to 125°C	22-LEAD (3mm x 4mm LQFN)	3	Tray, 490	CC-22-4
LT3074AV#TRPBF	-40°C to 125°C	22-LEAD (3mm x 4mm LQFN)	3	Reel, 2500	CC-22-4

1 All models are RoHS compliant.

EVALUATION BOARDS

Table 26. Evaluation Boards

Model [1]	Description
EVAL-LT3074-AZ	Evaluation Board

[1] The TBD is RoHS compliant.

RELATED PARTS

Table 27. Related Parts

PART NUMBER	DESCRIPTION	COMMENTS
LT3073	3A, Ultralow Noise, High PSRR, 45mV Dropout Ultrafast Linear Regulator	45mV Dropout Voltage, Digitally Programmable V_{OUT}: 0.5V to 4.2V, Digital Output Margining: ±2.5%, Ultralow Output Noise: 1.2µV_{RMS} (10Hz to 100kHz), Direct Parallelable, Soft-Start, Stable with Low ESR Ceramic Capacitance (10µF Minimum), 22-Lead 3mm × 4mm LQFN package.
LT3070-1	5A, Low Noise, Programmable V_{OUT}, 85mV Dropout Linear Regulator with Digital Margining	85mV Dropout Voltage, Digitally Programmable V_{OUT}: 0.8V to 1.8V, Digital Output Margining: ±1%, ±3% or ±5%, Low Output Noise:25µV_{RMS}; Directly Parallelable, Soft-Start, Stable with Low ESR Ceramic Output Capacitors (15µF Minimum), 28-Lead 4mm × 5mm QFN Package.
LT3072	Dual, Low Noise, 2.5A Programmable Output, 80mV Low Dropout Linear Regulator	Dual, Independent 2.5A Outputs, Dropout Voltage: 80mV, Low Output Noise: 12µV_{RMS} (10Hz to 100kHz), Digitally Programmable V_{OUT}: 0.6V to 2.5V, Output Tolerance: ±1.25%/±1.5% Overload, Line, and Temperature, Analog Output Margining: ±10% Range, 36-Lead 4mm × 7mm QFN Package.
ADP1763	3A, Low V_{IN}, Low Noise, CMOS Linear Regulator	95mV Dropout, Fixed (0.9V to 1.5V) and Adjustable (0.5V to 1.5V) V_{OUT}, V_{IN} = 1.1V to 1.98V, 2µV_{RMS} Noise (100Hz to 100kHz), Programmable Soft-Start, Direct Parallelable, Stable with Ceramic Capacitors (10µF Minimum), AEC-Q100 qualified, 16-Lead 3mm x 3mm LFCSP Package.
ADP1765	5A, Low V_{IN}, Low Noise, CMOS Linear Regulator	59mV Dropout, Fixed (0.55V to 1.5V) and Adjustable (0.5V to 1.5V) V_{OUT}, V_{IN} = 1.1V to 1.98V, 2µV_{RMS} Noise (100Hz to 100kHz), Programmable Soft-Start, Direct Parallelable, Stable with Ceramic Capacitors (22µF minimum), 16-Lead 3mm x 3mm LFCSP Package.
MAX38907	4A, High-Performance LDO Linear Regulator	79mV Dropout, Digitally Programmable V_{OUT}: 0.6V to 5V, V_{IN} = 0.9V to 5.5V, Digital Margining: ±5%, Programmable Soft Start, Reverse Current Protection, Active Discharge, 20-Lead 5mm x 5mm TQFN Package.

PART NUMBER	DESCRIPTION	COMMENTS
LT3041	20V, 1A, Ultralow Noise, Ultrahigh PSRR Linear Regulator with VIOC Control	1µV_{RMS} Noise (10Hz to 100kHz), 8µV_{P-P} Noise (0.1Hz to 10Hz), 80dB PSRR at 1MHz, V_{IN} = 2.2V to 20V, V_{OUT} = 0.2V to 15V, 310mV Dropout, Direct Parallelable, Programmable Current Limit, and Power Good, Stable with Low ESR Ceramic Capacitors (2x 10µF Minimum), 14-Lead 4mm x 3mm DFN Package.
LT3045	500mA, Ultralow Noise and Ultrahigh PSRR LDO	0.8µV_{RMS} Noise and 75dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 260mV Dropout Voltage, 3mm × 3mm DFN and MSOP Packages.
LT3042	200mA, Ultralow Noise and Ultrahigh PSRR LDO	0.8µV_{RMS} Noise and 79dB PSRR at 1MHz, V_{IN} = 1.8V to 20V, 350mV Dropout Voltage, Programmable Current Limit and Power Good, 3mm × 3mm DFN and MSOP Packages.

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