Data Sheet

# ADL5961

## 9 kHz to 26.5 GHz Integrated Vector Network Analyzer Front End

## FEATURES

- Wideband integrated bidirectional bridge
  - Raw directivity: 35.6 dB at 1 GHz, 16.7 dB at 18 GHz
  - Low insertion loss: 1.1 dB at 1 GHz, 2.0 dB at 18 GHz
  - Return loss: >12 dB typical
- SPI configurable LO interface
  - Divide by 2; multiply by 1, 2, or 4
  - Offset LO interface enables drive with $f_{RF} = f_{LO}$
  - Single-ended or differential drive
  - SYNC function—synchronization across multiple devices
- High dynamic range wideband IF signal path
  - SPI-programmable IF bandwidth from 1 MHz to 100 MHz
  - SPI-programmable IF gain, 6 dB step size
  - Externally adjustable output common-mode level
- 5-bit SPI readable temperature sensor
- Low power shutdown mode
- 3 mm × 4 mm, 26-lead LGA

## APPLICATIONS

- Broadband, multiport vector network analyzers
- S-parameter magnitude and phase measurement
- Inline RF power measurement
- Automated test equipment
- Reflectometers
- Materials analysis

## FUNCTIONAL BLOCK DIAGRAM

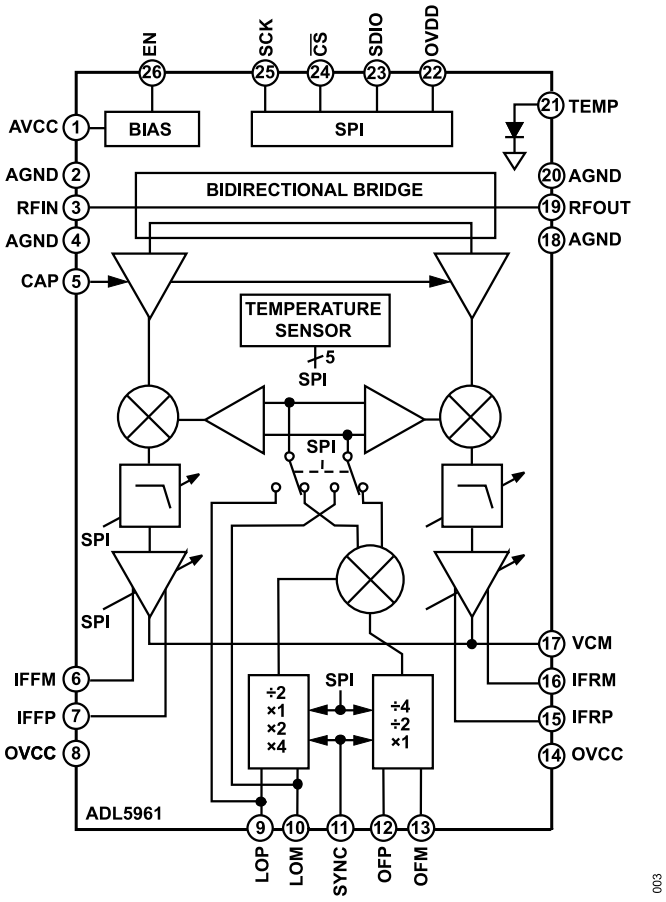



*Figure 1. Functional Block Diagram*

## GENERAL DESCRIPTION

The ADL5961 is a wideband, small form factor, vector network analyzer (VNA) front end consisting of a resistive bidirectional bridge, downconversion mixers, programmable IF amplifiers and filters, and a highly flexible local oscillator (LO) interface. The bridge provides >14 dB of directivity up to 17 GHz. The primary transmission line from RFIN to RFOUT is wideband matched to 50 Ω with only 1.1 dB loss at 9 kHz near DC, increasing to 1.8 dB loss at 26.5 GHz.

The ADL5961 supports several different LO interface configurations that simplify the clocking design of a VNA solution as well as the interfacing of the device to an analog-to-digital converter (ADC). The frequency divider and multipliers in the LO interface enable measurement sweeps beyond the operating frequency range of the LO source, enabling operation over the full 26.5 GHz frequency range of the ADL5961 using a 6 GHz synthesizer. The IF frequency offset mixer, driven through the offset interface formed by the OFP and OFM pins, enables further simplification by allowing the swept RF and LO interfaces to share the same frequency source.

The frequency of the IF output signals is then determined by the low-frequency source driving the OFP/OFM interface. When this interface is driven at the ADC sample frequency with the divide by 4 enabled, it automatically centers the IF output signal in the first Nyquist zone.

The IF filters with programmable bandwidth and IF amplifiers with individually programmable gain enable simultaneous dynamic range optimization of the IF output signals of the forward channel (IFFP, IFFM) and reverse channel (IFRP, IFRM). The IF amplifiers have an adjustable output common-mode level, sufficient drive capability, and wide output voltage swing to enable direct interfacing to a wide range of ADCs.

All configurations and functions in the ADL5961 are fully programmable through a 3-wire serial peripheral interface (SPI). The ADL5961 is offered in a 3 mm × 4 mm, 26-lead land grid array (LGA) package.

Rev. 0

## TABLE OF CONTENTS



## REVISION HISTORY

**10/2024—Revision 0: Initial Version**

## SPECIFICATIONS

AVCC = OVCC = 5.0 V, EN = OVDD = 3.3 V, VCM = 2.5 V, $T_A$ = 25°C, source impedance ($Z_O$) and load impedance ($Z_L$) = 50 Ω, continuous wave input at RFIN, RF power ($P_{RF}$) = 0 dBm, LO drive single-ended, LO power ($P_{LO}$) = 0 dBm, RF frequency ($f_{RF}$) = 1 GHz, LO frequency ($f_{LO}$) = $f_{RF}$ + 500 kHz, FGAIN (Register 0x23, Bits[6:0]) = RGAIN (Register 0x24, Bits[6:0]) = 24 (decimal), BYPASS (Register 0x20, Bit 4) = 1, default SPI register values, unless otherwise noted. Test circuit shown in Figure 72.

***Table 1. Specifications***

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| BIDIRECTIONAL BRIDGE | RFIN to RFOUT | | | | |
| RF Frequency Range | | | 0.000009 to 26.5 | | GHz |
| Insertion Loss | $f_{RF}$ = 100 kHz | | 0.9 | | dB |
| | $f_{RF}$ = 1 GHz | | 1.1 | | dB |
| | $f_{RF}$ = 10 GHz | | 1.8 | | dB |
| | $f_{RF}$ = 15 GHz | | 1.9 | | dB |
| | $f_{RF}$ = 18 GHz | | 2.0 | | dB |
| | $f_{RF}$ = 26.6 GHz | | 4.8 | | dB |
| Return Loss (S11) | $f_{RF}$ < 20 GHz | | >12 | | dB |
| Directivity[1] | $f_{RF}$ = 100 kHz, LOMODE = 0, BYPASS = 0 | | 40.5 | | dB |
| | $f_{RF}$ = 1 GHz | | 35.6 | | dB |
| | $f_{RF}$ = 10 GHz | | 20.4 | | dB |
| | $f_{RF}$ = 15 GHz | | 25.1 | | dB |
| | $f_{RF}$ = 18 GHz | | 16.7 | | dB |
| | $f_{RF}$ = 26.5 GHz | | 9.1 | | dB |
| Third-Order Intercept (IP3) | $f_{RF}$ = 1 GHz | | 71 | | dBm |
| VNA CHANNELS | RFIN to IFFP/IFFM, RFOUT to IFRP/IFRM | | | | |
| RF Frequency Range | | | 0.000009 to 26.5 | | GHz |
| RF to IF Leakage | $f_{RF}$ = 50 MHz, differential IF output | | −13.5 | | dBV |
| Maximum Voltage Conversion Gain[2] | FGAIN, RGAIN = 0x42 (66 dB), $f_{LO}$ = $f_{RF}$ + 10 MHz | | | | |
| | $f_{RF}$ = 100 kHz | | 51.1 | | dB |
| | $f_{RF}$ = 1 GHz | | 51.1 | | dB |
| | $f_{RF}$ = 10 GHz | | 48.9 | | dB |
| | $f_{RF}$ = 15 GHz | | 46.4 | | dB |
| | $f_{RF}$ = 18 GHz | | 45 | | dB |
| | $f_{RF}$ = 26.5 GHz | | 33.1 | | dB |
| Minimum Voltage Conversion Gain | FGAIN, RGAIN = 0x00 (0 dB), $f_{LO}$ = $f_{RF}$ + 10 MHz | | | | |
| | $f_{RF}$ = 100 kHz | | −11.2 | | dB |
| | $f_{RF}$ = 1 GHz | −13 | −11.2 | −9 | dB |
| | $f_{RF}$ = 10 GHz | | −13.4 | | dB |
| | $f_{RF}$ = 15 GHz | | −15.9 | | dB |
| | $f_{RF}$ = 18 GHz | | −17.3 | | dB |
| | $f_{RF}$ = 26.5 GHz | | −26.4 | | dB |
| Conversion Gain Step Size | See Table 12 | 4.4 | | 6.3 | dB |
| Input 1dB Compression Point (IP1dB) | $f_{RF}$ = 1 GHz, FGAIN = RGAIN = 0 | | 29 | | dBm |
| Output 1dB Compression Point (OP1dB) | FGAIN, RGAIN ≥ 12, 100 Ω differential load | | 18.4 | | dBm |
| Input Third-Order Intercept (IIP3)[3] | $f_{RF}$ = 1 GHz, FGAIN, RGAIN = 0 | | 32 | | dBm |
| Output Third-Order Intercept (OIP3) | FGAIN = RGAIN = 30 (decimal) | | 32.3 | | dBm |
| Input Second-Order Intercept (IIP2)[3] | $f_{RF}$ = 1 GHz, FGAIN = RGAIN = 0 | | 55 | | dBm |

## SPECIFICATIONS

*Table 1. Specifications (Continued)*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Noise Figure | FGAIN = RGAIN = 60 (decimal) | | | | |
| | $f_{RF}$ = 1 GHz | | 48.2 | | dB |
| | $f_{RF}$ = 10 GHz | | 48.1 | | dB |
| | $f_{RF}$ = 15 GHz | | 47.7 | | dB |
| | $f_{RF}$ = 18 GHz | | 49.5 | | dB |
| | $f_{RF}$ = 26.5 GHz | | 51.7 | | dB |
| LO INTERFACE | LOP, LOM | | | | |
| Input Frequency Range | BYPASS = 1 | | 0.01 to 26.6 | | GHz |
| | BYPASS = 0, LOMODE = 0 (divide by 2) | | 0.01 to 2.4 | | GHz |
| | BYPASS = 0, LOMODE = 1 (1×) | | 0.01 to 26.6 | | GHz |
| | BYPASS = 0, LOMODE = 2 (2×) | | 2 to 8 | | GHz |
| | BYPASS= 0, LOMODE = 3 (4×) | | 4 to 8 | | GHz |
| Return Loss | Characteristic impedance ($Z_O$) = 100 Ω differential | | >10 | | dB |
| Input Power | | −6 | 0 | +6 | dBm |
| LO to RF Leakage | BYPASS = 1, $f_{LO}$ | | −77.3 | | dBm |
| | BYPASS = 0, LOMODE = 0 (divide by 2), $f_{LO}/2$ | | −83.4 | | dBm |
| | BYPASS = 0, LOMODE = 0 (divide by 2), $f_{LO}$ | | −72.1 | | dBm |
| | BYPASS = 0, LOMODE = 1 (1×), $f_{LO}$ | | −80.4 | | dBm |
| | BYPASS = 0, LOMODE = 2 (2×), $f_{LO}$ | | −86.4 | | dBm |
| | BYPASS = 0, LOMODE = 2 (2×), $2f_{LO}$ | | −81.7 | | dBm |
| | BYPASS = 0, LOMODE = 3 (4×), $f_{LO}$ | | −93.4 | | dBm |
| | BYPASS = 0, LOMODE = 3 (4×), $2f_{LO}$ | | −102 | | dBm |
| | BYPASS = 0, LOMODE = 3 (4×), $4f_{LO}$ | | −92.1 | | dBm |
| LO to IF Leakage | $f_{RF}$ = 50 MHz, differential | | 13.6 | | dBV |
| OFFSET FREQUENCY (OF) INTERFACE | OFP, OFM | | | | |
| Input Frequency Range | | | 0.1 to 400 | | MHz |
| OF Induced Spurious Tone at $f_{IF}$[4] | OFMODE = 2 (divide by 4), $3f_{IF}$ = 1.5 MHz | | −3.2 | | dBc |
| | $5f_{IF}$ = 2.5 MHz | | −6.2 | | dBc |
| | $7f_{IF}$ = 3.5 MHz | | −8.7 | | dBc |
| Input Impedance | Differential | | 10\|\|0.5 | | kΩ\|\|pF |
| Voltage Swing | Differential | 0.125 | 0.5 | 2.0 | V p-p |
| IF OUTPUT INTERFACE | IFFP/IFFM and IFRP/IFRM | | | | |
| Output Frequency Range | | | 0.1 to 100 | | MHz |
| Maximum Peak-to-Peak Voltage | Differential | | 8 | | V p-p |
| Short-Circuit Output Current | Single-ended, sourcing, output voltage = 0 V | 200 | | | mA |
| Output Noise Spectral Density | f = $f_{IF}$ = 500 kHz, FGAIN = RGAIN = 60 (decimal), differential | | 207 | | μV/√Hz |
| VCM INTERFACE | VCM | | | | |
| Input Voltage Range | | 1.0 | | 4.0 | V |
| Output $V_{CM}$ Error | IF output common-mode voltage ($V_{CM}$) | −100 | 0 | +100 | mV |
| Input Impedance | | | 10k \|\| 4p | | Ω \|\| F |
| ENABLE INTERFACE | EN | | | | |
| Logic Low Input Voltage | | | | 0.8 | V |
| Logic High Input Voltage | | 2.0 | | | V |
| Current into Pin | | | | 20 | μA |
| SPI AND SYNC INTERFACE | $\overline{CS}$, SCK, SDIO, SYNC | | | | |
| Logic Low Input Voltage | | | | 0.3 × OVDD | V |
| Logic High Input Voltage | | 0.7 × OVDD | | | V |
| Input Voltage Hysteresis | | | 209 | | mV |

## SPECIFICATIONS

*Table 1. Specifications (Continued)*

| Parameter | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Current into Pin | $\overline{CS}$, SCK, SYNC | | | 20 | µA |
| Logic Low Output Voltage | SDIO, sinking 10 mA | | | 0.3 × OVDD | V |
| Logic High Output Voltage | SDIO, sourcing 10 mA | 0.7 × OVDD | | | V |
| POWER SUPPLY INTERFACES | AVCC, OVCC, OVDD | | | | |
| Supply Voltage (AVCC, OVCC) | | 4.75 | 5.0 | 5.25 | V |
| Supply Current (AVCC + OVCC) | EN = AVCC, Register 0x20 = 0x0B (BYPASS = 0, LOMODE = 3) | 200 | 225 | 250 | mA |
| | EN = AVCC, Register 0x20 = 0x1D (OFMODE = 3) | 110 | 120 | 130 | mA |
| | EN = 0 V (shutdown) | | 32 | 2000 | µA |
| SPI Supply Voltage (OVDD) | | 1.8 | 3.3 | 3.6 | V |
| SPI Supply Current (OVDD) | | 2 | 24 | 500 | µA |

[1] Error correction coefficient ($e_{00}$) obtained from measurements of the ratio of reverse and forward IF output ports for short, open, and load terminations on RFOUT. Printed circuit board (PCB) transmission line is deembedded by splitting the measured transmission matrix of the through line on the PCB in half and incorporating one half into the ideal model of the terminations. See the Calibration and Error Correction section for details.

[2] Voltage gain from RF input to differential IF output, with high-impedance IF load. Although the FGAIN and RGAIN bit fields are seven bits wide, values beyond 0x42 are of limited practical use because amplified noise starts to saturate the IF output drivers.

[3] Second RF tone power = 0 dBm, frequency = $f_{RF}$ + 100 kHz.

[4] Magnitude relative to the desired output at $f_{IF}$ = 500 kHz.

## SERIAL INTERFACE TIMING SPECIFICATIONS

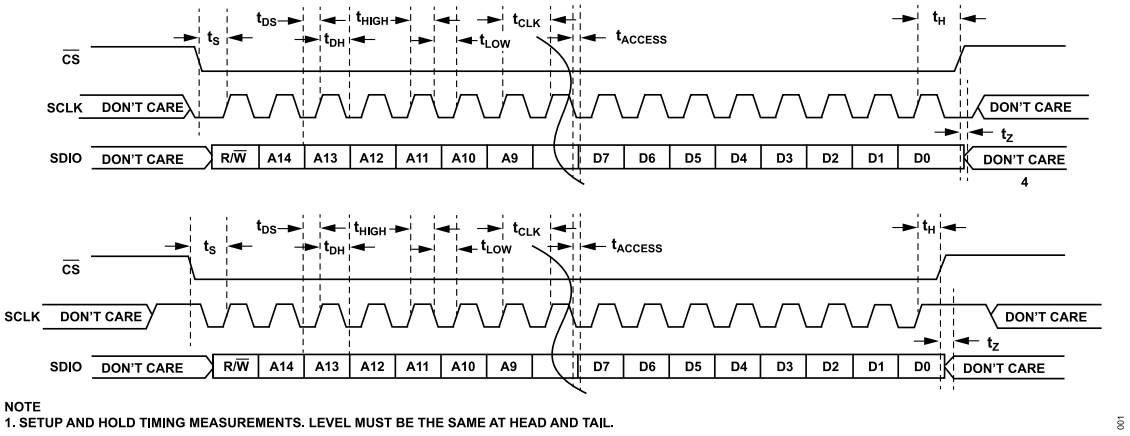



*Figure 2. SPI Timing Diagram*

*Table 2. SPI Timing Specifications*

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_{DS}$ | Setup time between data and rising edge of SCLK | 15 | | | ns |
| $t_{DH}$ | Hold time between data and rising edge of SCLK | 15 | | | ns |
| $t_{CLK}$ | Clock period | 150 | | | ns |
| $t_S$ | Setup time between $\overline{CS}$ and SCLK | 40 | | | ns |
| $t_H$ | Hold time between $\overline{CS}$ and SCLK | 40 | | | ns |
| $t_{HIGH}$ | Minimum period that SCLK must be in a logic high state | 75 | | | ns |
| $t_{LOW}$ | Minimum period that SCLK must be in a logic low state | 75 | | | ns |

## SPECIFICATIONS

*Table 2. SPI Timing Specifications (Continued)*

| Parameter | Description | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $t_Z$ | Maximum time delay between $\overline{CS}$ deactivation and SDIO bus return to high impedance | | | 150 | ns |
| $t_{ACCESS}$ | Maximum time delay between falling edge of SCLK and output data valid for a read operation | | | 30 | ns |

## ABSOLUTE MAXIMUM RATINGS

*Table 3. Absolute Maximum Ratings*

| Parameter | Rating |
|---|---|
| Supply Voltage (AVCC and OVCC) | 5.5 V |
| RFIN, RFOUT Input AC Power | |
| Average[1] | 30 dBm |
| Peak[1] | 35 dBm |
| DC Voltage | |
| OVDD | −0.3 V to +3.8 V |
| SCK, $\overline{CS}$, and SDIO | −0.3 V to OVDD + 0.3 V |
| IFFP, IFFM, IFRP, IFRM[2] | −0.3 V to OVCC + 0.3 V |
| Any Other Pin[3] | −0.3 V to AVCC + 0.3 V |
| DC Current RFIN to or from RFOUT | 100 mA |
| Temperature | |
| Maximum $T_J$ | 150°C |
| $T_A$ Operating Range | −40°C to +105°C |
| Storage Range | −65°C to +150°C |

1 Not production tested. Guaranteed by design and correlation to production tested parameters. Peak power duty cycle is 10% maximum.

2 The voltage on these pins must not exceed 5.5 V, OVCC + 0.3 V, or be less than –0.3 V.

3 The voltage on these pins must not exceed 5.5 V, AVCC + 0.3 V, or be less than –0.3 V.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

## THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

*Table 4. Thermal Resistance*

| Package Type[1] | $\theta_{JA}$[2] | $\theta_{JB}$[3] | $\theta_{JCT}$[4] | $\theta_{JCB}$[5] | $\Psi_{JT}$[6] | $\Psi_{JB}$[7] | Unit |
|---|---|---|---|---|---|---|---|
| CC-26-2 | 39.32 | 13.10 | 30.09 | 7.63 | 1.30 | 12.95 | °C/W |

1 Test Condition 1: thermal impedance simulated values are based upon use of 2S2P JEDEC PCB. See the Ordering Guide.

2 $\theta_{JA}$ is the junction to ambient (or die to ambient) thermal resistance measured in a one cubic foot sealed enclosure.

3 $\theta_{JB}$ is the junction-to-board thermal resistance.

4 $\theta_{JCT}$ is the junction-to-case top (or die to package) thermal resistance.

5 $\theta_{JCB}$ is the junction-to-case bottom thermal resistance.

6 $\Psi_{JT}$ refers to the junction to top thermal characterization number.

7 $\Psi_{JB}$ refers to the junction to board thermal characterization number.

## ELECTROSTATIC DISCHARGE (ESD) RATING

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

### ESD Ratings for ADL5961

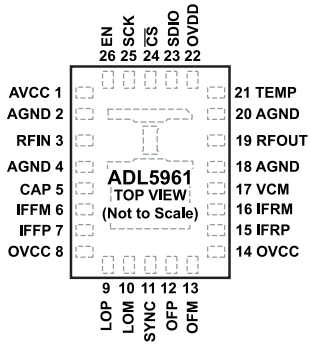
*Table 5. ADL5961, 26-Lead LGA*

| ESD Model | Withstand Threshold (V) | Class |
|---|---|---|
| HBM | 2000 | 2 |
| FICDM | 500 | 1B |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device**. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS




NOTES
1. EXPOSED PAD. THE EXPOSED PAD (EPAD) ON THE UNDERSIDE OF THE DEVICE IS ALSO INTERNALLY CONNECTED TO GROUND AND REQUIRES GOOD THERMAL AND ELECTRICAL CONNECTION TO THE GROUND OF THE PCB. CONNECT ALL GROUND PINS TO A LOW IMPEDANCE GROUND PLANE TOGETHER WITH THE EPAD. 002

*Figure 3. Pin Configuration*

*Table 6. Pin Function Descriptions*

| Pin No. | Mnemonic | Description |
|---|---|---|
| 1 | AVCC | Analog Positive Power Supply Pin. Bypass by placing 1 nF and 4.7 µF capacitors as closely as possible to the AVCC pin. On power-up, apply the AVCC voltage before the OVDD voltage. On power-down, remove the OVDD voltage before the AVCC voltage. |
| 2, 4, 18, 20 | AGND | Analog Ground Pins. All ground pins are internally connected. Use Pin 2 and Pin 4 as the RF return ground for the RFIN transmission line (Pin 3). Use Pin 18 and Pin 20 as the RF return ground for the RFOUT transmission line (Pin 19). |
| 3, 19 | RFIN, RFOUT | RF Input and Output of the Primary Transmission Line. RFIN and RFOUT have a 50 Ω load characteristic impedance. DC-blocking capacitors are required to source and load. When using open and short terminations, do not exceed the maximum power dissipation ratings. |
| 5 | CAP | Bypass Capacitor. A 100 nF capacitor is recommended for 100 kHz operation. |
| 6, 7, 15, 16 | IFFM, IFFP, IFRP, IFRM | Differential IF Outputs. Pin 6 and Pin 7 are coupled to the forward power transfer (from RFIN to RFOUT). Pin 15 and Pin 16 are coupled to the reverse power transfer (from RFOUT to RFIN). |
| 8, 14 | OVCC | IF Amplifier Positive Power Supply Pin. Bypass OVCC with a 1 nF and a 4.7 µF capacitor on each pin before connecting to AVCC. Place the capacitors as closely as possible to OVCC. On power-up, apply the OVCC voltage before the OVDD voltage. On power-down, remove the OVDD voltage before the OVCC voltage. |
| 9, 10 | LOP, LOM | Downconversion Mixer LO Inputs. LOP and LOM are internally terminated with a 100 Ω differential. A differential or single-ended signal source can drive the LOP and LOM pins. Register 0x20 configures the LO interface. DC-blocking capacitors are recommended for the LO interface. |
| 11 | SYNC | Synchronization Input. This complementary metal-oxide semiconductor (CMOS) input pin stops the dividers in the LO and IF input interfaces when driven high and initiates synchronization when driven back low. If left floating, an internal 415 kΩ pull-down resistor disables the SYNC function. |
| 12, 13 | OFP, OFM | IF Offset Reference Frequency Inputs. The OFP and OFM pins set the center frequency at the IF outputs when the OFMODE bits (Bits[3:2]) in Register 0x20 equal 0x0, 0x1, or 0x2. Setting the OFMODE bits to 0x3 disables this input. |
| 17 | VCM | IF Output Common-Mode Voltage Control. The VCM pin sets the output common-mode voltage at IFFM, IFFP, IFRP, and IFRM. Floats to OVCC/2 if left open. |
| 21 | TEMP | Temperature Sensing Diode. The TEMP pin connects to the anode of an on-chip junction diode. TEMP can be used to measure the die temperature by measuring the voltage at this pin, while forcing a known current into the pin. |
| 22 | OVDD | SPI Positive Power Supply Pin. Connect the OVDD pin to the power supply of the SPI controller to avoid the need of voltage level translators in the SPI bus connections. On power-up, apply the AVCC and OVCC voltages before the OVDD voltage. On power-down, remove the OVDD voltage before the AVCC and OVCC voltages. |
| 23 | SDIO | SPI Data Input and Output. If the SDIO pin is floating, an internal 415 kΩ pull-down resistor pulls SDIO to logic low. |
| 24 | $\overline{CS}$ | SPI Chip Select (Active Low). If the $\overline{CS}$ pin is floating, an internal 415 kΩ pull-up resistor ties the pin to OVDD. |
| 25 | SCK | SPI Clock Input. If SCK is left floating, an internal 415 kΩ pull-down resistor pulls SCK to logic low. |
| 26 | EN | Chip Enable. A logic high at the EN pin enables the chip. A logic low at the EN pin shuts down the ADL5961. If EN is left floating, an internal 415 kΩ pull-down resistor disables the ADL5961. |
| | EPAD | Exposed Pad. The exposed pad (EPAD) on the underside of the device is also internally connected to ground and requires good thermal and electrical connection to the ground of the PCB. Connect all ground pins to a low impedance ground plane together with the EPAD. |

## TYPICAL PERFORMANCE CHARACTERISTICS

AVCC = OVCC = 5.0 V, EN = OVDD = 3.3 V, VCM = 2.5 V, $T_A$ = 25°C, 50 Ω source and load impedance, continuous wave input at RFIN, $Z_O$ = 50 Ω, $P_{RF}$ = 0 dBm, LO drive single-ended, $P_{LO}$ = 0 dBm, $f_{RF}$ = 1 GHz, and $f_{LO}$ = $f_{RF}$ + 500 kHz, unless otherwise noted. BYPASS = 1, FGAIN = RGAIN = 24, CIF1 = CIF2 = 15. Test circuit shown in Figure 72. A 0.1 µF capacitor was used at RFOUT for all the directivity and voltage conversion gain measurements.

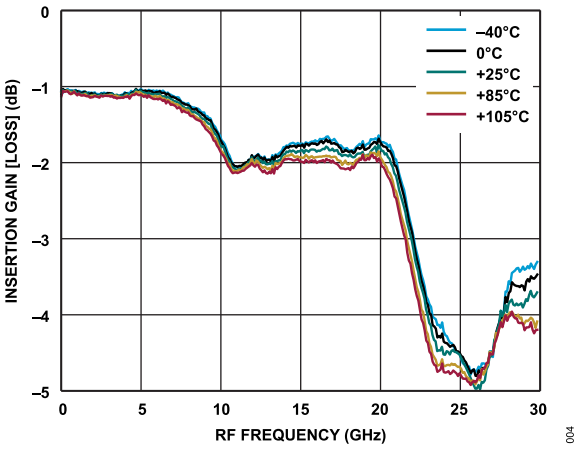



*Figure 4. RFIN to RFOUT Insertion Gain (Loss) vs. RF Frequency at Various Temperatures*

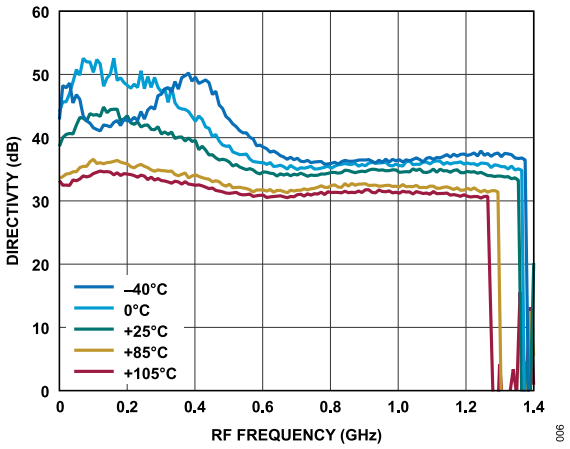



*Figure 6. Directivity vs. RF Frequency at Various Temperatures, LOMODE = 0, OFMODE = 3*

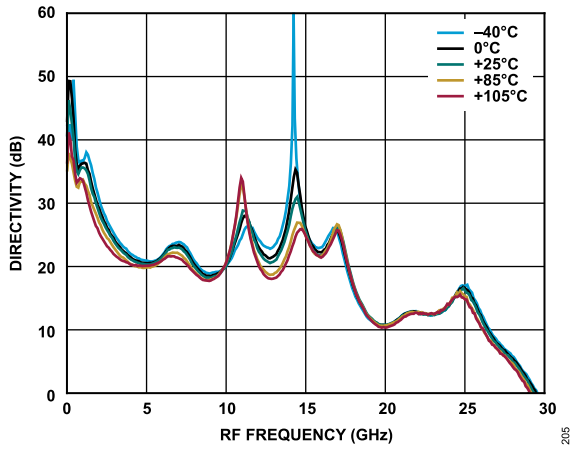



*Figure 5. Directivity vs. RF Frequency at Various Temperatures, BYPASS = 1*

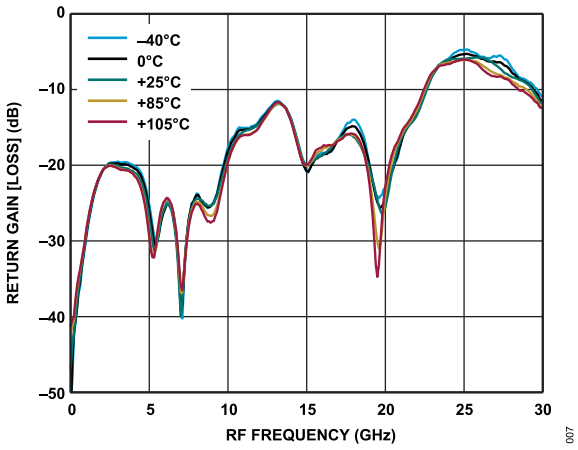



*Figure 7. RFIN and RFOUT Return Gain (Loss) vs. RF Frequency at Various Temperatures*

## TYPICAL PERFORMANCE CHARACTERISTICS

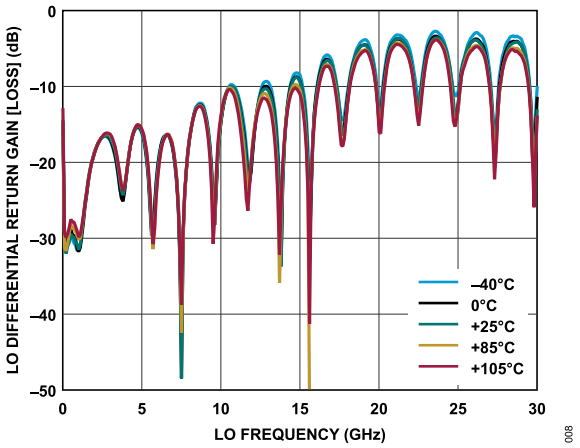



Figure 8. LO Differential Return Gain (Loss) vs. LO Frequency at Various Temperatures, $Z_O$ = 100 Ω

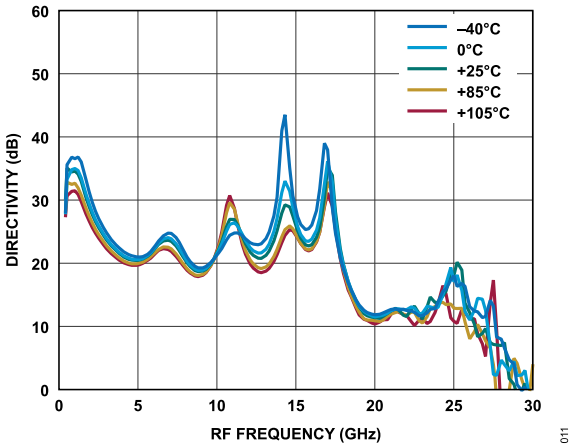



Figure 11. Directivity vs. RF Frequency at Various Temperatures, LOMODE = 1, OFMODE = 3

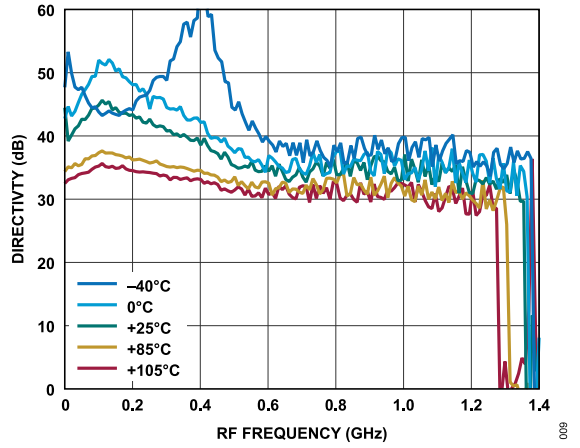



Figure 9. Directivity vs. RF Frequency at Various Temperatures LOMODE = 0, OFMODE = 2

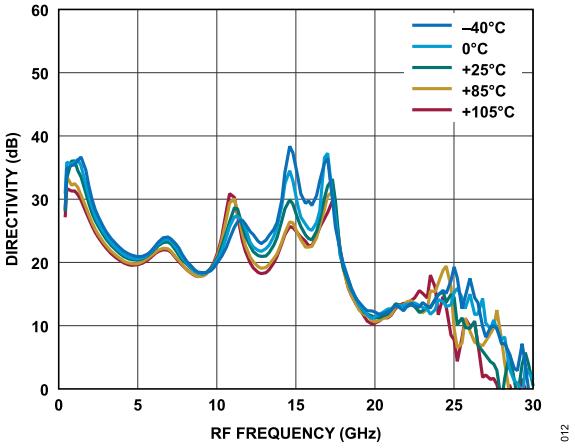



Figure 12. Directivity vs. RF Frequency at Various Temperatures, LOMODE = 2, OFMODE = 3

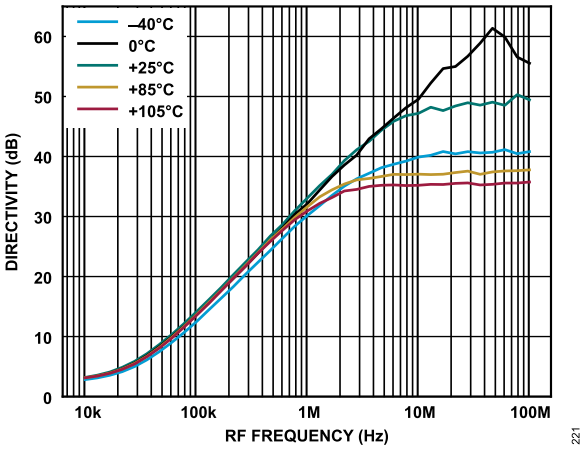



Figure 10. Directivity vs. RF Frequency at Various Temperatures, LOMODE = 0, OFMODE = 3

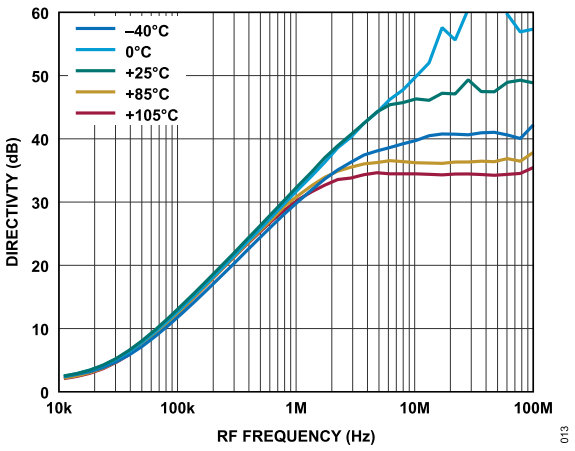



Figure 13. Directivity vs. Low RF Frequencies at Various Temperatures, LOMODE = 0, OFMODE = 2

## TYPICAL PERFORMANCE CHARACTERISTICS

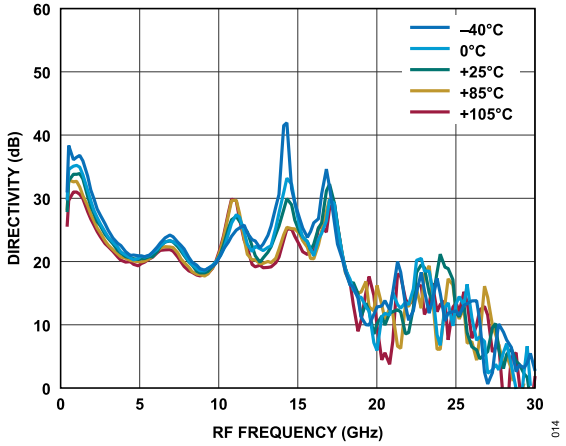



*Figure 14. Directivity vs. RF Frequency at Various Temepertures, LOMODE = 1, OFMODE = 2*

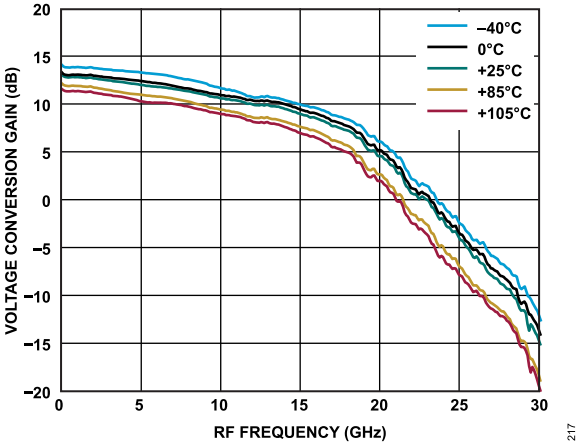



*Figure 17. Voltage Conversion Gain vs. RF Frequency at Various Temperatures*

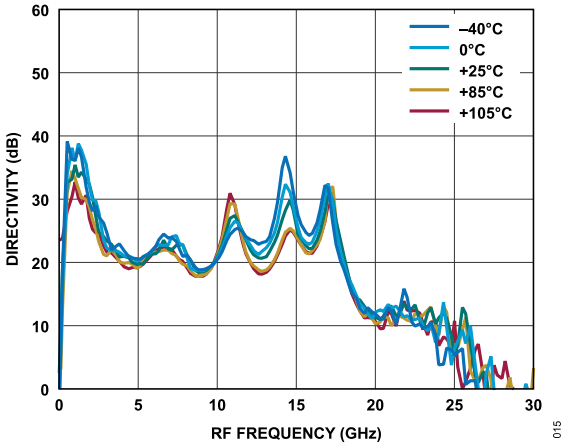



*Figure 15. Directivity vs. RF Frequency at Various Temperatures, LOMODE = 2, OFMODE = 2*

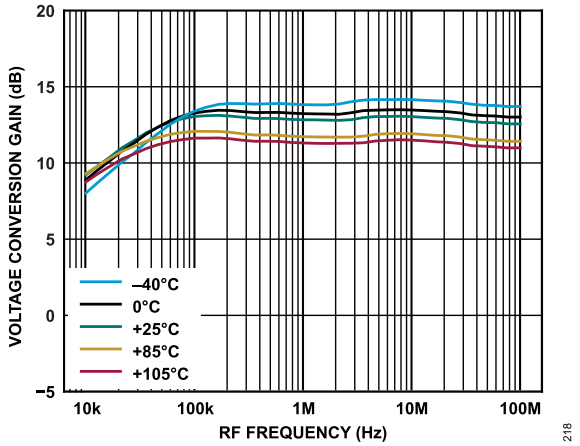



*Figure 18. Voltage Conversion Gain vs. RF Frequency at Various Temperatures, LOMODE = 0, OFMODE = 3*

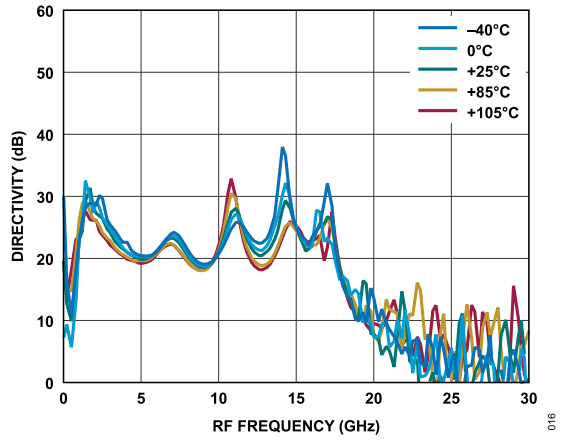



*Figure 16. Directivity vs. RF Frequency at Various Temperatures, LOMODE = 3, OFMODE = 3*

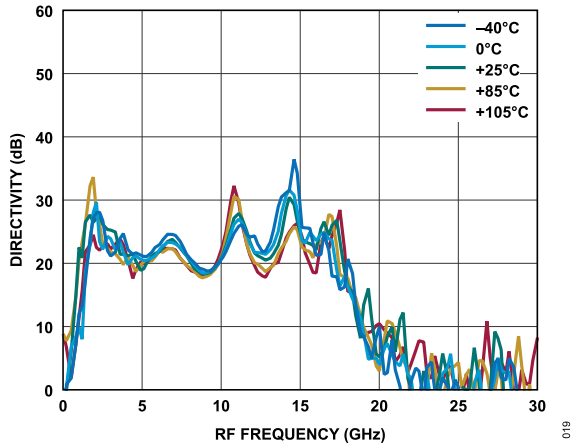



*Figure 19. Directivity vs. RF Frequency at Various Temperatures, LOMODE = 3, OFMODE = 2*

## TYPICAL PERFORMANCE CHARACTERISTICS

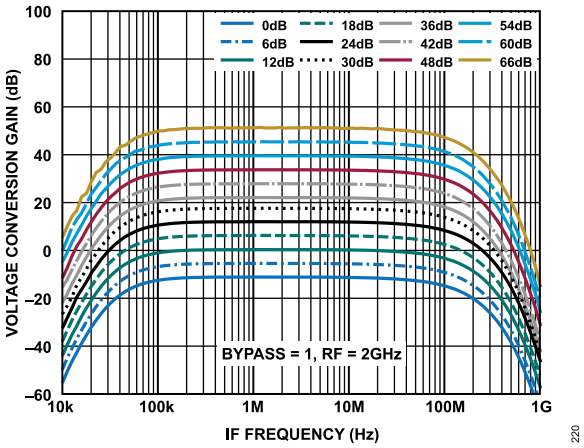



*Figure 20. Voltage Conversion Gain vs. IF Frequency for Various Gain Settings (FGAIN and RGAIN)*

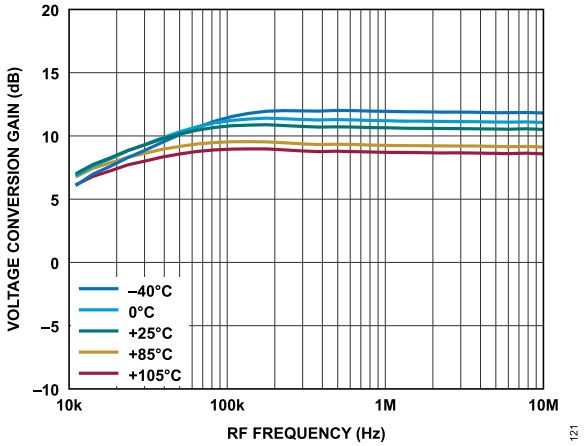



*Figure 21. Voltage Conversion Gain vs. RF Frequency at Various Temperatures, LOMODE = 0, OFMODE = 2*

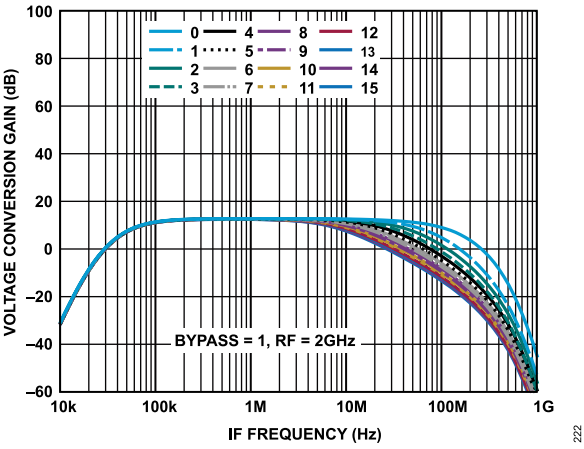



*Figure 22. Voltage Conversion Gain vs. IF Frequency and CIF1 Setting, CIF2 = 0, BYPASS = 1, RF = 2 GHz*

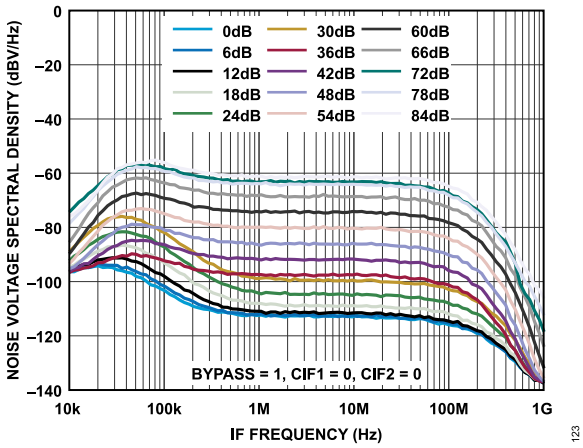



*Figure 23. Differential IF Output, Noise Voltage Spectral Density vs. IF Frequency for Various Gain Settings (FGAIN and RGAIN), BYPASS = 1, CIF1 = CIF2 = 0*

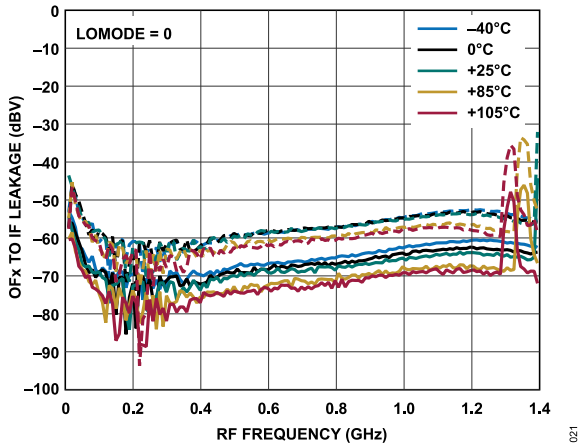



*Figure 24. OFx to IF Leakage vs. RF Frequency for Various Temperatures, LOMODE = 0, OFMODE = 2, Solid Lines: Forward Channel, and Dashed Lines: Reverse Channel*

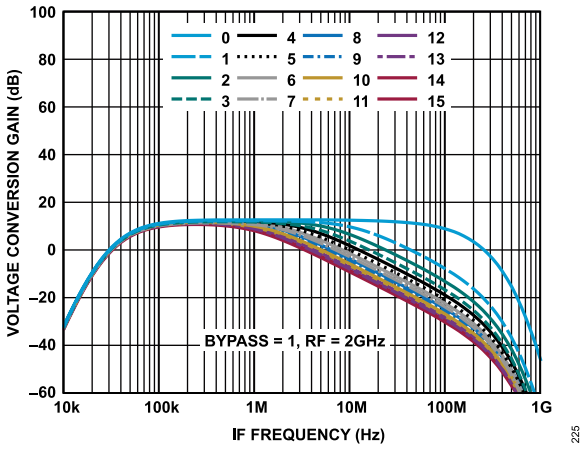



*Figure 25. Voltage Conversion Gain vs. IF Frequency for Various CIF2 Settings, CIF1 = 0 , BYPASS = 1, RF = 2 GHz*

## TYPICAL PERFORMANCE CHARACTERISTICS

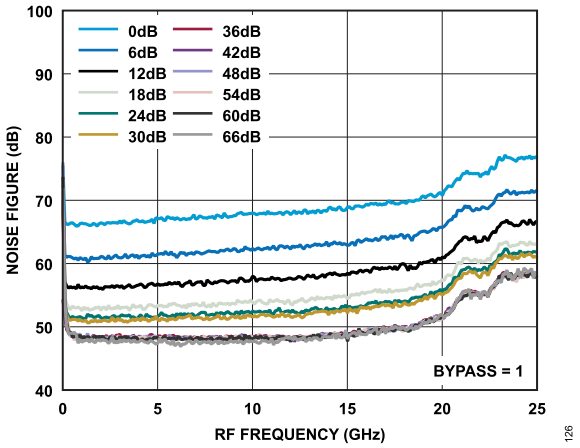



*Figure 26. Noise Figure vs. RF Frequency for Various IF Gain Settings, BYPASS = 1*

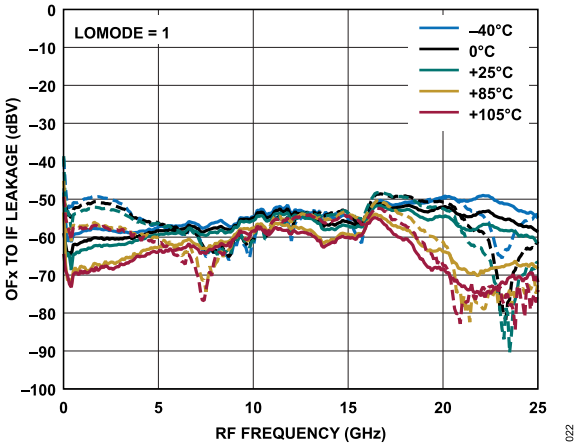



*Figure 27. OFx to IF Leakage vs. RF Frequency for Various Temperatures, LOMODE = 1, OFMODE = 2, Solid Lines: Forward Channel, and Dashed Lines: Reverse Channel*

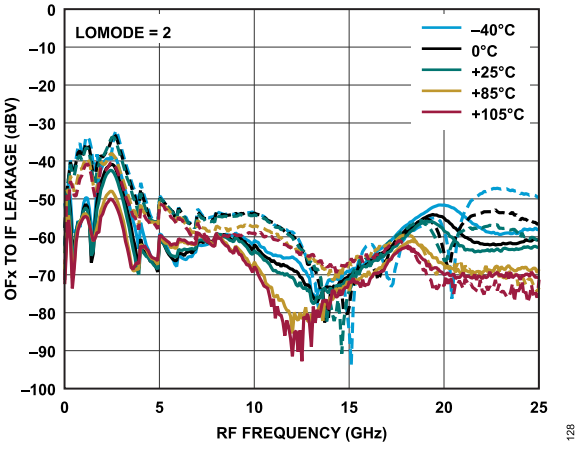



*Figure 28. OFx to IF Leakage vs. RF Frequency for Various Temperatures, LOMODE = 2, OFMODE = 2, Solid Lines: Forward Channel, and Dashed Lines: Reverse Channel*

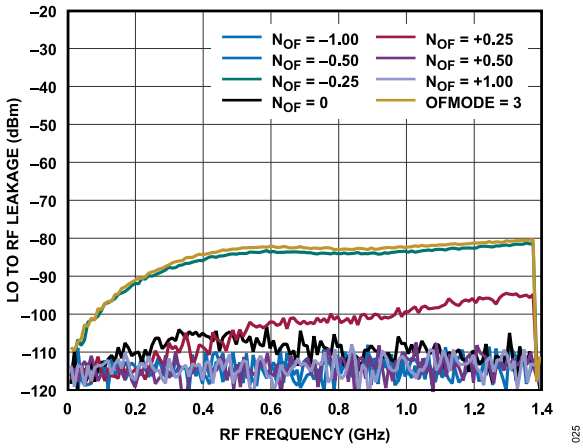



*Figure 29. LO to RF Leakage vs. RF Frequency for LOMODE = 0, Measurement Frequency = $f_{RF}$ + $N_{OF}$ × $f_{OF}$ for OFMODE = 2 and $f_{RF}$ + $f_{IF}$ for OFMODE = 3*

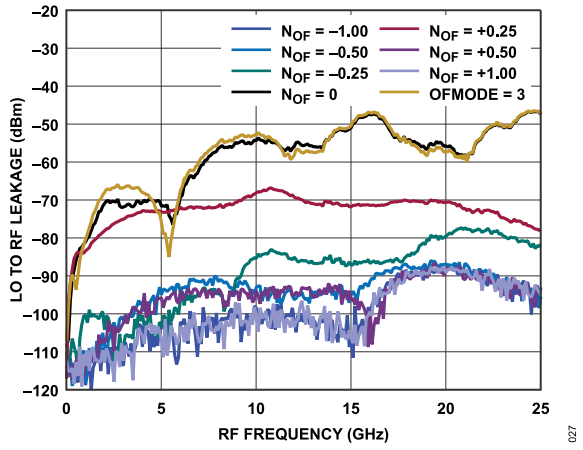



*Figure 30. LO to RF Leakage vs. RF Frequency for LOMODE = 1, Measurement Frequency = $f_{RF}$ + $N_{OF}$ × $f_{OF}$ for OFMODE = 2 and $f_{RF}$ + $f_{IF}$ for OFMODE = 3*

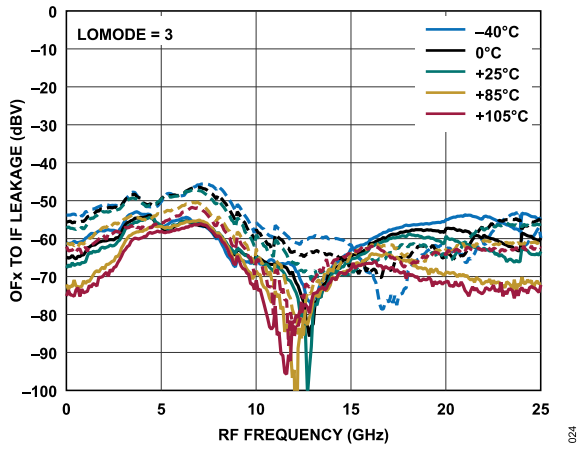



*Figure 31. OFx to IF Leakage vs. RF Frequency at Various Temperatures, LOMODE = 3, OFMODE = 2, Solid Lines: Forward Channel, Dashed Lines: Reverse Channel*

## TYPICAL PERFORMANCE CHARACTERISTICS

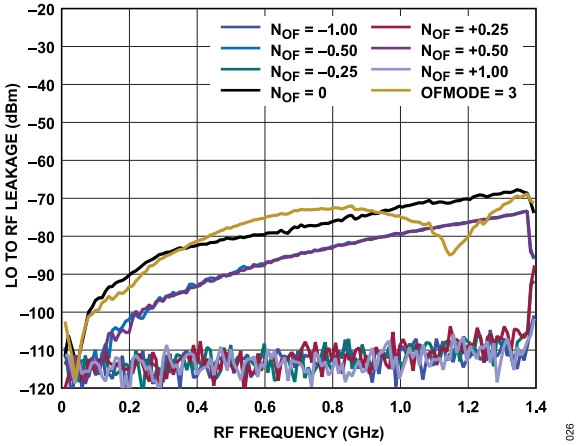



*Figure 32. LO to RF Leakage vs. RF Frequency for LOMODE = 0, Measurement Frequency = 2× $f_{RF}$ + $N_{OF}$ × $f_{OF}$ for OFMODE = 2, and 2× $f_{RF}$ + $f_{IF}$ for OFMODE = 3*

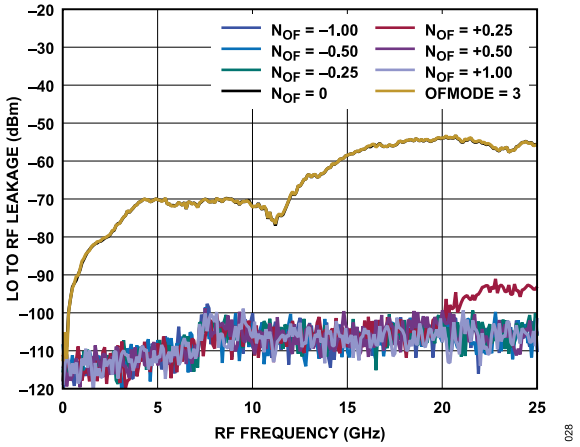



*Figure 33. LO to RF Leakage vs. RF Frequency for LOMODE = 2, Measurement Frequency = $f_{RF}$/2 + $N_{OF}$ × $f_{OF}$ for OFMODE = 2, and $f_{RF}$/2 + $f_{IF}$ for OFMODE = 3*

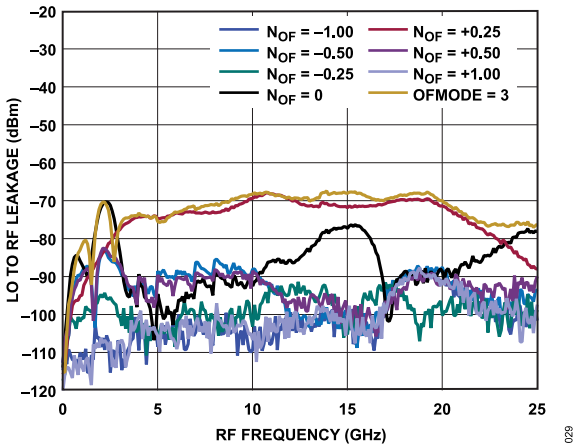



*Figure 34. LO to RF Leakage vs. RF Frequency for LOMODE = 2, Measurement Frequency = $f_{RF}$ + $N_{OF}$ × $f_{OF}$ for OFMODE = 2, and $f_{RF}$ + $f_{IF}$ for OFMODE = 3*

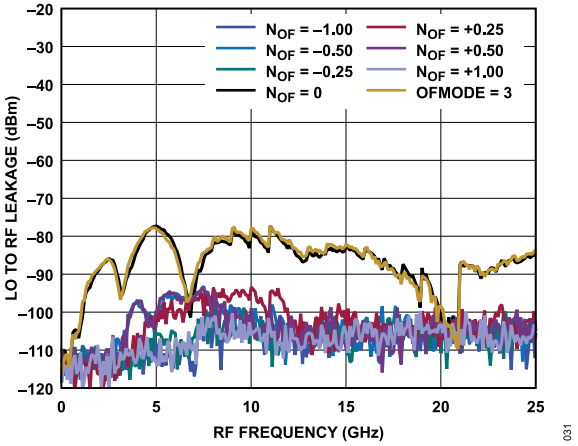



*Figure 35. LO to RF Leakage for RF Frequency for LOMODE = 3, Measurement Frequency = $f_{RF}$/2 + $N_{OF}$ × $f_{OF}$ for OFMODE = 2, and $f_{RF}$/2 + $f_{IF}$ for OFMODE = 3*

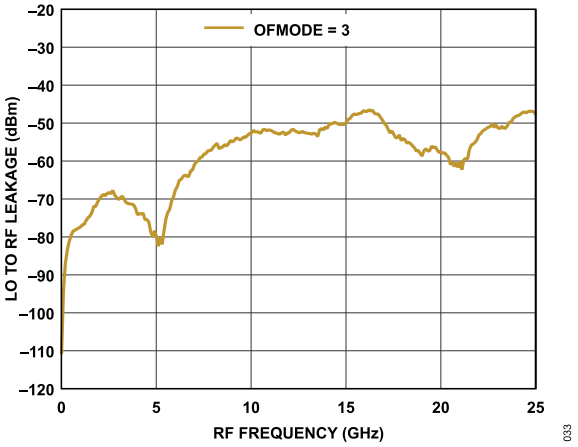



*Figure 36. LO to RF Leakage vs. RF Frequency for BYPASS = 1, Measurement Frequency = $f_{RF}$ + $f_{IF}$*

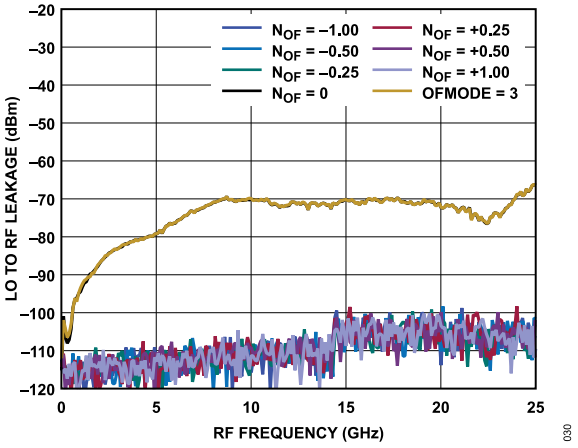



*Figure 37. LO to RF Leakage vs. RF Frequency for LOMODE = 3, Measurement Frequency = $f_{RF}$/4 + $N_{OF}$ × $f_{OF}$ for OFMODE = 2 and $f_{RF}$/4 + $f_{IF}$ for OFMODE = 3*

## TYPICAL PERFORMANCE CHARACTERISTICS

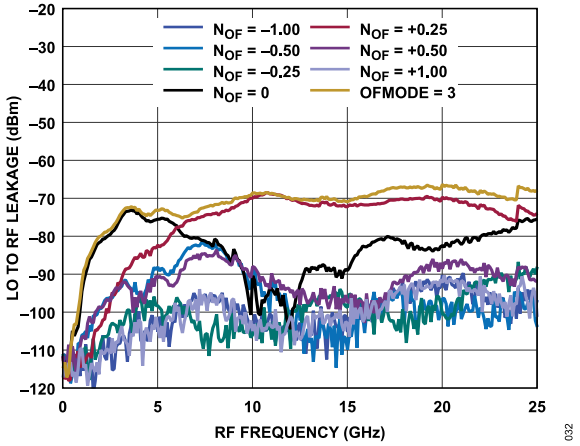



*Figure 38. LO to RF Leakage vs. RF Frequency for LOMODE = 3, Measurement Frequency = $f_{RF} + N_{OF} \times f_{OF}$ for OFMODE = 2, and $f_{RF} + f_{IF}$ for OFMODE = 3*

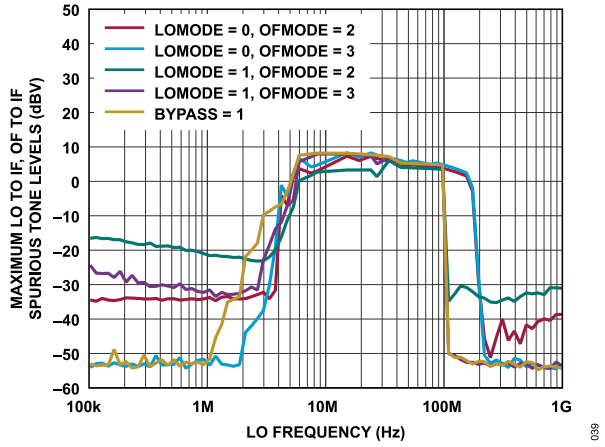



*Figure 39. Maximum LO to IF, OF to IF Spurious Tone Levels vs. LO Frequency, CIF1 = CIF2 = 0*

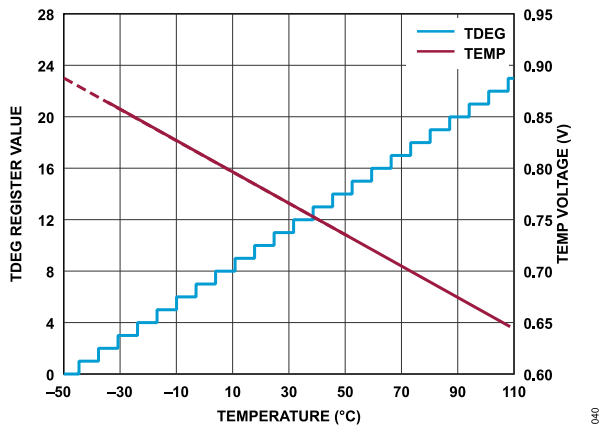



*Figure 40. TDEG Register Value and TEMP Voltage vs. Temperature (TEMP Current, $I_{TEMP}$ = 42 µA)*

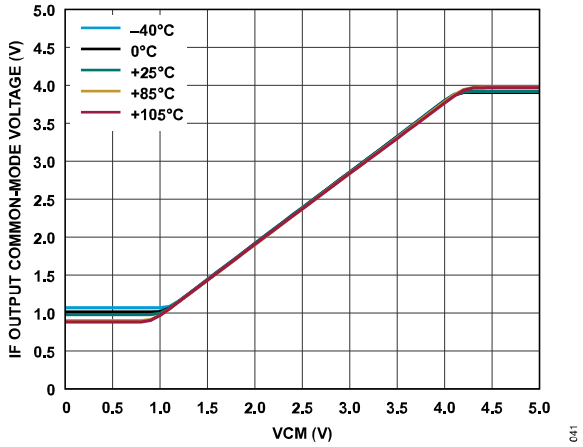



*Figure 41. IF Output Common-Mode Voltage vs. VCM at Various Temperatures*

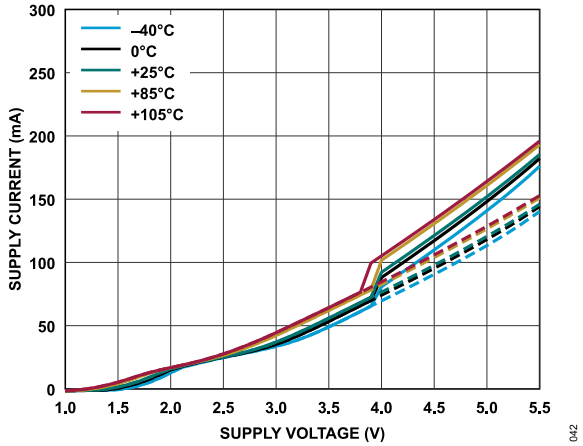



*Figure 42. Supply Current vs. Supply Voltage at Various Temperatures, LOMODE = 0, Solid Lines: OFMODE = 2, and Dashed Lines: OFMODE = 3*

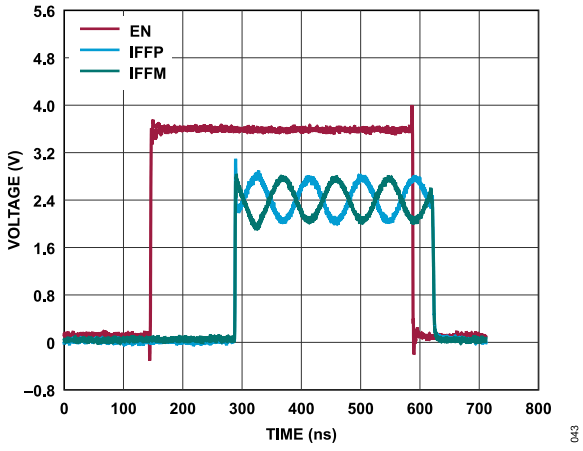



*Figure 43. Turn-On and Turn Off Time with Continuous Wave, RF = 1 GHz, 10 dBm, IF = 10 MHz, 50 Ω Load at IFFP and IFFM*

## TYPICAL PERFORMANCE CHARACTERISTICS

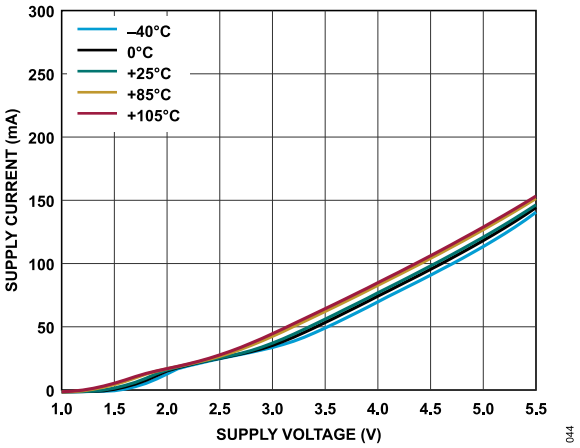



*Figure 44. Supply Current vs. Supply Voltage at Various Temperatures, BYPASS = 1*

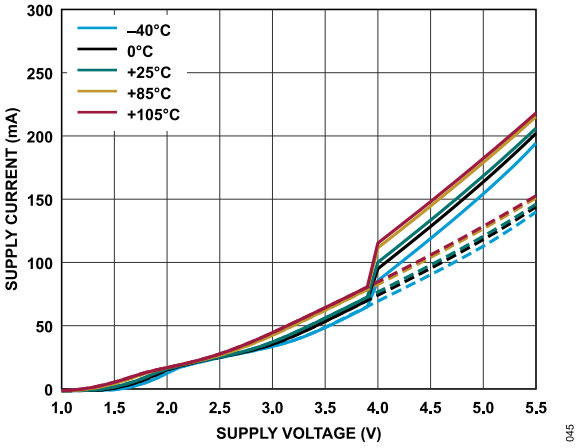



*Figure 45. Supply Current vs. Supply Voltage at Various Temperatures, LOMODE = 1, Solid Lines: OFMODE = 2, and Dashed Lines: OFMODE = 3*

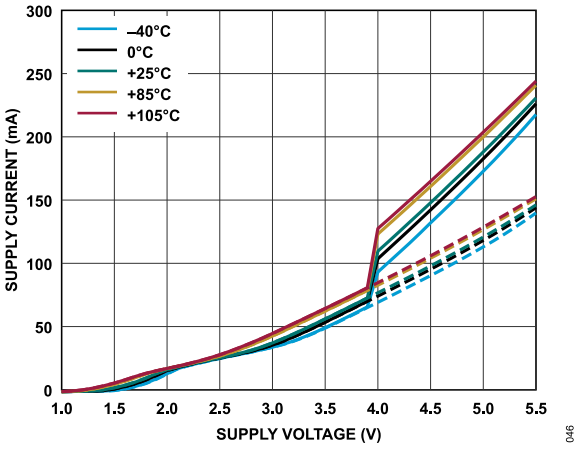



*Figure 46. Supply Current vs. Supply Voltage at Various Temperatures, LOMODE = 2, Solid Lines: OFMODE = 2, and Dashed Lines: OFMODE = 3*

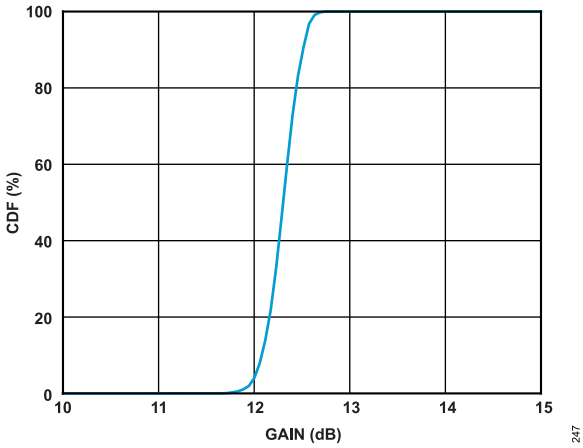



*Figure 47. Conversion Gain Distribution, RF = 100 MHz, FGAIN = 24, Sample Size 3500 Devices (Cumulative Distribution Function (CDF))*

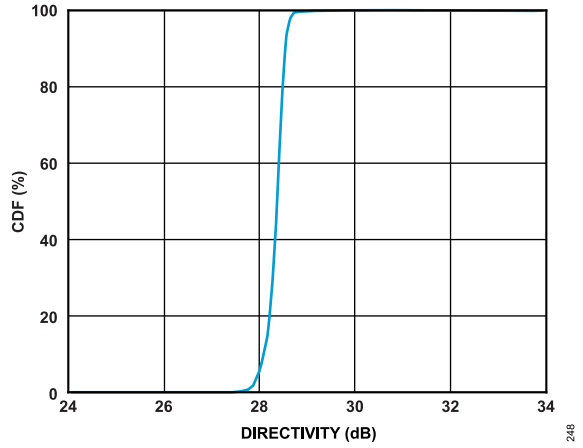



*Figure 48. Directivity Distribution, RF = 100 MHz, Sample Size 100 Devices*

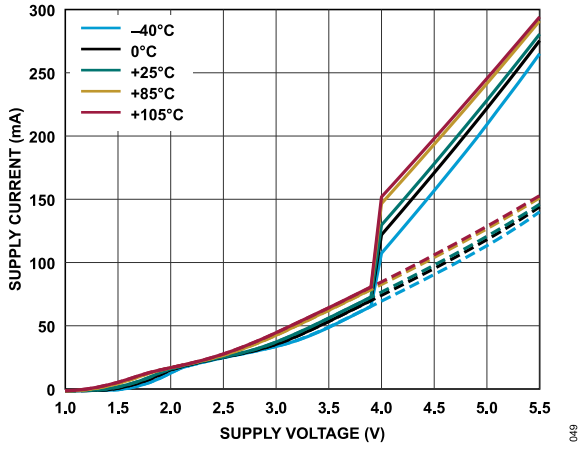



*Figure 49. Supply Current vs. Supply Voltage at Various Temperatures, LOMODE = 3, Solid Lines: OFMODE = 2, and Dashed Lines: OFMODE = 3*

## TYPICAL PERFORMANCE CHARACTERISTICS

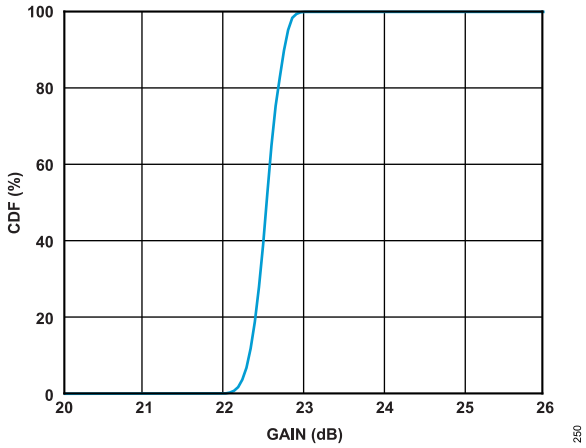



*Figure 50. Conversion Gain Distribution, RF = 100 MHz, FGAIN = 36, Sample Size 3500 Devices*

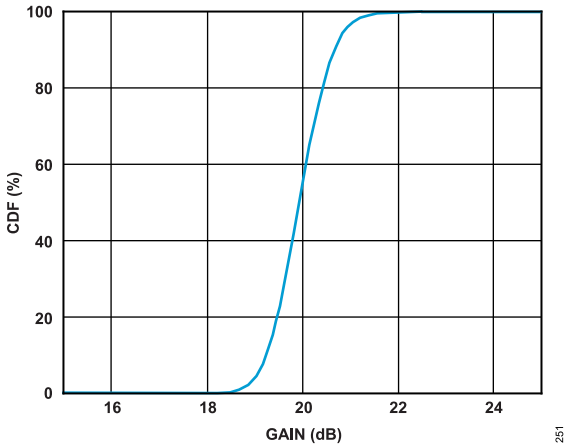



*Figure 51. Directivity Distribution, RF = 10 GHz, Sample Size 100 Devices*

## THEORY OF OPERATION

The ADL5961 is designed to enable broadband multiport network analyzer solutions in a small footprint.

The ADL5961 is built around an integrated broadband bidirectional resistive bridge and coupled to broadband, dual downconversion mixers. The differential IF outputs of the mixers are passed through low-pass filters (LPFs) with SPI-programmable bandwidth and IF amplifiers with individually SPI-programmable gain.

The LO interface to the mixers supports multiple SPI-programmable configurations and is designed to simplify the frequency plan in a VNA application. The LO interface contains frequency multipliers and dividers that enable a wider frequency range of operation than supported by the LO signal source itself. A second input to the LO interface, the offset interface formed by the OFP and OFM pins, enables a zero-offset operating mode with a simplified frequency plan. In this mode, only a single swept high-frequency signal source is needed, driving both the RF and LO interfaces of the ADL5961. The signal supplied to the OF interface controls the frequency of the IF output signal because it mixes with the LO signal supplied to the LOP and LOM interface before driving the downconversion mixers.

Multiple ADL5961 devices can be phase synchronized and operated simultaneously, which enables the construction of small footprint, multiport network analyzers using one ADL5961 device per network analyzer port.

### BASIC ONE-PORT VNA

A one-port VNA, or reflectometer, can be used to measure the magnitude and phase of the reflection coefficient of an unknown load vs. frequency.

Figure 52 shows the basic configuration of a one-port VNA based on the ADL5961. The RFIN interface of the ADL5961 connects to the RF signal source (typically continuous wave), while the RFOUT interface connects to the unknown load, the device under test (DUT). Because the ADL5961 is completely symmetric, the RF source can also be connected to RFOUT and the load to RFIN. The RF source injects an incident RF signal into the directional bridge of the ADL5961, traveling from the source to the load. At the load, part of this incident power wave is reflected and travels back to the source, while the other part is absorbed by the load. The reflection coefficient to be measured (both magnitude and phase) equals the ratio of the reflected power to the incident power at the load. For proper operation of the bidirectional bridge, it is important that the RF signal source has a 50 Ω characteristic impedance. The LO interface can either be driven by a 50 Ω single-ended source or a 100 Ω differential source.

The directional bridge on the ADL5961 supplies a fraction of the incident signal to the input of the forward IF channel, and, likewise, a fraction of the reflected signal to the input of the reverse IF channel. Both these IF signals are downconverted, filtered, amplified, and made available at the differential IF channel output interfaces, IFFx (with the IFFP and IFFM terminals) and IFRx (with the IFRP and IFRM terminals), respectively.

After analog-to-digital conversion, the IF output signals representing the incident and reflected waves are digitally quadrature (complex) downconverted, filtered, and decimated. Their ratio (reflected and forward) is then calculated to obtain the (complex) reflection coefficient.

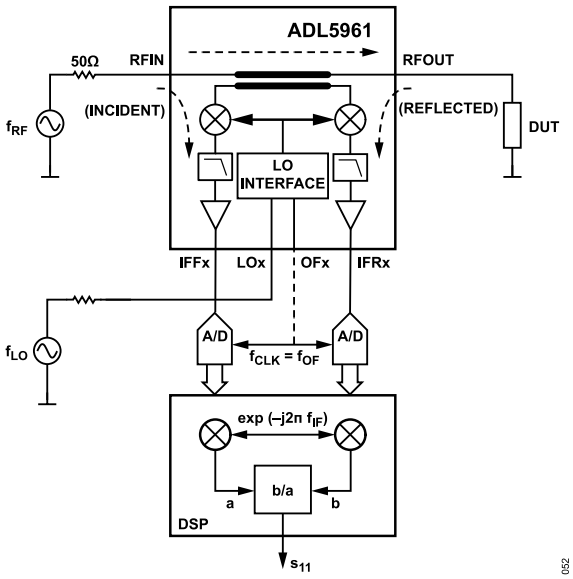



*Figure 52. ADL5961 Used as One-Port VNA (Reflectometer)*

### FREQUENCY PLANNING—LO CONFIGURATIONS

The LO interface of the ADL5961 supports several different configurations, some of which significantly simplify the VNA configuration in exchange for slightly degraded accuracy.

The bypass mode, selected by setting Bit 4 in Register 0x20, is the most basic and highest performance mode of operation of the ADL5961. In this mode, the LO signal supplied to the LO interface (that is, the LOP and LOM pins) directly drives the downconversion mixers, bypassing the frequency multipliers, dividers, and offset mixer. To maintain a fixed IF output frequency, the LO signal must maintain a fixed frequency offset relative to the RF signal across the entire frequency sweep.

$$f_{LO} = f_{RF} \pm f_{IF} \quad (1)$$

The plus sign corresponds to high-side injection, and the minus sign corresponds to low-side injection. High-side injection often results in slightly improved dynamic range because more of the mixing products calculate out at higher frequencies than the desired IF signal and can be suppressed by low-pass filtering. The ADL5961 supports IF frequencies up to 100 MHz. For high dynamic range, analog-to-digital conversion, an IF frequency of a few MHz is often preferable; however, an IF of 2 MHz to 3 MHz creates challenges for the signal sources, requiring an accurate, small

## THEORY OF OPERATION

frequency offset of a few MHz between RF and LO up to 26.5 GHz signal frequencies.

The frequency divider and frequency multipliers integrated into the LO interface of the ADL5961 enable measurement sweeps beyond the frequency range supported by the LO source itself, typically a frequency synthesizer. When Bit 4 in Register 0x20 is cleared (disabling bypass mode), the LOMODE bits (Register 0x20, Bits[1:0]) can be used to program the LO multiplication factor, $M_{LO}$ as shown in the following equation:

$$M_{LO} = 2^{\text{LOMODE} - 1} \quad (2)$$

That is, divide by 2, or multiply by 1, 2, or 4. To ensure that the desired output signal downconverts at the desired IF output frequency, $f_{IF}$, the frequency supplied to the LO interface must meet the following condition:

$$f_{LO} = (f_{RF} \pm f_{IF})/M_{LO} \quad (3)$$

Note, as previously detailed in Table 1, that the divide-by-2 mode can only be used for LO input frequencies up to 2.4 GHz, whereas the doubler and quadrupler modes only operate from 2 GHz to 8 GHz and from 4 GHz to 8 GHz, respectively. The LO interface also contains high-frequency filters that suppress the harmonics and subharmonics in the multiplier outputs. The center frequency of these filters can be programmed through Register 0x21 and Register 0x22.

### OFFSET FREQUENCY INTERFACE

Further simplification of the VNA configuration can be achieved by employing the differential offset frequency interface. In this configuration, a single swept source can be used to drive the RF and LO interfaces at the same frequency (zero frequency offset), while the IF output frequency is set by the signal applied to the offset frequency interface. To enable the offset mixer, clear Bit 4 in Register 0x20 and program the OFMODE bits in Bits[3:2] in Register 0x20. The offset frequency input interface, when enabled, contains a programmable divider with ratios of 1, 2, or 4. The multiplication factor, $M_{OF}$, is as shown in Table 7.

*Table 7. Offset Input Configuration*

| Register 0x20, Bits[3:2], OFMODE | Divide by | $M_{OF}$ |
|---|---|---|
| 00 | 1 | 1 |
| 01 | 2 | 0.5 |
| 10 (Default) | 4 | 0.25 |
| 11 | Dividers off | Not applicable |

The IF output signal frequency, including the offset mixer, is represented as follows:

$$f_{IF} = f_{RF} - M_{LO} \times f_{LO} + M_{OF} \times f_{OF} \quad (4)$$

For a true zero-offset sweep, the LO frequency, therefore, must satisfy the following:

$$f_{LO} = f_{RF}/M_{LO} \quad (5)$$

such that the first two terms of Equation 4 cancel out, and the IF output frequency equals the following:

$$f_{IF} = M_{OF} \times f_{OF} \quad (6)$$

The $M_{OF}$ = 1/4 (OFMODE = 2) setting is particularly useful and is the recommended OFMODE setting. When the offset frequency interface is driven by the ADC sample clock frequency, $f_S$, it centers precisely the IF output signal in the first Nyquist zone of the ADC, with 4× domain sample points per completed cycle of the IF waveform. In this mode, the discrete time nature of the IF waveform becomes evident due to the divide by 4 digital dividing of the offset input.

### IF SIGNAL PATH

The IF output signal of the mixers is passed through LPFs to remove unwanted mixing products and noise. The bandwidth of these filters is SPI-programmable through Register 0x25. The same bandwidth setting is applied to both ADL5961 IF channels.

The IF amplifiers that follow the LPFs have individually SPI-programmable gain, adjustable in 6 dB steps. This programmable gain enables optimal interfacing of both channels to the ADC input dynamic range.

The IF output interfaces of the ADL5961 are suited to drive a wide range of ADCs directly. To avoid aliasing of broadband noise, it is recommended to insert a simple antialiasing filter as shown in Figure 53.

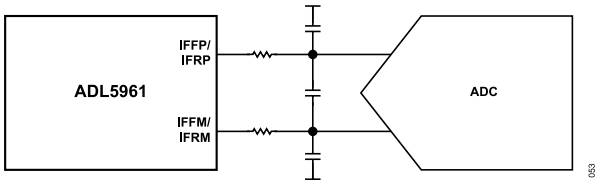



*Figure 53. Interfacing the ADL5961 to an ADC*

Each of the differential IF output nodes are low source impedance. For this reason, it is recommended to use series resistors when necessary, such as for driving filters or highly capacitive loads or cables, as shown on the test circuit (see Figure 72).

## THEORY OF OPERATION

### MULTIPORT VNA

The ADL5961 can also be used to create VNAs consisting of multiple ports, as shown in Figure 54. Each port connects to one ADL5961, and RF switches route the RF signal to one ADL5961 at a time. For optimum phase (and magnitude) accuracy, ensure that the connections from the RF source to all ports are equal in length. Furthermore, always terminate the RFIN ports of the ADL5961 devices with 50 Ω, that is, when the RF source is connected but also when the RF source is not connected to the port. To achieve this, use an SPxT nonreflective switch with the RF source connected to the pole. For VNAs with many ports, a cascade of nonreflective (terminated) RF switches can be used at the expense of larger insertion loss and potentially increased frequency tilt. Note that the connections to the RF source as drawn in Figure 54 are simplified and do not by any means follow the recommendations for an optimal layout of the system.

Phase synchronization between the ADL5961 devices is achieved through the LO and offset frequency signals. For optimal accuracy, match the propagation delays from the LO source to each of the ADL5961 devices. Residual delay differences can be addressed through calibration procedures for the VNA system. Routing of the signal lines to the offset interface is less critical because these lines operate at much lower frequencies.

The SYNC interface is used to force the LO and offset dividers in all ADL5961 devices to the same known initial state, such that no phase ambiguities exist between the devices. A single pulse applied to this input after power-on is sufficient to synchronize all devices. Perform this synchronization before an LO signal is applied. In this case, the timing of the SYNC pulse is not critical.

For optimal accuracy, simultaneous sampling of all ADL5961 IF channels is recommended. For high port counts, a multichannel simultaneous sampling ADC can significantly reduce the solution footprint. Some of these multichannel devices include built-in digital downconversion (DDC) and decimation filters, which reduce the amount of processing required in a digital signal processor (DSP).

The performance of the system can further be enhanced by inserting a programmable RF filter in the RF path to filter any harmonic content of the RF source and a programmable attenuator to compensate for the tilt vs. frequency introduced by any filters, switches, and transmission lines.

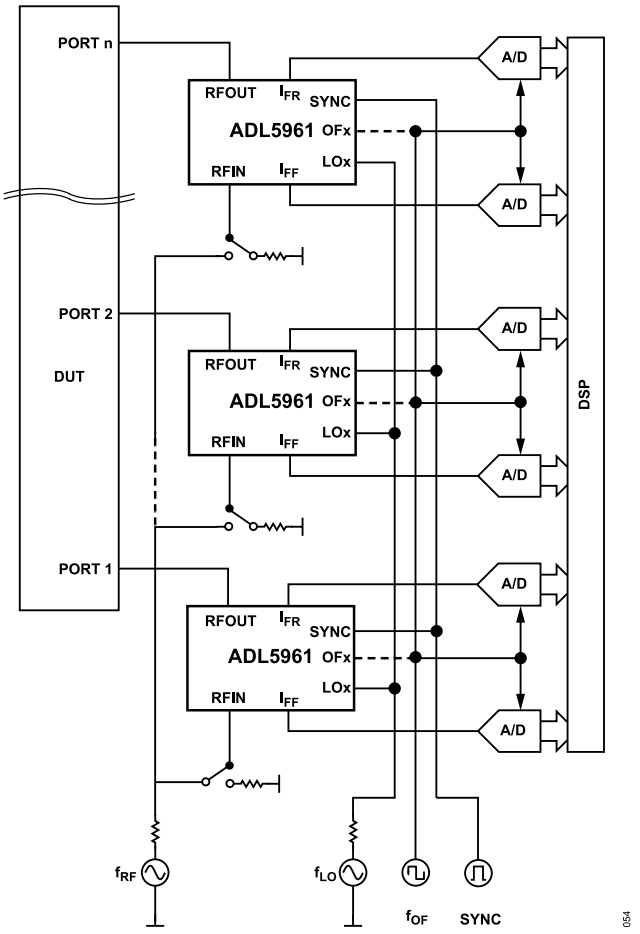



*Figure 54. Multiport VNA-Based on the ADL5961 ($I_{FR}$ Is IF Reverse, and $I_{FF}$ Is IF Forward)*

## THEORY OF OPERATION

### CALIBRATION AND ERROR CORRECTION

The accuracy of S-parameter measurements is prone to a variety of errors introduced by the hardware in VNAs. Systematic errors, those that are repeatable and predictable, can be eliminated from the measurement results using calibration and error correction techniques. The types of systematic errors that can be eliminated (to a certain extent) include the following:

- Impedance mismatches
- Gain and insertion loss differences between channels
- Crosstalk between channels

Various error correction and calibration techniques have been developed over the years (see, for example, *D. K. Rytting, "Network Analyzer Accuracy Overview," 58th ARFTG Conference Digest, 2001, pp. 1-13, doi: 10.1109/ARFTG.2001.327486*) that differ in their effectiveness to eliminate certain errors, complexity, and calibration standards used. The general principals that are applied, however, are the same for all. The systematic errors are determined by measuring the VNA response for a set of DUTs with accurately known S-parameters, the calibration standards. Comparing the measured S-parameters with the known S-parameters allows calculation of the error coefficients. These error coefficients, combined into what is often referred to as an error adapter, can then be used in a postprocessing step to calculate the error corrected S-parameters from the measured S-parameters of an unknown DUT. Figure 55 illustrates the concept.

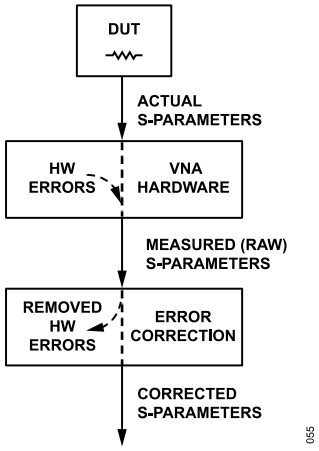



*Figure 55. Concept of Error Correction in VNAs*

Different error correction techniques require the use of different sets of calibration standards. Some of the most well known include short, open, load, thru (SOLT), thru, reflect, line (TRL), and thru, reflect, match (TRM). The standards within a set are chosen to have significantly different S-parameters, such that they span a large area on the Smith chart. The calibration standards themselves, particularly the ones with extreme S-parameter values such as short and open standards, are typically not completely ideal either and usually include a manufacturer supplied model for the S-parameters vs. frequency. In general, calibration standards can be subdivided into the two following categories:

- One-port calibration standards, measured at each VNA port
- Two-port calibration standards, measured for each combination of VNA ports

The calibration procedure for a VNA built from ADL5961 devices is similar to that for any other VNA system. For maximum accuracy, it is important to note the frequencies used. Additionally, the ADL5961 SPI gain, bandwidth, and frequency multiplier and/or divider settings used during calibration must exactly match the settings used during an actual DUT measurement. Calibrate the VNA for multiple different configurations if the settings are expected to be different during an actual measurement because gain and other settings are subject to device-to-device and channel-to-channel spread (mismatch).

Although S-parameters are the result of a power ratio calculation and, in principle, independent of absolute power levels, it is often important to accurately control the RF source power vs. frequency during a measurement. When the DUT exhibits nonlinearity across the applied RF power levels, such as semiconductor devices, a change in power level can result in a change of the DUT behavior that affects the measurement accuracy. The ADL5961 forward IF channel can be used to monitor the power levels in the RF signal path, particularly when the port is terminated with 50 Ω, such as during calibration of the system with a load standard. The conversion gain of the ADL5961 itself does exhibit roll-off vs. frequency as well, which must be taken into account to achieve an accurate power measurement.

## THEORY OF OPERATION

### One-Port Calibration

The calibration procedure for a one-port S-parameter measurement can be explained using the flow diagram in Figure 56 (see also *D. K. Rytting, "Network Analyzer Accuracy Overview," 58th ARFTG Conference Digest, 2001, pp. 1-13, doi: 10.1109/ARFTG.2001.327486*). The directional coupler and error model together describe the operation of a practical VNA. The incident wave, $a_0$, and reflected wave, $b_0$, represent the forward and reverse power measured by the VNA. When using the ADL5961, these vectors are obtained from the IF outputs, IFFx and IFRx. The actual power incident on the load is represented by $a_1$, whereas $b_1$ represents the actual power reflected by the load. An error-free VNA measures $a_1$ and $b_1$.

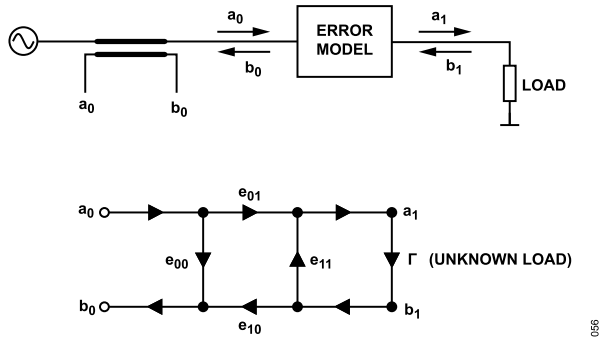



*Figure 56. Error Model for One-Port S-Parameter Measurements*

The flow diagram provides a more detailed description of the various error contributions that cause the measured reflection coefficient, $\Gamma_M = b_0/a_0$, to differ from the actual reflection coefficient, $\Gamma = b_1/a_1$. The factor, $e_{11}$, represents impedance mismatch of the VNA port (from 50 Ω). A fraction of $b_1$ is reflected back to the load. The $e_{01}$ and $e_{10}$ factors represent the tracking error. In relation to the ADL5961, the tracking error comprises insertion loss of the bridge, the conversion gain from RFIN to IFFx and RFOUT to IFRx, as well as the mismatch in conversion gain between the channels. Finally, $e_{00}$ represents the finite directivity of a practical VNA, a measure for the ability to separate the forward and reverse traveling power waves. If the load is a perfect 50 Ω, then $b_1 = 0$ and an ideal VNA measures $b_0 = 0$. However, in a practical VNA, the directivity is finite and some signal leaks from the forward path to the reverse path.

Using Figure 56, the measured reflection coefficient can be expressed in terms of the error coefficients and the reflection coefficient of the load as follows:

$$\Gamma_M = e_{00} + \frac{e_{01}e_{10}}{1 - \Gamma e_{11}}\Gamma \tag{7}$$

Equation 7 can be rearranged into a linear expression for the error coefficients as follows:

$$\begin{aligned} &e_{00} - \Delta_e\Gamma + e_{11}\Gamma_M = \Gamma_M \\ &\Delta_e = e_{00}e_{11} - e_{01}e_{10} \end{aligned} \tag{8}$$

A calibration procedure that measures three different known loads, that is, collects three combinations of measured and actual reflection coefficients, can then be used to calculate the error coefficients as follows:

$$\underbrace{\begin{pmatrix} 1 & -\Gamma_1 & \Gamma_{M1} \\ 1 & -\Gamma_2 & \Gamma_{M2} \\ 1 & -\Gamma_3 & \Gamma_{M3} \end{pmatrix}}_{T} \underbrace{\begin{pmatrix} e_{00} \\ \Delta_e \\ e_{11} \end{pmatrix}}_{\vec{e}} = \underbrace{\begin{pmatrix} \Gamma_{M1} \\ \Gamma_{M2} \\ \Gamma_{M3} \end{pmatrix}}_{\vec{\Gamma_M}} \Rightarrow \vec{e} = T^{-1}\vec{\Gamma_M} \tag{9}$$

After the system is calibrated, the corrected reflection coefficient can be calculated from the measured coefficient by rearranging Equation 7:

$$\Gamma = \frac{\Gamma_M - e_{00}}{e_{11}\Gamma_M - \Delta_e} \tag{10}$$

Although in principle any combination of sufficiently different standards can be used to calibrate the system, a combination of a short, an open, and a 50 Ω load are by far the most common choice. Note that the procedure outlined in Equation 9 needs to be repeated at every frequency point of interest.

### Two-Port Calibration

The calibration procedure for a two-port S-parameter measurement can be explained using Figure 57. The VNA is modeled by Port 0, Port 2, and the error model. As a result of the hardware errors in the system, the measured S-parameters at Port 0 differ from the actual DUT S-parameters observed at Port 1, and the S-parameters measured at Port 2 differ from the DUT S-parameters at Port 3. As long as the error contributions scale linearly with power, the incident and reflected waves at Port 0 and Port 2 can be related to those at Port 1 and Port 3 using the block matrix that follows:

$$\begin{pmatrix} b_0 \\ a_0 \\ b_2 \\ a_2 \end{pmatrix} = \begin{pmatrix} T_{01} & T_{03} \\ T_{21} & T_{23} \end{pmatrix} \begin{pmatrix} b_1 \\ a_1 \\ b_3 \\ a_3 \end{pmatrix} \tag{11}$$

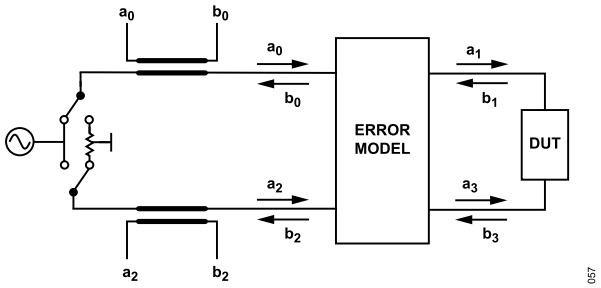



*Figure 57. Error Model for Two-Port S-Parameter Measurements*

Each of the matrix elements, T in Equation 11, is a 2 × 2 matrix that describes the interaction between one VNA port and one DUT port, resulting in a total of 16 unknown error coefficients. A wide range of

## THEORY OF OPERATION

different calibration strategies are reported in literature to determine either a subset of or all of the error coefficients (matrix elements).

One strategy to simplify the error model assumes that the crosstalk between the VNA channels is negligible, that is, that contributions of Port 1 to measurement errors in Port 2 and contributions of Port 3 to measurement errors in Port 0 are small. This assumption is plausible in a VNA based on the ADL5961 because each VNA port is realized by a separate device. Interaction between the VNA channels can be minimized through careful PCB layout. For this situation, only the block matrices on the diagonal in Equation 11 have nonzero elements, resulting in the following:

$$\begin{pmatrix} b_2 \\ a_2 \end{pmatrix} = T_{23}T_{31}T_{01}^{-1}\begin{pmatrix} b_0 \\ a_0 \end{pmatrix} = T_M\begin{pmatrix} b_0 \\ a_0 \end{pmatrix} \quad (12)$$

where:
$T_{31}$ represents the transmission matrix of the DUT itself (the quantity to be measured).
$T_M$ the transmission matrix measured by the VNA.

The error corrected transmission matrix can then be expressed as follows:

$$T_{CORRECTED} = T_{23}^{-1}T_M T_{01} \quad (13)$$

Many different calibration techniques are available to determine the transmission matrices, $T_{01}$ and $T_{23}$. One of the simplest yet effective methods is the SOLT calibration by which a one-port calibration is applied to each port, followed by the measurement of a thru connection (short between Port 1 and Port 3).

### Multiport Calibration

Calibration of VNAs consisting of more than two ports can be performed along similar procedures as the two-port calibration discussed in the Two-Port Calibration section. The number of error coefficients to be determined grows quadratically as $4n^2$, where n is the number of ports. However, when interactions between the VNA ports is neglected only the coefficients on the block diagonal of the error model must be taken into account, resulting in $4n$ remaining coefficients.

A practical problem arising with multiport calibration is that calibration standards are usually either one-port (loads) or two-port, whereas the calibration procedure, in principle, requires the measured n × n S-matrix and an n × n S-matrix for the actual standard S-parameters. This problem can be addressed by constructing the n-port S-matrix from a series of two-port measurements. Equation 14 illustrates the concept for a four-port system.

$$S = \begin{pmatrix} m_{12} & m_{12} & m_{13} & m_{14} \\ m_{12} & m_{12} & m_{23} & m_{24} \\ m_{13} & m_{23} & m_{13} & m_{34} \\ m_{14} & m_{24} & m_{34} & m_{14} \end{pmatrix} \quad (14)$$

where $m_{xy}$ indicates from which two-port measurement the corresponding S-parameter is determined.

For example, a two-port measurement using Port 1 and Port 2, indicated by $m_{12}$, can be used to determine $s_{11}$, $s_{12}$, $s_{21}$, and $s_{22}$. Measurements on different combinations of two ports are needed to fill the entire S-matrix. Some parameters are determined multiple times (like $s_{11}$) and can be disregarded in all but one measurement. In general, the full set of $n^2$ S-parameters can be determined with $n(n - 1)/2$ two-port measurement sessions.

When the SOLT calibration method is applied to an n-port VNA, for example, it requires measurement of three loads on each port, followed by a thru standard measurement between all combinations of two ports. The total number of measurement runs required for this is

$$3n + n(n - 1)/2 = n(n + 5)/2 \quad (15)$$

### Rejection of IF Spurious Tones

Besides the desired output signal, a variety of other spurious tones and mixing products are generally present in the IF output signal spectrum. Some of these undesired tones appear at the same frequency as the desired IF signal, and therewith reduce the measurement accuracy. The techniques described in this section can be used to reduce the impact of such undesired tones and enhance the measurement accuracy.

The LO interface configurations that use the OF interface are most vulnerable to IF spurious tones. Harmonics, subharmonics, mixing products between the LO and OF, and partially suppressed image frequencies contribute to spurious tones in the IF output spectrum. The impact of spurious tones is most pronounced when the DUT at the RFOUT port is well matched, such that the desired signal in the reverse IF output channel is small. Figure 58 illustrates the impact of spurious tones at the IF frequency, comparing a return loss measurement result corrected for IF spurious tones and a raw, uncorrected result. As apparent from Figure 58, spurious tones introduce ripple vs. frequency in the measurement result and reduce the measurement sensitivity, particularly at frequencies below 5 GHz.

## THEORY OF OPERATION

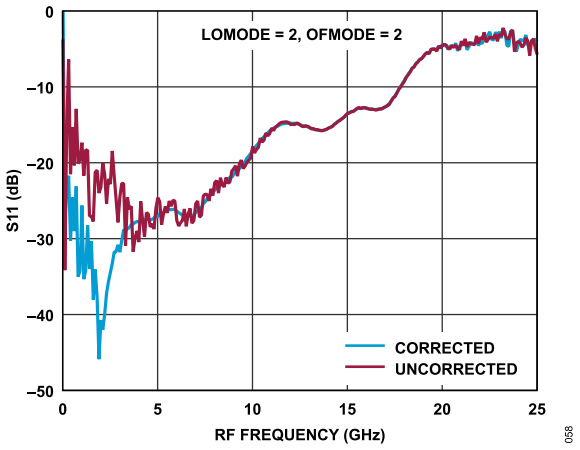



*Figure 58. Return Loss Measurement of a 50 Ω Load With and Without Correction of IF Spurious Tones*

The following simple procedure can significantly reduce the ripple due to spurious tones:

1. Measure the IF output signal with RF present.
2. Calculate the complex fast Fourier transform (FFT) frequency component at the IF output frequency.
3. Measure the IF output signal with the RF signal off or set to a low level.
4. Calculate the frequency component at the IF frequency for this case.
5. Subtract the result obtained in Step 4 from the result in Step 2.
6. Apply error correction and further processing to the result of Step 5).

The order of the steps described can be changed, and the frequency sweep without RF signal can be stored in the memory for correction of future measurements.

## APPLICATIONS INFORMATION

### INTERFACE DESCRIPTIONS

#### Power Supply Interfaces

The AVCC, OVCC, and OVDD pins have independent supply clamps and must be ramped slower than 100 µs to avoid triggering the clamps. Decoupling of the supply interfaces with 1 nF//4.7 µF capacitors is recommended to suppress residual high-frequency ripple. OVDD can be connected to the supply of the SPI controller to eliminate the need for logic level translators in the SPI bus lines.

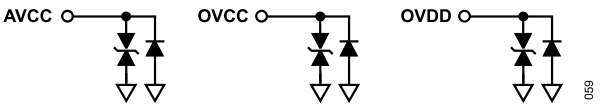



*Figure 59. Simplified Power Supply Interface Schematics*

#### RFIN and RFOUT Interface

RFIN and RFOUT are both single-ended RF inputs with 50 Ω characteristic impedance. Because both interfaces are internally coupled, the input impedance observed at RFIN (or RFOUT) is 50 Ω if, and only if, the other interface, RFOUT (or RFIN), is terminated with 50 Ω.

Both pins are internally DC-coupled through a 6 Ω series resistance of the bidirectional bridge. DC blocking capacitors must be used on these pins to prevent debiasing the input RF mixers. The bridge is designed to support average signal levels up to 30 dBm in matched conditions and peak levels up to 35 dBm. Signal voltages on the interfaces must stay within the −5 V to +10 V range under extreme mismatched conditions, such as an open circuit that can result in larger voltage swings than observed with a matched termination.

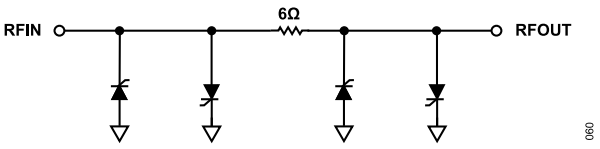



*Figure 60. Simplified RFIN and RFOUT Interfaces*

To achieve the best possible bridge directivity, both RFIN and RFOUT must be connected to carefully matched 50 Ω broadband transmission lines. A grounded coplanar waveguide (GCPW), as shown in Figure 61, is a suitable implementation for this purpose. Use Pin 2 and Pin 4 (AGND) as the RF return path for the RFIN interface, and use Pin 18 and Pin 20 as the return path for the RFOUT interface. A ground shield between RFIN and RFOUT is necessary to minimize interaction outside of the bridge, which also impacts the measured directivity. The top ground and bottom ground layers must be connected with as many vias as possible in the shield between RFIN and RFOUT and around the edge of the ground return conductors of the GCPW.

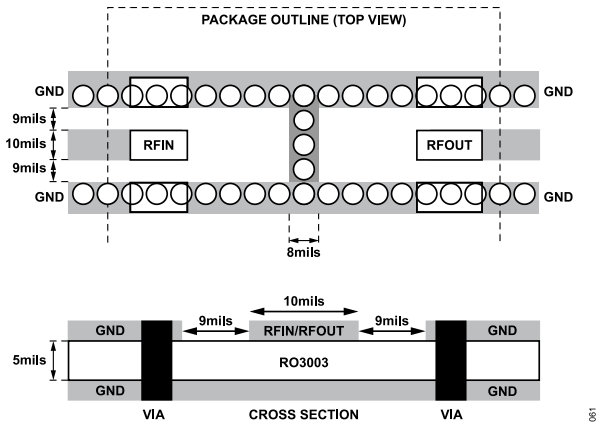



*Figure 61. Example GCPW Design for Interfacing RFIN and RFOUT*

#### IFFP, IFFM, IFRP, and IFRM Interfaces

The differential IF output amplifiers are capable of driving 100 Ω differential loads up to 8 V p-p. In the event of an output short circuit to ground or AVCC, an internal clamp limits the current to less than roughly 200 mA for each of the single-ended outputs (IFFM, IFFP, IFRP, and IFRM).

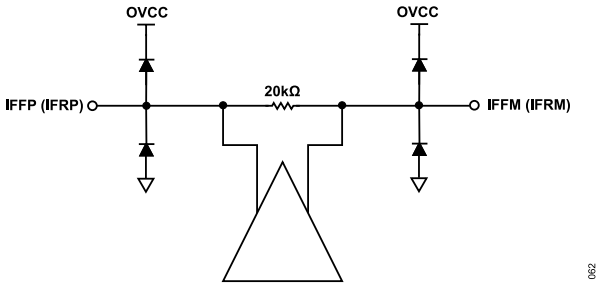



*Figure 62. Simplified Schematic of the IF Output Interfaces*

#### VCM Interface

The VCM interface controls the common-mode voltage level at the IFFx and IFRx output interfaces and simplifies DC-coupled interfacing to a wide variety of ADCs. If provided by the ADC of choice, VCM can be connected to the common-mode output or reference output pin to align the common-mode levels and maximize the available dynamic range.

When the VCM pin is left floating, an internal voltage-divider sets the common-mode voltage level to OVCC/2. When externally driven, a low-impedance voltage source must be used to set the voltage on VCM. The tracking range of the VCM voltage to the common-mode output voltage is linear in the 1 V to 4 V range. For voltage levels outside this range, the output common-mode level is clamped to 1 V or 4 V, respectively.

## APPLICATIONS INFORMATION

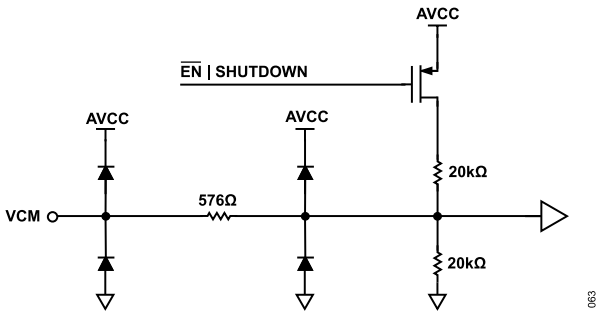



*Figure 63. Simplified Schematic of the Common-Mode Control Interface*

### LOP and LOM Interface

The LO interface can be driven differentially or single-ended. A differentially driven LO with a well designed PCB layout (for example, using a ground, signal, signal, ground coplanar waveguide (CPW)) can help to reduce LO signal radiated emission and unwanted coupling to other nets in the system. The LOP and LOM inputs are internally biased at AVCC/2. When driven single-ended, the internal 100 Ω termination can be impedance matched using a 2:1 external balun.

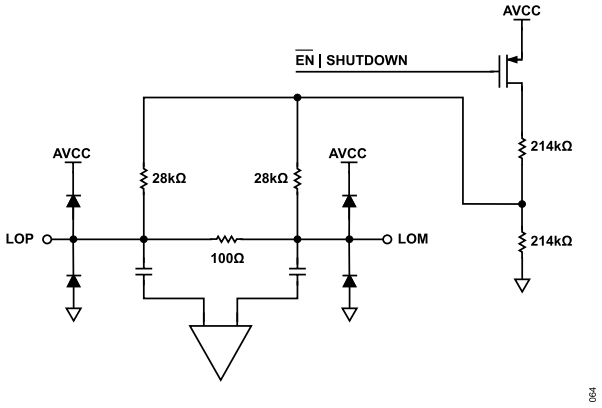



*Figure 64. Simplified LO Interface*

### OFP and OFM Interface

The offset frequency interface (OFP and OFM) is internally biased at a common-mode level of 3.3 V and must be AC-coupled to an external signal source. The inputs can be driven differentially or single-ended with one terminal AC grounded with a high value capacitor. A value of 10 nF or higher is recommended for a 400 kHz input frequency.

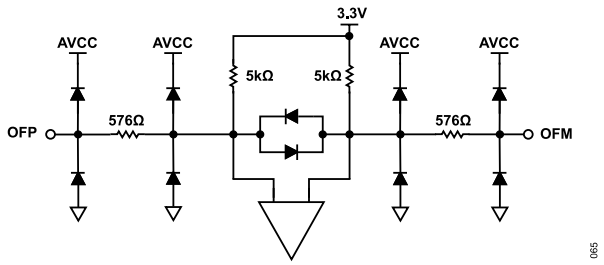



*Figure 65. Simplified Offset Frequency Interface*

### EN Interface

The chip is in shutdown if either the shutdown bit in DEVICE_CONFIG (Register 0x02, Bit 1) is set, or the EN pin is de-asserted. An internal 415 kΩ pull-down ensures the device is off (shut down) if the EN pin is left floating.

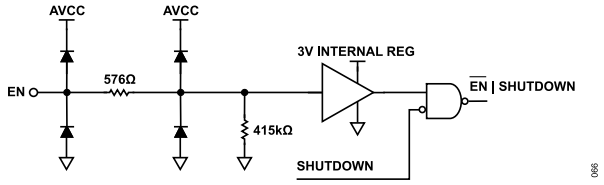



*Figure 66. Simplified Enable Interface*

### SYNC and SCK Interfaces

The SYNC and SCK interfaces are both high-impedance CMOS logic input interfaces. As listed in Table 1, the logic high and logic low levels are defined relative to the serial port supply interface, OVDD. Both inputs are internally pulled low when left floating.

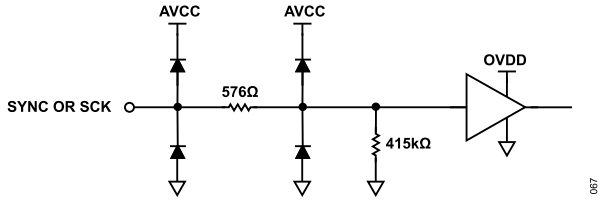



*Figure 67. SYNC and SPI Clock Interface*

The SYNC interface is used to synchronize all ADL5961 devices in a system. A falling edge on this interface resets the frequency dividers in the LO and OF interfaces to a known, predefined state. All ADL5961 devices receive the negative SYNC edge before the next edge on the LO or OF interface arrives. The SYNC pulse can also be applied directly after power-on, before an LO and OF clock are applied.

### $\overline{CS}$ Interface

The $\overline{CS}$ interface controls the start and ending of communications through the serial interface of the ADL5961. The SPI is active when the voltage on $\overline{CS}$ is logic low, and it is disabled when the voltage on $\overline{CS}$ is logic high, as defined in Table 1. The input is internally pulled high, disabling the SPI, when the $\overline{CS}$ pin is left floating.

## APPLICATIONS INFORMATION

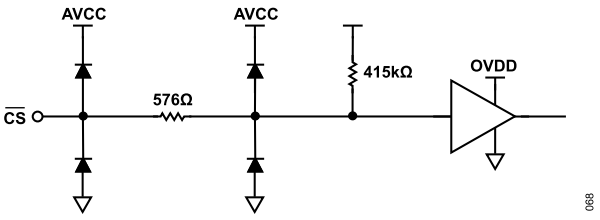



*Figure 68. SPI Chip Select Interface*

### SDIO Interface

The ADL5961 implements a 3-wire SPI that uses a single line for transmission and reception of data. When receiving data, that is, during a write operation to the ADL5961, the transmitter output becomes high-impedance such that the transmitting device can pull the data line low or high as desired. To connect this interface to an SPI controller using a 4-wire interface, with separate data input and data output lines, a series current-limiting resistor, as is shown in Figure 70, is recommended to isolate the controller and target outputs. This resistor provides protection in the event that both outputs become simultaneously active.

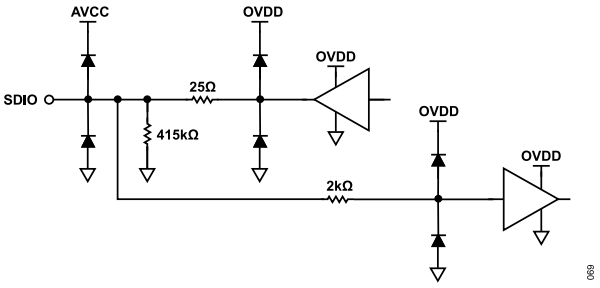



*Figure 69. Simplified SDIO Interface*

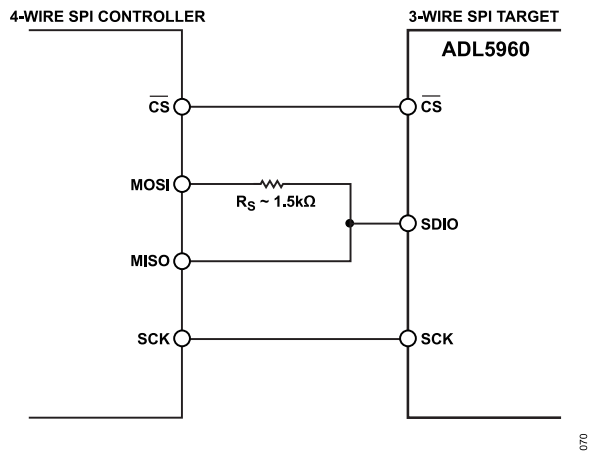



*Figure 70. SPI 4-Wire to 3-Wire Interfacing*

### TEMP Interface

In addition to the on-chip digital thermometer, the TEMP pin can be used to monitor the die temperature by applying a known reference current into the TEMP pin and measure the pin voltage relative to ground. An injected current of 42 µA results in a nominal voltage of 0.775 V at 25°C and a temperature slope of approximately −1.54 mV/°C.

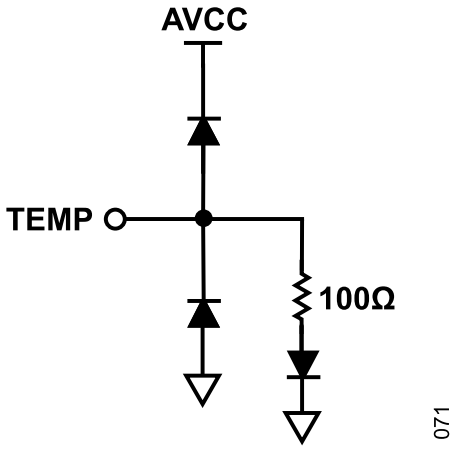



*Figure 71. Temperature Diode Interface*

## LO INTERFACE CONFIGURATION

The LO interface supports a bypass mode, three different multiply modes, and one divide mode that are selectable through Register 0x20 in the SPI. Each of these operating modes is discussed in the Bypass Mode (BYPASS = 1) section through the Multiply by 4 Mode (LOMODE = 3) section.

### Bypass Mode (BYPASS = 1)

The LO signal is routed directly to the internal downconversion mixers, bypassing the frequency multipliers and dividers. The LO multipliers and dividers and the offset frequency interface are disabled. The ADL5961 achieves the widest bandwidth and the highest dynamic range in this mode.

### Divide by 2 Mode (LOMODE = 0)

The frequency of the LO input signal is divided by two before being passed through the offset mixer and supplied to the downconversion mixers. If supported by the frequency range of the RF signal, this LO operating mode provides a means to extend the VNA measurements frequency range to less than the minimum frequency supported by the LO source itself. This operating mode can be used either with the offset frequency interface enabled or disabled.

### Multiply by 1 Mode (LOMODE = 1)

The LO signal bypasses the LO multipliers and dividers but is routed through the offset mixer to the downconversion mixers. The intended use is with the offset frequency interface enabled. Although it can be used with the offset frequency interface disabled, improved performance is achieved by selecting the bypass mode (BYPASS = 1) instead.

## APPLICATIONS INFORMATION

### Multiply by 2 Mode (LOMODE = 2)

The LO signal is passed through a frequency doubler, a programmable band-pass filter, and an offset mixer to the downconversion mixers. The band-pass filter suppresses the subharmonics in the doubler output signal and can be tuned by programming the CT2 bits in Register 0x21, Bits[4:0]. Table 8 lists the recommended setting for different 2× $f_{LO}$ ranges. All CT2 settings are valid. For CT2 settings not shown in Table 8, for example CT2 = 2, CT2 = 5, ..., CT2 = 30, the minimum and maximum 2× $f_{LO}$ can be linearly interpolated based on the table entries shown in Table 8. The multiply by 2 mode can be used as a standalone or in combination with the offset frequency interface.

*Table 8. Recommended CT2 Band-Pass Filter Settings for LOMODE = 2*

| CT2 | Minimum 2× $f_{LO}$ (GHz) | Maximum 2× $f_{LO}$ (GHz) |
|---|---|---|
| 0 | 15 | 20 |
| 1 | 14 | 15 |
| 3 | 11 | 14 |
| 4 | 10 | 12 |
| 6 | 9 | 10 |
| 8 | 8 | 9 |
| 12 | 7 | 8 |
| 15 | 6 | 7 |
| 22 | 5 | 6 |
| 31 | 4 | 5 |

### Multiply by 4 Mode (LOMODE = 3)

The LO signal is passed first through a frequency doubler, followed by the band-pass filter tuned through the CT2 bits (Register 0x21, Bits[4:0]), through a second frequency doubler, and followed by a second band-pass filter tuned through the CT4 bits in Register 0x22, Bits[3:0]. The signal is then passed through the offset mixer to the downconversion mixers. Table 9 lists the recommended setting for different 4× $f_{LO}$ ranges; however, this list is not exhaustive. Other valid combinations exist that result in frequency ranges partially or entirely overlapping with the recommended settings. This mode can be used as a standalone or in combination with the offset frequency interface.

*Table 9. Recommended CT2/CT4 Band-Pass Filter Settings for LOMODE = 3*

| CT2 | CT4 | Minimum 4× $f_{LO}$ (GHz) | Maximum 4× $f_{LO}$ (GHz) |
|---|---|---|---|
| <5 | <12 | >20 | >21 |
| 5 | 12 | 20 | 21 |
| 6 | 13 | 19 | 20 |
| 7 | 14 | 17 | 19 |
| 12 | 15 | 14 | 17 |

## IF SIGNAL PATH CONFIGURATION

The IF signal path following the downconversion mixers can be configured to optimize the output signal dynamic range and to achieve optimal interfacing to a wide range of ADCs.

Two cascaded LPFs provide programmable IF bandwidth for suppression of out of band noise and spurious tones. The first filter provides coarse bandwidth adjustment through the CIF1 bits in Register 0x25, Bits[3:0], as listed in Table 10 and shown in Figure 22.

*Table 10. IF −3 dB Bandwidth vs. CIF1 with CIF2 = 0*

| CIF1 | $f_{-3dB}$ (MHz) |
|---|---|
| 0 | 126 |
| 1 | 64.0 |
| 2 | 41.0 |
| 3 | 30.1 |
| 4 | 24.1 |
| 5 | 19.7 |
| 6 | 16.7 |
| 7 | 14.5 |
| 8 | 13.0 |
| 9 | 11.6 |
| 10 | 10.5 |
| 11 | 9.5 |
| 12 | 8.8 |
| 13 | 8.1 |
| 14 | 7.6 |
| 15 | 7.0 |

The second filter provides finely spaced lower bandwidth settings programmable through the CIF2 bits in Register 0x25, Bits[7:4], listed in Table 11 and shown in Figure 25. Both output channels are programmed to the same IF bandwidth.

*Table 11. IF −3 dB Bandwidth vs. CIF2 with CIF1 = 0*

| CIF2 | $f_{-3dB}$ (MHz) |
|---|---|
| 0 | 126 |
| 1 | 11.1 |
| 2 | 5.9 |
| 3 | 3.8 |
| 4 | 3.1 |
| 5 | 2.3 |
| 6 | 2 |
| 7 | 1.6 |
| 8 | 1.5 |
| 9 | 1.3 |
| 10 | 1.2 |
| 11 | 1.0 |
| 12 | 0.99 |
| 13 | 0.86 |

## APPLICATIONS INFORMATION

*Table 11. IF −3 dB Bandwidth vs. CIF2 with CIF1 = 0 (Continued)*

| CIF2 | $f_{-3dB}$ (MHz) |
|---|---|
| 14 | 0.80 |
| 15 | 0.70 |

Following the filters are differential output amplifiers with individually programmable gain. The adjustable gain feature is to accommodate the actual RF drive level in use, and this feature also enables dynamic range optimization of both the forward and reverse channels over a wide range of port terminations. For example, if the bridge is terminated with an impedance close to 50 Ω, the bridge output signal level in the reverse (reflected) channel is much lower than in the forward (incident) channel. To compensate for this difference, the reverse channel amplifier can be programmed to a higher gain setting than the forward channel, so both channels use the full input dynamic range of the ADC connected to the IF outputs. To achieve optimal measurement accuracy, a calibration procedure must cover all used gain setting combinations for the forward and reverse channels.

The gain for the forward and reverse channel can be programmed through the FGAIN bits in Register 0x23, Bits[6:0], and the RGAIN bits in Register 0x24, Bits[6:0], respectively, in 6 dB steps, as shown in Table 12. Note that the bit values also must be increased in steps of 6 to select the next gain setting (see Figure 20). Although gain levels beyond 48 dB are supported, these levels are usually of little practical significance because amplified noise starts to saturate the IF channels.

*Table 12. IF Amplifier Gain vs. FGAIN and RGAIN Settings*

| FGAIN, RGAIN | IF Gain (dB) |
|---|---|
| 0 to 5 | 0 |
| 6 to 11 | 6 |
| 12 to 17 | 12 |
| 18 to 23 | 18 |
| 24 to 29 | 24 |
| 30 to 35 | 30 |
| 36 to 41 | 36 |
| 42 to 47 | 42 |
| 48 to 53 | 48 |
| … | … |

The adjustable output common-mode level, an up to 8 V p-p output-voltage swing and an up to 200 mA current drive capability, provides enough flexibility to interface with a broad range of suitable Σ-Δ, successive approximation register (SAR), or pipeline-based ADCs with sample rates up to several hundred MHz.

## SERIAL PERIPHERAL INTERFACE

### PROTOCOL

The ADL5961 can be connected to an SPI bus as a peripheral device to control and monitor several of its internal functions. See the Serial Interface Timing Specifications section for detailed timing requirements. The 3-wire interface with a shared data input and output line uses 16-bit addresses to access the 8-bit wide registers. Each SPI instruction consists of the register address followed by one or more data bytes, with the MSB transferred first. The ADL5961 supports single-byte read and write operations as well as streaming read and write methods.

### REGISTER ADDRESS

The 15 LSBs of the 16-bit register address define an address space with $2^{15}$ = 32,768 unique register addresses. Only a fraction of these addresses are used by the ADL5961. The MSB is reserved to distinguish between a write operation to the device register (MSB = 0) and a readback from the register address (MSB = 1).

### READ AND WRITE METHODS

The ADL5961 supports both single register read and write methods and streaming read and write methods, transferring data to and from multiple registers in a single operation.

Each instruction starts with a high to low transition of the $\overline{CS}$ line. Data is latched, starting with the MSB address bit, at each rising edge of the clock as long as $\overline{CS}$ remains low. The instruction ends with a low to high transition on $\overline{CS}$. When a read instruction is executed, the SDIO shared input and output line changes from a high-impedance input (SDI) to a low-impedance output (SDO) during the ½ clock cycle immediately following the rising edge on SCLK that latched the last address bit and the next falling edge on SCLK. SDIO returns to a high-impedance input (SDI) state when $\overline{CS}$ is de-asserted.

Streaming read and write methods operate in autodecrement mode only, reading and writing the next data byte to and from the register with the address that is one lower than the previous one.

### REGISTER DETAILS

Register 0x00 through Register 0x03 configure the SPI and contain device identifiers. Register 0x20 to Register 0x26 control the analog circuit functionality of the ADL5961. See Table 13 for further details.

#### Interface Configuration Register

Register 0x00 is the serial interface configuration register and is implemented as a 4-bit palindrome with each nibble a mirror of the other. This mirror ensures that regardless of which way data is shifting, the ADL5961 can be programmed if device synchronization is lost. Therefore, when writing to this address, the palindrome is always required to eliminate any ambiguity in configuring this register.

*Table 13. ADL5961 SPI Register Details*

| Addr | Name | Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|---|---|
| 0x00 | SPI_CONFIG_A | 7 | SOFTRESET_ | Soft Reset. Copy of Bit 0. | 0x0 | R/W |
| | | 6 | LSB_FIRST_ | LSB First. Copy of Bit 1. | 0x0 | R/W |
| | | 5 | ASCENSION_ | Address Ascension. Copy of Bit 2. | 0x0 | R/W |
| | | [4:3] | RESERVED | Reserved. | 0x0 | R |
| | | 2 | ASCENSION | Address Ascension. When set, causes address ascension address mode to be enabled. When clear, addresses descend.<br>0: Address Autodecrement.<br>1: Address Autoincrement. | 0x0 | R/W |
| | | 1 | LSB_FIRST | LSB First. When set, causes input and output data to be oriented as LSB first. If this bit is clear, the data is oriented as MSB first.<br>1: LSB First.<br>0: MSB First. | 0x0 | R/W |
| | | 0 | SOFTRESET | Soft Reset. Setting this bit initiates a reset equivalent to a hard reset with the exception that the bits of 0x00 (this register) and the SPI state machine are unaffected. This bit is autoclearing after the soft reset is complete.<br>1: Reset Asserted.<br>0: Reset Not Asserted. | 0x0 | R/W |
| 0x01 | SPI_CONFIG_B | 7 | SINGLE_INSTRUCTION | Single Instruction. When this bit is set, streaming is disabled and only one read or write operation is performed regardless of the state of the $\overline{CS}$ line. When this bit is clear, streaming is enabled. If this bit is set and the $\overline{CS}$ remains asserted, the state machine resets after the data byte as if $\overline{CS}$ was deasserted and awaits the next instruction. This forces each data byte to | 0x0 | R/W |

## SERIAL PERIPHERAL INTERFACE

*Table 13. ADL5961 SPI Register Details (Continued)*

| Addr | Name | Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|---|---|
| | | | | be preceded with a new instruction even though the $\overline{CS}$ line has not been deasserted by the SPI controller. | | |
| | | 6 | CSB_STALL | $\overline{CS}$ Stalling. When SINGLE_INSTRUCTION is enabled and CSB_STALL is enabled, the $\overline{CS}$ signal does not reset the SPI state machine when pulled high. When CSB_STALL is disabled, the SPI state machine always resets when $\overline{CS}$ signal is high. | 0x0 | R/W |
| | | 5 | CONTROLLER_TARGET_RB | Controller or Target Device Readback. Setting this bit allows readback of the SPI controller flip-flop outputs. Clearing this bit provides access to the internal SPI register outputs. | 0x0 | R/W |
| | | [4:0] | RESERVED | Reserved. | 0x0 | R |
| 0x02 | DEVICE_CONFIG | [7:2] | RESERVED | Reserved. | 0x0 | R/W |
| | | 1 | SHUTDOWN | Device Shutdown. If shutdown is asserted, the ADL5961 is powered off. Also see the EN Interface section.<br>0: Normal Operation.<br>1: Shutdown. | 0x0 | R/W |
| | | 0 | RESERVED | Reserved. | 0x0 | R |
| 0x03 | CHIPTYPE | [7:0] | CHIPTYPE | Chip Type, Read Only. | 0x1 | R |
| 0x20 | LO_CONFIG | [7:5] | RESERVED | Reserved. | 0x0 | R |
| | | 4 | BYPASS | Bypass LO Path. When asserted, the LO chain is configured to have all multipliers and dividers turned off. IFMODE and LOMODE have no effect. The LO inputs are connected to the RF mixers by the LO amplifier only. | 0x1 | R/W |
| | | [3:2] | OFMODE | OFMODE. Configures the divider in the offset reference frequency interface.<br>00: ×1 no dividers enabled.<br>01: Divide by 2 mode.<br>10: Divide by 4 mode.<br>11: Dividers off, offset reference signal disconnected. | 0x2 | R/W |
| | | [1:0] | LOMODE | LOMODE. Configures the LO chain divider and multipliers.<br>00: Divide by 2.<br>01: Multiply by 1×.<br>10: Multiply by 2 (2×).<br>11: Multiply by 4 (4×). | 0x1 | R/W |
| 0x21 | CT2 | [7:5] | RESERVED | Reserved. | 0x0 | R |
| | | [4:0] | CT2 | CT2 Filter Setting. Sets the center frequency of the filter in the 2× frequency multiplier in the LO interface. | 0x0 | R/W |
| 0x22 | CT4 | [7:4] | RESERVED | Reserved. | 0x0 | R |
| | | [3:0] | CT4 | CT4 Filter Setting. Sets the center frequency of the filter in the 4× frequency multiplier in the LO interface. | 0x0 | R/W |
| 0x23 | FGAIN | 7 | RESERVED | Reserved. | 0x0 | R |
| | | [6:0] | FGAIN | Forward Gain. Configures the gain of the IF amplifier in the forward path, to the IFFP and IFFM output, in 6 dB steps. Decimal register value represents the gain in dB. | 0x0 | R/W |
| 0x24 | RGAIN | 7 | RESERVED | Reserved. | 0x0 | R |
| | | [6:0] | RGAIN | Reverse Gain. Configures the gain of the IF amplifier in the reverse path, to the IFRP and IFRM output, in 6 dB steps. Decimal register value represents the gain in dB. See Table 12. | 0x0 | R/W |
| 0x25 | CIF2_CIF1 | [7:4] | CIF2 | Narrow-Band IF Filter Setting. Sets the corner frequency of the narrow bandwidth IF filter. See Figure 25. | 0x0 | R/W |
| | | [3:0] | CIF1 | Wideband IF Filter Setting. Sets the corner frequency of the wide bandwidth IF filter. See Figure 22. | 0x0 | R/W |

## SERIAL PERIPHERAL INTERFACE

*Table 13. ADL5961 SPI Register Details (Continued)*

| Addr | Name | Bits | Bit Name | Description | Reset | Access |
|---|---|---|---|---|---|---|
| 0x26 | TDEG | [7:5] | RESERVED | Reserved. | 0x0 | R |
| | | [4:0] | TDEG | Thermometer Register. These bits are a 5-bit thermometer read out. Also, see Figure 40. Approximately 7.4°C/step, TDEG = 0 to TDEG = 1 transition at −44.6°C. | 0x0 | R |

## TYPICAL APPLICATION TEST CIRCUIT

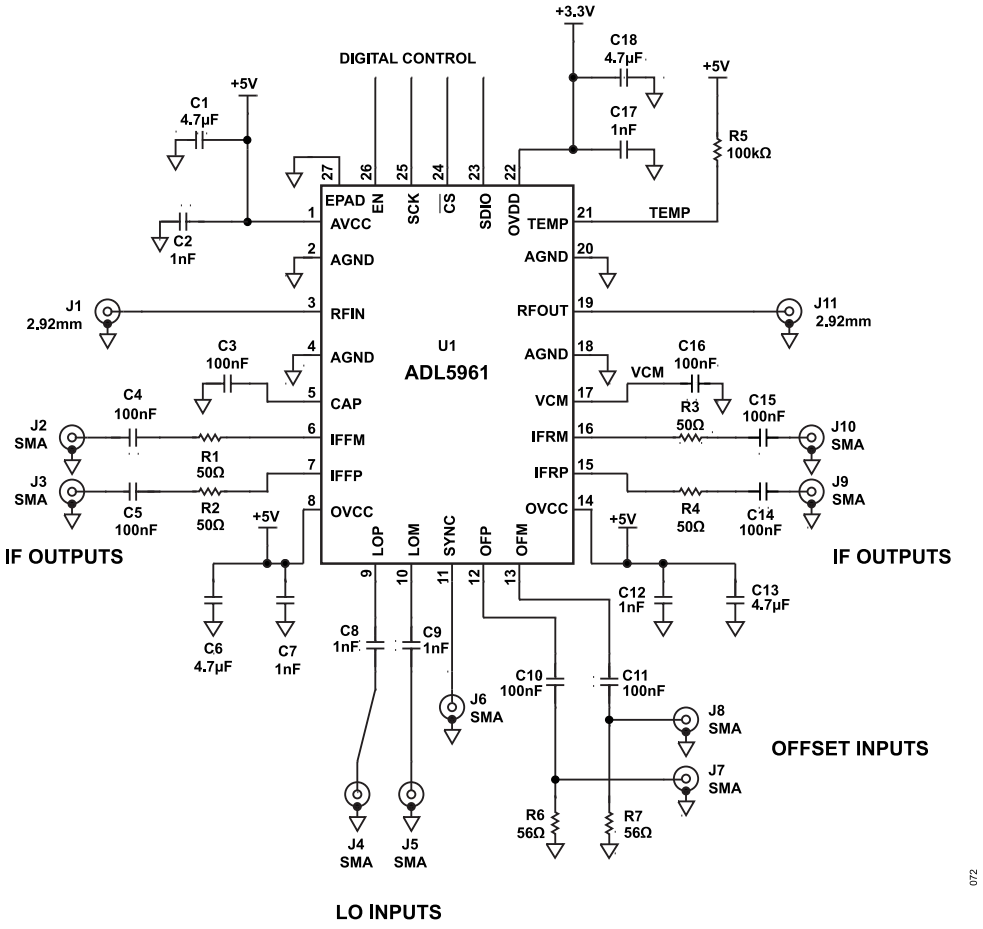



*Figure 72. Test Circuit*

See the EVAL-ADL5961 user guide for details on the evaluation board components.

## OUTLINE DIMENSIONS

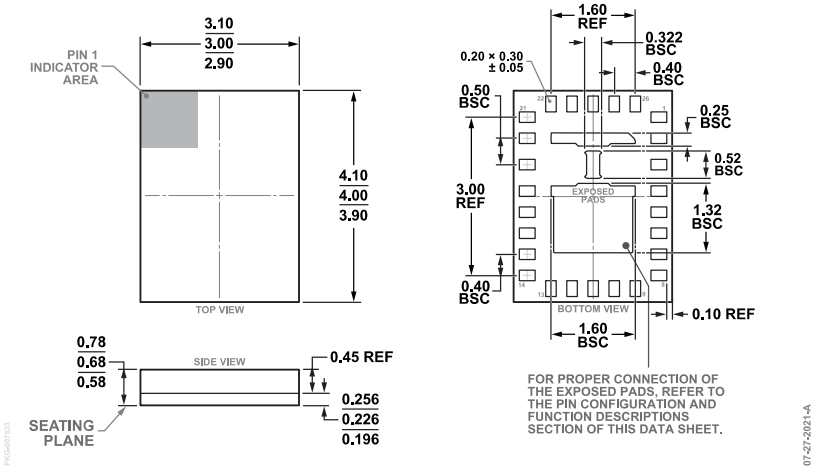



*Figure 73. 26-Lead Land Grid Array [LGA]*
*(CC-26-2)*
*Dimensions shown in millimeters*

Updated: July 05, 2023

## ORDERING GUIDE

| Model[1] | Temperature Range | Package Description | Packing Quantity | Package Option |
|---|---|---|---|---|
| ADL5961ACCZ | −40°C to +105°C | 26-Lead Land Grid Array [LGA] | | CC-26-2 |
| ADL5961ACCZ-R2 | −40°C to +105°C | 26-Lead Land Grid Array [LGA] | Reel, 250 | CC-26-2 |
| ADL5961ACCZ-R7 | −40°C to +105°C | 26-Lead Land Grid Array [LGA] | Reel, 1500 | CC-26-2 |

[1] Z = RoHS Compliant Part.

## EVALUATION BOARDS

| Model[1, 2, 3] | Description |
|---|---|
| ADL5961-EVALZ | Evaluation Board |
| ADL5961-KIT-EVALZ | RF Evaluation Board Kit |

[1] Z = RoHS Compliant Part.

[2] The ADL5961-EVALZ package includes the board only.

[3] A preprogrammed DC2026C Linduino One controller board is included with the ADL5961-KIT-EVALZ.

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