



# **DATASHEET**

## **ENSEMBLE™ FAMILY E8 SERIES EMBEDDED FUSION PROCESSORS**

**LOW POWER FUSION PROCESSOR: DUAL CORTEX-A32, DUAL CORTEX-M55, ETHOS-U85 & U55 NPUs, SECURITY, MIPI-DSI/CSI, ISP, 2D GPU, DUAL HEXSPI, ANALOG INTERFACES, 9.75MB SRAM, 5.5MB MRAM**

## Features

### High-Performance Quad-Core Fusion Processor

- Dual Arm® Cortex®-A32 Cores with Arm Neon™ SIMD Extension up to 800 MHz, 512KB Shared L2, 32KB L1 Instruction and Data Caches, MMU, Armv8-A ISA with Arm TrustZone®
- High-Performance (HP) Arm® Cortex®-M55 Core, up to 400 MHz, with Helium™ Vector Processing Extension, Double-Precision FPU, 1.25MB SRAM 0-wait State Tightly-Coupled Memory (TCM), 32KB Instruction and Data Caches, Armv8.1-M ISA with Arm TrustZone®, and 4.37 CoreMark®/MHz Performance Benchmark.
- High-Efficiency (HE) Arm® Cortex®-M55 Core, up to 160 MHz, with Helium™ Vector Processing Extension, Double-Precision FPU, 512KB of SRAM 0-wait State Tightly Coupled Memory, 32KB Instruction and Data Caches, Armv8.1-M ISA with Arm TrustZone®, and 4.37 CoreMark®/MHz Performance Benchmark.
- High-Performance 400-MHz 64-bit and 128-bit AXI Bus Fabric Common Across System

### Efficient NPUs for Generative AI/ML Acceleration

- 1× Arm Ethos™-U85 Neural Processing Unit (NPU) for Generative AI (NPU-HG), 256 MAC/cycle up to 400 MHz and 204 GOPS, Supporting Recurrent Neural Networks (RNN), Convolutional Neural Networks (CNN), and Transformer Networks, Fed by 128-bit wide High-Bandwidth Local Memory at over 12 GB/s
- 1× Arm Ethos-U55 NPU (NPU-HP), 256 MAC/cycle up to 400 MHz and 204 GOPS, Supporting RNN and CNN Networks
- 1× Arm Ethos-U55 NPU (NPU-HE), 128 MAC/cycle up to 160 MHz and 46 GOPS, Supporting RNN and CNN Networks
- On-the-Fly Weight Decompression with Dedicated DMA Controllers

### Extreme-Low Power Technology

- Autonomous Intelligent Power Management (aiPM™)

- FD-SOI Low Leakage Process
- 1.3 µA Consumed in STOP Mode with LPRTC, LPTIMER, LPCMP, BOR, 4KB Utility SRAM, Wake Pins
- As Low as 27 µA/MHz Dynamic Consumption for High-Efficiency Cortex-M55
- Multiple Power Domains, Dynamic Power Gating, Voltage and Clock Scaling, DC-DC Converter

### On-Chip Application Memory

- High Endurance MRAM Non-Volatile Memory
  - 5.5MB, Minimum 100,000 Write Cycles
- SRAM
  - 9.75MB total SRAM: 8MB Bulk + 1.25MB M55-HP TCM + 0.5MB M55-HE TCM
  - Optional Data Retention of Bulk SRAM and M55-HE TCM SRAM Contents
  - 4KB Always-On Utility SRAM

### External Memory Interfaces

- 2× 16-bit Hex SPI, each up to 400 MB/s SDR, 800 MB/s DDR, with Inline AES Decryption and Support for XIP and HyperBus
- 1× SD® v4.2, eMMC™ v5.1 Channel with DMA

### Secure Enclave

- Hardware-based Root-of-Trust (RoT) with Unique Device ID
- Secure Key Generation and Storage, Secure Certificate Storage, Secure Boot
- In-Factory Provisioned Private Keys
- Crypto Accelerators—AES (up to AES-256), ECC (up to 384 bits), SHA (up to SHA-256), RSA (up to RSA-3072), and NIST compliant TRNG
- Secure Debugging with Certificate Authentication

### Timing Control and Measurement

- 12× Universal High-Resolution 32-bit Timers Capable of Motor and LED Lighting Control
- 3× Low-Power Universal High-Resolution 32-bit Timers
- 4× Watchdog Timers
- 4× Low-Power 32-bit Timers

- 1× Real-Time Counter
- 4× Quadrature Encoder Counters

#### Serial Communication Interfaces

- 1× 10/100 Ethernet with DMA
- 1× USB 2.0 HS/FS Host/Device with DMA
- 1× SDIO v4.1 Channel with DMA
- 1× CAN FD Channel up to 10 Mbps
- 1× MIPI® I3C® Channels
- 1× Low-Power I3C Channel
- 4× I2C Channels up to 3.4 Mbps Throughput
- 2× Low-Power I2C Channels
- 8× UART Channels up to 5 Mbps (4× with RS-485 Driver Control)
- 1× Low-Power UART Channel
- 4× SPI Channels up to 50 Mbps Throughput
- 1× Low-Power SPI Channel

#### Analog Interface Capabilities

- 3× 12-bit SAR ADC (18 Single-Ended Inputs)
- 1× 24-bit Sigma-Delta ADC (4 Differential Inputs)
  - Programmable Gain Instrumentation Amplifier (1× to 128×)
- 2× 12-bit DACs (2 channels)
- 4× High-Speed Analog Comparators with 2.5-ns Response (16 Inputs)
- 1× Low-Power Analog Comparator (4 Inputs)
- Internal Temperature Sensor
- Internal Precision Reference Voltage

#### Camera Interfaces

- 1× 2-Lane MIPI D-PHY CSI-2®, 2.5 Gbps each lane
- Option for 2× MIPI D-PHY CSI-2 Interface by using the MIPI D-PHY DSI in Slave Mode. Allows Interleaving Two Image Streams from Two Separate Image Sensors
- 1× Camera Parallel Interface (CPI), up to 16 bits
- 1× Low-Power CPI, up to 8 bits

#### ISP Acceleration Unit

- Clocked up to 400 MHz, 64-bit Bus Connection
- Maximum Input/Output Resolution: 2MP (1920 × 1080)
- Configurable Frame Rate Control: 1 to 60 FPS
- Input Monochrome Formats: 8-bit, 10-bit
- Conversions: Demosaic Bayer to RGB, YUV422 to YUV444 to RGB
- Output Formats: 8-bit Monochrome, RAW 8/10/12-bit with Raster Scanning, RGB888 Planar, YUV, Y-only

- Auto White Balance and Auto Exposure
- Gamma Correction
- Crop, Scale, Binning, Black Level, Gain

#### JPEG Encoder

- Works in Tandem with ISP to Store Compressed Images and Motion JPEG (MJPEG) Video Clips
- Maximum Performance: 2MP at 200 FPS
- Input Formats: YUV400, YUV420, YUV422, RGB
- Supports JPEG ISO/IEC 10918-1, ITU-T T.81
- Supports MJPEG T.81 Format
- Encoding Color Space: YUV 4:0:0, 4:2:0, 4:2:2
- Cropping, Rotation, Padding

#### Display Interfaces

- Graphics LCD Controller
- 1× Display Parallel Interface (DPI), 24-bit RGB
- 1× 2-Lane MIPI D-PHY DSI®, 2.5 Gbps each lane

#### Graphics

- D/AVE 2D Graphics Processing Unit

#### Audio Interfaces

- 4× I2S Synchronous Stereo Audio Interfaces
- 1× Low-Power I2S Stereo Audio Interface
- 4× 2-channel Pulse Density Modulation (PDM) Microphone Inputs (8 Mono Microphones)
- 4× 2-channel Low-Power Pulse Density Modulation (LPPDM) Microphone Inputs (8 Mono Microphones)

#### General Input/Output

- Up to 136× 1.8-V GPIOs (Shared with Peripherals)
- Up to 8× Selectable 1.8-V to 3.3-V GPIOs (Shared with Peripherals)

#### Clock Generation

- LFRC - Internal Low-Frequency RC Oscillator (32.7 kHz, ±4%)
- HFRC - Internal High-Frequency RC Oscillator (Up to 76.8 MHz, ±2%)
- LFXO - External Low-Power Crystal Oscillator or Quartz Crystal (32.768 kHz)
- HFXO - External High-Frequency Crystal Oscillator or Quartz Crystal (24 MHz to 38.4 MHz)
- One Fractional-N PLL to Generate System Clock, Additional Fractional-N PLL to Generate Audio Clock

**System**

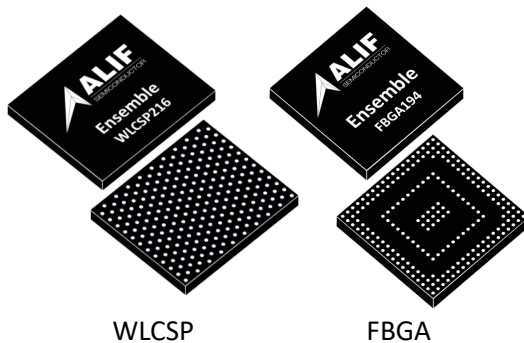
- Global Event Mapping to Configurable Triggers
- 3× 32-Channel General DMA Controllers
- CRC Calculation Accelerator with Programmable Polynomials
- Programmable Low Supply Voltage Detect Warning (Brown-Out Detect)
- Power-On Reset and Brown Out Reset
- Real-Time Clock
- JTAG/SWD Debug Interface

**Operating Parameters**

- 1.75 V to 4.8 V Primary Supply Range
- 1.08 V to 1.98 V I/O Supply Range (1.8 V I/O)
- 3.0 V to 4.0 V I/O Supply Range (3.3 V Flex I/O)
- -40 °C to 75 °C Ambient Temperature Range
- -40 °C to 105 °C Junction Temperature Range

**Packages**

- WLCSP216, 0.4 mm Pitch
- FBGA194, 0.5 mm Pitch



WLCSP

FBGA

|                                                                |           |                                                |           |
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## **1 Preface**

This document contains fundamental technical information for the Alif Semiconductor E8 series devices.

Device information herein includes features description, electrical and mechanical characteristics with specifications, and ordering information.

There are references to third-party technical documents as noted within this document.

For more information on processors, peripheral functions, and programming settings, refer to the corresponding device series-specific Hardware Reference Manual.

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the [Alif Conductor](#) tool.

## 2 Device Overview

### 2.1 Device Description

The families of fusion processors and microcontrollers (MCUs) from Alif Semiconductor create a scalable and compatible continuum of highly integrated embedded processor devices for use in low-end to high-end intelligent IoT end-point applications. Architected for power efficiency and long battery life, these devices deliver high computation and ML/AI capability, multi-layered security, computer vision, and highly interactive human-machine interface.

Individual device selections within a family of devices scale up starting with single-core MCUs, dual-core MCUs, triple-core MCU/MPU fusion processors, and quad-core MCU/MPU fusion processors to match specific applications. Across all devices are common peripherals, common power management schemes, and a common interconnection fabric making it easy to re-use software and hardware over many varied projects.

This document covers the second-generation quad-core embedded fusion processors from the Ensemble™ family, designated as the E8 series.

**Power efficiency**—In addition to the use of FD-SOI silicon process technology, *aiPM* provides fine granular control over the processing, memory, and peripheral resources of the device, resulting in extreme power conservation that consumes only what is needed, when its needed, at any given instant based on use case.

**Computation and ML/AI**—Quad-core design with two Arm Cortex-A32 application cores, and two Arm Cortex-M55 Real-Time cores, with one of the Real-Time cores optimized for extreme low power operation. Machine Learning and AI tasks are accelerated by triple Arm Ethos neural processing units, generating as much as 454 GOPS in total. One NPU is the Ethos-U85 that enables RNN, CNN, and TNN transformer-based ML models for generative AI. The other two NPUs are Ethos-U55 for RNN and CNN ML models. E8 devices can operate with an RTOS, an OS such as Linux, or both, while using only the on-chip memory resources. Additional RAM and Flash memory may be accessed externally through two high-speed 16-bit Hex SPI interfaces supporting XIP mode and HyperBus protocol. An in-line AES decryption module in each Hex SPI interface ensures the confidentiality of the data and/or code stored in the external memory devices.

**Connectivity**—E8 devices support many wired interfaces including Ethernet, USB, SDIO, CANFD, I3C, I2C, and more.

**Security**—An isolated Secure Enclave manages the entire life cycle of the end application from manufacture, to deployment, to secure Firmware Over-The-Air updates, and to retirement. A unique Root-of-Trust existing in the enclave enables a trusted on-chip platform for key generation, secure storage, secure boot, cryptographic acceleration, and more. The Secure Enclave also enables certificate-based secure debugging.

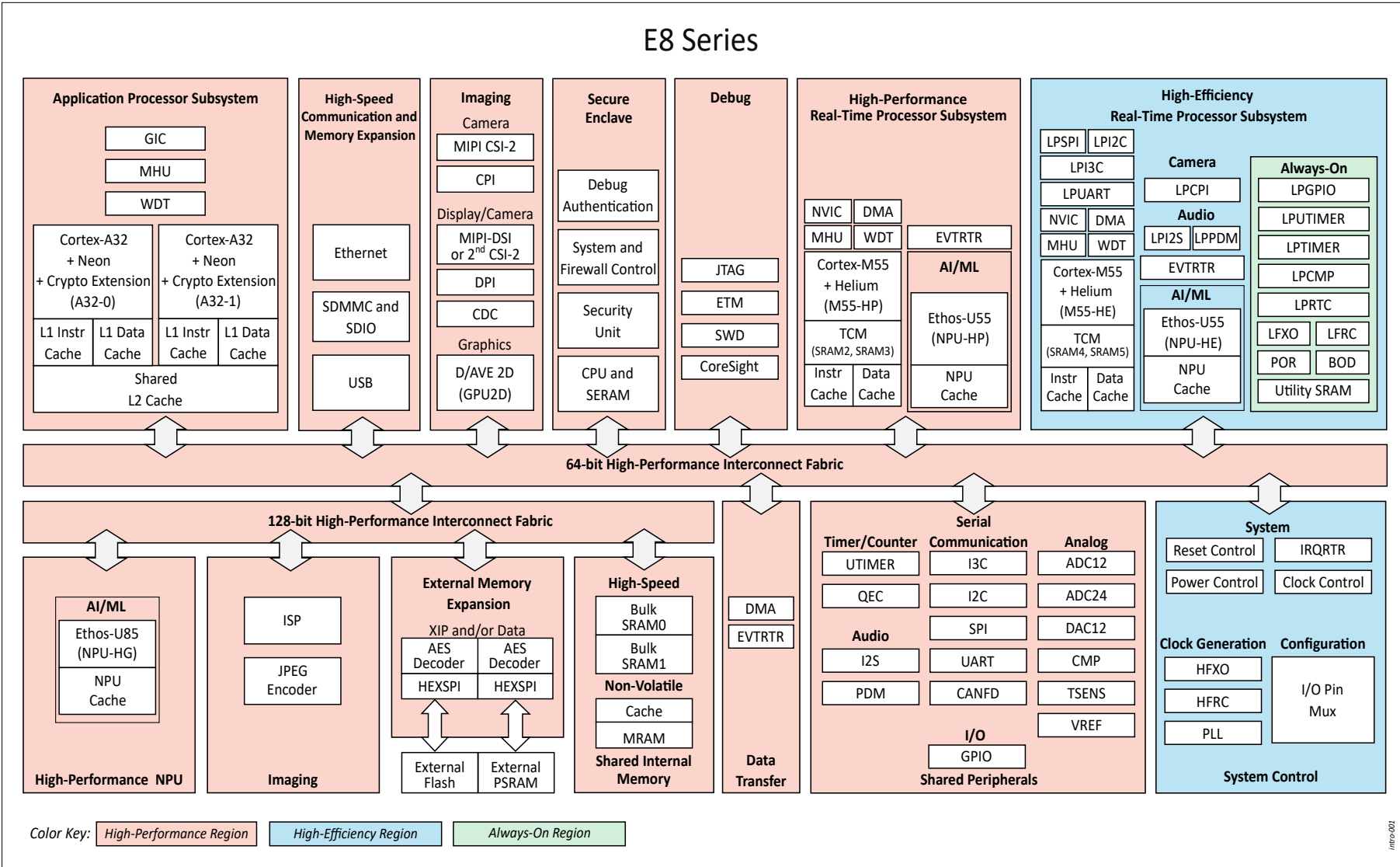
**Computer Vision**—Integrated camera interfaces, including one or two MIPI CSI-2 with hardware Image Signal Processing (ISP) and JPEG compression, enable easy connection of low-power image sensors for AI image classification using the Arm Ethos NPUs. Biometric ID, face detection, object classification, barcode reading, and other vision applications can execute while consuming very little energy.

**Human Machine Interface**—Integrated color display interfaces, including MIPI DSI, can drive a wide range of display panels with vivid graphics supported by the on-chip 2D graphics processing unit for attractive user interfaces. Digital audio inputs and outputs are supported by PDM and I2S interfaces. The Arm Ethos NPUs can apply ML inference to audio input streams for key word spotting, contextual-aware speech recognition, failure prediction, and more.

## 2.2 Device Block Diagram

Figure 2-1 presents a simplified diagram of the operating regions and main internal components of the Alif Semiconductor E8 Series of devices.

Figure 2-1 Device Block Diagram



## 2.3 Device Features Summary and Comparison

Table 2-1 presents device features supported and package options.

**Table 2-1 Device Features and Peripherals**

| Feature                                 |                         | Definition                                                   |
|-----------------------------------------|-------------------------|--------------------------------------------------------------|
| Package options                         |                         | WLCSP216, FBGA194                                            |
| <b>Processors and Accelerators</b>      |                         |                                                              |
| Dual Arm Cortex-A32                     | A32-0                   | Up to 800 MHz                                                |
|                                         | A32-1                   |                                                              |
| High-Performance Arm Cortex-M55         | M55-HP                  | Up to 400 MHz                                                |
| High-Efficiency Arm Cortex-M55          | M55-HE                  | Up to 160 MHz                                                |
| Arm Ethos-U55 Neural Processing Units   | NPU-HP                  | Up to 204 GOPS                                               |
|                                         | NPU-HE                  | Up to 46 GOPS                                                |
| Arm Ethos-U85 Neural Processing Unit    | NPU-HG                  | Up to 204 GOPS                                               |
| D/AVE 2D Graphics Processing Unit       | GPU2D                   | Yes                                                          |
| <b>Security Subsystem</b>               |                         |                                                              |
| Secure Enclave                          | SE                      | Yes                                                          |
| <b>Memory</b>                           |                         |                                                              |
| On-Chip Non-volatile Application Memory | MRAM                    | 5.5MB                                                        |
| On-Chip Application SRAM                | SRAM                    | 9.75MB                                                       |
| <b>Timers and Counters</b>              |                         |                                                              |
| Low-Power Timer                         | LPTIMER <sup>(2)</sup>  | 4 × 32-bit                                                   |
| Universal Timer                         | UTIMER                  | 12 × 32-bit                                                  |
|                                         | LPUTIMER <sup>(2)</sup> | 3 × 32-bit                                                   |
| Watchdog Timer                          | WDT                     | 4                                                            |
| Quadrature Encoder Counter              | QEC                     | 4                                                            |
| Low-Power Real-Time Counter             | LPRTC <sup>(2)</sup>    | 1                                                            |
| <b>General Input and Output</b>         |                         |                                                              |
| General Purpose I/O pins                | GPIO                    | Optional <sup>(3)</sup><br>132 (1.8 V)<br>4 (1.8 V or 3.3 V) |
| Low-Power General Purpose I/O pins      | LPGPIO <sup>(2)</sup>   | 4 (1.8 V)<br>4 (1.8 V or 3.3 V)                              |
| <b>Communication Peripherals</b>        |                         |                                                              |
| Controller Area Network                 | CANFD                   | 1                                                            |
| Ethernet 10/100 Controller              | ETH                     | 1                                                            |
| Inter-Integrated Circuit                | I2C                     | 4                                                            |
|                                         | LPI2C <sup>(2)</sup>    | 2                                                            |
| Inter-IC Sound                          | I2S                     | 4                                                            |
|                                         | LPI2S <sup>(2)</sup>    | 1                                                            |

| Feature                                     |                       | Definition                                  |
|---------------------------------------------|-----------------------|---------------------------------------------|
| MIPI Improved Inter-Integrated Circuit      | I3C                   | 1                                           |
|                                             | LPI3C <sup>(2)</sup>  | 1                                           |
| Pulse Density Modulation                    | PDM                   | 4× 2-channel                                |
|                                             | LPPDM <sup>(2)</sup>  | 4× 2-channel                                |
| Serial Peripheral Interface                 | SPI                   | 4                                           |
|                                             | LPSPi <sup>(2)</sup>  | 1                                           |
| Universal Asynchronous Receiver/Transmitter | UART                  | 8                                           |
|                                             | LPUART <sup>(2)</sup> | 1                                           |
| Universal Serial Bus                        | USB                   | USB 2.0 HS/FS Host/Device                   |
| Secure Digital Input Output                 | SDIO                  | SDIO v4.1 <sup>(1)</sup>                    |
| <b>External Memory Interfaces</b>           |                       |                                             |
| Hex SPI                                     | HEXSPI                | 2                                           |
| Secure Digital Multimedia Card              | SDMMC                 | SD v4.2, eMMC v5.1 <sup>(1)</sup>           |
| <b>Camera Subsystem</b>                     |                       |                                             |
| Camera Parallel Interface                   | CPI                   | Up to 16-bit                                |
|                                             | LPCPI <sup>(2)</sup>  | Up to 8-bit                                 |
| MIPI Camera Serial Interface 2              | CSI                   | 2-Lane                                      |
| <b>Display Subsystem</b>                    |                       |                                             |
| Graphics LCD Controller                     | CDC                   | 1                                           |
| Display Parallel Interface                  | DPI                   | Up to 24-bit RGB                            |
| MIPI Display Serial Interface               | DSI                   | 2-Lane                                      |
| <b>Imaging Subsystem</b>                    |                       |                                             |
| Image Signal Processor                      | ISP                   | Yes                                         |
| JPEG Encoder                                | JPEG                  | Yes                                         |
| <b>Analog Peripherals</b>                   |                       |                                             |
| Analog-to-Digital Converter                 | ADC12                 | 3 × 12-bit<br>(Up to 18 inputs)             |
|                                             | ADC24                 | 1 × 24-bit<br>(Up to 4 differential inputs) |
| Digital-to-Analog Converter                 | DAC12                 | 2 × 12-bit                                  |
| High-Speed Comparator                       | CMP                   | 4<br>(16 inputs)                            |
| Low Power Comparator                        | LPCMP <sup>(2)</sup>  | 1<br>(4 inputs)                             |
| Temperature Sensor                          | TSENS                 | Yes                                         |

1. SDIO, SD, and eMMC are functions of memory card controller. There is only one memory card controller in the device.
2. All Low Power (LP) peripherals are single-master accessible. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.
3. For devices supporting optional features, see [Section 7 Ordering Information](#).

## 3 Functional Overview

### 3.1 Application Processor

#### 3.1.1 A32 Overview

The Arm Cortex-A32 processor is a very efficient, low-power, 32-bit processor. The pair of A32 cores in this device is used for application processing and resides in the Application Processor Subsystem (APSS). The APSS also includes various memories and peripherals.

The A32 processor supports the following main features:

- Dual-core configuration:
  - Symmetric Multi-Processing (SMP) within the processor cluster
  - CPU core revision: r1p0
- Full compliance with the Armv8 architecture:
  - A32 instruction set
  - T32 instruction set
  - AArch32 execution state:
    - Supports all exception levels (EL0 to EL3)
    - Provides full compatibility with Armv7
- Arm TrustZone security technology
- Arm Neon Advanced SIMD and floating-point architecture
- Cryptographic extension
- 8-stage, in-order pipeline with direct and indirect branch prediction
- Level 1 (L1) memory system that supports separate data and instruction sides:
  - 32KB L1 instruction cache
  - 32KB L1 data cache
  - Memory Management Unit (MMU)
- Level 2 (L2) memory system that provides cluster memory coherency:
  - 512KB shared L2 cache:
    - L2 data RAM input latency: 1 cycle
    - L2 data RAM output latency: 2 cycles
  - Snoop Control Unit (SCU)
  - Accelerator Coherency Port (ACP)
- Debug and trace support:
  - Armv8 debug logic
  - Arm CoreSight™ SoC-400 components
  - Performance Monitoring Unit (PMU)
  - Trace infrastructure
  - Debug memory map (v7)
- Arm AMBA® 4 AXI as the main bus interface
- Generic Interrupt Controller (GIC) CPU interface to connect to an external distributor (GIC-400)

### 3.2 Real-Time Processor

#### 3.2.1 M55-HP Overview

The Cortex-M55 High-Performance (M55-HP) processor implements the Armv8.1-M Mainline architecture that includes support for the M-profile Vector Extension (MVE), also known as Helium™. The M55-HP

achieves high compute performance across scalar and vector operations, operating up to 400 MHz.

The device includes a single M55-HP processor that resides in the High-Performance Real-Time Subsystem (RTSS-HP). The RTSS-HP also includes various memories and peripherals.

The M55-HP processor supports the following main features:

- CPU revision: r1p0
- CPU core logic that includes:
  - In-order, four-stage integer pipeline with early completion of common arithmetic instructions
  - Instruction Fetch Unit (IFU) with 32-bit instruction fetch data width
  - Data Processing Unit (DPU) with 64-bit load/store data width
  - Support for up to  $2 \times 32$ -bit vector load operations in parallel
- Extension Processing Unit (EPU) that works closely with the CPU core to support:
  - Scalar floating-point (VFPv5) operations: half-, single-, and double-precision
  - Vectored operations through MVE (Helium):
    - Integer
    - 128-bit SIMD floating-point: half- and single-precision
- Double-Precision FPU
- Support for other Extensions such as:
  - Armv8.1-M Main Extension (16-bit and 32-bit Thumb® instruction set)
  - Armv8-M Security Extension (TrustZone)
  - DSP Extension
  - DSP Debug Extension
  - Reliability, Availability, and Serviceability (RAS) Extension
  - Unprivileged Debug Extension (UDE)
- Memory architecture that includes:
  - Memory Authentication Unit (MAU) for memory access control:
    - Secure Memory Protection Unit (MPU) supporting 16 regions
    - Non-secure MPU supporting 16 regions
    - Security Attribution Unit (SAU) supporting 8 regions
    - TCM Gate Units (TGU):
      - Instruction TGU (ITGU) protecting 16 address regions, each 16KB in size
      - Data TGU (DTGU) protecting 64 address regions, each 16KB in size
  - Memory system:
    - 32KB L1 Instruction Cache (IRAM)
    - 32KB L1 Data Cache (DRAM)
    - 256KB Instruction TCM (ITCM); access to ITCM is over a single interface
    - 1024KB Data TCM (DTCM); access to DTCM is over four interfaces
    - Master AXI (M-AXI) interface for high latency memory or peripheral access
- Interrupt control:
  - Nested Vectored Interrupt Controller (NVIC) for low-latency interrupt processing:
    - Supports 480 external interrupts, with 256 priority levels per interrupt
  - Wakeup interrupt control to allow the processor to enter low-power state:
    - Internal Wakeup Interrupt Controller (IWIC)
    - External Wakeup Interrupt Controller (EWIC)
- Secure and non-secure Vector Table Offset Register (VTOR)

- Debug and trace support:
  - Full set debug:
    - Breakpoint Unit (BPU) with 8 comparators
    - Data Watchpoint and Trace (DWT) unit with 4 comparators and Performance Monitoring Unit (PMU)
  - Trace infrastructure
  - CoreSight-compliant Debug Access Port (DAP):
    - Supports dynamic switching—Serial Wire / JTAG Debug Port (SWJ-DP)

### 3.2.2 M55-HE Overview

The Cortex-M55 High-Efficiency (M55-HE) processor implements the Armv8.1-M Mainline architecture that includes support for the M-profile Vector Extension (MVE), also known as Helium™. The M55-HE achieves high compute efficiency across scalar and vector operations, operating up to 160 MHz.

The M55-HE memories are based on ultra-low leakage memory cells which results in low power consumption in sleep mode. The choice of TCM retention allows application-optimized tradeoff between current leakage during sleep and fast wake-up time.

The device includes a single M55-HE processor that resides in the High-Efficiency Real-Time Subsystem (RTSS-HE). The RTSS-HE also includes various memories and peripherals.

The M55-HE processor supports the following main features:

- CPU revision: r1p0
- CPU core logic that includes:
  - In-order, four-stage integer pipeline with early completion of common arithmetic instructions
  - Instruction Fetch Unit (IFU) with 32-bit instruction fetch data width
  - Data Processing Unit (DPU) with 64-bit load/store data width
  - Support for up to  $2 \times 32$ -bit vector load operations in parallel
- Extension Processing Unit (EPU) that works closely with the CPU core to support:
  - Scalar floating-point (VFPv5) operations: half-, single-, and double-precision
  - Vectored operations through MVE (Helium)
    - Integer
    - 128-bit SIMD floating-point: half- and single-precision
- Double-Precision FPU
- Support for other Extensions such as:
  - Armv8.1-M Main Extension (16-bit and 32-bit Thumb instruction set)
  - Armv8-M Security Extension (TrustZone)
  - DSP Extension
  - DSP Debug Extension
  - Reliability, Availability, and Serviceability (RAS) Extension
  - Unprivileged Debug Extension (UDE)
- Memory architecture that includes:
  - Memory Authentication Unit (MAU) for memory access control:
    - Secure Memory Protection Unit (MPU) supporting 16 regions
    - Non-secure MPU supporting 16 regions
    - Security Attribution Unit (SAU) supporting 8 regions
  - TCM Gate Units (TGU):
    - Instruction TGU (ITGU) protecting 16 address regions, each 16KB in size
    - Data TGU (DTGU) protecting 16 address regions, each 16KB in size

- Memory system:
  - 32KB L1 Instruction Cache (IRAM)
  - 32KB L1 Data Cache (DRAM)
  - 256KB Instruction TCM (ITCM); access to ITCM is over a single interface
  - 256KB Data TCM (DTCM); access to DTCM is over four interfaces
  - Master AXI (M-AXI) interface for high latency memory or peripheral access
- Interrupt control:
  - Nested Vectored Interrupt Controller (NVIC) for low-latency interrupt processing:
    - Supports 480 external interrupts, with 256 priority levels per interrupt
  - Wakeup interrupt control to allow the processor to enter low-power state:
    - Internal Wakeup Interrupt Controller (IWIC)
    - External Wakeup Interrupt Controller (EWIC)
- Secure and non-secure Vector Table Offset Register (VTOR)
- Debug and trace support:
  - Full set debug:
    - Breakpoint Unit (BPU) with 8 comparators
    - Data Watchpoint and Trace (DWT) unit with 4 comparators and Performance Monitoring Unit (PMU)
  - Trace infrastructure
  - CoreSight-compliant Debug Access Port (DAP):
    - Supports dynamic switching—Serial Wire / JTAG Debug Port (SWJ-DP)

### 3.3 Neural Processing Unit (NPU)

The Neural Processing Unit (NPU) is a Machine Learning (ML) coprocessor that improves the inference performance of neural networks (NN). The device includes:

- One Arm Ethos-U55 NPU coprocessor dedicated to the M55-HP CPU—NPU-HP
- One Arm Ethos-U55 NPU coprocessor dedicated to the M55-HE CPU—NPU-HE
- One Arm Ethos-U85 NPU coprocessor for general usage—NPU-HG

The Arm Ethos-U55 NPU targets 8-bit and 16-bit integer quantized Convolutional Neural Networks (CNN) and Recurrent Neural Networks (RNN). In addition to CNN and RNN, the Arm Ethos-U85 NPU offers support for transformer-based models (Transformer Neural Networks—TNN) for generative AI applications. The Ethos-U85 NPU also provides more energy efficiency than previous Ethos-U generations and enables higher performance edge AI use cases.

Each NPU includes a Direct Memory Access (DMA) controller that can read and write to external memory. The DMA controller reads the neural network description and transfers the input and output feature maps.

#### 3.3.1 NPU-HP Overview

The NPU-HP supports the following main features:

- Up to 204 GOPS performance using up to 256 MAC/cycle
- Network support: CNN, RNN
- On-the-fly weight decompression (8-bit weights)
- 8-bit and 16-bit activations (input data)
- Activation functions:
  - ReLU, ReLU1, ReLU6, and Leaky ReLU (LReLU)
  - Tanh
  - Sigmoid

- Configurable Look-Up Table (LUT)
- None or bypass
- Element-wise operations:
  - Element-wise ADD and SUB
  - Element-wise Multiplication (MUL)
  - Element-wise Min and Max
  - Element-wise ABS
  - Element-wise Shift Left (SHL) and Shift Right (SHR)
  - Element-wise Count-Leading Zero (CLZ)
- 48KB of internal shared cache memory (SHRAM)
- Integrated DMA controller
- Layer-by-layer visibility with Performance Monitoring Units (PMUs)

### 3.3.2 NPU-HE Overview

The NPU-HE supports the following main features:

- Up to 46 GOPS performance using up to 128 MAC/cycle
- Network support: CNN, RNN
- On-the-fly weight decompression (8-bit weights)
- 8-bit and 16-bit activations (input data)
- Activation functions:
  - ReLU, ReLU1, ReLU6, and Leaky ReLU (LReLU)
  - Tanh
  - Sigmoid
  - Configurable Look-Up Table (LUT)
  - None or bypass
- Element-wise operations:
  - Element-wise ADD and SUB
  - Element-wise Multiplication (MUL)
  - Element-wise Min and Max
  - Element-wise ABS
  - Element-wise Shift Left (SHL) and Shift Right (SHR)
  - Element-wise Count-Leading Zero (CLZ)
- 24KB of internal shared cache memory (SHRAM)
- Integrated DMA controller
- Layer-by-layer visibility with Performance Monitoring Units (PMUs)

### 3.3.3 NPU-HG Overview

The NPU-HG supports the following main features:

- Up to 204 GOPS performance using up to 256 MAC/cycle
- Network support: TNN, CNN, and RNN, capable of generative AI
- On-the-fly weight decompression (8-bit weights)
- 8-bit and 16-bit activations (input data)
- Activation functions:
  - ReLU
  - Leaky ReLU (LReLU)
  - Programmable Look-Up Table (LUT) as a generic activation function
- 48KB of internal shared cache memory (SHRAM) plus 4KB of specialized SRAM

- Integrated DMA controller
  - One 128-bit AMBA 5 AXI interface (AXI\_EXT) for DMA access to off-chip memory
  - Two 128-bit AMBA 5 AXI interfaces (AXI\_SRAM0/1) for DMA access to on-chip SRAM
- Layer-by-layer visibility with Performance Monitoring Units (PMUs)

### 3.4 2D-Graphics Accelerator (GPU)

The D/AVE 2D Graphics Processing Unit (GPU2D) provides hardware acceleration for sophisticated vector-based graphical applications.

The device includes one GPU2D module.

The GPU2D supports the following main features:

- Subpixel accurate rendering
- Resolutions of up to 2048 × 2048 pixels
- Operating clock frequency at 400 MHz. GPU render pipeline produces one pixel per clock cycle.
- 16 blending modes
- Patterns and gradients with alpha channel on all primitives
- Render to texture
- Textures up to 2048 × 1024 pixels
- Texture blending
- Bilinear filtering
- Graphical primitives available:
  - Block Image Transfers (BLIT)—direct and stretch
  - Box
  - Circle—filled or empty (ring)
  - Convex polygon
  - Line
    - Supported caps:
      - Butt
      - Round
      - Square
    - Supported line joins:
      - Bevel
      - Miter
      - Round
    - Supporting different start and end widths
  - Quad
  - Triangle
  - Triangle fan
  - Triangle list
  - Triangle stripe
  - Wedge-filled or empty
- Graphical primitives attributes:
  - Anti-aliasing
  - Blend modes
  - Color
  - Edge blur
  - Linear alpha gradient
  - Pattern

- Texture
  - U/V clamp, repeat support
  - No-, linear-, bilinear-filtering support
  - Run-Length Encoding (RLE)
- Supported color coding formats:
  - Input
    - ARGB8888, RGB565, ARGB4444, ARGB1555, ALPHA8, AI44, RGBA8888, RGBA4444, RGBA5551, I8, I4, I2, I1, ALPHA4, ALPHA2, ALPHA1
  - Output
    - ARGB8888, RGB565, ARGB4444, ALPHA8, RGBA8888, RGBA4444

## 3.5 Secure Enclave Subsystem (SESS)

### 3.5.1 Security Architecture Overview

The device contains an advanced Secure Enclave (SE) that is responsible for managing the device security. The SE is an isolated subsystem with its own dedicated resources. The isolated subsystem reduces the attack surface for the SE along with the minimal software interfaces that are restricted to the Inter-Process Communication (IPC) Message Handling Units (MHUs).

The SE boots first on Power-On-Reset (cold start). It runs the First Stage bootloader code from a private, immutable ROM. The SE performs certificate-based integrity and authenticity check on the Second Stage bootloader. It is loaded to the SE SRAM (SERAM) and the flow of execution is transferred to it. This mechanism enables the secure update of the Second Stage bootloader on the field. The boot process continues with processing of the application-specific device configuration. The SE applies configuration settings that partition the system resources (memory and peripherals) between the different application cores. Next, the SE bootloader performs a signature verification of the installed application binaries. If needed, it copies the specified binaries to their designated SRAM regions. Finally, a designated core is released from Reset to run its application. This completes the secure boot procedure. The remaining cores can be booted by the SE in response to a service request.

The SE is also involved in the process of waking up from STOP mode. When a wakeup event is triggered, the SE CPU boots first. It checks if the SERAM is retained and continues the execution flow there. The SERAM code maps the wakeup event to an application core and promptly boots it. If the SERAM is not retained, then the SE validates the wakeup source and boots the RTSS-HE core. The retention of SERAM in the Secure Enclave or the SRAM (M55-HE TCM) in the RTSS-HE offers trade-off options between the leakage current and the wakeup time of the device.

The SE provides traditional security functions such as:

- Secure boot
- Secure device configuration
- HW Root-of-Trust (RoT)
- Key management
- Signature validation
- Crypto operations
- Life cycle management

The Supervisor is responsible to:

- Manage the OEM provisioning process and the Life Cycle State (LCS)
- Apply the system configuration settings to the security firewalls and security HW in the system

- Securely boot the Application core (A32) / Real-time cores (M55-HP and M55-HE) as defined by the user's configuration file

### 3.5.2 Cryptographic Services

The Secure Enclave (SE) supports a variety of Runtime Security and Cryptographic services that enable the OEM's application code to control security functions for the device and request cryptographic operations. These runtime services make use of IPC.

The Runtime Cryptographic services include the ability of the OEM application code to make requests for standard and device-specific cryptographic operations like:

- Creating keys
- Using the keys to encrypt or decrypt
- Return the device certificate
- Authenticate the device
- Validate the signature of images against the provisioned keys in the device
- Secure boot a core
- Write to MRAM memory
- Process Alif Semiconductor's firmware updates

## 3.6 Interconnect

The system interconnect provides the means of connecting bus masters (CPU cores, DMA controllers) to memory modules and peripherals. It is based on the Arm AMBA bus architecture utilizing a mix of AXI, AHB and APB buses.

The backbone of the device interconnect is based on an AXI4 bus, featuring multiple master and slave ports. The processing subsystems have their own local buses connected as masters to the main AXI bus. The memory blocks and the peripheral subsystems connect as slaves to the main AXI bus. Some peripherals (such as ETH, SDMMC, and USB) also can act as bus masters and connect via both master and slave ports. The master ports serve their DMA controllers to transfer data without CPU intervention, while the slave ports are intended for accessing their registers.

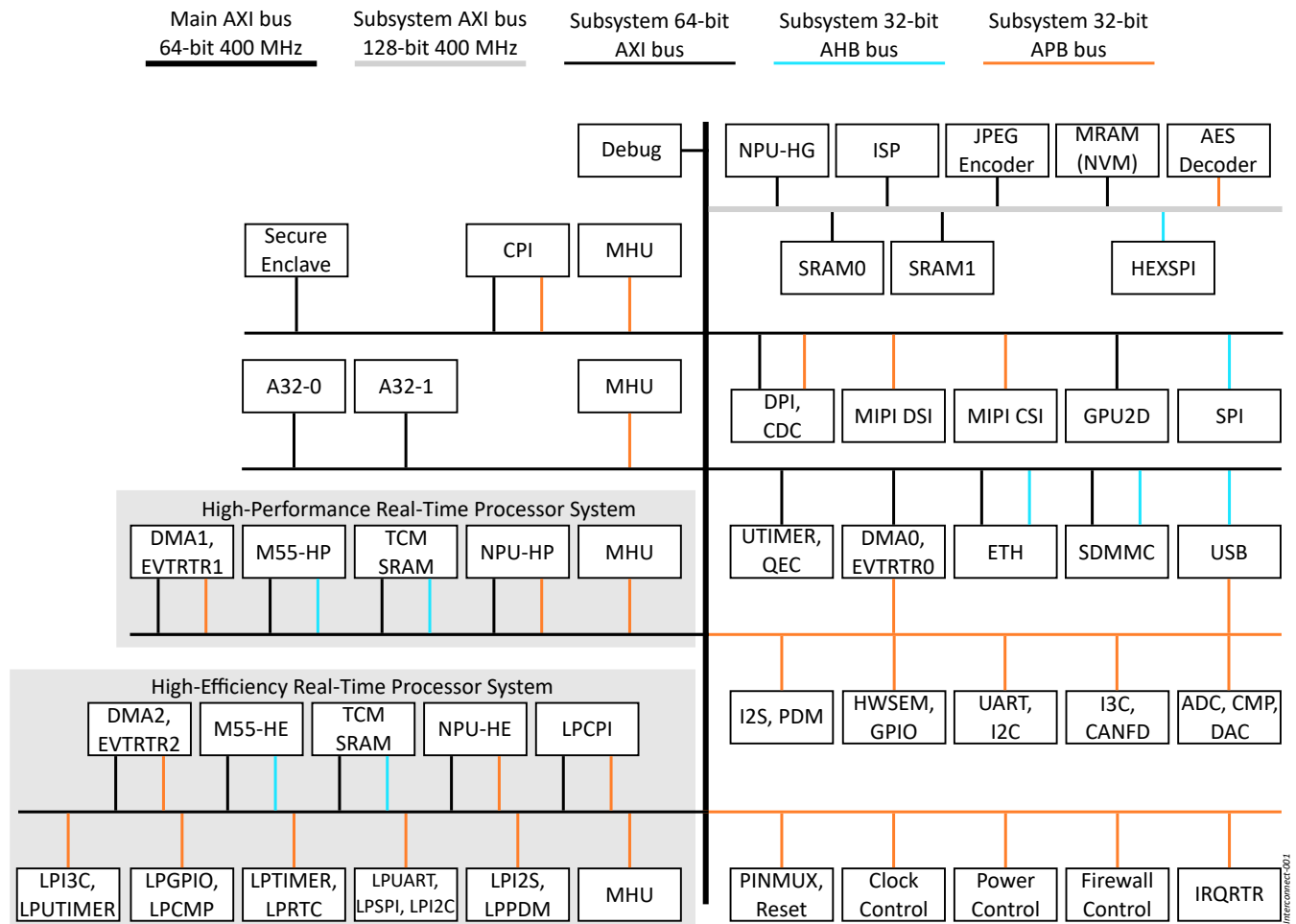
Each master and slave port connects to the main AXI bus through Firewall Components (FC). They enforce run-time configurable access rights policy and address translation. Transaction gating is based on master ID, transaction type (instruction or data fetch) and TrustZone-defined secure world context. The FC configuration settings are set by the SE during the secure boot process. The applications specify their desired access paths and address regions in a dedicated region of the on-chip Non-Volatile Memory (NVM), which is MRAM. The SE applies these settings during the device boot process.

The device interconnect supports the following main features:

- High-performance AXI4 bus protocol
- 64-bit and 128-bit wide read and write data paths
- 400 MHz bus clock frequency
- Burst-based transactions for optimizing bandwidth efficiency
- TrustZone aware
- Firewall controller and 14 firewall components to enforce secure policy constraining the bus master's access to the device resources
- Firewall security monitoring function raising an interrupt when unauthorized access is attempted

Figure 3-1 provides a high-level overview of the system interconnect implementation in the device.

**Figure 3-1 Interconnect Overview**



**NOTE**

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the [Alif Conductor](#) tool.

## 3.7 Power Supply Management

The device has three operating regions that encapsulate top-level functions from a power consumption perspective:

- **Always-On (AON) Region**—a group of rudimentary functions that are always powered when a constant power source is connected to the VDD\_BATT pin.
- **High-Efficiency (HE) Region**—a group of compute, sensing, AI functions designed to operate at the highest efficiency. Many tasks can be performed in this region to conserve power and/or extend battery life before waking up the HP Region.
- **High-Performance (HP) Region**—a group of compute, AI, Human-Machine Interface (HMI), and high-speed connectivity functions designed to operate at maximum performance. These functions are invoked only as required to conserve energy.

The device block diagram (see [Figure 2-1](#)) illustrates these three operating regions and the functions available within each of the regions.

A smart power management scheme named *aiPM* (autonomous intelligent Power Management) utilizes a hierarchy of multiple power domains, multiple internal voltage supplies, and multiple power modes to power on, in fine granularity, portions of the device only when they are needed based on use case, and off when not needed. Powering on and off portions of the device occurs automatically in hardware as required, but the power management policies are configured by software.

**Multiple power domains**—There are eight independent power domains in the device, each one with a dedicated power controller that is coordinated by digital logic and software configuration for automatic transitions—from power-up to full GO mode, and all modes in between. This scheme achieves optimum power efficiency based on the dynamic power demand of the device at any given moment in time.

**Multiple voltage supplies**—There are internal device voltage supplies consisting of a series of Low Drop-Out (LDO) regulators and a dual-mode DC-to-DC buck converter (DC-DC) to generate 0.55 V, 0.8 V, and 1.8 V internal voltage rails that are automatically switched on and off as required for optimum performance and efficiency.

**Multiple power modes**—Below are top-level device modes listed from highest to lowest power consumption:

- GO—any or all processing cores operate up to their max frequency
- READY—all processing cores are clock gated off, but peripherals can run
- IDLE—all processing cores are powered off, but some peripherals can run
- STANDBY—all processing cores are powered off, but a few low-power peripherals can run
- STOP—entire device is powered off except the AON Region where rudimentary low-power peripherals and wake-up sources are active, as well as optional retained SRAM blocks

### 3.7.1 Power Domains

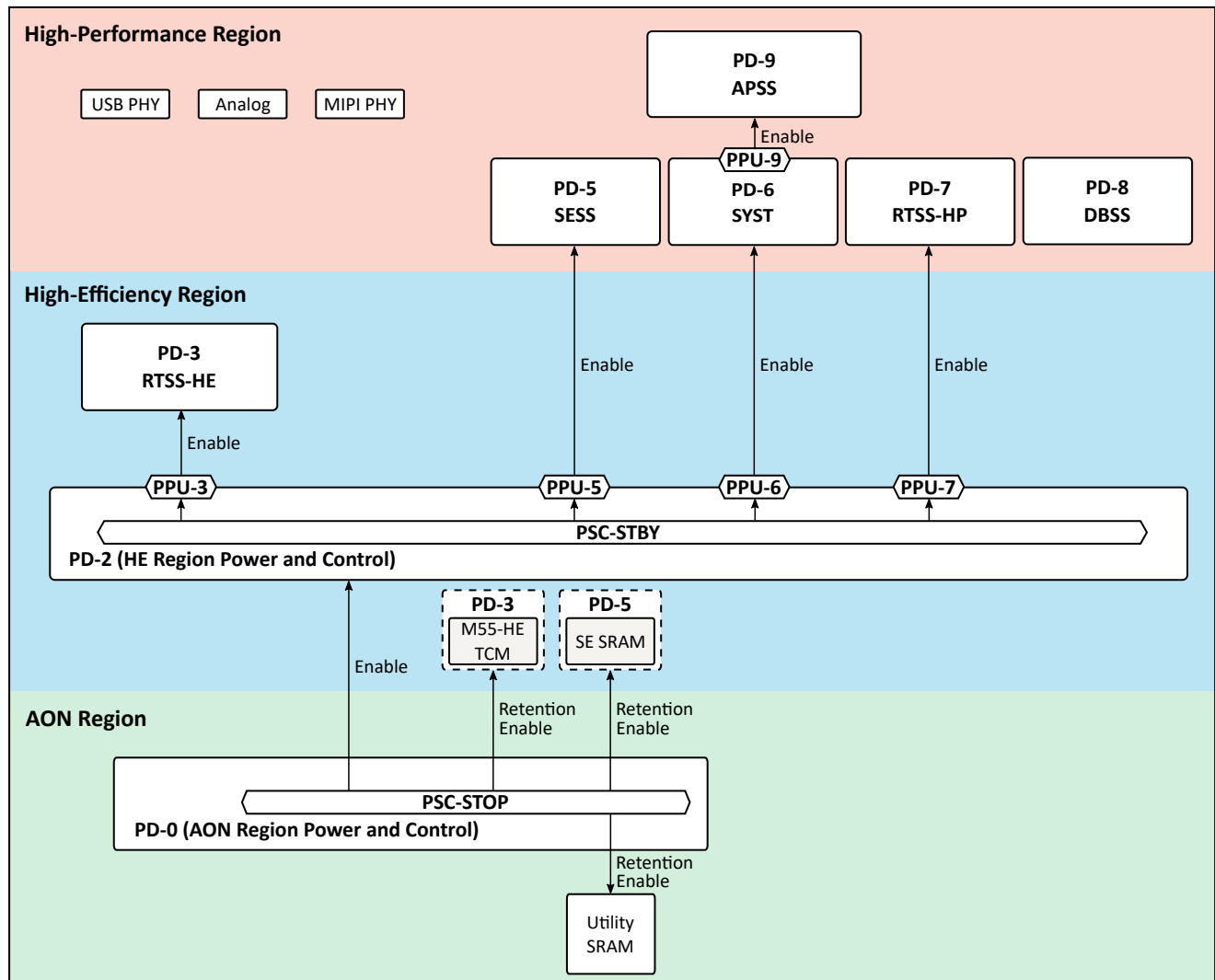
The device Power Domains (PD) are managed by a Power Sequence Controller (PSC) and several Power Policy Units (PPU). The PSC is a state machine that monitors a fixed set of inputs and automatically acts to turn power on or off in power domains at the lower levels. PPUs take inputs from the PSC, inputs from the device condition status, and inputs from configuration settings from the application code, then PPUs act autonomously to turn on or off power to the domains, and PPUs also control domain clock sources. Thus, the operational processes of the PSC and PPUs automatically and dynamically achieve the best power consumption based on instantaneous power demand.

Figure 3-2 illustrates the power domains, control hierarchy, transition possibilities, and relevance to the three operating regions of the device. The power-up sequence of the shown regions and domains is:

1. If VDD\_BATT is connected to a constant voltage source, the PD-0 domain and the AON Region are Always-On.
2. The PD-2 domain is first to power up.
3. The next order of powering up the domains depends on whether the device executes an initial boot (cold), or a wake up (warm).

PDs in each of the three device regions are defined as follows:

- AON Region
  - PD-0, AON power and control
- HE Region
  - PD-2, High Efficiency Region power and control
  - PD-3, Real Time Subsystem-High Efficiency (RTSS-HE)
- HP Region
  - PD-5, Secure Enclave Subsystem (SESS)
  - PD-6, Shared Peripherals / Shared System Resources (SYST)
  - PD-7, Real Time Subsystem-High Performance (RTSS-HP)
  - PD-8, Debug Subsystem (DBSS)
  - PD-9, Application Processor Subsystem (APSS)

**Figure 3-2 Device Power Domain Hierarchy and Transitions**


For more details about PDs power-up and transitions, see the device series-specific Hardware Reference Manual.

[Table 3-1](#) illustrates which specific resources are available within each of the power domains, and how the power domains are related to the three operational regions.

Table 3-1 Device Resources per Power Domain

| AON Region                                                                                                                                                                                                                                                                                         | High-Efficiency Region                                                                                                                                                                       |                                                                                                                                                                                                     | High-Performance Region                                                 |                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                      |      |                                                                          |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------------------------------|------|--------------------------------------------------------------------------|
| PD-0                                                                                                                                                                                                                                                                                               | PD-2                                                                                                                                                                                         |                                                                                                                                                                                                     | PD-5                                                                    | PD-6                                                                                                                                                                                                                                                                                                                                                                                                                             | PD-7                                                                                                 | PD-8 | PD-9                                                                     |
|                                                                                                                                                                                                                                                                                                    |                                                                                                                                                                                              | PD-3                                                                                                                                                                                                |                                                                         |                                                                                                                                                                                                                                                                                                                                                                                                                                  |                                                                                                      |      |                                                                          |
| PSC-STOP<br>LPTIMER<br>LPCMP<br>LPGPIO<br>LPRTC<br>BOR_BOD<br>POR<br>VTOR<br>LFRC<br>LFXO<br>VBAT<br>ANA<br>STOP_MODE<br>LPGPIO_CTRL<br><br>Optional SRAM Retention:<br><ul style="list-style-type: none"> <li>Utility SRAM</li> <li>M55-HE TCM (SRAM4, SRAM5)</li> <li>SE SRAM (SERAM)</li> </ul> | PPU-3<br>PPU-5<br>PPU-6<br>PPU-7<br>PINMUX<br>LPUART<br>LPI2C0<br>EWIC<br>IRQRTR<br>JTAG<br>HFRC<br>HFXO<br>PLL<br>PPU-HP<br>PPU-HE<br>CGU<br>AON<br>CLKCTL_SYS<br>Host Debug<br>GPIO[16-17] | M55-HE<br>M55-HE L1 Cache<br>M55-HE TCM (SRAM4, SRAM5)<br>NPU-HE<br>LPCPI<br>LPPDM<br>LPI2S<br>LPSPI<br>LPI3C<br>LPUTIMER<br>LPI2C1<br>DMA2<br>MHU<br>WDT_HE<br>EVTSTR2<br>M55HE_CFG<br>LPGPIO_FAST | SE CPU<br>SE SRAM (SERAM)<br>Security Unit<br>System Controls<br>SEUART | PPU-9 <sup>(1)</sup><br>NPU-HG<br>ISP<br>JPEG Encoder<br>GPIO[0-14]<br>MRAM<br>Bulk SRAM (SRAM0, SRAM1)<br>DMA0<br>ETH<br>USB<br>CANFD/CAN-CNT<br>GPU2D<br>CSI<br>DSI<br>DPI/CDC<br>CPI<br>HEXSPI/AES<br>SDMMC/SDIO<br>UTIMER<br>QEC<br>I3C<br>I2C<br>SPI<br>I2S<br>PDM<br>UART<br>ADC12<br>ADC24<br>ADC_VREF<br>DAC12<br>DAC6<br>CMP<br>TSENS<br>VREF<br>HWSEM<br>EVTSTR0<br>CLKCTL_PER_MST<br>CLKCTL_PER_SLV<br>CRC<br>AXI Bus | M55-HP<br>M55-HP L1 Cache<br>M55-HP TCM (SRAM2, SRAM3)<br>NPU-HP<br>DMA1<br>MHU<br>WDT_HP<br>EVTSTR1 | SWD  | A32-0<br>A32 L1 Cache<br>A32 L2 Cache<br>GIC<br>MHU<br>WDT_APSS<br>A32-1 |

1. Only for A32 clock and reset control.

### 3.7.2 Voltage Supplies

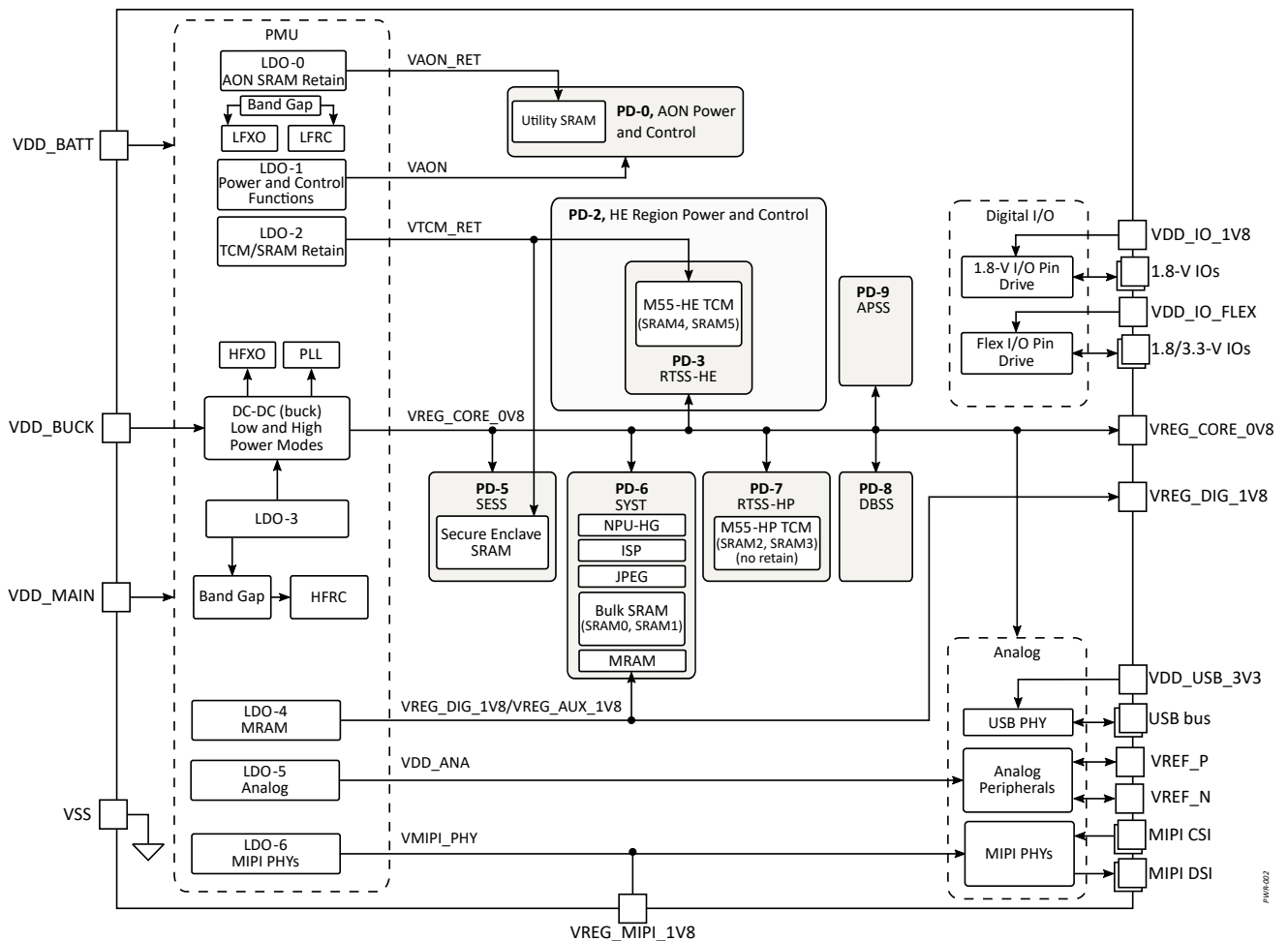
The device power domains are supplied with voltages from several internal supply sources. Power domains that feature SRAM retention have dual voltage supplies.

The device voltage supply and distribution system is architected to:

- Implement the *aiPM* strategy to dynamically power on only what is needed within the most optimum region of the device
- Minimize leakage current in STOP and STANDBY modes
- Rapidly exit low power modes upon a wake-up event
- Minimize dynamic current consumption in GO mode

Figure 3-3 illustrates the voltage distribution inside the device including highly efficient LDO regulators and a DC-DC buck converter. Very few external power sources are required because of the power management capability within the device to generate multiple voltage rails and to correctly sequence the supplies during power up and power down.

**Figure 3-3 Device Voltage Distribution**



For more information about power supply voltage ranges and general operating conditions, see [Section 5.2.1 General Operating Conditions](#).

[Table 3-2](#) presents power supply signals and provides descriptions to their functions.

Table 3-2 Power Supply Signal Descriptions

| Signal Name    | Pin Name                    | Type | Description                                                                                                                                 |
|----------------|-----------------------------|------|---------------------------------------------------------------------------------------------------------------------------------------------|
| VDD_MAIN       | VDD_MAIN <sup>(1)(5)</sup>  | PWR  | Main power supply                                                                                                                           |
| VDD_BATT       | VDD_BATT                    | PWR  | Always-On domain power input                                                                                                                |
| VDD_BUCK       | VDD_BUCK <sup>(5)</sup>     | PWR  | Internal DC-DC converter power input                                                                                                        |
| VDD_USB_3V3    | VDD_USB_3V3 <sup>(6)</sup>  | PWR  | USB power input                                                                                                                             |
| VDD_IO_FLEX    | VDD_IO_FLEX                 | PWR  | GPIO flex pads (1.8 V <sup>(2)</sup> - 3.3 V) power input                                                                                   |
| VDD_IO_1V8     | VDD_IO_1V8                  | PWR  | GPIO standard pads (1.8 V) power input                                                                                                      |
| VREG_DIG_1V8   | VREG_DIG_1V8 <sup>(3)</sup> | PWR  | Internal 1.8 V regulator output                                                                                                             |
| VREG_AUX_1V8   | VREG_AUX_1V8                | PWR  | Auxiliary 1.8 V output from internal Voltage Regulator; power supply for external components                                                |
| VREG_AUX_1_1V8 | VREG_AUX_1_1V8              | PWR  | Auxiliary 1.8 V output from internal Voltage Regulator; power supply for external components                                                |
| VREG_AUX_2_1V8 | VREG_AUX_2_1V8              | PWR  | Auxiliary 1.8 V output from internal Voltage Regulator; power supply for external components                                                |
| VDD_ANA_0V8    | VDD_ANA_0V8                 | PWR  | Analog power input<br>(must be connected to VREG_CORE_0V8)                                                                                  |
| VSS_RF         | VSS_RF                      | PWR  | Analog ground                                                                                                                               |
| VDD_MIPI_1V8   | VDD_MIPI_1V8                | PWR  | MIPI PHY power input<br>(connect to VREG_MIPI_1V8)                                                                                          |
| VREG_MIPI_1V8  | VREG_MIPI_1V8               | PWR  | Internal MIPI PHY 1.8 V power output                                                                                                        |
| VDD_CORE_0V8   | VDD_CORE_0V8                | PWR  | Main digital supply<br>(connect to VREG_CORE_0V8)                                                                                           |
| VREG_MIPI_0V8  | VREG_MIPI_0V8               | PWR  | MIPI PHY 0.8 V supply decoupling.<br>Connect to decoupling capacitors only.                                                                 |
| VREG_CORE_0V8  | VREG_CORE_0V8               | PWR  | Internal DC-DC converter power output                                                                                                       |
| VDD_SX_0V8     | VDD_SX_0V8                  | PWR  | Power supply for the HFXO, as well as the digital sections of PLL and Audio PLL<br>(connect to VREG_CORE_0V8)                               |
| VDD_PLL_0V8    | VDD_PLL_0V8                 | PWR  | Power supply to the high-frequency sections of PLL and Audio PLL, as well as the Band-Gap Reference<br>(must be connected to VREG_CORE_0V8) |
| VREG_AON       | VREG_AON <sup>(4)</sup>     | PWR  | Internal voltage supply - output of internal Always-On 0.8 V LDO regulator                                                                  |
| VREG_LP_1V8    | VREG_LP_1V8                 | PWR  | Internal voltage supply - output of internal low-power LDO regulator                                                                        |
| VREF_P         | VREF_P <sup>(8)</sup>       | A    | External positive voltage reference input to chip or output from internal reference generator. Used for ADC12, ADC24, DAC12, and DAC6.      |
| VREF_N         | VREF_N <sup>(7)</sup>       | A    | Negative voltage reference for ADC                                                                                                          |
| VSW            | VSW                         | PWR  | DC-DC converter switching output (connect to inductor)                                                                                      |
| VSS_BUCK       | VSS_BUCK                    | GND  | DC-DC converter ground                                                                                                                      |
| VSS_ANA        | VSS_ANA                     | GND  | Analog ground                                                                                                                               |
| VSS            | VSS                         | GND  | Digital ground                                                                                                                              |

1. When an external reset supervisor device is used, and VDD\_MAIN is less than 1.8 V, it is important that the supply voltage to the supervisor device does not dip during start-up and trigger the supervisor device.
2. VDD\_IO\_FLEX should be connected to VDD\_IO\_1V8 when 1.8-V mode is used.
3. VREG\_DIG\_1V8 must be bypassed to ground through a 1-μF capacitor.

4. VREG\_AON must be bypassed to ground through a 1-μF capacitor in series with a 1.0 kΩ resistor.
5. VDD\_MAIN and VDD\_BUCK must be tied together.
6. If USB function is not used, VDD\_USB\_3V3 must be tied to ground.
7. VREF\_N should be grounded.
8. VREF\_P should be bypassed to ground through 1-uF capacitor.

#### CAUTION

The decoupling for VREG\_AON and VREG\_DIG\_1V8 pins must be present on the PCB or otherwise the device may be at risk for damage.

#### NOTE

An external brownout supervisor must be connected to VDD\_MAIN/VDD\_BUCK. The brownout supervisor must assert before voltage input to the chip falls below 1.65V. Care (that is, sufficient decoupling) must be taken to ensure that supply noise/transients do not spuriously trigger resets. Refer to the Alif Application Note AAPN0036, *PCB Layout Guidelines for Ensemble E4, E6, E8 MCUs and Fusion Processors*, for more details and detailed information about power decoupling for all power pins.

For use of the device with external reference for VREF\_P or VREF\_N, please contact an Alif representative.

For more information about power supply voltage ranges and general operating conditions, see [Section 5.2.1 General Operating Conditions](#).

### 3.7.3 Power Modes

Using *aiPM*, this device provides significant flexibility to balance power, performance, and wake-up time per application use case. The device-level power modes described in [Table 3-4](#) make use of the power domains and the voltage supplies, described in [Section 5.2.1 General Operating Conditions](#), to achieve this balance. Within each power mode the clock speed and clock gating can be fine-tuned for each core and peripheral to reduce power consumption.

**Table 3-3 Individual CPU States Summary**

| CPU State          | Description                                            |
|--------------------|--------------------------------------------------------|
| RUN                | When a CPU core is running and executing code.         |
| SLEEP              | When a CPU core is clock gated and can quickly resume. |
| OFF <sup>(1)</sup> | When a CPU core is powered down.                       |

1. If RTSS-HE is powered down, then the LPI3C, LPUTIMER, LPI2C1, LPCPI, LPI2S, LPPDM, and LPSPIO/1 in the same subsystem are also powered down.

**Table 3-4 Device Power Mode Summary**

| Device Power Mode | Description                                                                         | Wake-Up Peripherals |
|-------------------|-------------------------------------------------------------------------------------|---------------------|
| GO                | One or more processing subsystems are in RUN state. See <a href="#">Table 3-3</a> . | All                 |
| READY             | All processing subsystems are in SLEEP state. See <a href="#">Table 3-3</a> .       | All                 |
| IDLE              | All processing subsystems are in OFF state. See <a href="#">Table 3-3</a> .         | All <sup>(1)</sup>  |

| Device Power Mode | Description                                                                                                                                     | Wake-Up Peripherals                        |
|-------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|
| STANDBY           | All processing subsystems and shared resources in the HP Region are powered down.                                                               | LPUART, LPI2C0, plus STOP mode peripherals |
| STOP              | All processing subsystems and shared resources in the HP and HE Regions are powered down. Few peripherals remain on with extremely low leakage. | LPTIMER, LPCMP, LPRTC, and LPGPIO          |

1. If RTSS-HE is powered down, then the LPI3C, LPUTIMER, LPI2C1, LPCPI, LPI2S, LPPDM, and LPSPIO/1 in the same subsystem are also powered down.

For more details about specific power consumption and wake-up times per power mode, see [Section 5.2.2 Device Power Modes](#).

### 3.7.4 Power Supply Supervisors

The device has integrated supervisory circuits for Brown-Out Reset (BOR), Brown-Out Detect (BOD), and Power-On-Reset (POR).

There is one POR circuit, VBAT\_POR, which monitors the VDD\_BATT (AON Region) and keeps the entire device in reset during initial power ramp to the device.

The BOD circuit monitors the VDD\_MAIN power supply and generates interrupts when the voltage falls below a programmable threshold. The BOD interrupt can be used as a wake-up source from STANDBY and from STOP low-power modes.

The BOR circuit monitors the VDD\_MAIN power supply and causes an immediate reset to the main SoC when the voltage falls below a programmable threshold.

The POR circuit is described further in [Section 3.8 Reset Management Overview](#).

[Table 3-5](#) summarizes the power supply supervisory functions.

**Table 3-5 Power Supply Supervisory Functions**

| Power Supply | Supervisor Type | Supervisory Function                                                                                                                                       |
|--------------|-----------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| VDD_BATT     | POR             | Fixed threshold, resets the entire device. All device state is lost, including the state of circuitry within the debug and Always-On power domains.        |
| VDD_MAIN     | BOR             | Programmable threshold, resets the entire device. All device state is lost, including the state of circuitry within the debug and Always-On power domains. |
| VDD_MAIN     | BOD             | Programmable threshold, triggers interrupts to the A32, M55-HP, M55-HE and SE, and a request to DMA.                                                       |

## 3.8 Reset Management Overview

A reset brings the entire device (cold reset) or part of the device (warm reset) to a known good state.

The reset subsystem of the device is based on a Reset Controller (RSTC). The RSTC handles top-level reset conditions—VBAT\_POR and software reset requests.

[Figure 3-4](#) shows the main reset sources in the device.

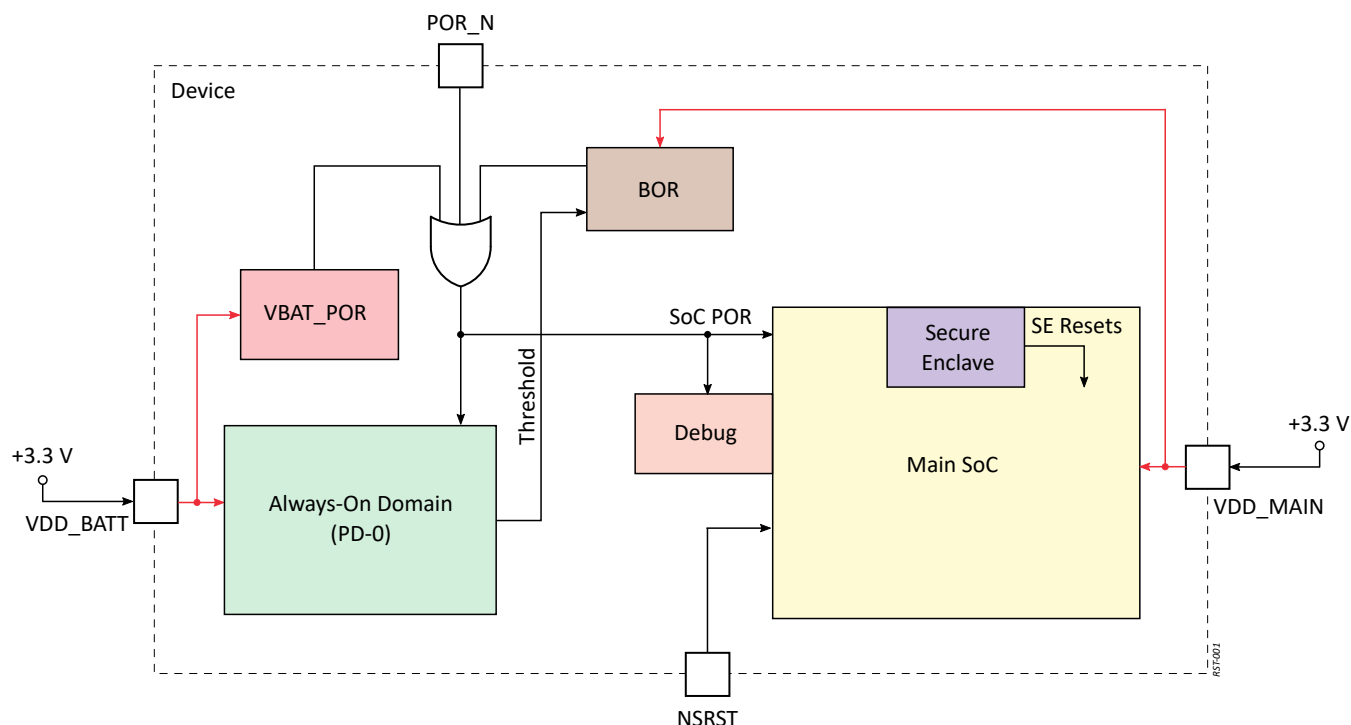
**Figure 3-4 Top-Level Reset Diagram**


Table 3-6 lists the main reset sources along with their types and functions.

**Table 3-6 Device Main Reset Sources**

| Reset Source           | Hardware/Software | Description                                                                                                                                                                                                                                |
|------------------------|-------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| POR_N pin (active-low) | HW                | System cold reset pin. Asserting this pin is equivalent to turning the device power off. After POR_N is deasserted, the device completes a full power on cycle, which is equivalent to a cold start. No logic or memory retains its state. |
| NSRST pin (active-low) | HW                | System warm reset pin. Typically, an external debugger asserts this reset pin. It resets all logic in the device except for PD-0 Always-On peripherals, debug logic, and the JTAG interface.                                               |
| VBAT_POR monitor       | HW                | Fundamental POR. VBAT_POR keeps the entire device in reset during a power-on ramp-up until the device reaches the operational threshold.                                                                                                   |
| BOR monitor            | HW and SW         | Brown-out reset. BOR assertion is equivalent to turning the device power off. After BOR is deasserted, the device completes a full power on cycle, which is equivalent to a cold start.                                                    |
| Secure Enclave Reset   | SW                | Warm reset by Secure Enclave. Initializes all logic except for PD-0 Always-On, the debug logic, and the JTAG interface.                                                                                                                    |
| SW_HOST_RST            | SW                | Warm reset by Secure Enclave. Resets all logic except for PD-0 Always-On, the Secure                                                                                                                                                       |

| Reset Source | Hardware/Software | Description                                                                                                                                 |
|--------------|-------------------|---------------------------------------------------------------------------------------------------------------------------------------------|
|              |                   | Enclave, and the External Debug Bus.                                                                                                        |
| SW_HP_RST    | SW                | High-performance subsystem (RTSS-HP) reset.<br>Warm reset by Secure Enclave.<br>RTSS-HP reset reasons are logged to RTSS_HP_RESET register. |
| SW_HE_RST    | SW                | High-efficiency subsystem (RTSS-HE) reset.<br>Warm reset by Secure Enclave.<br>RTSS-HE reset reasons are logged to RTSS_HE_RESET register.  |

Table 3-7 presents Reset signals and provides descriptions to their functions.

**Table 3-7 Reset Signal Descriptions**

| Signal Name | Pin Name | Type | Description                            |
|-------------|----------|------|----------------------------------------|
| NSRST       | NSRST    | I    | JTAG reset (system reset) active low   |
| POR_N       | POR_N    | I    | Power-On-Reset (cold reset) active low |

### 3.9 Clock Generation and Control

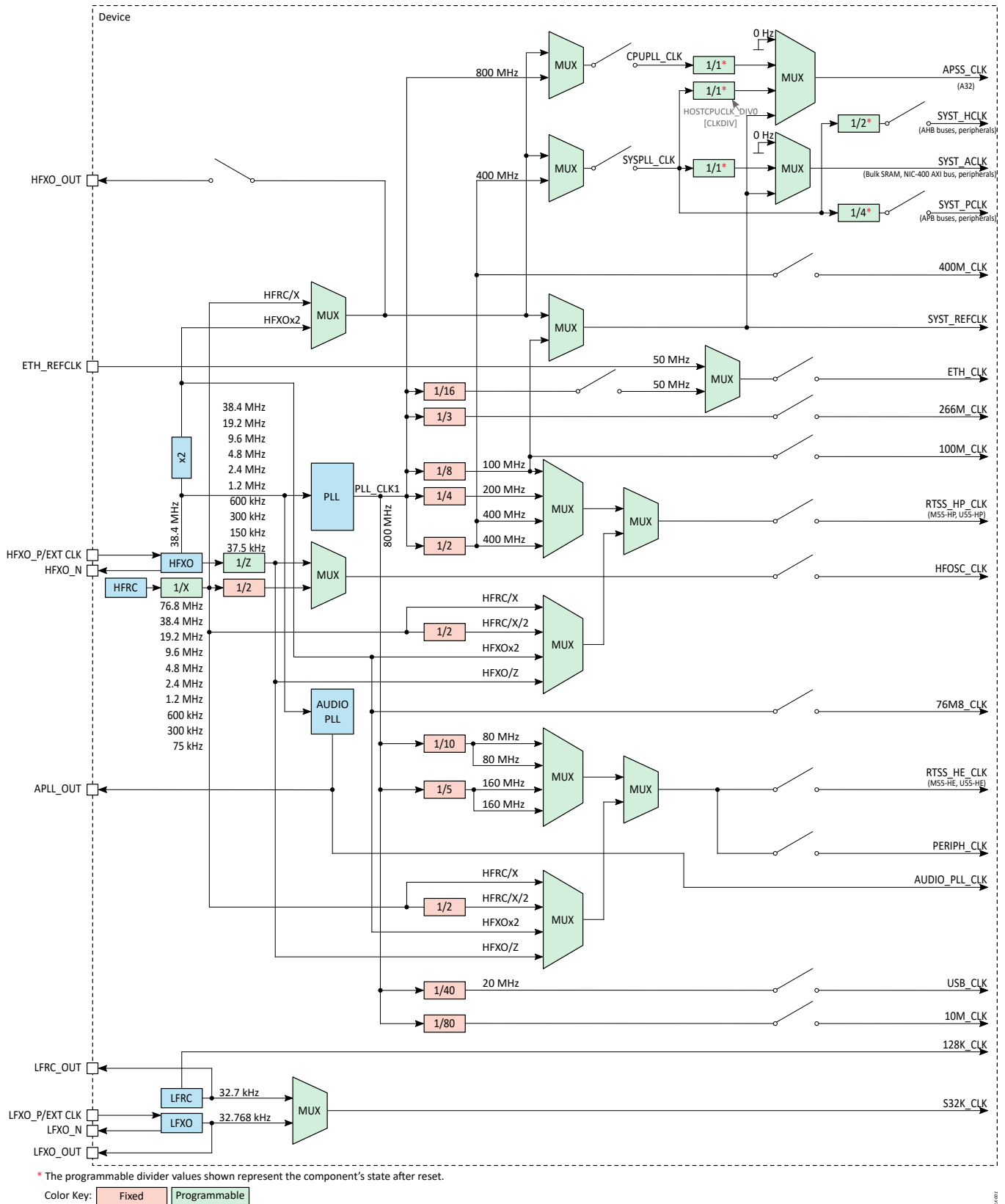
The device includes several clock domains, PLLs, clock dividers, clock multiplexers, oscillators.

The device clock sources are as follows:

- Low-Frequency Resistor-Capacitor (LFRC) oscillator—a low-power, internal RC oscillator powered by VDD\_BATT. This oscillator is used during the power-up sequence, with a typical clock frequency accuracy of 32.7 kHz  $\pm$ 4%.
- Low-Frequency crystal Oscillator (LFXO)—a low-power oscillator that is used with a high-accuracy 32.768 kHz external crystal. This oscillator is powered by VDD\_BATT. It is enabled at power-up and is the typical clock source for LPRTC. The LFXO oscillator input may optionally be configured in bypass mode for connection to an external 32.768 kHz clock source.
- High-Frequency Resistor-Capacitor (HFRC) oscillator—a low-power internal RC oscillator that generates 76.8 MHz. When the LFXO clock source is available, the HFRC oscillator can be trimmed to reach an accuracy of  $\pm$ 2% or better over temperature. The HFRC oscillator is available in all power modes except for STOP mode. This oscillator is used during power-up for rapid initialization and fast start-up.
- High-Frequency crystal Oscillator (HFXO)—a power-optimized oscillator that is used with an external crystal with a frequency between 24 MHz and 38.4 MHz. This oscillator is enabled by software after initial device configuration and is typically the source clock for the PLL. The HFXO oscillator input may optionally be configured in bypass mode for connection to an external high-speed clock source/oscillator.
- System PLL (Phase-Locked Loop)—a power-optimized, fast-locking clock multiplier with fractional mode. It has a single clock output used to supply most of the device subsystems, modules, and interconnects.
- Audio PLL—a power-optimized, fast-locking clock multiplier with fractional mode. It has a single clock output used to clock the I2S and PDM audio peripherals.

Figure 3-5 provides a high-level overview of the clocking scheme implementation in the device.

Figure 3-5 Device Clocking Scheme Overview



## NOTE

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the [Alif Conductor](#) tool.

Table 3-8 presents clock interface signals and provides descriptions to their functions.

**Table 3-8 Clock Signal Descriptions**

| Signal Name | Pin Name | Type | Description                                                  |
|-------------|----------|------|--------------------------------------------------------------|
| HFXO_OUT_A  | P3_6     | O    | High-frequency clock output to external devices              |
| HFXO_OUT_B  | P9_3     |      |                                                              |
| LFXO_OUT_A  | P7_5     | O    | Low-frequency clock output to external devices               |
| LFXO_OUT_B  | P14_1    |      |                                                              |
| LFXO_OUT_C  | P15_4    |      |                                                              |
| LFRC_OUT_A  | P6_4     | O    | Low-frequency RC oscillator clock output to external devices |
| LFRC_OUT_B  | P14_0    |      |                                                              |
| LFRC_OUT_C  | P15_5    |      |                                                              |
| APLL_OUT_A  | P4_0     | O    | Audio PLL clock output to external devices                   |
| APLL_OUT_B  | P14_7    |      |                                                              |
| APLL_OUT_C  | P14_1    |      |                                                              |
| HFXO_P      | HFXO_P   | I    | High-frequency oscillator input                              |
| HFXO_N      | HFXO_N   | O    | High-frequency oscillator output                             |
| LFXO_P      | LFXO_P   | I    | Low-frequency oscillator input                               |
| LFXO_N      | LFXO_N   | O    | Low-frequency oscillator output                              |

## NOTE

The LFRC\_OUT and LFXO\_OUT signals are routed to device pins both through regular signal multiplexing and through the LPGPIO module. See [Section 3.10.1 Signal Multiplexing](#) for more details.

## 3.10 Signal Multiplexing and I/O Buffer Configuration

### 3.10.1 Signal Multiplexing

The device offers a sophisticated signal-to-pin multiplexing scheme. Each I/O pin may be assigned to one of up to eight peripheral signals, and vice versa, a peripheral signal may be routed to up to four I/O pins. This assignment is pseudo-static and must be performed once during boot time.

The multiplexed pins are divided into 8-pin groups, also referred to as 'ports'. A pin identifier 'Pn\_i' may be used, where  $n$  is the port number and  $i$  is the pin number within that port. A pin may be referenced also with the GPIO peripheral's signal name 'GPIO\_n\_i' because it shares the same numbering convention. For more information on the GPIO peripheral, see [Section 3.16 General-Purpose Input/Output Module](#).

MIPI-CSI, MIPI-DSI, USB PHY pins, and power and ground pins have fixed functions and cannot be multiplexed.

[Figure 3-6](#) shows the P0\_0 multiplexing as an example. The Pn\_i[PINMUX] register bitfield, where  $n = i = 0$ , selects a peripheral signal to be available on P0\_0. The multiplexer switches three signals at a time: IN, OUT,

and OEN (output enable). OEN could be dynamically driven by the peripheral, for example by the I2C which needs to change the Data pin direction very frequently. For many other peripherals OEN could be static, and for GPIO it is programmable via its Data Direction register. The analog peripherals are not multiplexed between themselves and all three can read P0\_0 when [PINMUX] = 7. For more information on configuration registers, refer to the corresponding device series-specific Hardware Reference Manual.

**Figure 3-6 I/O Signal Multiplexing (P0\_0 Example)**

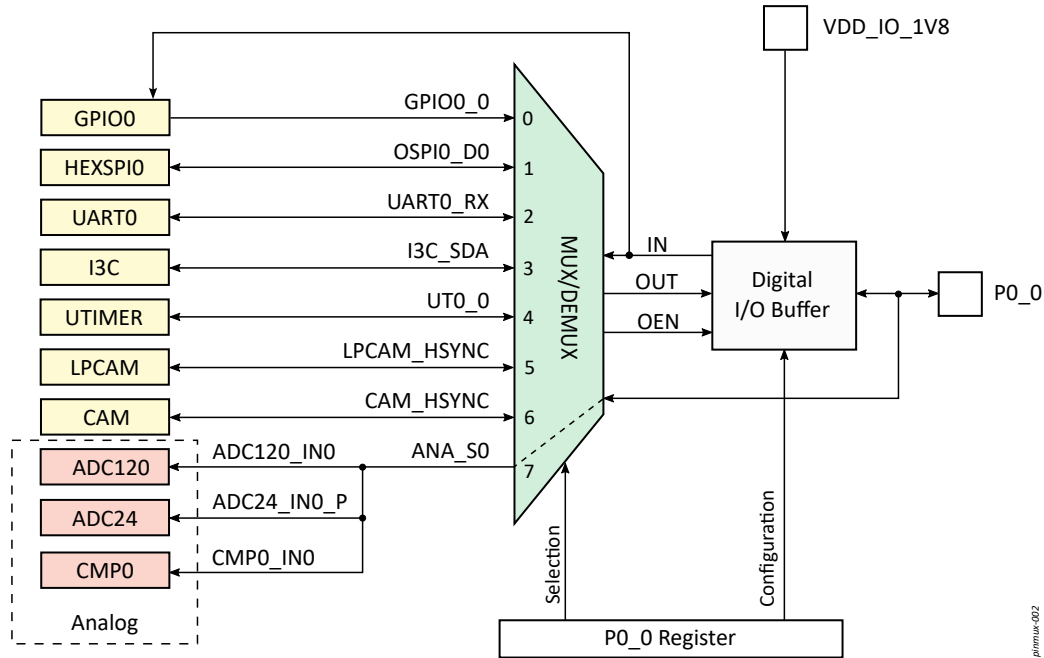
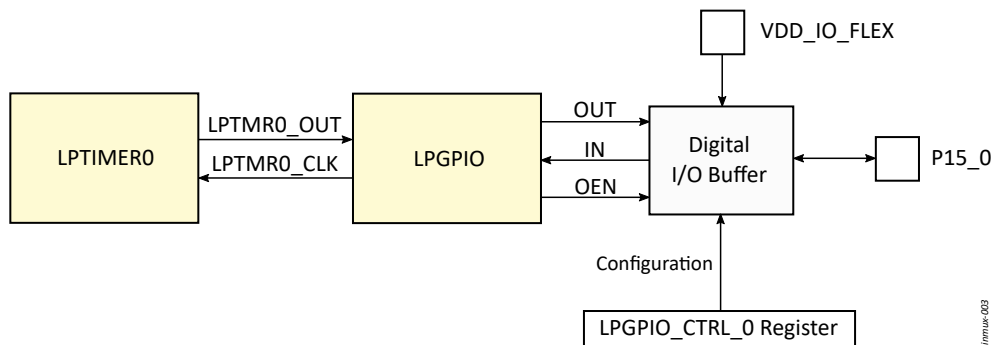


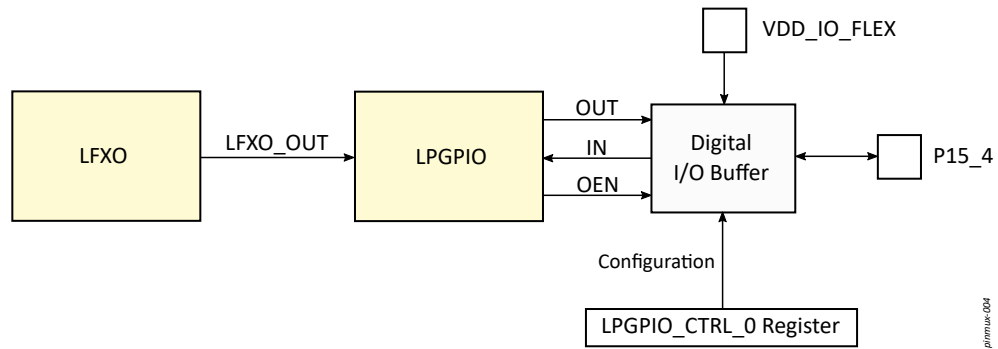
Figure 3-7 shows the LPGPIO pin sharing. Because Port 15 is located in the Always-On domain, here pin sharing is achieved differently. That is, there is no multiplexing as such. In this example, LPTIMER0 gets access to P15\_0 via the LPGPIO module. LPGPIO controls the pin direction depending on the value written to its Data Direction register.

**Figure 3-7 LPGPIO/LPTIMER Pin Sharing (P15\_0 Example)**

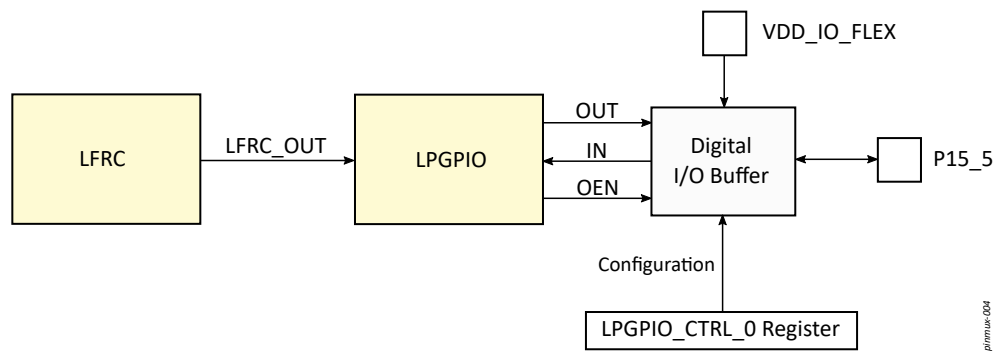


Similarly, LFXO and LFRF get access to P15\_4 and P15\_5 via the LPGPIO module. Figure 3-8 and Figure 3-9 show these cases.

**Figure 3-8 LPGPIO/LFXO Pin Sharing (P15\_4 Example)**



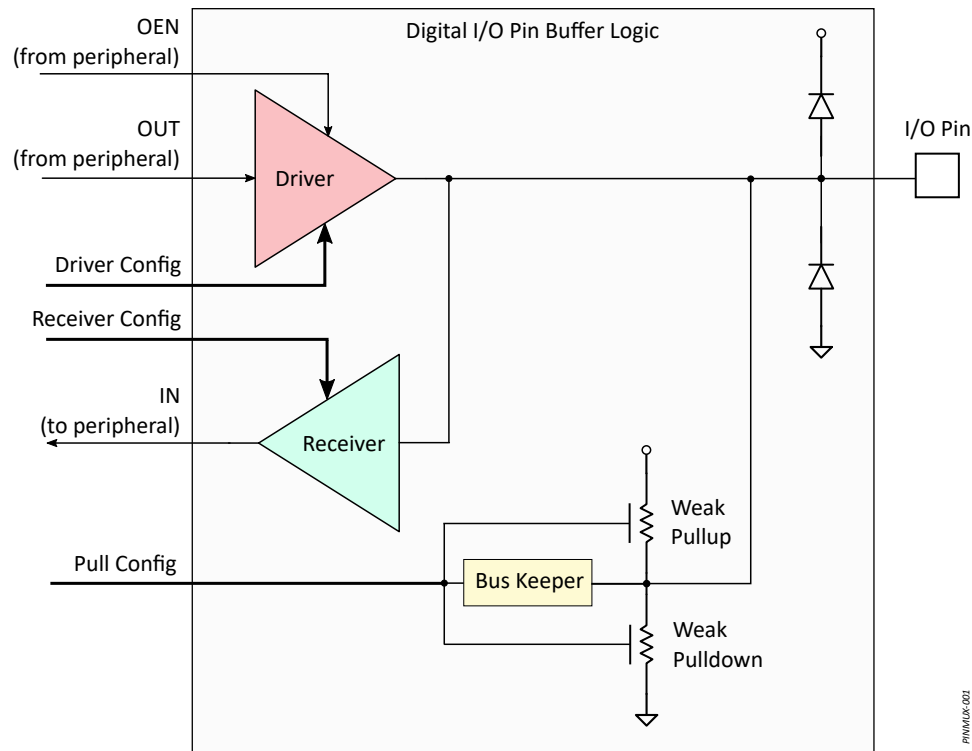
**Figure 3-9 LPGPIO/LFRC Pin Sharing (P15\_5 Example)**



### 3.10.2 I/O Buffer Configuration

Figure 3-10 shows a top-level block diagram of a digital I/O buffer module. I/O buffer consists of configurable output buffer (driver), input buffer (receiver), pull-up/pull-down block, and protective diodes.

Figure 3-10 I/O Buffer Block Diagram



The I/O buffer has the following main features:

- Configurable direction (input, output or both)
- Selectable driver-disabled state:
  - No pull (Hi-Z, floating)
  - Weak pull-up
  - Weak pull-down
  - Bus keeper (keeps the last state seen on the pin)
- Configurable drive strength
- Configurable slew rate
- Output driver can be open drain or push-pull type
- Input may have a Schmitt trigger enabled which adds hysteresis to signal transitions
- Dedicated power rails:
  - VDD\_IO\_FLEX for the 1.8-V/3.3-V pins (GPIO7\_[4-7] and GPIOV\_[0-3])
  - VDD\_IO\_1V8 for the 1.8-V pins

The Pn\_i registers contain bitfields controlling the following parameters:

- Driver type—[DRV] (open drain or push-pull)
- Output drive strength—[E] (2 mA, 4 mA, 8 mA, or 12 mA)
- Driver disabled state—[P] (Hi-Z, Pull-up, Pull-down, or Bus Keeper)
- Slew rate—[SR] (slow [half-speed] or fast)
- Schmitt trigger enable—[SMT]
- Receiver enable—[REN]

Similar I/O buffer controls exist also for Port 15 in the LPGPIO\_CTRL\_n[DRIVER] and LPGPIO\_CTRL\_n[RECEIVER] register bitfields.

---

**NOTE**

For more information on I/O buffer configuration registers, refer to sub-sections *PINMUX Registers Guide* and *LPGPIO\_CTRL Registers Guide* in Section *Signal Multiplexing and I/O Buffer Configuration* of the corresponding device series-specific Hardware Reference Manual.

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the [Alif Conductor](#) tool.

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## **3.11 Inter-Processor Communication**

### **3.11.1 HWSEM Overview**

The Hardware Semaphore (HWSEM) provides a mechanism for coordinating the concurrency between processor cores when they access shared resources—memory regions or peripherals.

The device includes 16 HWSEM modules with individual interrupt requests. Each of the semaphores can be assigned depending on the application needs.

Each HWSEM module supports the following main features:

- Acquire, Release, and Reset functions as atomic operation
- Single-processor access at a time
- An internal acquisition counter for enabling processor owning of a HWSEM to acquire it multiple times
- An interrupt assertion once the HWSEM becomes available

### **3.11.2 MHU Overview**

The Message Handling Unit (MHU) provides point-to-point communication between the Secure Enclave processor, the Application processor (A32), and the two Real-Time processors (M55-HP and M55-HE). The MHU is an interrupt-based communication between two processing entities.

The device includes up to 24 unidirectional MHU modules.

Each of the MHU modules supports the following main features:

- Two memory mapped register frames—Sender and Receiver
- Unidirectional communication interface
- Read and write access—32-bit word aligned
- Dual transport channels
- Different transport protocols—Doorbell, Single-Word transfer, and Multi-Word
- Dedicated interrupt lines for the Sender and Receiver

The software responsibilities are:

- To request the Receiver to be powered
- To ensure that the Sender remains powered until the transfer has been finished
- To use Ready to Send protocol to send the transfer

Each processor entity includes only one of the Sender or Receiver frame. To ensure a bi-directional (full-duplex) communication between the entities, two MHUs with reversed Sender and Receiver parts are implemented.

## 3.12 Memories

### 3.12.1 MRAM Overview

The MRAM module is a type of non-volatile random-access memory which stores information in magnetic elements.

The MRAM operates at 66 MHz clock frequency over 128-bit data bus. The 128-bit (16-byte) word represents the minimum sector size for the MRAM. The smaller granularity offers much better efficiency compared to the legacy flash memory modules. It takes flash memories longer to be programmed/erased due to their much larger sector sizes.

The MRAM module implements a state machine controlling the erase and programming sequence of 16-byte memory blocks. This operation is transparent to the CPU core.

The MRAM controller implements read cache and write buffer mechanism that enables the concurrent read and write operations. This greatly benefits the implementation of multi-core applications that are not required to coordinate the access to the MRAM. Up to four bus masters can originate concurrent write operations, while the number of concurrent read operations is not limited.

The MRAM supports the following main features:

- 5.5MB
- High endurance (more than 100 000 erase cycles)
- More than 10 years data retention (at 125 °C junction temperature)
- 16 ECC bits for each 128-bit data word
- 2× 16 bytes read cache to accelerate access to frequently used data and non-16-byte aligned read requests
- Built-in state machine controlling 16-byte program/erase cycle (no need of driver)
- Concurrent write (up to four bus masters) and read operations (no need for synchronization between them)
- DMA write operation with up to 128 bytes in each DMA write cycle data payload

### 3.12.2 SRAM Overview

The device contains the following types of on-chip SRAM memories:

- User SRAM available for all bus masters:
  - Bulk SRAM: SRAM0 and SRAM1, with optional retention
  - M55-HP TCM: SRAM2 (M55-HP ITCM) and SRAM3 (M55-HP DTCM)
  - M55-HE TCM: SRAM4 (M55-HE ITCM) and SRAM5 (M55-HE DTCM), with optional retention
- Processor cache memories:
  - A32 Level 1 cache and Level 2 cache
  - M55-HP Level 1 cache
  - M55-HE Level 1 cache
- Utility SRAM
  - Located in Always-On domain

The embedded bulk SRAM is a general-purpose memory to be shared among all applications. It is partitioned into two blocks, which can be accessed in parallel over 128-bit AXI bus running at 400 MHz.

The TCM is an SRAM block providing high-bandwidth and low latency access. The TCM is primarily used by the M55 core it is attached to. Alternatively, it can be shared with other bus masters in the device.

The cache memory is a high-performance SRAM accelerating the CPU access to frequently used instructions and data. A32 Level 1 cache memory is dedicated to an individual A32 core. The Level 2 cache is shared between the two A32 cores. The M55 processors have Level 1 cache memories dedicated to each M55 core. The data retention of SRAM is used for context saving during low power modes.

The device includes the following quantities of SRAM with their performance characteristics:

- User SRAM available to all bus masters:
  - 9.75MB:
    - 4MB bulk SRAM0 + 4MB bulk SRAM1, with optional data retention
    - 0.25MB SRAM2 (M55-HP ITCM) + 1MB SRAM3 (M55-HP DTCM)
    - 0.25MB SRAM4 (M55-HE ITCM) + 0.25MB SRAM5 (M55-HE DTCM), with optional data retention
  - 400 MHz parallel read/write access
- Application processor (A32) cache memories:
  - Level 1 Cache: 32KB Instruction and 32KB Data cache per core
  - Level 2 Cache: 512KB shared between the two A32 cores
- Real-time processors (M55) cache memories:
  - Level 1 Cache: 32KB Instruction and 32KB Data cache per core
- Utility SRAM:
  - 4KB in Always-On power domain PD-0
  - 100 MHz read/write access (32-bit wide access only)

### 3.12.3 TCM Overview

The Tightly Coupled Memory (TCM) is a high-bandwidth and low latency memory. The TCM enables the Cortex-M55 cores to perform vector operations with high efficiency and process interrupts with minimum latency. The TCM access time is a single clock cycle with no wait states for reads. The TCM interface is based on Harvard architecture—it has one instruction memory (ITCM0) bus and four data memory (DTCM0/1/2/3) buses, all 32-bit wide.

Both M55-HP and M55-HE cores can use the ITCM for storing data and can fetch instructions out of the DTCM. In this scenario, the TCM access time is slower and vector operations are not supported.

The Cortex-M55 cores have the following TCM configurations:

- M55-HP:
  - 256KB of ITCM and 4 × 256KB of DTCM (total of 1.25MB)
  - 1 × 32-bit ITCM and 4 × 32-bit DTCM memory buses
  - Single-cycle read/write access at 400 MHz
  - Concurrent share of TCM with the other processing entities via AHB slave port
- M55-HE:
  - 256KB of ITCM and 4 × 64KB of DTCM (total of 512KB)
  - 1 × 32-bit ITCM and 4 × 32-bit DTCM memory buses
  - Single-cycle read/write access at 160 MHz
  - Concurrent share of TCM with the other processing entities via AHB slave port
  - Optional content retention

### 3.12.4 External Memory Expansion Options

The device provides two options to expand the memory using external devices:

- 1× SDMMC interface
- 2× HEXSPI interface

The SDMMC interface can be used to access embedded or external memory cards with clock frequency up to 50 MHz. The data bus is up to 8 bits wide. This external memory interface is suitable for expanding the bulk data storage capacity in the form of an external flash-based file system. The SDMMC interface supports legacy 4-bit cards as well.

The HEXSPI interfaces can be used to access external flash memory devices. Each HEXSPI supports Double Data Rate (DDR) mode transferring 16-bit data on both edges of the clock signal. The maximum clock frequency is up to 200 MHz, delivering raw SDR bandwidth of up to 400 MB/s, and DDR bandwidth of up to 800 MB/s.

The HEXSPI interface could access the memory in two modes—directly (through register read/write operations) or indirectly (through memory-mapped operations). The indirect access supports eXecute-in-Place (XIP) mode which translates the instruction fetch operations to proper address and data read transactions. This way, the external memory devices expand the available non-volatile memory.

The HEXSPI interfaces support legacy Single, Dual, Quad, Octal, or Hex SPI, and 16-bit flash memory devices. Each HEXSPI interface also supports the HyperBus protocol in direct and indirect modes. This enables the integration of external Static or Pseudo-Static RAM devices. See operation limitations in [Section 3.18.1 Cryptographic HEXSPI Overview](#).

Each HEXSPI interface can be attached to a flash or SRAM devices based on the application needs.

The device includes two AES decoders—one for each HEXSPI interface. The decoders are implemented in hardware and enable on-the-fly decoding of the external memory content. This allows protecting the HEXSPI code or the confidentiality of the data stored in external devices. The decoders effectively add no latency while maintaining the overall external memory interface bandwidth.

### 3.12.5 Memory Mapping

Refer to the device series-specific Hardware Reference Manual for details on the memory mapping.

## 3.13 Interrupts and Events Management

### 3.13.1 GIC Overview

The Arm Generic Interrupt Controller (GIC-400) is a high-performance, area-optimized interrupt controller that detects, manages, and distributes interrupts to the A32 application processor.

The GIC module supports the following main features:

- Supports both cores inside the A32 processor cluster
- 16 Software Generated Interrupts (SGIs) per core
- 6 external and 1 internal Private Peripheral Interrupts (PPIs) per core
- 480 Shared Peripheral Interrupts (SPIs)
- Interrupt masking and prioritization
- Interrupt assignment to either of two groups:
  - Group 0 (secure)
  - Group 1 (non-secure)
- Interrupt virtualization
- AMBA 4 AXI configuration interface

### 3.13.2 NVIC Overview

The Nested Vectored Interrupt Controller (NVIC) resides in each of the M55-HP and M55-HE processors, and it is closely integrated with the Cortex-M55 core to achieve low-latency interrupt processing. Both NVIC

modules have the same configuration in the device.

Each NVIC module supports the following main features:

- Maintaining the current execution priority of the Cortex-M55 processor
- Maintaining the pending and active status of all exceptions that are supported
- Invoking preemption when a pending exception has priority
- Providing wake-up signals to wake up the Cortex-M55 processor from deep sleep mode
- Providing support to the Internal Wakeup Interrupt Controller (IWIC) and External Wakeup Interrupt Controller (EWIC)
- Providing priority and exception information to other processor components
- 480 external interrupts, with 256 priority levels per interrupt

### 3.13.3 IRQRTR Overview

The shared Interrupt Router (IRQRTR) is intended to route interrupt signals from the device peripherals to all processing entities. It has an input port wired to the interrupt sources and four output ports connected to the Secure Enclave, the Application Processor Subsystem and the two Real-Time Processing interrupt controllers.

The router configuration registers define which interrupt sources are enabled and their destination output ports. Once configured, the router can be locked fully or partially so that further changes can be restricted.

**The access to the IRQRTR configuration may be constrained based on the device security policy. In this case, the interrupt routing can be indirectly setup by service call to the Secure Enclave.**

The IRQRTR supports the following main features:

- Manages up to 427 shared interrupts
- Configures routing of the interrupt signals to up to four processing entities
- Supports configuration access lockdown
- Reports tamper interrupts to the Secure Enclave

### 3.13.4 EVTRTR Overview

The device integrates a large number of peripherals that can generate events indicating changes in their state, receiving of data or completion of an operation. The Event Router (EVTRTR) is a module that can associate an event originated by one peripheral with an action executed by another.

The function of the EVTRTR is similar to the shared Interrupt Router (IRQRTR), which targets an interrupt controller and ultimately a CPU core. Unlike the IRQRTR, the EVTRTR is connecting the event signal to a peripheral that executes an action without involving any CPU core.

Modules generating such event signals include: GPIO, UTIMER, I2C, SPI, UART, and others. The EVTRTR passes the signals through edge-detection circuits and gating logic before routing them to specific targets.

The device includes three Event Routers, each dedicated to a specific target:

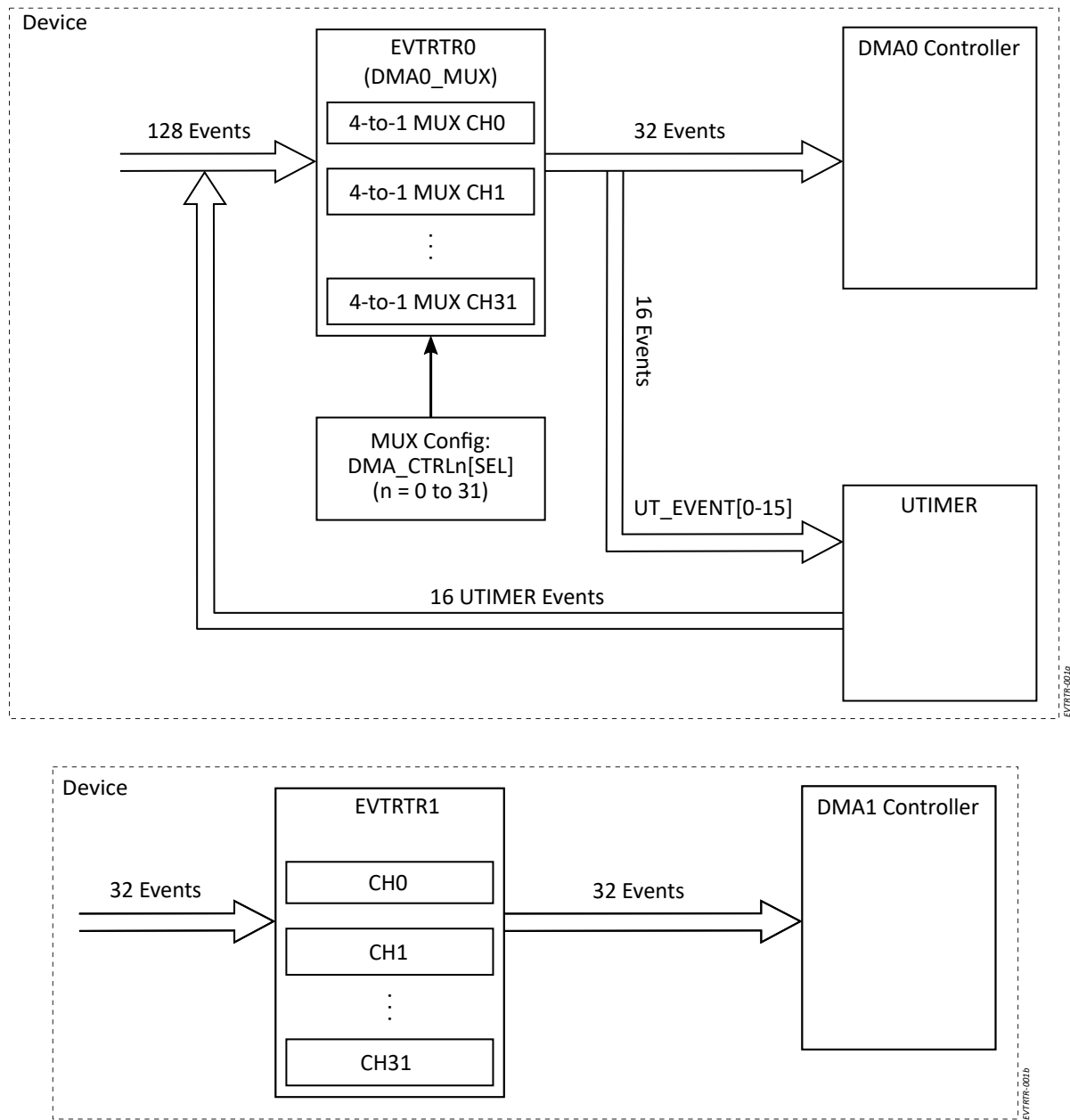
- EVTRTR0, dedicated to DMA0 controller and UTIMER
- EVTRTR1, dedicated to DMA1 controller
- EVTRTR2, dedicated to DMA2 controller and LPUTIMER

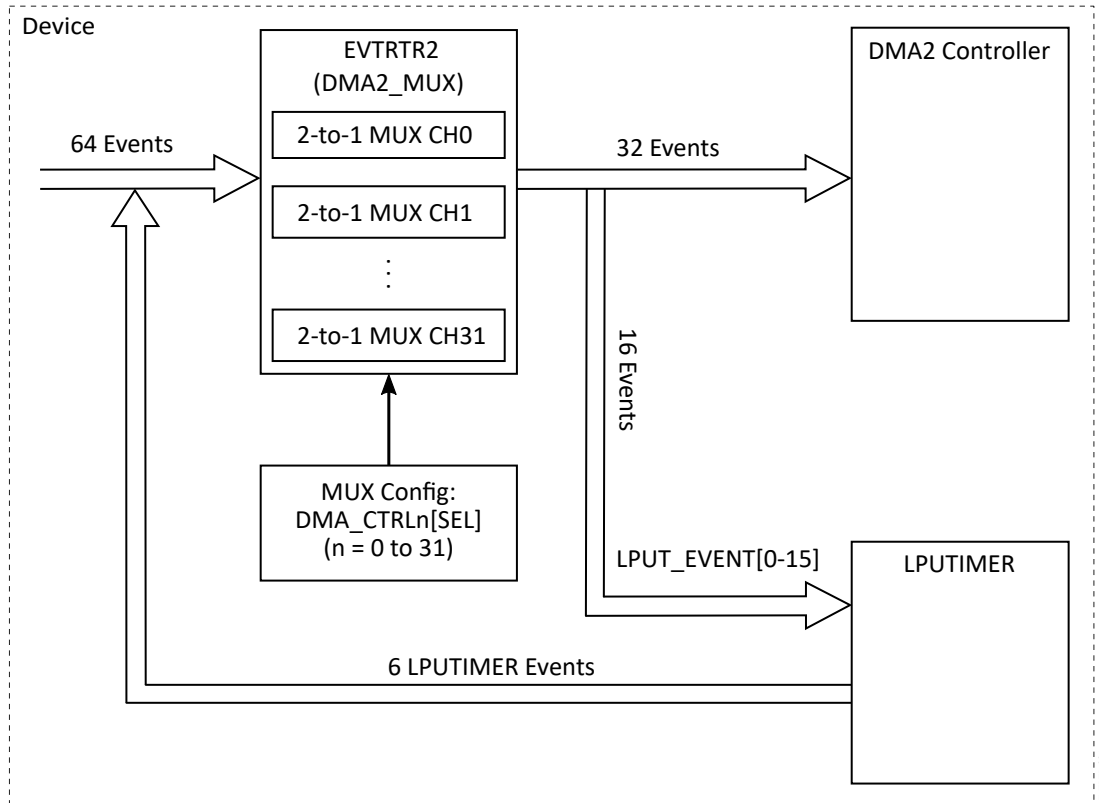
Each EVTRTR provides the following main features:

- Software generated events
- Zero wait state for event routing between peripherals in the same clock domain
- Automatic synchronization of events and triggers between peripherals in different clock domains
- DMA channel enable, handshake status and type selection

Figure 3-11 provides a high-level overview of the EVTRTR implementation in the device.

**Figure 3-11 EVTRTR Overview**





EVTRTR0 is also referred to as DMA0\_MUX and expands the available 32 inputs of DMA0 by exposing the DMA channels to 128 different peripheral events via  $32 \times 4$ -to-1 multiplexers. The first 16 multiplexed DMA0 requests are also routed as input triggers to the Universal Timer (UTIMER). This mechanism enables the implementation of complex state machines involving the use of peripheral or time-based events that trigger data transfers and/or timer triggers.

EVTRTR1 supports 32 input events/output DMA channels without implementing events multiplexing.

EVTRTR2 is also referred to as DMA2\_MUX and expands the available 32 inputs of DMA2 by exposing the DMA channels to 64 different peripheral events via  $32 \times 2$ -to-1 multiplexers. Sixteen multiplexed DMA2 requests are also routed as input triggers to the LPUTIMER.

## 3.14 DMA Management

### 3.14.1 DMA Architecture Overview

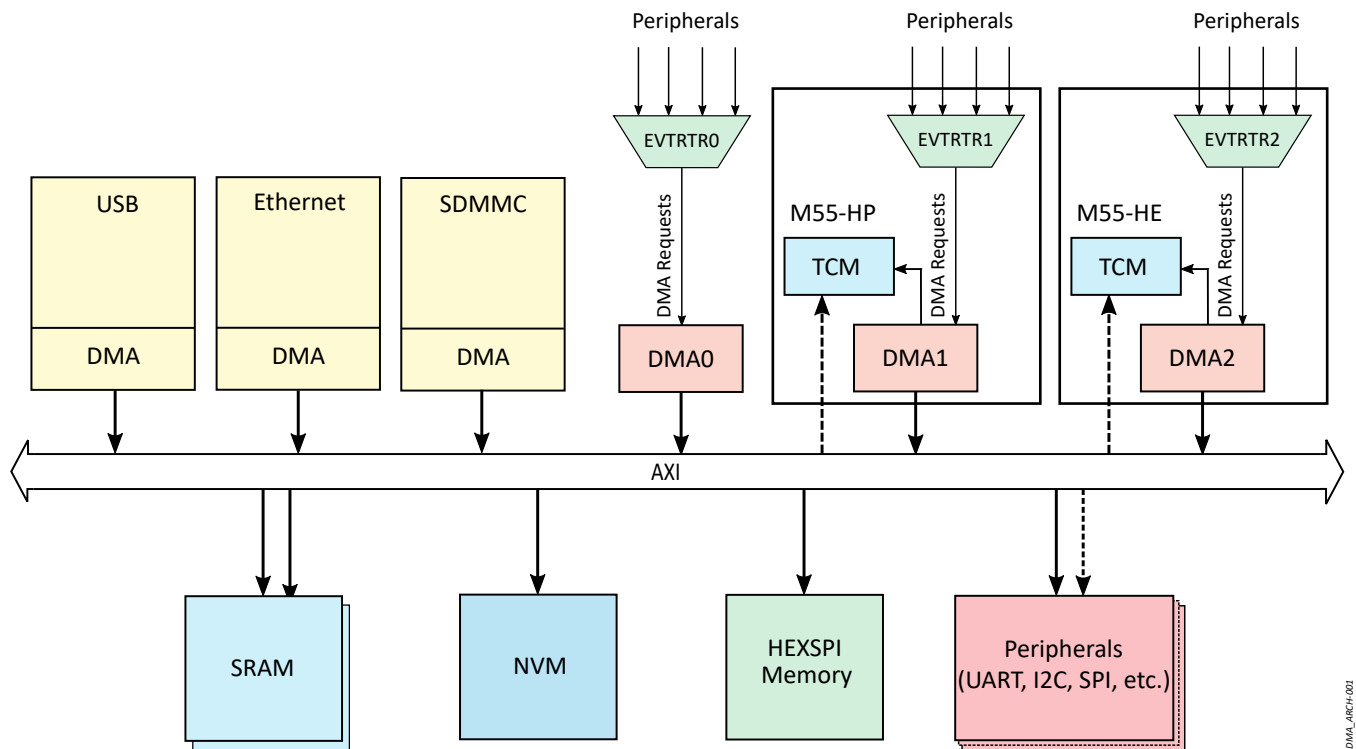
The device features Direct Memory Access (DMA) controllers to offload the CPUs from repeated data transfer tasks. The device has the following DMA controllers:

- USB embedded DMA controller
- Ethernet embedded DMA controller
- SDMMC embedded DMA controller
- DMA0: Can be shared by all of the CPU cores
  - It carries out data transfers from/to ADC, PDM, I2C, I3C, CANFD, SPI, HEXSPI, and UART.
  - DMA0 also supports multiple DMA triggers like GPIO pin transitions and timer events.
- DMA1: Dedicated to the RTSS-HP subsystem and serves DMA requests from CMP, QEC, UART, UTIMER, and via GPIO9 pins.

- **DMA2:** Dedicated to the RTSS-HE subsystem
  - DMA2 can move data from/to the following peripherals: Low Power (LP) peripherals (such as LPUART, LPSPI, etc.), ADC, CANFD, and I3C.
  - BOD, LPTIMER, LPCMP, LPCAM\_VSYNC, LPCAM\_HSYNC, GPIO16, and LPGPIO I/O transitions can trigger DMA requests.

Figure 3-12 gives a high-level overview of the DMA architecture in the device.

**Figure 3-12 DMA Architecture**



The high-speed interface peripherals (USB, ETH, and SDMMC) have their own, embedded DMA controllers. They are optimized for the specific needs of these interfaces.

DMA0, DMA1 and DMA2 are general-purpose, programmable, multi-channel, and TrustZone-aware DMA controllers (DMACs). Each DMAC has 32 inputs for accepting DMA requests from various device peripherals and triggers (for example, UART Tx and Rx, ADC conversion done, etc). The Event Routers positioned in front of the DMA controllers provide support for DMA handshaking between peripherals and DMACs. Additionally, EVTRTR0 provides  $32 \times 4$ -to-1 programmable multiplexers, which expose the 32 DMA0 inputs to 128 possible DMA requests from peripherals, thus providing an increased flexibility. Likewise, EVTRTR2 provides  $32 \times 2$ -to-1 programmable multiplexers, which expose the 32 DMA2 inputs to 64 possible DMA requests from peripherals. Each DMA controller supports 8 internal data channels (FIFOs). All channels can perform independently programmed transactions including different data lengths, source and destination addresses, single or burst transfers.

DMA0 controller can be shared by all of the CPU cores. The security privilege of each channel is run-time programmable. DMA0 initiates transactions on the main AXI bus with its unique Stream ID. Each of the 32 request interfaces can generate an interrupt request signal. The interrupts are shared over the Interrupt Router (IRQRTR) with all of the CPU cores.

DMA1 and DMA2 controllers are assigned to the M55-HP and M55-HE CPU cores, respectively. They reside in their domains and share their AXI-bus Stream IDs (and security policy). The DMA1 and DMA2 request interfaces can generate individual interrupt requests, attached locally to their respective M55 cores.

### 3.14.2 DMA Controllers Overview

The device includes three copies of the general-purpose DMA Controller (DMAC):

- DMA0 can be shared among all CPU cores
- DMA1, dedicated to the RTSS-HP
- DMA2, dedicated to the RTSS-HE

Each DMAC supports the following main features:

- Flexible instruction set for programming DMA transfers
- Transfer types:
  - Memory-to-memory
  - Memory-to-peripheral
  - Peripheral-to-memory
  - Scatter-gather
- 32 peripheral request interfaces (DMA\_Req/DMA\_Ack)
- 8 DMA channels (VFIFOs)
- Flagging of various DMA events using 33 interrupt signals
  - 32 interrupts, one per DMA request interface
  - One data abort interrupt
- Dual slave interfaces, secure and non-secure, for accessing registers
- Programmable security state for each DMA channel
- Arm TrustZone technology
- 4 active AXI read transactions
- 4 active AXI write transactions
- 32 deep internal data buffer (MFIFO)
- 4 lines in the instruction cache with 8 words in a line
- 8 deep read instruction queue
- 8 deep write instruction queue
- Request acceptance capability of a peripheral request interface—4 requests

## 3.15 Timers and Counters

### 3.15.1 LPTIMER Overview

The 32-bit Low-Power Timer (LPTIMER) module counts down from a programmed value and generates an interrupt when the count reaches zero. Two events can cause the timer to load the initial value from which it counts down. The first event is when the timer is enabled after being reset or disabled, and the second event is when the timer count reaches zero.

The device includes up to four independent LPTIMER modules (“channels”), accessible through a single bus.

Each LPTIMER module supports the following main features:

- 32-bit down counter
- Free-running and user-defined count modes
- Asynchronous event counting
- Individual toggle output with PWM capability
- Individual interrupt output

- Independent clock input that can be connected either to internal clocks or to an external clock source
- Each odd numbered LPTIMER module can be concatenated with the previous even numbered LPTIMER module to form up to a 64-bit timer
- The LPTIMER interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

#### NOTE

All Low Power peripherals are single-master accessible, including LPTIMER. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-9 presents LPTIMER interface signals and provides descriptions to their functions.

**Table 3-9 LPTIMER Signal Descriptions**

| Signal Name     | Pin Name | Type | Description                                                                                                                                                                                           |
|-----------------|----------|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| <b>LPTIMER0</b> |          |      |                                                                                                                                                                                                       |
| LPTMR0_CLK_IO   | P15_0    | IO   | LPTIMER0_CLK: LPTIMER0 input clock from pin.<br>LPTIMER0_OUT: LPTIMER0 toggle output. Changes state each time the timer counter reloads. The output is disabled to 0 each time the timer is disabled. |
| <b>LPTIMER1</b> |          |      |                                                                                                                                                                                                       |
| LPTMR1_CLK_IO   | P15_1    | IO   | LPTIMER1_CLK: LPTIMER1 input clock from pin.<br>LPTIMER1_OUT: LPTIMER1 toggle output. Changes state each time the timer counter reloads. The output is disabled to 0 each time the timer is disabled. |
| <b>LPTIMER2</b> |          |      |                                                                                                                                                                                                       |
| LPTMR2_CLK_IO   | P15_2    | IO   | LPTIMER2_CLK: LPTIMER2 input clock from pin.<br>LPTIMER2_OUT: LPTIMER2 toggle output. Changes state each time the timer counter reloads. The output is disabled to 0 each time the timer is disabled. |
| <b>LPTIMER3</b> |          |      |                                                                                                                                                                                                       |
| LPTMR3_CLK_IO   | P15_3    | IO   | LPTIMER3_CLK: LPTIMER3 input clock from pin.<br>LPTIMER3_OUT: LPTIMER3 toggle output. Changes state each time the timer counter reloads. The output is disabled to 0 each time the timer is disabled. |

#### NOTE

The LPTMRn\_CLK\_IO signals are routed to device pins through the LPGPIO module. See [Section 3.10.1 Signal Multiplexing](#) for more details.

### 3.15.2 UTIMER Overview

The 32-bit high-resolution Universal Timer (UTIMER) typically serves as a standard signal timing generator and a pulse counter. In addition, the UTIMER can also be used to implement a quadrature encoder interface and serve as a Quadrature Encoder Counter (QEC).

The device includes up to sixteen independent UTIMER modules (“channels”), which are allocated as follows:

- Up to twelve standard UTIMER modules: Channel 0 (UTIMER0) to Channel 11 (UTIMER11)
- Up to four UTIMER modules configured as QEC: Channel 12 (QEC0) to Channel 15 (QEC3)

The device also includes up to three independent QEC-enabled Low-Power UTIMER modules (“LP channels”): LP Channel 0 (LPUTIMER0) to LP Channel 2 (LPUTIMER2).

In measurement mode, each UTIMER channel can capture the timing of internal events or external signal pulse edges. In counting mode, each channel can count external pulses, internal events, or decode quadrature pulse sequences.

As a signal generator, each UTIMER channel can be configured to produce PWM outputs with independent or complementary polarity and has the following main characteristics:

- Outputs configurable option to automatically insert dead-time suitable for power stages with asymmetric switching characteristics
- Multiple channels can be synchronized to drive three-phase inverters with variety of modulation schemes
- Driving up to 4 three-phase motors at once

Each QEC channel is a multifunctional counter with two inputs that can be configured to support different counting modes and an additional pin for zero signal used for reference run (zero-point calibration).

A QEC channel is intended to operate primarily as a decoder of a quadrature encoder pulse sequence. The input signals are passed through a digital filter to improve the noise immunity of the circuit. The count direction can be configured to depend on the phase difference between two signals (quadrature encoding) or on the level of one of them (pulse and direction encoding). Alternatively, one of the signals can be configured to increment and the other to decrement the timer counter values.

In measurement mode, each LPUTIMER channel can capture the timing of internal events or external signal pulse edges.

In counting mode, each LPUTIMER channel can serve as a multifunctional counter with two inputs that can be configured to support different counting modes and count external pulses, internal events, or decode quadrature encoder pulse sequences. The input signals are passed through a digital filter to improve the noise immunity of the circuit. The count direction can be configured to depend on the phase difference between two signals (quadrature encoding) or on the level of one of them (pulse and direction encoding). Alternatively, one of the signals can be configured to increment and the other to decrement the timer counter values.

Each UTIMER channel supports the following main features:

- Clocked at high-resolution, up to 400 MHz clock with 2.5 ns accuracy (up to 160 MHz clock with 6.25 ns accuracy for the LPUTIMER channels) when generating a PWM output or when measuring input signal timing characteristics
- Dedicated digital inputs configurable as external synchronization sources or as fault signals that trigger automatic shut-off of the output drivers
- 32-bit wide counters and compare registers
- Double-buffered compare registers to support update of PWM duty cycle to occur upon several events, including at the middle or at the end of a PWM period. When buffer operation is enabled, it can be configured to use single or double stage.
- Up to 2 high-resolution PWM outputs with independent or complimentary polarity
- Support of capturing events placed closely together when the channel is configured as a pulse counter
- Capture and compare modes

- Compare registers dedicated to ADC synchronization—on a match they trigger ADC conversion, thus avoiding a power stage switching noise
- 8 interrupt events—some can be shared among channels to enable the implementation of complex state machines that can operate in a deterministic manner
- Configurable to use two I/O pins as inputs and to drive the two I/O pins

Each QEC channel has the following main features:

- 32-bit wide counters and compare registers
- Decoding quadrature encoder pulse sequence
- Counting in pulse/direction or increment/decrement modes
- Measurement of pulse width, period, or duty cycle
- Digital filter on the input signals for up to 32 peripheral clock cycles
- Generation of interrupts on two compare/match events
- Internal clock frequency up to 400 MHz
- External signals frequency up to 50 MHz

#### NOTE

All Low Power peripherals are single-master accessible, including LPUTIMER. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-10 presents UTIMER interface signals and provides descriptions to their functions.

**Table 3-10 UTIMER Signal Descriptions**

| Signal Name   | Pin Name | Type | Description                                           |
|---------------|----------|------|-------------------------------------------------------|
| UTIMER0 A/B/C |          |      |                                                       |
| UT0_T0_A      | P0_0     | IO   | UTIMER0 input event on channel A / output to driver A |
| UT0_T0_B      | P5_0     |      |                                                       |
| UT0_T0_C      | P10_0    |      |                                                       |
| UT0_T1_A      | P0_1     | IO   | UTIMER0 input event on channel B / output to driver B |
| UT0_T1_B      | P5_1     |      |                                                       |
| UT0_T1_C      | P10_1    |      |                                                       |
| UTIMER1 A/B/C |          |      |                                                       |
| UT1_T0_A      | P0_2     | IO   | UTIMER1 input event on channel A / output to driver A |
| UT1_T0_B      | P5_2     |      |                                                       |
| UT1_T0_C      | P10_2    |      |                                                       |
| UT1_T1_A      | P0_3     | IO   | UTIMER1 input event on channel B / output to driver B |
| UT1_T1_B      | P5_3     |      |                                                       |
| UT1_T1_C      | P10_3    |      |                                                       |
| UTIMER2 A/B/C |          |      |                                                       |
| UT2_T0_A      | P0_4     | IO   | UTIMER2 input event on channel A / output to driver A |
| UT2_T0_B      | P5_4     |      |                                                       |
| UT2_T0_C      | P10_4    |      |                                                       |
| UT2_T1_A      | P0_5     | IO   | UTIMER2 input event on channel B / output to driver B |
| UT2_T1_B      | P5_5     |      |                                                       |

| Signal Name   | Pin Name | Type | Description                                           |
|---------------|----------|------|-------------------------------------------------------|
| UT2_T1_C      | P10_5    |      |                                                       |
| UTIMER3 A/B/C |          |      |                                                       |
| UT3_T0_A      | P0_6     | IO   | UTIMER3 input event on channel A / output to driver A |
| UT3_T0_B      | P5_6     |      |                                                       |
| UT3_T0_C      | P10_6    |      |                                                       |
| UT3_T1_A      | P0_7     | IO   | UTIMER3 input event on channel B / output to driver B |
| UT3_T1_B      | P5_7     |      |                                                       |
| UT3_T1_C      | P10_7    |      |                                                       |
| UTIMER4 A/B/C |          |      |                                                       |
| UT4_T0_A      | P1_0     | IO   | UTIMER4 input event on channel A / output to driver A |
| UT4_T0_B      | P6_0     |      |                                                       |
| UT4_T0_C      | P11_0    |      |                                                       |
| UT4_T1_A      | P1_1     | IO   | UTIMER4 input event on channel B / output to driver B |
| UT4_T1_B      | P6_1     |      |                                                       |
| UT4_T1_C      | P11_1    |      |                                                       |
| UTIMER5 A/B/C |          |      |                                                       |
| UT5_T0_A      | P1_2     | IO   | UTIMER5 input event on channel A / output to driver A |
| UT5_T0_B      | P6_2     |      |                                                       |
| UT5_T0_C      | P11_2    |      |                                                       |
| UT5_T1_A      | P1_3     | IO   | UTIMER5 input event on channel B / output to driver B |
| UT5_T1_B      | P6_3     |      |                                                       |
| UT5_T1_C      | P11_3    |      |                                                       |
| UTIMER6 A/B/C |          |      |                                                       |
| UT6_T0_A      | P1_4     | IO   | UTIMER6 input event on channel A / output to driver A |
| UT6_T0_B      | P6_4     |      |                                                       |
| UT6_T0_C      | P11_4    |      |                                                       |
| UT6_T1_A      | P1_5     | IO   | UTIMER6 input event on channel B / output to driver B |
| UT6_T1_B      | P6_5     |      |                                                       |
| UT6_T1_C      | P11_5    |      |                                                       |
| UTIMER7 A/B/C |          |      |                                                       |
| UT7_T0_A      | P1_6     | IO   | UTIMER7 input event on channel A / output to driver A |
| UT7_T0_B      | P6_6     |      |                                                       |
| UT7_T0_C      | P11_6    |      |                                                       |
| UT7_T1_A      | P1_7     | IO   | UTIMER7 input event on channel B / output to driver B |
| UT7_T1_B      | P6_7     |      |                                                       |
| UT7_T1_C      | P11_7    |      |                                                       |
| UTIMER8 A/B/C |          |      |                                                       |
| UT8_T0_A      | P2_0     | IO   | UTIMER8 input event on channel A / output to driver A |
| UT8_T0_B      | P7_0     |      |                                                       |
| UT8_T0_C      | P12_0    |      |                                                       |
| UT8_T1_A      | P2_1     | IO   | UTIMER8 input event on channel B / output to driver B |
| UT8_T1_B      | P7_1     |      |                                                       |
| UT8_T1_C      | P12_1    |      |                                                       |
| UTIMER9 A/B/C |          |      |                                                       |
| UT9_T0_A      | P2_2     | IO   | UTIMER9 input event on channel A / output to driver A |

| Signal Name    | Pin Name | Type | Description                                             |
|----------------|----------|------|---------------------------------------------------------|
| UT9_T0_B       | P7_2     | IO   | UTIMER9 input event on channel B / output to driver B   |
| UT9_T0_C       | P12_2    |      |                                                         |
| UT9_T1_A       | P2_3     |      |                                                         |
| UT9_T1_B       | P7_3     |      |                                                         |
| UT9_T1_C       | P12_3    |      |                                                         |
| UTIMER10 A/B/C |          |      |                                                         |
| UT10_T0_A      | P2_4     | IO   | UTIMER10 input event on channel A / output to driver A  |
| UT10_T0_B      | P7_4     |      |                                                         |
| UT10_T0_C      | P12_4    |      |                                                         |
| UT10_T1_A      | P2_5     | IO   | UTIMER10 input event on channel B / output to driver B  |
| UT10_T1_B      | P7_5     |      |                                                         |
| UT10_T1_C      | P12_5    |      |                                                         |
| UTIMER11 A/B/C |          |      |                                                         |
| UT11_T0_A      | P2_6     | IO   | UTIMER11 input event on channel A / output to driver A  |
| UT11_T0_B      | P7_6     |      |                                                         |
| UT11_T0_C      | P12_6    |      |                                                         |
| UT11_T1_A      | P2_7     | IO   | UTIMER11 input event on channel B / output to driver B  |
| UT11_T1_B      | P7_7     |      |                                                         |
| UT11_T1_C      | P12_7    |      |                                                         |
| LPUTIMER0 A/B  |          |      |                                                         |
| LPUT0_T0_A     | P7_0     | IO   | LPUTIMER0 input event on channel A / output to driver A |
| LPUT0_T0_B     | P12_0    |      |                                                         |
| LPUT0_T1_A     | P7_1     |      | LPUTIMER0 input event on channel B / output to driver B |
| LPUT0_T1_B     | P12_1    |      |                                                         |
| LPUTIMER1 A/B  |          |      |                                                         |
| LPUT1_T0_A     | P7_2     | IO   | LPUTIMER1 input event on channel A / output to driver A |
| LPUT1_T0_B     | P12_2    |      |                                                         |
| LPUT1_T1_A     | P7_3     |      | LPUTIMER1 input event on channel B / output to driver B |
| LPUT1_T1_B     | P12_3    |      |                                                         |
| LPUTIMER2 A/B  |          |      |                                                         |
| LPUT2_T0_A     | P7_4     | IO   | LPUTIMER2 input event on channel A / output to driver A |
| LPUT2_T0_B     | P12_4    |      |                                                         |
| LPUT2_T1_A     | P7_5     |      | LPUTIMER2 input event on channel B / output to driver B |
| LPUT2_T1_B     | P12_5    |      |                                                         |

Table 3-11 presents UTIMER QEC interface signals and provides descriptions to their functions.

**Table 3-11 UTIMER QEC Signal Descriptions**

| Signal Name       | Pin Name | Type | Description                   |
|-------------------|----------|------|-------------------------------|
| <b>QEC0 A/B/C</b> |          |      |                               |
| QEC0_X_A          | P3_0     | I    | QEC0 input event on channel A |
| QEC0_X_B          | P8_4     |      |                               |
| QEC0_X_C          | P13_0    |      |                               |
| QEC0_Y_A          | P3_1     | I    | QEC0 input event on channel B |
| QEC0_Y_B          | P8_5     |      |                               |

| Signal Name | Pin Name | Type | Description                   |
|-------------|----------|------|-------------------------------|
| QEC0_Y_C    | P13_1    | I    | QEC0 input for zero signal    |
| QEC0_Z_A    | P3_2     |      |                               |
| QEC0_Z_B    | P8_6     |      |                               |
| QEC0_Z_C    | P13_2    |      |                               |
| QEC1 A/B/C  |          |      |                               |
| QEC1_X_A    | P3_3     | I    | QEC1 input event on channel A |
| QEC1_X_B    | P8_7     |      |                               |
| QEC1_X_C    | P13_3    |      |                               |
| QEC1_Y_A    | P3_4     | I    | QEC1 input event on channel B |
| QEC1_Y_B    | P9_0     |      |                               |
| QEC1_Y_C    | P13_4    |      |                               |
| QEC1_Z_A    | P3_5     | I    | QEC1 input for zero signal    |
| QEC1_Z_B    | P9_1     |      |                               |
| QEC1_Z_C    | P13_5    |      |                               |
| QEC2 A/B/C  |          |      |                               |
| QEC2_X_A    | P3_6     | I    | QEC2 input event on channel A |
| QEC2_X_B    | P9_2     |      |                               |
| QEC2_X_C    | P13_6    |      |                               |
| QEC2_Y_A    | P3_7     | I    | QEC2 input event on channel B |
| QEC2_Y_B    | P9_3     |      |                               |
| QEC2_Y_C    | P13_7    |      |                               |
| QEC2_Z_A    | P4_0     | I    | QEC2 input for zero signal    |
| QEC2_Z_B    | P9_4     |      |                               |
| QEC2_Z_C    | P14_0    |      |                               |
| QEC3 A/B/C  |          |      |                               |
| QEC3_X_A    | P4_1     | I    | QEC3 input event on channel A |
| QEC3_X_B    | P9_5     |      |                               |
| QEC3_X_C    | P14_1    |      |                               |
| QEC3_Y_A    | P4_2     | I    | QEC3 input event on channel B |
| QEC3_Y_B    | P9_6     |      |                               |
| QEC3_Y_C    | P14_2    |      |                               |
| QEC3_Z_A    | P4_3     | I    | QEC3 input for zero signal    |
| QEC3_Z_B    | P9_7     |      |                               |
| QEC3_Z_C    | P14_3    |      |                               |

Table 3-12 presents UTIMER common interface signals and provides descriptions to their functions.

**Table 3-12 UTIMER Common Signal Descriptions**

| Signal Name         | Pin Name | Type | Description                                                               |
|---------------------|----------|------|---------------------------------------------------------------------------|
| <b>Common A/B/C</b> |          |      |                                                                           |
| FAULT0_A            | P4_4     | I    | Fault signal 0. Used to trigger automatic shut-off of the output drivers. |
| FAULT0_B            | P8_0     |      |                                                                           |
| FAULT0_C            | P14_4    |      |                                                                           |
| FAULT1_A            | P4_5     | I    | Fault signal 1. Used to trigger automatic shut-off of the output drivers. |
| FAULT1_B            | P8_1     |      |                                                                           |

| Signal Name | Pin Name | Type | Description                                                               |
|-------------|----------|------|---------------------------------------------------------------------------|
| FAULT1_C    | P14_5    |      |                                                                           |
| FAULT2_A    | P4_6     | I    | Fault signal 2. Used to trigger automatic shut-off of the output drivers. |
| FAULT2_B    | P8_2     |      |                                                                           |
| FAULT2_C    | P14_6    |      |                                                                           |
| FAULT3_A    | P4_7     | I    | Fault signal 3. Used to trigger automatic shut-off of the output drivers. |
| FAULT3_B    | P8_3     |      |                                                                           |
| FAULT3_C    | P14_7    |      |                                                                           |

### 3.15.3 WDT\_RTSS Overview

The Real-Time Subsystem Watchdog Timer module, hereinafter referred to as WDT\_RTSS, is a timer based on a 32-bit down-counter. The basic function of the WDT\_RTSS is to count for a fixed period, during which it expects to be serviced by the system, indicating normal operation. The WDT\_RTSS provides a mechanism to detect errant system behavior and recover from an unknown state by causing Non-Maskable Interrupt (NMI) of the system if the count period elapses without intervention.

The device includes up to two WDT\_RTSS modules:

- WDT\_HP: Dedicated to the Arm Cortex-M55 High-Performance (M55-HP) processor
- WDT\_HE: Dedicated to the Arm Cortex-M55 High-Efficiency (M55-HE) processor

The WDT\_RTSS module supports the following main features:

- 32-bit down-counter
- Counter decrements by one on each positive watchdog clock edge
- Configurable NMI generation upon watch period expiration
- Configurable CPU reset upon watch period expiration

### 3.15.4 WDT\_APSS Overview

The Application Subsystem Watchdog Timer, hereinafter referred to as WDT\_APSS, is based on a 64-bit compare value and comparator. The WDT\_APSS uses the generic timer system counter as the time base against which the decision to trigger an interrupt is made. The compare value can either be loaded directly or indirectly on an explicit refresh or timeout refresh.

The device includes up to two WDT\_APSS modules:

- WDT\_AP is the non-secure timer in the APSS
- WDT\_AP\_S is the secure timer in the APSS

The WDT\_APSS module supports the following main features:

- 64-bit comparator
- Counter decrements by one on each generic timer system counter clock
- Configurable NMI generation upon watch period expiration:
  - WDT\_AP provides two interrupts routed to the A32 GIC
  - WDT\_AP\_S provides one NMI routed to the A32 GIC and a second interrupt routed to the Secure Enclave
- Configurable CPU reset upon watch period expiration

### 3.15.5 LPRTC Overview

The Low-Power Real-Time Counter (LPRTC) module is a configurable high-range binary counter, which can generate an interrupt on a user-specified interval.

The device includes one LPRTC module located in the PD-0 power domain, allowing it to run even when the device is in the lowest power state and power is present on VDD\_BATT.

The LPRTC module supports the following main features:

- 32.768 kHz typical reference clock
- 32-bit incrementing counter
- 16-bit programmable prescaler
- Interrupt generation upon programmed count match
- Counter wrap mode
- The LPRTC interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

---

#### NOTE

All Low Power peripherals are single-master accessible, including LPRTC. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

---

The LPRTC module can be utilized for the following use cases:

- Real-time clock—to keep track of the current time
- Long-term exact chronometer—to keep track of time from now up to 136 years in the future (when clocked with a 1 Hz clock signal)
- Alarm function—to generate an interrupt after a programmed number of cycles
- Long time base counter—when clocked with a kHz range clock signal from either LFXO or LFRC

### 3.15.6 System Timers Overview

The system timer is composed of one counter and several timer modules. The counter provides count value to the timer modules, which generate interrupts when a certain timer condition is met.

The device includes two system timers – REFCLK\_TMR and S32KCLK\_TMR. The REFCLK\_TMR system timer is clocked by SYST\_REFCLK and has four timer modules – REFCLK\_CNT\_BASE[0-3]. The S32KCLK\_TMR system timer is clocked by S32K\_CLK and has two timer modules – S32KCLK\_CNT\_BASE[0-1].

Each system timer supports the following main features:

- Provides a uniform view of system time
- Provides 64-bit up counters and 32-bit down counters
- Has 64-bit wide counter and compare registers
- Supports virtual time by offsetting the real time via dedicated registers
- Can be incremented by larger amounts at a lower frequency (for example, increment by 4 at 4 times lower frequency)
- Has individual interrupt output for each timer module (CNT\_BASEn)

## 3.16 General-Purpose Input/Output Module

The General-Purpose Input/Output (GPIO) module provides means for driving and reading from digital I/O pins when they are not used by other peripheral (like UART, I2C, etc.). GPIO module can be used for tasks like lighting LEDs or reading the state of push-buttons, switches, etc. The GPIO module also offers switch contact debounce and interrupt capabilities.

The device includes up to nineteen GPIO modules with support of up to 144 I/O pins in total. The I/O signals are distributed as follows:

- GPIO[0-14, 16-17]: 8 I/O signals each
- LPGPIO: 8 I/O signals
- LPGPIO\_FAST: Shares I/O signals with LPGPIO

The I/O pins are typically powered by VDD\_IO\_1V8 with the exception of 8 I/O pins, which are powered by the VDD\_IO\_FLEX rail that is 1.8 V or 3.3 V.

The GPIO modules are integrated in four power domains:

- Power Domain PD-6: GPIO[0-14]
- Power Domain PD-2: GPIO[16-17]
- Power Domain PD-0 (AON): LPGPIO
- Power Domain PD-3: LPGPIO\_FAST

Each GPIO module supports the following main features:

- Data register allows driving and reading each GPIO pin individually
- Data Direction register selects pin direction – input or output
- Bit manipulation registers for GPIO pin set, clear, and toggle
- Debounce function driven by the 32-kHz clock for switch/push-button contacts debouncing
- Individual interrupt generation for every pin of GPIO[0-14] and LPGPIO/LPGPIO\_FAST
- Common (combined) interrupt generation for the pin events of GPIO[16-17] and LPGPIO/LPGPIO\_FAST
- The LPGPIO/LPGPIO\_FAST interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

#### NOTE

All Low Power peripherals are single-master accessible, including LPGPIO/LPGPIO\_FAST. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-13 presents GPIO interface signals and provides descriptions to their functions.

**Table 3-13 GPIO Signal Descriptions**

| Signal Name  | Pin Name | Type | Description                                 |
|--------------|----------|------|---------------------------------------------|
| <b>GPIO0</b> |          |      |                                             |
| GPIO0_0      | P0_0     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO0_1      | P0_1     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO0_2      | P0_2     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO0_3      | P0_3     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO0_4      | P0_4     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO0_5      | P0_5     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO0_6      | P0_6     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO0_7      | P0_7     | IO   | General-purpose input/output <sup>(1)</sup> |
| <b>GPIO1</b> |          |      |                                             |
| GPIO1_0      | P1_0     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO1_1      | P1_1     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO1_2      | P1_2     | IO   | General-purpose input/output <sup>(1)</sup> |

| Signal Name  | Pin Name | Type | Description                                 |
|--------------|----------|------|---------------------------------------------|
| GPIO1_3      | P1_3     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO1_4      | P1_4     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO1_5      | P1_5     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO1_6      | P1_6     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO1_7      | P1_7     | IO   | General-purpose input/output <sup>(1)</sup> |
| <b>GPIO2</b> |          |      |                                             |
| GPIO2_0      | P2_0     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO2_1      | P2_1     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO2_2      | P2_2     | IO   | General-purpose input/output <sup>(2)</sup> |
| GPIO2_3      | P2_3     | IO   | General-purpose input/output <sup>(2)</sup> |
| GPIO2_4      | P2_4     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO2_5      | P2_5     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO2_6      | P2_6     | IO   | General-purpose input/output <sup>(1)</sup> |
| GPIO2_7      | P2_7     | IO   | General-purpose input/output <sup>(1)</sup> |
| <b>GPIO3</b> |          |      |                                             |
| GPIO3_0      | P3_0     | IO   | General-purpose input/output                |
| GPIO3_1      | P3_1     | IO   | General-purpose input/output                |
| GPIO3_2      | P3_2     | IO   | General-purpose input/output                |
| GPIO3_3      | P3_3     | IO   | General-purpose input/output                |
| GPIO3_4      | P3_4     | IO   | General-purpose input/output                |
| GPIO3_5      | P3_5     | IO   | General-purpose input/output                |
| GPIO3_6      | P3_6     | IO   | General-purpose input/output                |
| GPIO3_7      | P3_7     | IO   | General-purpose input/output                |
| <b>GPIO4</b> |          |      |                                             |
| GPIO4_0      | P4_0     | IO   | General-purpose input/output                |
| GPIO4_1      | P4_1     | IO   | General-purpose input/output                |
| GPIO4_2      | P4_2     | IO   | General-purpose input/output                |
| GPIO4_3      | P4_3     | IO   | General-purpose input/output                |
| GPIO4_4      | P4_4     | IO   | General-purpose input/output                |
| GPIO4_5      | P4_5     | IO   | General-purpose input/output                |
| GPIO4_6      | P4_6     | IO   | General-purpose input/output                |
| GPIO4_7      | P4_7     | IO   | General-purpose input/output                |
| <b>GPIO5</b> |          |      |                                             |
| GPIO5_0      | P5_0     | IO   | General-purpose input/output                |
| GPIO5_1      | P5_1     | IO   | General-purpose input/output                |
| GPIO5_2      | P5_2     | IO   | General-purpose input/output                |
| GPIO5_3      | P5_3     | IO   | General-purpose input/output                |
| GPIO5_4      | P5_4     | IO   | General-purpose input/output                |
| GPIO5_5      | P5_5     | IO   | General-purpose input/output                |
| GPIO5_6      | P5_6     | IO   | General-purpose input/output                |
| GPIO5_7      | P5_7     | IO   | General-purpose input/output                |
| <b>GPIO6</b> |          |      |                                             |
| GPIO6_0      | P6_0     | IO   | General-purpose input/output                |
| GPIO6_1      | P6_1     | IO   | General-purpose input/output                |
| GPIO6_2      | P6_2     | IO   | General-purpose input/output                |

| Signal Name   | Pin Name | Type | Description                                 |
|---------------|----------|------|---------------------------------------------|
| GPIO6_3       | P6_3     | IO   | General-purpose input/output                |
| GPIO6_4       | P6_4     | IO   | General-purpose input/output                |
| GPIO6_5       | P6_5     | IO   | General-purpose input/output                |
| GPIO6_6       | P6_6     | IO   | General-purpose input/output                |
| GPIO6_7       | P6_7     | IO   | General-purpose input/output                |
| <b>GPIO7</b>  |          |      |                                             |
| GPIO7_0       | P7_0     | IO   | General-purpose input/output                |
| GPIO7_1       | P7_1     | IO   | General-purpose input/output                |
| GPIO7_2       | P7_2     | IO   | General-purpose input/output                |
| GPIO7_3       | P7_3     | IO   | General-purpose input/output                |
| GPIO7_4       | P7_4     | IO   | General-purpose input/output <sup>(3)</sup> |
| GPIO7_5       | P7_5     | IO   | General-purpose input/output <sup>(3)</sup> |
| GPIO7_6       | P7_6     | IO   | General-purpose input/output <sup>(3)</sup> |
| GPIO7_7       | P7_7     | IO   | General-purpose input/output <sup>(3)</sup> |
| <b>GPIO8</b>  |          |      |                                             |
| GPIO8_0       | P8_0     | IO   | General-purpose input/output                |
| GPIO8_1       | P8_1     | IO   | General-purpose input/output                |
| GPIO8_2       | P8_2     | IO   | General-purpose input/output                |
| GPIO8_3       | P8_3     | IO   | General-purpose input/output                |
| GPIO8_4       | P8_4     | IO   | General-purpose input/output                |
| GPIO8_5       | P8_5     | IO   | General-purpose input/output                |
| GPIO8_6       | P8_6     | IO   | General-purpose input/output                |
| GPIO8_7       | P8_7     | IO   | General-purpose input/output                |
| <b>GPIO9</b>  |          |      |                                             |
| GPIO9_0       | P9_0     | IO   | General-purpose input/output                |
| GPIO9_1       | P9_1     | IO   | General-purpose input/output                |
| GPIO9_2       | P9_2     | IO   | General-purpose input/output                |
| GPIO9_3       | P9_3     | IO   | General-purpose input/output                |
| GPIO9_4       | P9_4     | IO   | General-purpose input/output                |
| GPIO9_5       | P9_5     | IO   | General-purpose input/output                |
| GPIO9_6       | P9_6     | IO   | General-purpose input/output                |
| GPIO9_7       | P9_7     | IO   | General-purpose input/output                |
| <b>GPIO10</b> |          |      |                                             |
| GPIO10_0      | P10_0    | IO   | General-purpose input/output                |
| GPIO10_1      | P10_1    | IO   | General-purpose input/output                |
| GPIO10_2      | P10_2    | IO   | General-purpose input/output                |
| GPIO10_3      | P10_3    | IO   | General-purpose input/output                |
| GPIO10_4      | P10_4    | IO   | General-purpose input/output                |
| GPIO10_5      | P10_5    | IO   | General-purpose input/output                |
| GPIO10_6      | P10_6    | IO   | General-purpose input/output                |
| GPIO10_7      | P10_7    | IO   | General-purpose input/output                |
| <b>GPIO11</b> |          |      |                                             |
| GPIO11_0      | P11_0    | IO   | General-purpose input/output                |
| GPIO11_1      | P11_1    | IO   | General-purpose input/output                |
| GPIO11_2      | P11_2    | IO   | General-purpose input/output                |

| Signal Name   | Pin Name | Type | Description                  |
|---------------|----------|------|------------------------------|
| GPIO11_3      | P11_3    | IO   | General-purpose input/output |
| GPIO11_4      | P11_4    | IO   | General-purpose input/output |
| GPIO11_5      | P11_5    | IO   | General-purpose input/output |
| GPIO11_6      | P11_6    | IO   | General-purpose input/output |
| GPIO11_7      | P11_7    | IO   | General-purpose input/output |
| <b>GPIO12</b> |          |      |                              |
| GPIO12_0      | P12_0    | IO   | General-purpose input/output |
| GPIO12_1      | P12_1    | IO   | General-purpose input/output |
| GPIO12_2      | P12_2    | IO   | General-purpose input/output |
| GPIO12_3      | P12_3    | IO   | General-purpose input/output |
| GPIO12_4      | P12_4    | IO   | General-purpose input/output |
| GPIO12_5      | P12_5    | IO   | General-purpose input/output |
| GPIO12_6      | P12_6    | IO   | General-purpose input/output |
| GPIO12_7      | P12_7    | IO   | General-purpose input/output |
| <b>GPIO13</b> |          |      |                              |
| GPIO13_0      | P13_0    | IO   | General-purpose input/output |
| GPIO13_1      | P13_1    | IO   | General-purpose input/output |
| GPIO13_2      | P13_2    | IO   | General-purpose input/output |
| GPIO13_3      | P13_3    | IO   | General-purpose input/output |
| GPIO13_4      | P13_4    | IO   | General-purpose input/output |
| GPIO13_5      | P13_5    | IO   | General-purpose input/output |
| GPIO13_6      | P13_6    | IO   | General-purpose input/output |
| GPIO13_7      | P13_7    | IO   | General-purpose input/output |
| <b>GPIO14</b> |          |      |                              |
| GPIO14_0      | P14_0    | IO   | General-purpose input/output |
| GPIO14_1      | P14_1    | IO   | General-purpose input/output |
| GPIO14_2      | P14_2    | IO   | General-purpose input/output |
| GPIO14_3      | P14_3    | IO   | General-purpose input/output |
| GPIO14_4      | P14_4    | IO   | General-purpose input/output |
| GPIO14_5      | P14_5    | IO   | General-purpose input/output |
| GPIO14_6      | P14_6    | IO   | General-purpose input/output |
| GPIO14_7      | P14_7    | IO   | General-purpose input/output |
| <b>GPIO16</b> |          |      |                              |
| GPIO16_0      | P16_0    | IO   | General-purpose input/output |
| GPIO16_1      | P16_1    | IO   | General-purpose input/output |
| GPIO16_2      | P16_2    | IO   | General-purpose input/output |
| GPIO16_3      | P16_3    | IO   | General-purpose input/output |
| GPIO16_4      | P16_4    | IO   | General-purpose input/output |
| GPIO16_5      | P16_5    | IO   | General-purpose input/output |
| GPIO16_6      | P16_6    | IO   | General-purpose input/output |
| GPIO16_7      | P16_7    | IO   | General-purpose input/output |
| <b>GPIO17</b> |          |      |                              |
| GPIO17_0      | P17_0    | IO   | General-purpose input/output |
| GPIO17_1      | P17_1    | IO   | General-purpose input/output |
| GPIO17_2      | P17_2    | IO   | General-purpose input/output |

| Signal Name   | Pin Name | Type | Description                                           |
|---------------|----------|------|-------------------------------------------------------|
| GPIO17_3      | P17_3    | IO   | General-purpose input/output                          |
| GPIO17_4      | P17_4    | IO   | General-purpose input/output                          |
| GPIO17_5      | P17_5    | IO   | General-purpose input/output                          |
| GPIO17_6      | P17_6    | IO   | General-purpose input/output                          |
| GPIO17_7      | P17_7    | IO   | General-purpose input/output                          |
| <b>LPGPIO</b> |          |      |                                                       |
| GPIOV_0       | P15_0    | IO   | Low-power general-purpose input/output <sup>(3)</sup> |
| GPIOV_1       | P15_1    | IO   | Low-power general-purpose input/output <sup>(3)</sup> |
| GPIOV_2       | P15_2    | IO   | Low-power general-purpose input/output <sup>(3)</sup> |
| GPIOV_3       | P15_3    | IO   | Low-power general-purpose input/output <sup>(3)</sup> |
| GPIOV_4       | P15_4    | IO   | Low-power general-purpose input/output                |
| GPIOV_5       | P15_5    | IO   | Low-power general-purpose input/output                |
| GPIOV_6       | P15_6    | IO   | Low-power general-purpose input/output                |
| GPIOV_7       | P15_7    | IO   | Low-power general-purpose input/output                |

1. Serves also as analog input. See [Section 3.21.6 Analog Signals](#).
2. Serves also as analog input/output. See [Section 3.21.6 Analog Signals](#).
3. Powered by VDD\_IO\_FLEX supply rail

## 3.17 Communication Peripherals

### 3.17.1 CANFD Overview

The Controller Area Network (CANFD) module performs serial communication according to the CAN protocol. The CAN bus interface uses the basic CAN principle and meets all constraints of the CAN Specification 2.0B active. The CANFD module supports both classic CAN and CAN with Flexible Data-rate (FD) specifications.

The device includes up to one CANFD module.

The CANFD module supports the following main features:

- CAN specifications:
  - CAN 2.0B (up to 8 bytes payload, verified by Bosch reference model)
  - CAN FD (up to 64 bytes payload, ISO 11898-1:2015 or non-ISO Bosch)
- Free programmable data rates:
  - Data rates up to 10 Mbps
  - CAN FD rates are limited by the transceiver and the clock frequency of the CAN controller
- Programmable baud rate prescaler (1 to 1/256)
- One receive buffer and two transmit buffers—primary transmit buffer (PTB) and secondary transmit buffer (STB):
  - Buffer size: 640 words
  - Number of buffer slots: 16
- 3× independent and programmable internal 29-bit acceptance filters
- Extended features:
  - Single Shot Transmission mode (for PTB and/or for STB)
  - Listen-Only mode
  - Loop Back mode (internal and external)
  - Transceiver Standby mode
- Extended status and error report:
  - Capturing of last occurred Kind Of Error (KOER) and arbitration lost position
  - Programmable Error Warning Limit

- 32-bit synchronous Host controller interfaces
- Configurable interrupt sources
- Dual port memory block for frame buffer
- CiA 603 32-bit timestamping
- Compatible with AUTOSAR
- Optimized for SAE J1939

Table 3-14 presents CANFD interface signals and provides descriptions to their functions.

**Table 3-14 CANFD Signal Descriptions**

| Signal Name        | Pin Name | Type | Description                                             |
|--------------------|----------|------|---------------------------------------------------------|
| <b>CANFD A/B/C</b> |          |      |                                                         |
| CAN_RXD_A          | P7_0     | I    | CANFD serial data input (from external CAN transceiver) |
| CAN_RXD_B          | P0_4     |      |                                                         |
| CAN_RXD_C          | P12_4    |      |                                                         |
| CAN_TXD_A          | P7_1     | O    | CANFD serial data output (to external CAN transceiver)  |
| CAN_TXD_B          | P0_5     |      |                                                         |
| CAN_TXD_C          | P12_5    |      |                                                         |
| CAN_STBY_A         | P7_3     | O    | CANFD transceiver standby mode signal                   |
| CAN_STBY_B         | P0_6     |      |                                                         |
| CAN_STBY_C         | P12_6    |      |                                                         |

### 3.17.2 CRC Overview

The Cyclic Redundancy Check (CRC) calculation module can produce 8-, 16-, and 32-bit codes for variety of polynomials. This function is used to validate the integrity of a communication packet received or the integrity of a binary image that is an update candidate. This is achieved by computing and comparing the CRC code with the one received after the data packet transmission.

The device includes up to two CRC modules.

Each CRC module has the following main features:

- Built-in support for the following CRC algorithms:
  - CRC-8-CCITT
  - CRC-16
  - CRC-16-CCITT
  - CRC-32
  - CRC-32C
- Support of customized polynomials configured by register settings
- 8- or 32-bits of data processed at a time
- Configurable byte and bit swapping of data

### 3.17.3 ETH Overview

The Ethernet Controller (ETH) enables the device to transmit and receive data over Ethernet in compliance with IEEE 802.3-2008.

The device includes one ETH module.

The ETH module supports the following main features:

- Compliance with standards:
  - IEEE 1588-2008 standard for precision networked clock synchronization
  - RMII specification version 1.2 from RMII consortium

- **MAC features:**
  - 10 and 100 Mbps data transfer rates with RMI interface to communicate with an external fast Ethernet PHY
  - Full-duplex operation:
    - IEEE 802.3x flow control automatic transmission of zero-quanta pause frame on flow control input de-assertion
    - Forwarding of received pause frames to the user application
  - Half-duplex operation:
    - CSMA/CD protocol support
    - Flow control using backpressure support
  - Preamble and Start of Frame Data (SFD) insertion in transmit path
  - Preamble and Start Frame Delimiter (SFD) deletion in the receive path
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Automatic pad and CRC stripping options for receive frames
  - Programmable frame length to support standard or jumbo Ethernet frames of up to 16KB
  - Programmable Interframe Gap (IFG) (40-bit to 96-bit times in steps of 8)
  - Transmit frames with reduced preamble size
  - Separate 32-bit status for transmit and receive packets
  - IEEE 802.1Q VLAN tag detection for reception frames
  - Separate transmission, reception, and control interfaces to the application
  - Little-endian for transmit and receive paths
  - 64-bit data transfer interface on system-side
  - Detection of remote wake-up frames
  - Receive module for checksum off-load for received IPv4 and TCP packets encapsulated by the Ethernet frame (Type 1)
  - Receive module for checking IPv4 header checksum and TCP, UDP, or ICMP checksum encapsulated in IPv4 or IPv6 datagrams (Type 2)
  - MDIO master interface for PHY device configuration and management
  - Programmable watchdog timeout limit in the receive path
  - Programmable jabber timeout in the range of 2 KB to 16383 bytes (with 1 KB granularity) in the transmit path
- **MAC Transaction Layer (MTL) features:**
  - 2KB transmit FIFO with programmable threshold
  - 2KB receive FIFO with programmable threshold
  - Single-channel transmit and receive engines
  - Data transfers executed using simple FIFO protocol
  - Optimization for packet-oriented transfers with frame delimiters
  - Programmable burst length for starting a burst up to half the size of the MTL Rx and Tx FIFO
  - Insertion of receive status vectors into the receive FIFO after the EOF transfer
  - Store and forward mechanism for transmission to the MAC
  - Automatic generation of pause frame control or backpressure signal to the MAC based on receive FIFO-fill (threshold configurable) level
  - Automatic retransmission of collision frames for transmission
  - Discard frames on late collision, excessive collisions, excessive deferral, and under-run conditions
  - Software control to flush the transmit FIFO
- **DMA features:**
  - Exchanges data between the MTL block and system memory
  - Single-channel transmit and receive engines
  - Optimization for packet-oriented DMA transfers with frame delimiters

- Byte-aligned addressing for data buffer support
- Descriptor architecture to allow large blocks of data transfer with minimum CPU intervention (each descriptor can transfer up to 8KB of data)
- Comprehensive status reporting for normal operation and transfers with errors
- Individual programmable burst size for transmit and receive DMA engines for optimal system bus utilization
- Programmable interrupt options for different operational conditions
- Per-frame transmit or receive complete interrupt control
- Round-robin or fixed-priority arbitration between receive and transmit engines
- Monitoring and testing features:
  - DMA states (Tx and Rx) as status bits
  - Status registers that give status of FSMs in transmit and receive data-paths and FIFO fill levels
  - Application abort status bits
  - Current Tx/Rx buffer pointer as status registers
  - Current Tx/Rx descriptor pointer as status registers

Table 3-15 presents Ethernet interface signals and provides descriptions to their functions.

**Table 3-15 Ethernet Signal Descriptions**

| Signal Name      | Pin Name | Type | Description                                |
|------------------|----------|------|--------------------------------------------|
| <b>ETH A/B/C</b> |          |      |                                            |
| ETH_RXD0_A       | P5_5     | I    | ETH PHY receive data bit 0                 |
| ETH_RXD0_B       | P11_3    |      |                                            |
| ETH_RXD0_C       | P1_0     |      |                                            |
| ETH_TXD0_A       | P6_0     | O    | ETH PHY transmit data bit 0                |
| ETH_TXD0_B       | P10_4    |      |                                            |
| ETH_TXD0_C       | P1_3     |      |                                            |
| ETH_RXD1_A       | P5_6     | I    | ETH PHY receive data bit 1                 |
| ETH_RXD1_B       | P11_4    |      |                                            |
| ETH_RXD1_C       | P1_1     |      |                                            |
| ETH_TXD1_A       | P6_1     | O    | ETH PHY transmit data bit 1                |
| ETH_TXD1_B       | P10_5    |      |                                            |
| ETH_TXD1_C       | P1_4     |      |                                            |
| ETH_TXEN_A       | P6_2     | O    | ETH PHY transmit data enable               |
| ETH_TXEN_B       | P10_6    |      |                                            |
| ETH_TXEN_C       | P1_5     |      |                                            |
| ETH_CRSDV_A      | P6_7     | I    | ETH carrier sense/receive data valid       |
| ETH_CRSDV_B      | P11_5    |      |                                            |
| ETH_CRSDV_C      | P2_2     |      |                                            |
| ETH_RST_A        | P5_7     | O    | ETH reset to the external PHY module       |
| ETH_RST_B        | P11_6    |      |                                            |
| ETH_RST_C        | P1_2     |      |                                            |
| ETH_IRQ_A        | P6_3     | I    | ETH interrupt from the external PHY module |
| ETH_IRQ_B        | P11_7    |      |                                            |
| ETH_IRQ_C        | P1_6     |      |                                            |
| ETH_REFCLK_A     | P6_4     | IO   | ETH 50-MHz reference clock                 |
| ETH_REFCLK_B     | P11_0    |      |                                            |
| ETH_REFCLK_C     | P1_7     |      |                                            |

| Signal Name | Pin Name | Type | Description                |
|-------------|----------|------|----------------------------|
| ETH_MDIO_A  | P6_5     | IO   | ETH management data in/out |
| ETH_MDIO_B  | P11_1    |      |                            |
| ETH_MDIO_C  | P2_0     |      |                            |
| ETH_MDC_A   | P6_6     | O    | ETH management data clock  |
| ETH_MDC_B   | P11_2    |      |                            |
| ETH_MDC_C   | P2_1     |      |                            |

### 3.17.4 I2C Overview

The Inter-Integrated Circuit (I2C) module is a synchronous, master/slave serial communication bus which is suitable for different system control applications.

The device includes:

- Up to four I2C modules in Shared Peripherals
- Two Low-Power I2C modules (LPI2C0 slave-only and LPI2C1 master-only) in the RTSS-HE

The I2C and LPI2C1 modules support the following main features:

- Operating bus speed:
  - Standard Speed (SS) mode (up to 100 kbps)
  - Fast Speed (FS) mode (up to 400 kbps)
  - Fast Mode Plus (FM+) mode (up to 1 Mbps)
  - High Speed (HS) mode (up to 3.4 Mbps)
- Master or slave operation (LPI2C1 is master-only)
- 7- or 10-bit addressing
- 7- or 10-bit combined format transfers
- 32-byte deep receive and transmit FIFOs
- Bulk transmit mode
- Interrupt or polled-mode operation
- Bit and byte waiting at all bus speeds
- DMA handshaking interface
- Programmable SDA hold time
- Bus clear feature

The LPI2C0 module supports the following main features:

- Operating bus speed:
  - Standard Speed (SS) mode (up to 100 kbps)
  - Fast Speed (FS) mode (up to 400 kbps)
- Slave operation only
- 7-bit addressing only
- Hardcoded slave bus address (0x40)
- 8-byte deep inbound and outbound FIFOs
- Interrupt or polled-mode operation
- The LPI2C interrupt can be used as a wake-up source from STANDBY low-power mode

## NOTE

All Low Power peripherals are single-master accessible, including LPI2C. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-16 presents I2C interface signals and provides descriptions to their functions.

**Table 3-16 I2C Signal Descriptions**

| Signal Name  | Pin Name | Type | Description                                                                   |
|--------------|----------|------|-------------------------------------------------------------------------------|
| I2C0 A/B/C/D |          |      |                                                                               |
| I2C0_SCL_A   | P0_3     | IO   | I2C0 serial clock line. Open-drain output driver, requires external pull-up.  |
| I2C0_SCL_B   | P3_4     |      |                                                                               |
| I2C0_SCL_C   | P7_1     |      |                                                                               |
| I2C0_SCL_D   | P10_5    |      |                                                                               |
| I2C0_SDA_A   | P0_2     | IO   | I2C0 serial data line. Open-drain output driver, requires external pull-up.   |
| I2C0_SDA_B   | P3_5     |      |                                                                               |
| I2C0_SDA_C   | P7_0     |      |                                                                               |
| I2C0_SDA_D   | P10_4    |      |                                                                               |
| I2C1 A/B/C/D |          |      |                                                                               |
| I2C1_SCL_A   | P0_5     | IO   | I2C1 serial clock line. Open-drain output driver, requires external pull-up.  |
| I2C1_SCL_B   | P3_7     |      |                                                                               |
| I2C1_SCL_C   | P7_3     |      |                                                                               |
| I2C1_SCL_D   | P10_7    |      |                                                                               |
| I2C1_SDA_A   | P0_4     | IO   | I2C1 serial data line. Open-drain output driver, requires external pull-up.   |
| I2C1_SDA_B   | P3_6     |      |                                                                               |
| I2C1_SDA_C   | P7_2     |      |                                                                               |
| I2C1_SDA_D   | P10_6    |      |                                                                               |
| I2C2 A/B/C   |          |      |                                                                               |
| I2C2_SCL_A   | P0_6     | IO   | I2C2 serial clock line. Open-drain output driver, requires external pull-up.  |
| I2C2_SCL_B   | P5_1     |      |                                                                               |
| I2C2_SCL_C   | P5_6     |      |                                                                               |
| I2C2_SDA_A   | P0_7     | IO   | I2C2 serial data line. Open-drain output driver, requires external pull-up.   |
| I2C2_SDA_B   | P5_0     |      |                                                                               |
| I2C2_SDA_C   | P5_7     |      |                                                                               |
| I2C3 A/B/C   |          |      |                                                                               |
| I2C3_SCL_A   | P1_1     | IO   | I2C3 serial clock line. Open-drain output driver, requires external pull-up.  |
| I2C3_SCL_B   | P9_7     |      |                                                                               |
| I2C3_SCL_C   | P9_5     |      |                                                                               |
| I2C3_SDA_A   | P1_0     | IO   | I2C3 serial data line. Open-drain output driver, requires external pull-up.   |
| I2C3_SDA_B   | P9_6     |      |                                                                               |
| I2C3_SDA_C   | P9_4     |      |                                                                               |
| LPI2C0 A/B   |          |      |                                                                               |
| LPI2C0_SCL_A | P7_4     | I    | LPI2C0 serial clock line. Slave-only, requires external pull-up.              |
| LPI2C0_SCL_B | P5_2     |      |                                                                               |
| LPI2C0_SDA_A | P7_5     | IO   | LPI2C0 serial data line. Open-drain output driver, requires external pull-up. |

| Signal Name         | Pin Name | Type | Description                                                                    |
|---------------------|----------|------|--------------------------------------------------------------------------------|
| LPI2C0_SDA_B        | P5_3     |      |                                                                                |
| <b>LPI2C1 A/B/C</b> |          |      |                                                                                |
| LPI2C1_SCL_A        | P4_3     | IO   | LPI2C1 serial clock line. Open-drain output driver, requires external pull-up. |
| LPI2C1_SCL_B        | P6_6     |      |                                                                                |
| LPI2C1_SCL_C        | P7_7     |      |                                                                                |
| LPI2C1_SDA_A        | P4_2     | IO   | LPI2C1 serial data line. Open-drain output driver, requires external pull-up.  |
| LPI2C1_SDA_B        | P6_5     |      |                                                                                |
| LPI2C1_SDA_C        | P7_6     |      |                                                                                |

### 3.17.5 I2S Overview

The Inter-IC Sound (I<sup>2</sup>S™) is a low pin count, serial bus standard for a stereo audio data link between ADCs, DACs, CODECs, DSPs, and others. As the I<sup>2</sup>S only handles the transfer of audio data, the control and sub-coding signals need to be transferred separately using a different bus interface (such as I<sup>2</sup>C).

The device includes:

- Up to four I2S modules in Shared Peripherals
- One Low-Power I2S module (LPI2S) in the RTSS-HE

Each I2S module supports the following main features:

- I<sup>2</sup>S transmitter and receiver based on the Philips I<sup>2</sup>S serial protocol
- One stereo channel for transmitter and one for receiver
- Full duplex communication due to the independence of transmitter and receiver
- Master mode of operation
- Two input clock sources: 76.8 MHz or external audio clock
- 8, 16, 32, 44.1, 48, 88.2, 96, and 192 kHz sampling frequencies
- 16, 24, or 32 clocks word-select cycles (left/right audio channel select)
- 12, 16, 20, 24, and 32 bits of audio data resolution
- FIFO depth of 16 words for each of receiver and transmitter
- Programmable FIFO thresholds
- DMA hardware handshaking interface
- Time Division Multiplexed (TDM) interface
- 32-bit APB data bus

#### NOTE

All Low Power peripherals are single-master accessible, including LPI2S. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-17 presents I2S interface signals and provides descriptions to their functions.

**Table 3-17 I2S Signal Descriptions**

| Signal Name     | Pin Name | Type | Description       |
|-----------------|----------|------|-------------------|
| <b>I2S0 A/B</b> |          |      |                   |
| I2S0_SCLK_A     | P3_0     | O    | I2S0 serial clock |
| I2S0_SCLK_B     | P4_3     |      |                   |

| Signal Name  | Pin Name | Type | Description                   |
|--------------|----------|------|-------------------------------|
| I2S0_SDI_A   | P1_6     | I    | I2S0 serial data input line   |
| I2S0_SDI_B   | P4_1     |      |                               |
| I2S0_SDO_A   | P1_7     | O    | I2S0 serial data output line  |
| I2S0_SDO_B   | P4_2     |      |                               |
| I2S0_WS_A    | P3_1     | O    | I2S0 word select line         |
| I2S0_WS_B    | P4_4     |      |                               |
| I2S1 A/B     |          |      |                               |
| I2S1_SCLK_A  | P3_4     | O    | I2S1 serial clock             |
| I2S1_SCLK_B  | P12_2    |      |                               |
| I2S1_SDI_A   | P3_2     | I    | I2S1 serial data input line   |
| I2S1_SDI_B   | P12_0    |      |                               |
| I2S1_SDO_A   | P3_3     | O    | I2S1 serial data output line  |
| I2S1_SDO_B   | P12_1    |      |                               |
| I2S1_WS_A    | P4_0     | O    | I2S1 word select line         |
| I2S1_WS_B    | P12_3    |      |                               |
| I2S2 A/B     |          |      |                               |
| I2S2_SCLK_A  | P8_3     | O    | I2S2 serial clock             |
| I2S2_SCLK_B  | P10_7    |      |                               |
| I2S2_SDI_A   | P8_1     | I    | I2S2 serial data input line   |
| I2S2_SDI_B   | P10_5    |      |                               |
| I2S2_SDO_A   | P8_2     | O    | I2S2 serial data output line  |
| I2S2_SDO_B   | P10_6    |      |                               |
| I2S2_WS_A    | P8_4     | O    | I2S2 word select line         |
| I2S2_WS_B    | P11_0    |      |                               |
| I2S3 A/B     |          |      |                               |
| I2S3_SCLK_A  | P9_4     | O    | I2S3 serial clock             |
| I2S3_SCLK_B  | P8_6     |      |                               |
| I2S3_SDI_A   | P9_2     | I    | I2S3 serial data input line   |
| I2S3_SDI_B   | P9_0     |      |                               |
| I2S3_SDO_A   | P9_3     | O    | I2S3 serial data output line  |
| I2S3_SDO_B   | P9_1     |      |                               |
| I2S3_WS_A    | P9_5     | O    | I2S3 word select line         |
| I2S3_WS_B    | P8_7     |      |                               |
| LPI2S A/B/C  |          |      |                               |
| LPI2S_SCLK_A | P2_6     | O    | LPI2S serial clock            |
| LPI2S_SCLK_B | P10_3    |      |                               |
| LPI2S_SCLK_C | P13_6    |      |                               |
| LPI2S_SDI_A  | P2_4     | I    | LPI2S serial data input line  |
| LPI2S_SDI_B  | P10_1    |      |                               |
| LPI2S_SDI_C  | P13_4    |      |                               |
| LPI2S_SDO_A  | P2_5     | O    | LPI2S serial data output line |
| LPI2S_SDO_B  | P10_2    |      |                               |
| LPI2S_SDO_C  | P13_5    |      |                               |
| LPI2S_WS_A   | P2_7     | O    | LPI2S word select line        |
| LPI2S_WS_B   | P10_4    |      |                               |

| Signal Name | Pin Name | Type | Description |
|-------------|----------|------|-------------|
| LPI2S_WS_C  | P13_7    |      |             |

### 3.17.6 I3C Overview

The MIPI Improved Inter-Integrated Circuit (I3C) provides an interface to external I3C devices.

The device includes:

- One I3C module in Shared Peripherals
- One Low-Power I3C (LPI3C) module in the RTSS-HE

Each I3C module supports the following main features:

- Secondary Master function
- Data rates:
  - Fast Mode (FM) (up to 400 kbps)
  - Fast Mode Plus (FM+) (up to 1 Mbps)
  - Single Data Rate (SDR) (up to 10 Mbps)
  - High Data Rate—Double Data Rate (HDR-DDR) (up to 20 Mbps)
- Support for legacy I2C devices
- Separate command and data buffers for each of the transfers
- Buffer depths (each location can hold 4 bytes of data):
  - Commands buffer: 8 (16 locations)
  - Response buffer: 8 (8 locations)
  - Transmit and receive data buffers: 64 (64 locations) each
- Up to  $2^{16}$  (65536) write/read bytes with a single command
- Hardware assisted Dynamic Address Assignment (DAA) support
- Hardware assisted device role switching between current master and slave
- Hot-Join support with user controllable filter
- CRC/parity generation and validation
- Broadcast and directed Common Command Code (CCC) transfers
- DMA support through hardware handshake interface
- Autonomous clock stalling
- Device address table for addressing multiple slaves
- Dedicated buffer for capturing information from ENTDA CCC command
- Detects arbitration loss due to incoming In-Band Interrupt (IBI) and subsequently re-transmits the command
- Use of duty cycle to achieve lower effective speed for SDR transfers to work with slower I3C slaves
- Programmable Serial Data (SDA) transmit hold
- Programmable retry count for transfers that are addressed by slaves
- IBI with 16 locations of IBI status (no IBI payload)
- Defining Byte support for vendor specific broadcast and directed CCC transfers

## NOTE

All Low Power peripherals are single-master accessible, including LPI3C. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-18 presents I3C interface signals and provides descriptions to their functions.

**Table 3-18 I3C Signal Descriptions**

| Signal Name | Pin Name | Type | Description             |
|-------------|----------|------|-------------------------|
| I3C A/B/C/D |          |      |                         |
| I3C_SCL_A   | P0_1     | IO   | I3C serial clock line   |
| I3C_SCL_B   | P1_3     |      |                         |
| I3C_SCL_C   | P3_3     |      |                         |
| I3C_SCL_D   | P7_7     |      |                         |
| I3C_SDA_A   | P0_0     | IO   | I3C serial data line    |
| I3C_SDA_B   | P1_2     |      |                         |
| I3C_SDA_C   | P3_2     |      |                         |
| I3C_SDA_D   | P7_6     |      |                         |
| LPI3C A/B/C |          |      |                         |
| LPI3C_SCL_A | P6_3     | IO   | LPI3C serial clock line |
| LPI3C_SCL_B | P7_7     |      |                         |
| LPI3C_SCL_C | P14_3    |      |                         |
| LPI3C_SDA_A | P6_2     | IO   | LPI3C serial data line  |
| LPI3C_SDA_B | P7_6     |      |                         |
| LPI3C_SDA_C | P14_2    |      |                         |

### 3.17.7 PDM Overview

The Pulse Density Modulation (PDM) module provides an interface to Digital Microphones (DMIC). The DMIC signal first gets amplified, and then sampled at a high rate and quantized by a DMIC's internal PDM modulator. The device PDM module provides clock and decodes the received 1-bit PDM stream into 16-bit values in Pulse Code Modulation (PCM) format.

The device includes:

- One PDM module in Shared Peripherals
- One Low-Power PDM module (LPPDM) in the RTSS-HE

Each PDM module supports the following main features:

- 4× 2-channel PDM microphone inputs for total support of up to 8 PDM channels (mono DMICs) for PDM module
- Audio signal bandwidth of up to 96 kHz
- DMA controller interface for storing audio samples
- 16-bit PCM output per channel
- Selection between 9 modes of PDM clock frequencies from 512 kHz to 4.8 MHz (oversampling). The mode applies to all channels.
- Microphone sleep mode when at 128 kHz PDM clock
- Independent phase adjustment per channel to allow beam forming

- Independent gain adjustment per channel
- Independent peak detector per channel with programmable thresholds
- Peak detection interrupt per channel producing wake-up event
- Independent programmable DC blocking Infinite Impulse Response (IIR) filter per channel
- Independent programmable Finite Impulse Response (FIR) filter per channel
- FIFO with a capability to store up to 8 PCM samples for each channel for CPU to read
- Programmable FIFO watermark level to generate *data available* interrupt
- FIFO overrun error interrupt

#### NOTE

All Low Power peripherals are single-master accessible, including LPPDM. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-19 presents PDM interface signals and provides descriptions to their functions.

**Table 3-19 PDM Signal Descriptions**

| Signal Name | Pin Name | Type | Description                                                    |
|-------------|----------|------|----------------------------------------------------------------|
| PDM A/B/C   |          |      |                                                                |
| AUDIO_CLK_A | P8_0     | I    | PDM and I2S clock input                                        |
| AUDIO_CLK_B | P9_6     |      |                                                                |
| AUDIO_CLK_C | P12_0    |      |                                                                |
| PDM_C0_A    | P0_5     | O    | PDM clock output 0 to DMIC (shared between channels 0 and 1)   |
| PDM_C0_B    | P3_1     |      |                                                                |
| PDM_C0_C    | P6_1     |      |                                                                |
| PDM_C1_A    | P0_7     | O    | PDM clock output 1 to DMIC (shared between channels 2 and 3)   |
| PDM_C1_B    | P3_3     |      |                                                                |
| PDM_C1_C    | P6_3     |      |                                                                |
| PDM_C2_A    | P6_7     | O    | PDM clock output 2 to DMIC (shared between channels 4 and 5)   |
| PDM_C2_B    | P11_4    |      |                                                                |
| PDM_C3_A    | P5_2     | O    | PDM clock output 3 to DMIC (shared between channels 6 and 7)   |
| PDM_C3_B    | P11_5    |      |                                                                |
| PDM_D0_A    | P0_4     | I    | PDM data input 0 from DMIC (shared between channels 0 and 1)   |
| PDM_D0_B    | P3_0     |      |                                                                |
| PDM_D0_C    | P6_0     |      |                                                                |
| PDM_D1_A    | P0_6     | I    | PDM data input 1 from DMIC (shared between channels 2 and 3)   |
| PDM_D1_B    | P3_2     |      |                                                                |
| PDM_D1_C    | P6_2     |      |                                                                |
| PDM_D2_A    | P5_0     | I    | PDM data input 2 from DMIC (shared between channels 4 and 5)   |
| PDM_D2_B    | P5_4     |      |                                                                |
| PDM_D3_A    | P5_1     | I    | PDM data input 3 from DMIC (shared between channels 6 and 7)   |
| PDM_D3_B    | P5_5     |      |                                                                |
| LPPDM A/B   |          |      |                                                                |
| LPPDM_C0_A  | P2_1     | O    | LPPDM clock output 0 to DMIC (shared between channels 0 and 1) |
| LPPDM_C0_B  | P3_4     |      |                                                                |

| Signal Name | Pin Name | Type | Description                                                    |
|-------------|----------|------|----------------------------------------------------------------|
| LPPDM_C1_A  | P2_3     | O    | LPPDM clock output 1 to DMIC (shared between channels 2 and 3) |
| LPPDM_C1_B  | P3_6     |      |                                                                |
| LPPDM_C2_A  | P7_4     | O    | LPPDM clock output 2 to DMIC (shared between channels 4 and 5) |
| LPPDM_C2_B  | P11_2    |      |                                                                |
| LPPDM_C3_A  | P7_6     | O    | LPPDM clock output 3 to DMIC (shared between channels 6 and 7) |
| LPPDM_C3_B  | P11_3    |      |                                                                |
| LPPDM_D0_A  | P2_0     | I    | LPPDM data input 0 from DMIC (shared between channels 0 and 1) |
| LPPDM_D0_B  | P3_5     |      |                                                                |
| LPPDM_D1_A  | P2_2     | I    | LPPDM data input 1 from DMIC (shared between channels 2 and 3) |
| LPPDM_D1_B  | P3_7     |      |                                                                |
| LPPDM_D2_A  | P7_5     | I    | LPPDM data input 2 from DMIC (shared between channels 4 and 5) |
| LPPDM_D2_B  | P11_6    |      |                                                                |
| LPPDM_D3_A  | P7_7     | I    | LPPDM data input 3 from DMIC (shared between channels 6 and 7) |
| LPPDM_D3_B  | P11_7    |      |                                                                |

### 3.17.8 SPI Overview

The Serial Peripheral Interface (SPI) module is a programmable low pin count, full-duplex master or slave synchronous serial interface.

The device includes:

- Up to four high-speed SPI modules in Shared Peripherals
- Up to two Low-Power SPI modules (LPSPI0 and LPSPI1) in the RTSS-HE, sharing device pins and thus forming a single LPSPI channel

The SPI modules support the following main features:

- 32-bit data bus width for AHB interface (SPI modules) and APB interface (LPSPI modules)
- Standard SPI mode
- Up to four slave select lines for the SPI modules, up to six slave select lines for the LPSPI
- Multi-master contention detection
- Programmable delay on the sample time of received serial data bit for the high-speed SPI modules (when programmed in Master mode) and LPSPI0
- Separate Transmit and Receive FIFO buffers:
  - Buffer width of 32 bits
  - Buffer depth of 16 words (high-speed SPI modules only) and 32 words (LPSPI modules)
- DMA requests
- Combined interrupt lines and active high-level interrupts
- Operation modes:
  - Serial Master or Slave modes for the high-speed SPI modules
  - Master mode only for LPSPI0, and Slave mode only for LPSPI1
- Programmable frame formats:
  - Motorola Serial Peripheral Interface
  - Texas Instruments Synchronous Serial Protocol (SSP)
  - National Semiconductor Microwire
- Programmable data transfer clock bit rate for dynamic control of the serial bit rate
- Programmable data item size (4 to 32 bits) for each data transfer

## NOTE

All Low Power peripherals are single-master accessible, including LPSPI. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-20 presents SPI interface signals and provides descriptions to their functions.

**Table 3-20 SPI Signal Descriptions**

| Signal Name | Pin Name | Type | Description                                                                                         |
|-------------|----------|------|-----------------------------------------------------------------------------------------------------|
| SPI0 A/B/C  |          |      |                                                                                                     |
| SPI0_SCLK_A | P1_2     | IO   | SPI0 serial clock (driven by master)                                                                |
| SPI0_SCLK_B | P5_3     |      |                                                                                                     |
| SPI0_SCLK_C | P7_2     |      |                                                                                                     |
| SPI0_SS0_A  | P1_3     | IO   | In Master mode, slave select 0 output. In Slave mode, slave select 0 input from an external master. |
| SPI0_SS0_B  | P5_2     |      |                                                                                                     |
| SPI0_SS0_C  | P7_3     |      |                                                                                                     |
| SPI0_SS1_A  | P1_4     | O    | SPI0 slave select 1 (driven by master)                                                              |
| SPI0_SS1_B  | P3_5     |      |                                                                                                     |
| SPI0_SS2_A  | P1_5     | O    | SPI0 slave select 2 (driven by master)                                                              |
| SPI0_SS2_B  | P3_6     |      |                                                                                                     |
| SPI0_SS3_A  | P5_4     | O    | SPI0 slave select 3 (driven by master)                                                              |
| SPI0_SS3_B  | P8_2     |      |                                                                                                     |
| SPI0_MISO_A | P1_0     | IO   | SPI0 master in slave out                                                                            |
| SPI0_MISO_B | P5_0     |      |                                                                                                     |
| SPI0_MISO_C | P7_0     |      |                                                                                                     |
| SPI0_MOSI_A | P1_1     | IO   | SPI0 master out slave in                                                                            |
| SPI0_MOSI_B | P5_1     |      |                                                                                                     |
| SPI0_MOSI_C | P7_1     |      |                                                                                                     |
| SPI1 A/B/C  |          |      |                                                                                                     |
| SPI1_SCLK_A | P2_6     | IO   | SPI1 serial clock (driven by master)                                                                |
| SPI1_SCLK_B | P8_5     |      |                                                                                                     |
| SPI1_SCLK_C | P14_6    |      |                                                                                                     |
| SPI1_SS0_A  | P2_7     | IO   | In Master mode, slave select 0 output. In Slave mode, slave select 0 input from an external master. |
| SPI1_SS0_B  | P6_4     |      |                                                                                                     |
| SPI1_SS0_C  | P14_7    |      |                                                                                                     |
| SPI1_SS1_A  | P3_7     | O    | SPI1 slave select 1 (driven by master)                                                              |
| SPI1_SS1_B  | P6_5     |      |                                                                                                     |
| SPI1_SS2_A  | P4_0     | O    | SPI1 slave select 2 (driven by master)                                                              |
| SPI1_SS2_B  | P6_6     |      |                                                                                                     |
| SPI1_SS3_A  | P4_1     | O    | SPI1 slave select 3 (driven by master)                                                              |
| SPI1_SS3_B  | P6_7     |      |                                                                                                     |
| SPI1_MISO_A | P2_4     | IO   | SPI1 master in slave out                                                                            |
| SPI1_MISO_B | P8_3     |      |                                                                                                     |
| SPI1_MISO_C | P14_4    |      |                                                                                                     |
| SPI1_MOSI_A | P2_5     | IO   | SPI1 master out slave in                                                                            |

| Signal Name  | Pin Name | Type | Description                                                                                         |
|--------------|----------|------|-----------------------------------------------------------------------------------------------------|
| SPI1_MOSI_B  | P8_4     |      |                                                                                                     |
| SPI1_MOSI_C  | P14_5    |      |                                                                                                     |
| SPI2 A/B     |          |      |                                                                                                     |
| SPI2_SCLK_A  | P4_4     | IO   | SPI2 serial clock (driven by master)                                                                |
| SPI2_SCLK_B  | P9_4     |      |                                                                                                     |
| SPI2_SS0_A   | P4_5     | IO   | In Master mode, slave select 0 output. In Slave mode, slave select 0 input from an external master. |
| SPI2_SS0_B   | P9_5     |      |                                                                                                     |
| SPI2_SS1_A   | P4_6     | O    | SPI2 slave select 1 (driven by master)                                                              |
| SPI2_SS1_B   | P9_6     |      |                                                                                                     |
| SPI2_SS2_A   | P4_7     | O    | SPI2 slave select 2 (driven by master)                                                              |
| SPI2_SS2_B   | P9_7     |      |                                                                                                     |
| SPI2_SS3_A   | P13_3    | O    | SPI2 slave select 3 (driven by master)                                                              |
| SPI2_SS3_B   | P10_0    | O    | SPI2 slave select 3 (driven by master)                                                              |
| SPI2_MISO_A  | P4_2     | IO   | SPI2 master in slave out                                                                            |
| SPI2_MISO_B  | P9_2     |      |                                                                                                     |
| SPI2_MOSI_A  | P4_3     | IO   | SPI2 master out slave in                                                                            |
| SPI2_MOSI_B  | P9_3     |      |                                                                                                     |
| SPI3 A/B     |          |      |                                                                                                     |
| SPI3_SCLK_A  | P12_6    | IO   | SPI3 serial clock (driven by master)                                                                |
| SPI3_SCLK_B  | P10_7    | IO   | SPI3 serial clock (driven by master)                                                                |
| SPI3_SS0_A   | P12_7    | IO   | In Master mode, slave select 0 output. In Slave mode, slave select 0 input from an external master. |
| SPI3_SS0_B   | P11_0    |      |                                                                                                     |
| SPI3_SS1_A   | P13_0    | O    | SPI3 slave select 1 (driven by master)                                                              |
| SPI3_SS1_B   | P11_1    | O    | SPI3 slave select 1 (driven by master)                                                              |
| SPI3_SS2_A   | P13_1    | O    | SPI3 slave select 2 (driven by master)                                                              |
| SPI3_SS2_B   | P11_2    | O    | SPI3 slave select 2 (driven by master)                                                              |
| SPI3_SS3_A   | P13_2    | O    | SPI3 slave select 3 (driven by master)                                                              |
| SPI3_SS3_B   | P11_3    | O    | SPI3 slave select 3 (driven by master)                                                              |
| SPI3_MISO_A  | P12_4    | IO   | SPI3 master in slave out                                                                            |
| SPI3_MISO_B  | P10_5    | IO   | SPI3 master in slave out                                                                            |
| SPI3_MOSI_A  | P12_5    | IO   | SPI3 master out slave in                                                                            |
| SPI3_MOSI_B  | P10_6    | IO   | SPI3 master out slave in                                                                            |
| LPSPi A/B    |          |      |                                                                                                     |
| LPSPi_SCLK_A | P7_6     | IO   | LPSPi serial clock (driven by master)                                                               |
| LPSPi_SCLK_B | P11_6    |      |                                                                                                     |
| LPSPi_MISO_A | P7_4     | IO   | LPSPi master in slave out                                                                           |
| LPSPi_MISO_B | P11_4    |      |                                                                                                     |
| LPSPi_MOSI_A | P7_5     | IO   | LPSPi master out slave in                                                                           |
| LPSPi_MOSI_B | P11_5    |      |                                                                                                     |
| LPSPi_SS0_A  | P7_7     | IO   | LPSPi slave select 0 output                                                                         |
| LPSPi_SS0_B  | P11_7    |      |                                                                                                     |
| LPSPi_SS1_A  | P6_0     | IO   | LPSPi slave select 1 output                                                                         |
| LPSPi_SS1_B  | P14_4    |      |                                                                                                     |
| LPSPi_SS2_A  | P6_1     | IO   | LPSPi slave select 2 output                                                                         |
| LPSPi_SS2_B  | P14_5    |      |                                                                                                     |

| Signal Name | Pin Name | Type | Description                 |
|-------------|----------|------|-----------------------------|
| LPSPI_SS3_A | P9_0     | IO   | LPSPI slave select 3 output |
| LPSPI_SS3_B | P14_6    |      |                             |
| LPSPI_SS4_A | P9_1     | IO   | LPSPI slave select 4 output |
| LPSPI_SS4_B | P14_7    |      |                             |
| LPSPI_SS5_A | P11_1    | IO   | LPSPI slave select 5 output |
| LPSPI_SS5_B | P14_2    |      |                             |

### 3.17.9 UART Overview

The Universal Asynchronous Receiver/Transmitter (UART) module implements asynchronous serial communication interface based on standard Non-Return-to-Zero (NRZ) frame format.

The device includes:

- Up to eight UART modules in Shared Peripherals
- One Low-Power UART module (LPUART) in the RTSS-HE
- One UART module in the SESS (SEUART)—not accessible by user application

The UART modules are integrated in the following power domains:

- Power Domain PD-6: UART[0-7]
- Power Domain PD-2: LPUART
- Power Domain PD-5: SEUART

Each UART module supports the following main features:

- Full duplex operation
- Programmable baud rates up to 5 Mbps with a fractional baud rate divisor
- Interrupt driven or DMA controlled data transfer
- Auto flow control compatible with 16750 devices
- Configurable character length—5, 6, 7, 8 or 9 bits
- Optional parity bit—Even, Odd, Stick
- Number of stop bits—1, 1.5, 2 bits
- Line break generation and detection
- CTS/RTS signals for hardware flow control
- Drive enable output for RS485 interface support on UART[4-7] only
- Transmit (Tx) and Receive (Rx) FIFO depth of 32 characters
- Loopback mode for test and troubleshooting
- False start bit detection
- Compatible with the industry standard 16550 devices
- The LPUART interrupt can be used as a wake-up source from STANDBY low-power mode

#### NOTE

All Low Power peripherals are single-master accessible, including LPUART. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-21 presents UART interface signals and provides descriptions to their functions.

Table 3-21 UART Signal Descriptions

| Signal Name | Pin Name | Type | Description               |
|-------------|----------|------|---------------------------|
| UART0 A/B   |          |      |                           |
| UART0_RX_A  | P0_0     | I    | UART0 serial data input   |
| UART0_RX_B  | P1_4     |      |                           |
| UART0_TX_A  | P0_1     | O    | UART0 serial data output  |
| UART0_TX_B  | P1_5     |      |                           |
| UART0_CTS_A | P0_2     | I    | UART0 clear to send       |
| UART0_CTS_B | P6_6     |      |                           |
| UART0_RTS_A | P0_3     | O    | UART0 request to send     |
| UART0_RTS_B | P6_7     |      |                           |
| UART1 A/B   |          |      |                           |
| UART1_RX_A  | P0_4     | I    | UART1 serial data input   |
| UART1_RX_B  | P1_6     |      |                           |
| UART1_TX_A  | P0_5     | O    | UART1 serial data output  |
| UART1_TX_B  | P1_7     |      |                           |
| UART1_CTS_A | P0_6     | I    | UART1 clear to send       |
| UART1_CTS_B | P5_6     |      |                           |
| UART1_RTS_A | P0_7     | O    | UART1 request to send     |
| UART1_RTS_B | P5_7     |      |                           |
| UART2 A/B   |          |      |                           |
| UART2_RX_A  | P1_0     | I    | UART2 serial data input   |
| UART2_RX_B  | P2_0     |      |                           |
| UART2_TX_A  | P1_1     | O    | UART2 serial data output  |
| UART2_TX_B  | P2_1     |      |                           |
| UART2_CTS_A | P6_2     | I    | UART2 clear to send       |
| UART2_CTS_B | P6_4     |      |                           |
| UART2_RTS_A | P6_3     | O    | UART2 request to send     |
| UART2_RTS_B | P6_5     |      |                           |
| UART3 A/B   |          |      |                           |
| UART3_RX_A  | P1_2     | I    | UART3 serial data input   |
| UART3_RX_B  | P2_2     |      |                           |
| UART3_TX_A  | P1_3     | O    | UART3 serial data output  |
| UART3_TX_B  | P2_3     |      |                           |
| UART3_CTS_A | P5_4     | I    | UART3 clear to send       |
| UART3_CTS_B | P7_2     |      |                           |
| UART3_RTS_A | P5_5     | O    | UART3 request to send     |
| UART3_RTS_B | P7_3     |      |                           |
| UART4 A/B/C |          |      |                           |
| UART4_RX_A  | P3_0     | I    | UART4 serial data input   |
| UART4_RX_B  | P12_1    |      |                           |
| UART4_RX_C  | P5_0     |      |                           |
| UART4_TX_A  | P3_1     | O    | UART4 serial data output  |
| UART4_TX_B  | P12_2    |      |                           |
| UART4_TX_C  | P5_1     |      |                           |
| UART4_DE_A  | P6_0     | O    | UART4 RS485 driver enable |

| Signal Name  | Pin Name  | Type | Description               |
|--------------|-----------|------|---------------------------|
| UART4_DE_B   | P12_3     |      |                           |
| UART5 A/B/C  |           |      |                           |
| UART5_RX_A   | P3_4      | I    | UART5 serial data input   |
| UART5_RX_B   | P11_3     |      |                           |
| UART5_RX_C   | P5_2      |      |                           |
| UART5_TX_A   | P3_5      | O    | UART5 serial data output  |
| UART5_TX_B   | P11_4     |      |                           |
| UART5_TX_C   | P5_3      |      |                           |
| UART5_DE_A   | P6_1      | O    | UART5 RS485 driver enable |
| UART5_DE_B   | P11_7     |      |                           |
| UART6 A/B/C  |           |      |                           |
| UART6_RX_A   | P10_5     | I    | UART6 serial data input   |
| UART6_RX_B   | P11_5     |      |                           |
| UART6_RX_C   | P14_0     |      |                           |
| UART6_TX_A   | P10_6     | O    | UART6 serial data output  |
| UART6_TX_B   | P11_6     |      |                           |
| UART6_TX_C   | P14_1     |      |                           |
| UART6_DE_A   | P11_2     | O    | UART6 RS485 driver enable |
| UART6_DE_B   | P10_0     |      |                           |
| UART7 A/B/C  |           |      |                           |
| UART7_RX_A   | P10_7     | I    | UART7 serial data input   |
| UART7_RX_B   | P9_3      |      |                           |
| UART7_RX_C   | P14_2     |      |                           |
| UART7_TX_A   | P11_0     | O    | UART7 serial data output  |
| UART7_TX_B   | P9_4      |      |                           |
| UART7_TX_C   | P14_3     |      |                           |
| UART7_DE_A   | P11_1     | O    | UART7 RS485 driver enable |
| UART7_DE_B   | P9_7      |      |                           |
| LPUART A/B   |           |      |                           |
| LPUART_RX_A  | P7_6      | I    | LPUART serial data input  |
| LPUART_RX_B  | P9_1      |      |                           |
| LPUART_TX_A  | P7_7      | O    | LPUART serial data output |
| LPUART_TX_B  | P9_2      |      |                           |
| LPUART_CTS_A | P7_4      | I    | LPUART clear to send      |
| LPUART_CTS_B | P3_6      |      |                           |
| LPUART_RTS_A | P7_5      | O    | LPUART request to send    |
| LPUART_RTS_B | P3_7      |      |                           |
| SEUART       |           |      |                           |
| SEUART_RX    | SEUART_RX | I    | SEUART serial data input  |
| SEUART_TX    | SEUART_TX | O    | SEUART serial data output |

### 3.17.10 USB Overview

The Universal Serial Bus (USB) provides an expandable, bi-directional, hot-pluggable, serial interface that allows to plug different peripherals into a USB port and have them automatically configured and ready to

use. USB host and devices use memory FIFO buffers to implement data endpoints used to accept or send data from and to its endpoint counterpart.

The device includes one USB module. The USB module consists of an xHCI USB2.0 Dual-Role Device (DRD) controller, a FIFO RAM, and an on-chip PHY.

The USB module supports the following main features:

- Compliant with USB Specification 2.0
- Eight bi-directional endpoints including the bi-directional control endpoint 0, or 16 uni-directional endpoints
- Same programming model for Low-Speed (LS) (1.5 Mbit/s, host mode only), Full-Speed (FS) (12 Mbit/s), and High-Speed (HS) (480 Mbit/s) bit rates
- Internal DMA controller
- Power-saving features (clock gating)
- Link Power Management (LPM) protocol
- Hardware-controlled LPM support in Host mode
- Single 2001 × 64-bit RAM, accommodating registers, descriptor cache, Rx buffers and Tx prefetch
  - Dynamic FIFO memory allocation for endpoints
- Keep-alive feature in LS mode and (micro-)SOFs in FS and HS modes
- (micro-)SOFs (Start-of-Frame)
- Software-controlled standard USB commands (USB SETUP commands detected and forwarded to application for decoding)
- Hardware-controlled USB bus level and packet level error handling
- Low CPU utilization needs
  - Driver involved only in setting up transfers and high-level error recovery
  - Hardware handles data packing and routing to a specific pipe
- Descriptor caching and data prefetching used to meet system performance in high-latency systems
- Interrupt moderation
- On-chip PHY via an USB 2.0 Transceiver Macrocell Interface (UTMI+)

Table 3-22 presents USB interface signals and provides descriptions to their functions.

**Table 3-22 USB Signal Descriptions**

| Signal Name | Pin Name  | Type | Description                                                              |
|-------------|-----------|------|--------------------------------------------------------------------------|
| USB_DP      | USB_DP    | IO   | USB 2.0 differential data (positive)                                     |
| USB_DM      | USB_DM    | IO   | USB 2.0 differential data (negative)                                     |
| USB_VBUS    | USB_VBUS  | A    | USB V <sub>BUS</sub> -sense input                                        |
| USB_IO_ID   | USB_IO_ID | A    | USB A/B-device detect—leave unconnected (Device) or tie to ground (Host) |
| USB_REXT    | USB_REXT  | P    | External calibration resistor (200 Ω ±1%) to GND                         |

## 3.18 External Memory Interfaces

### 3.18.1 Cryptographic HEXSPI Overview

The cryptographic HEXSPI implementation in the device consists of the Hex Serial Peripheral Interface (HEXSPI) module and the ancillary Advanced Encryption Standard (AES) engine.

The HEXSPI is an intelligent peripheral offering various memory expansion options. The HEXSPI can work either in a direct access mode to directly read and write data to the external SPI memory, or in a decryption mode where the incoming data is decrypted on-the-fly via the AES engine.

The device includes up to two 16-bit HEXSPI modules, each assisted by a dedicated AES engine for the cryptographic operations.

Each HEXSPI module supports the following main features:

- Single, Dual, Quad, Octal, or Hex SPI Master mode operation
- Up to 200 MHz clock for up to 400 MB/s Single Data Rate (SDR) and 800 MB/s Dual Data Rate (DDR) support
- HyperBus protocol (2.0/2.0e) support for integration of HyperRAM™ modules
- Programmable instruction length, address length, wait cycles and data frame size
- Programmable option to skip address and instruction phase
- Read data strobe support in DDR mode for higher frequencies
- Support of Motorola Serial Peripheral Interface protocol
- DMA controller interface
- Programmable delay on the sample time of Received Serial Data (RXD) bit compensating routing delays
- Programmable frame size of each data transfer from 4 to 32 bits
- 256 words deep Rx and Tx FIFO buffers
- Execute-in-Place (XIP) support for read and write transfers—translates memory access requests to SPI transactions for code memory expansion. This mode supports the following main features:
  - Programmable instruction length and address length in XIP mode
  - Data frame size mapping directly from AHB transfers
  - Fixed data frame size for all the transfers
  - Continuous transfer mode for read transactions
  - Data mask support
  - Configurable data pre-fetch during XIP read transaction
  - Concurrent XIP and non-XIP transactions
  - Automatic slave select (SS) line control based on the target memory address within the HEXSPI allocated space in the system memory map
- eXpanded SPI (xSPI) with all the command formats as described in JEDEC xSPI version 1.0
- Two xSPI command modes:
  - 1S-1S-1S—one IO signal used during command transfer, command modifier transfer, and data transfer. All phases are SDR.
  - 8D-8D-8D—eight IO signals used during command transfer, command modifier transfer, and data transfer. All phases are DDR.

Each AES engine supports the following main features:

- On-the-fly decryption, transparent for the HEXSPI read transactions from external memory
- Electronic Codebook (ECB) mode of operation
- 128-bit long AES keys
- Secure setup and lockup of the decryption keys by the Secure Enclave at boot time

Table 3-23 presents HEXSPI interface signals and provides descriptions to their functions.

**Table 3-23 HEXSPI Signal Descriptions**

| Signal Name                   | Pin Name | Type | Description                                                                                 |
|-------------------------------|----------|------|---------------------------------------------------------------------------------------------|
| <b>HEXSPIO Data Bus A/B/C</b> |          |      |                                                                                             |
| OSPIO_D0_A                    | P0_0     | IO   | HEXSPIO data input/output 0 in enhanced SPI modes. Data output (MOSI) in standard SPI mode. |
| OSPIO_D0_B                    | P2_0     |      |                                                                                             |
| OSPIO_D0_C                    | P6_0     |      |                                                                                             |
| OSPIO_D1_A                    | P0_1     | IO   | HEXSPIO data input/output 1 in enhanced SPI modes. Data input (MISO) in standard SPI mode.  |
| OSPIO_D1_B                    | P2_1     |      |                                                                                             |

| Signal Name                                           | Pin Name | Type | Description                                                                   |
|-------------------------------------------------------|----------|------|-------------------------------------------------------------------------------|
| OSPI0_D1_C                                            | P6_1     | IO   | HEXSPI0 data 2                                                                |
| OSPI0_D2_A                                            | P0_2     |      |                                                                               |
| OSPI0_D2_B                                            | P2_2     |      |                                                                               |
| OSPI0_D2_C                                            | P6_2     | IO   | HEXSPI0 data 3                                                                |
| OSPI0_D3_A                                            | P0_3     |      |                                                                               |
| OSPI0_D3_B                                            | P2_3     |      |                                                                               |
| OSPI0_D3_C                                            | P6_3     | IO   | HEXSPI0 data 4                                                                |
| OSPI0_D4_A                                            | P0_4     |      |                                                                               |
| OSPI0_D4_B                                            | P2_4     |      |                                                                               |
| OSPI0_D4_C                                            | P6_4     | IO   | HEXSPI0 data 5                                                                |
| OSPI0_D5_A                                            | P0_5     |      |                                                                               |
| OSPI0_D5_B                                            | P2_5     |      |                                                                               |
| OSPI0_D5_C                                            | P6_5     | IO   | HEXSPI0 data 6                                                                |
| OSPI0_D6_A                                            | P0_6     |      |                                                                               |
| OSPI0_D6_B                                            | P2_6     |      |                                                                               |
| OSPI0_D6_C                                            | P6_6     | IO   | HEXSPI0 data 7                                                                |
| OSPI0_D7_A                                            | P0_7     |      |                                                                               |
| OSPI0_D7_B                                            | P2_7     |      |                                                                               |
| OSPI0_D7_C                                            | P6_7     | IO   | HEXSPI0 data 8                                                                |
| OSPI0_D8_A                                            | P13_0    |      |                                                                               |
| OSPI0_D8_B                                            | P16_0    | IO   | HEXSPI0 data 9                                                                |
| OSPI0_D9_A                                            | P13_1    |      |                                                                               |
| OSPI0_D9_B                                            | P16_1    | IO   | HEXSPI0 data 10                                                               |
| OSPI0_D10_A                                           | P13_2    |      |                                                                               |
| OSPI0_D10_B                                           | P16_2    | IO   | HEXSPI0 data 11                                                               |
| OSPI0_D11_A                                           | P13_3    |      |                                                                               |
| OSPI0_D11_B                                           | P16_3    | IO   | HEXSPI0 data 12                                                               |
| OSPI0_D12_A                                           | P13_4    |      |                                                                               |
| OSPI0_D12_B                                           | P16_4    | IO   | HEXSPI0 data 13                                                               |
| OSPI0_D13_A                                           | P13_5    |      |                                                                               |
| OSPI0_D13_B                                           | P16_5    | IO   | HEXSPI0 data 14                                                               |
| OSPI0_D14_A                                           | P13_6    |      |                                                                               |
| OSPI0_D14_B                                           | P16_6    | IO   | HEXSPI0 data 15                                                               |
| OSPI0_D15_A                                           | P13_7    |      |                                                                               |
| OSPI0_D15_B                                           | P16_7    |      |                                                                               |
| <b>HEXSPI0 Clock, Slave Select, Data Strobe A/B/C</b> |          |      |                                                                               |
| OSPI0_SCLKN_A                                         | P3_5     | O    | HEXSPI0 serial clock (negative)                                               |
| OSPI0_SCLKN_B                                         | P3_1     |      |                                                                               |
| OSPI0_SCLKN_C                                         | P12_1    |      |                                                                               |
| OSPI0_SCLK_A                                          | P1_7     | O    | HEXSPI0 serial clock                                                          |
| OSPI0_SCLK_B                                          | P3_0     |      |                                                                               |
| OSPI0_SCLK_C                                          | P12_0    |      |                                                                               |
| OSPI0_RXDS0_A                                         | P3_4     | IO   | HEXSPI0 read data strobe 0 (RXDS) when input. Data mask (TXD_DM) when output. |
| OSPI0_RXDS0_B                                         | P1_6     |      |                                                                               |
| OSPI0_RXDS0_C                                         | P12_2    |      |                                                                               |

| Signal Name            | Pin Name | Type | Description                                                                                 |
|------------------------|----------|------|---------------------------------------------------------------------------------------------|
| OSPIO_RXDS1_A          | P8_5     | IO   | HEXSPIO read data strobe 1 (RXDS) when input. Data mask (TXD_DM) when output.               |
| OSPIO_RXDS1_B          | P14_5    |      |                                                                                             |
| OSPIO_RXDS1_C          | P8_7     |      |                                                                                             |
| OSPIO_SS0_A            | P1_4     | O    | HEXSPIO slave select 0 <sup>(1)</sup>                                                       |
| OSPIO_SS0_B            | P3_2     |      |                                                                                             |
| OSPIO_SS0_C            | P12_3    |      |                                                                                             |
| OSPIO_SS1_A            | P1_5     | O    | HEXSPIO slave select 1 <sup>(1)</sup>                                                       |
| OSPIO_SS1_B            | P3_3     |      |                                                                                             |
| OSPIO_SS1_C            | P12_4    |      |                                                                                             |
| HEXSPI1 Data Bus A/B/C |          |      |                                                                                             |
| OSPI1_D0_A             | P11_0    | IO   | HEXSPI1 data input/output 0 in enhanced SPI modes. Data output (MOSI) in standard SPI mode. |
| OSPI1_D0_B             | P13_0    |      |                                                                                             |
| OSPI1_D0_C             | P9_5     |      |                                                                                             |
| OSPI1_D1_A             | P11_1    | IO   | HEXSPI1 data input/output 1 in enhanced SPI modes. Data input (MISO) in standard SPI mode.  |
| OSPI1_D1_B             | P13_1    |      |                                                                                             |
| OSPI1_D1_C             | P9_6     |      |                                                                                             |
| OSPI1_D2_A             | P11_2    | IO   | HEXSPI1 data 2                                                                              |
| OSPI1_D2_B             | P13_2    |      |                                                                                             |
| OSPI1_D2_C             | P9_7     |      |                                                                                             |
| OSPI1_D3_A             | P11_3    | IO   | HEXSPI1 data 3                                                                              |
| OSPI1_D3_B             | P13_3    |      |                                                                                             |
| OSPI1_D3_C             | P10_0    |      |                                                                                             |
| OSPI1_D4_A             | P11_4    | IO   | HEXSPI1 data 4                                                                              |
| OSPI1_D4_B             | P13_4    |      |                                                                                             |
| OSPI1_D4_C             | P10_1    |      |                                                                                             |
| OSPI1_D5_A             | P11_5    | IO   | HEXSPI1 data 5                                                                              |
| OSPI1_D5_B             | P13_5    |      |                                                                                             |
| OSPI1_D5_C             | P10_2    |      |                                                                                             |
| OSPI1_D6_A             | P11_6    | IO   | HEXSPI1 data 6                                                                              |
| OSPI1_D6_B             | P13_6    |      |                                                                                             |
| OSPI1_D6_C             | P10_3    |      |                                                                                             |
| OSPI1_D7_A             | P11_7    | IO   | HEXSPI1 data 7                                                                              |
| OSPI1_D7_B             | P13_7    |      |                                                                                             |
| OSPI1_D7_C             | P10_4    |      |                                                                                             |
| OSPI1_D8_B             | P12_0    | IO   | HEXSPI1 data 8                                                                              |
| OSPI1_D8_C             | P17_0    |      |                                                                                             |
| OSPI1_D9_B             | P12_1    | IO   | HEXSPI1 data 9                                                                              |
| OSPI1_D9_C             | P17_1    |      |                                                                                             |
| OSPI1_D10_B            | P12_2    | IO   | HEXSPI1 data 10                                                                             |
| OSPI1_D10_C            | P17_2    |      |                                                                                             |
| OSPI1_D11_B            | P12_3    | IO   | HEXSPI1 data 11                                                                             |
| OSPI1_D11_C            | P17_3    |      |                                                                                             |
| OSPI1_D12_B            | P12_4    | IO   | HEXSPI1 data 12                                                                             |
| OSPI1_D12_C            | P17_4    |      |                                                                                             |
| OSPI1_D13_B            | P12_5    | IO   | HEXSPI1 data 13                                                                             |

| Signal Name                                    | Pin Name | Type | Description                                                                   |
|------------------------------------------------|----------|------|-------------------------------------------------------------------------------|
| OSPI1_D13_C                                    | P17_5    |      |                                                                               |
| OSPI1_D14_B                                    | P12_6    | IO   | HEXSPI1 data 14                                                               |
| OSPI1_D14_C                                    | P17_6    |      |                                                                               |
| OSPI1_D15_B                                    | P14_6    | IO   | HEXSPI1 data 15                                                               |
| OSPI1_D15_C                                    | P17_7    |      |                                                                               |
| HEXSPI1 Clock, Slave Select, Data Strobe A/B/C |          |      |                                                                               |
| OSPI1_SCLKN_A                                  | P5_2     | O    | HEXSPI1 serial clock (negative)                                               |
| OSPI1_SCLKN_B                                  | P14_1    |      |                                                                               |
| OSPI1_SCLKN_C                                  | P8_0     |      |                                                                               |
| OSPI1_SCLK_A                                   | P5_3     | O    | HEXSPI1 serial clock                                                          |
| OSPI1_SCLK_B                                   | P14_0    |      |                                                                               |
| OSPI1_SCLK_C                                   | P5_5     |      |                                                                               |
| OSPI1_RXDS0_A                                  | P5_0     | IO   | HEXSPI1 read data strobe 0 (RXDS) when input. Data mask (TXD_DM) when output. |
| OSPI1_RXDS0_B                                  | P12_7    |      |                                                                               |
| OSPI1_RXDS0_C                                  | P10_7    |      |                                                                               |
| OSPI1_RXDS1_A                                  | P14_4    | IO   | HEXSPI1 read data strobe 1 (RXDS) when input. Data mask (TXD_DM) when output. |
| OSPI1_RXDS1_B                                  | P8_6     |      |                                                                               |
| OSPI1_RXDS1_C                                  | P9_0     |      |                                                                               |
| OSPI1_SS0_A                                    | P5_1     | O    | HEXSPI1 slave select 0 <sup>(1)</sup>                                         |
| OSPI1_SS0_B                                    | P14_2    |      |                                                                               |
| OSPI1_SS0_C                                    | P5_7     |      |                                                                               |
| OSPI1_SS1_A                                    | P5_4     | O    | HEXSPI1 slave select 1 <sup>(1)</sup>                                         |
| OSPI1_SS1_B                                    | P14_3    |      |                                                                               |
| OSPI1_SS1_C                                    | P8_1     |      |                                                                               |

1. In XIP mode of operation, the slave select signals are automatically controlled based on the target memory address within the HEXSPI allocated space in the system memory map.

### 3.18.2 SDMMC Overview

The Secure Digital / MultiMediaCard (SDMMC) module provides an interface to embedded MultiMediaCard (eMMC™), Secure Digital® (SD®) card, and SD Input/Output (SDIO). The communication between the SDMMC module and eMMC/SD/SDIO device is performed according to the eMMC/SD/SDIO protocol.

The device includes one SDMMC module.

The SDMMC module supports the following main features:

- SD card interface:
  - 4-bit data bus
  - Complaint with SD Host Controller Standard Specification v4.20
  - Complaint with SD Physical Layer Specification v6.00
  - Backward compatible with earlier SD card specifications
  - UHS-I mode
  - Speed modes:
    - Default-Speed (DS)
    - High-Speed (HS)
    - SDR12
    - SDR25

- SDIO interface:
  - 4-bit data bus
  - Complaint with SD Specifications Part E1 SDIO Specification Version 4.10
  - SDIO read wait
  - SDIO card interrupts in both 1-bit and 4-bit modes
  - Wake-up on card interrupt
- eMMC interface:
  - 4-bit/8-bit data bus
  - Complaint with JEDEC eMMC 5.1 Specification (JESD84-B51)
  - Backward compatible with earlier eMMC specifications
  - Speed legacy modes:
    - High Speed SDR
  - Boot operation and alternative boot operation
- 32-bit slave AHB and 64-bit master AXI interface
- Data transfer types for SD and eMMC:
  - CPU
  - SDMA
  - ADMA2
  - ADMA3
- Clocking:
  - Supports independent clocks for the host controller, slave interface, and master interface
  - Supports gating of host controller base clock, if host controller is inactive
  - Supports context aware functional clock gates
- Interrupt outputs:
  - Combined and separate interrupt outputs
  - Interrupt enabling and masking
- Data buffering:
  - Automatic packing/unpacking of data to fit buffer width

Table 3-24 presents SDMMC interface signals and provides descriptions to their functions.

**Table 3-24 SDMMC Signal Descriptions**

| Signal Name                   | Pin Name | Type | Description       |
|-------------------------------|----------|------|-------------------|
| <b>SDMMC Data Bus A/B/C/D</b> |          |      |                   |
| SD_D0_A                       | P5_0     | IO   | SDMMC data line 0 |
| SD_D0_B                       | P13_0    |      |                   |
| SD_D0_C                       | P8_0     |      |                   |
| SD_D0_D                       | P6_0     |      |                   |
| SD_D1_A                       | P5_1     | IO   | SDMMC data line 1 |
| SD_D1_B                       | P13_1    |      |                   |
| SD_D1_C                       | P8_1     |      |                   |
| SD_D1_D                       | P6_1     |      |                   |
| SD_D2_A                       | P5_2     | IO   | SDMMC data line 2 |
| SD_D2_B                       | P13_2    |      |                   |
| SD_D2_C                       | P8_2     |      |                   |
| SD_D2_D                       | P6_2     |      |                   |
| SD_D3_A                       | P5_3     | IO   | SDMMC data line 3 |
| SD_D3_B                       | P13_3    |      |                   |
| SD_D3_C                       | P8_3     |      |                   |

| Signal Name                        | Pin Name | Type | Description                         |
|------------------------------------|----------|------|-------------------------------------|
| SD_D3_D                            | P6_3     | IO   | SDMMC data line 4                   |
| SD_D4_A                            | P5_4     |      |                                     |
| SD_D4_B                            | P13_4    |      |                                     |
| SD_D4_C                            | P8_4     |      |                                     |
| SD_D4_D                            | P6_4     |      |                                     |
| SD_D5_A                            | P5_5     | IO   | SDMMC data line 5                   |
| SD_D5_B                            | P13_5    |      |                                     |
| SD_D5_C                            | P8_5     |      |                                     |
| SD_D5_D                            | P6_5     |      |                                     |
| SD_D6_A                            | P5_6     | IO   | SDMMC data line 6                   |
| SD_D6_B                            | P13_6    |      |                                     |
| SD_D6_C                            | P8_6     |      |                                     |
| SD_D6_D                            | P6_6     |      |                                     |
| SD_D7_A                            | P5_7     | IO   | SDMMC data line 7                   |
| SD_D7_B                            | P13_7    |      |                                     |
| SD_D7_C                            | P8_7     |      |                                     |
| SD_D7_D                            | P6_7     |      |                                     |
| SDIO Command, Clock, Reset A/B/C/D |          |      |                                     |
| SD_CMD_A                           | P7_0     | IO   | SDMMC command/response line         |
| SD_CMD_B                           | P14_0    | IO   |                                     |
| SD_CMD_C                           | P9_0     | IO   |                                     |
| SD_CMD_D                           | P4_2     | IO   |                                     |
| SD_CLK_A                           | P7_1     | O    | SDMMC host to card clock line       |
| SD_CLK_B                           | P14_1    | O    |                                     |
| SD_CLK_C                           | P9_1     | O    |                                     |
| SD_CLK_D                           | P4_1     | O    |                                     |
| SD_RST_A                           | P7_2     | O    | SDMMC reset line (for eMMC devices) |
| SD_RST_B                           | P14_2    | O    |                                     |
| SD_RST_C                           | P9_2     | O    |                                     |
| SD_RST_D                           | P4_3     | O    |                                     |

## 3.19 Camera Interfaces and ISP

### 3.19.1 CPI Overview

The digital Camera Parallel Interface (CPI) enables pixel data reception from external CMOS sensors and camera modules, or from the internal MIPI CSI controller. The data transfer rate is limited by the maximum supported pixel clock and data bus width. CPI can direct the output data to either the system memory for software-based image signal processing or to the internal Image Signal Processor (ISP).

The device includes:

- One CPI controller in Shared Peripherals
  - The CPI receives parallel data from either of the following sources:
    - External camera sensor (up to 16-bit data bus)
    - Internal MIPI CSI controller (16-bit or 48-bit IPI data bus)

- The CPI outputs the processed data on the following independent ports:
  - 64-bit AXI port to system memory
  - 12-bit port to the ISP
- One Low-Power CPI (LPCPI) controller in the RTSS-HE
  - The LPCPI receives parallel data from an external camera sensor (up to 8-bit data bus)
  - The LPCPI outputs the processed data on 64-bit AXI port to system memory

Each CPI controller supports the following main features:

- Up to 50 MHz pixel clock
- Programmable polarity for the pixel clock, horizontal and vertical synchronization signals
- Single frame capture or continuous video frames capture
- Pixel clock output to external camera sensor

Each CPI controller supports the following specific features depending on the pixel data source and bus width:

- External camera sensor source:
  - Data modes: 1-, 2-, 4-, 8-, and 16-bit (CPI only)
  - Data mask for 16-bit data mode (CPI only)
  - Programmable MSB/LSB selection
  - Transfer 10-bit pixel encoding over 8-bit wide data bus
- MIPI CSI controller source:
  - Data modes: 8-, 16-, 32-, and 64-bit
  - Halt function to prevent FIFO overflow

#### NOTE

All Low Power peripherals are single-master accessible, including LPCPI. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

Table 3-25 presents CPI interface signals and provides descriptions to their functions.

**Table 3-25 CPI Signal Descriptions**

| Signal Name             | Pin Name | Type | Description                                        |
|-------------------------|----------|------|----------------------------------------------------|
| <b>CPI Data Bus A/B</b> |          |      |                                                    |
| CAM_D0_A                | P2_4     | I    | CPI pixel data from external camera sensor bit [0] |
| CAM_D0_B                | P8_0     |      |                                                    |
| CAM_D1_A                | P2_5     | I    | CPI pixel data from external camera sensor bit [1] |
| CAM_D1_B                | P8_1     |      |                                                    |
| CAM_D2_A                | P2_6     | I    | CPI pixel data from external camera sensor bit [2] |
| CAM_D2_B                | P8_2     |      |                                                    |
| CAM_D3_A                | P2_7     | I    | CPI pixel data from external camera sensor bit [3] |
| CAM_D3_B                | P8_3     |      |                                                    |
| CAM_D4_A                | P3_0     | I    | CPI pixel data from external camera sensor bit [4] |
| CAM_D4_B                | P8_4     |      |                                                    |
| CAM_D5_A                | P3_1     | I    | CPI pixel data from external camera sensor bit [5] |
| CAM_D5_B                | P8_5     |      |                                                    |

| Signal Name            | Pin Name | Type | Description                                              |
|------------------------|----------|------|----------------------------------------------------------|
| CAM_D6_A               | P3_2     | I    | CPI pixel data from external camera sensor bit [6]       |
| CAM_D6_B               | P8_6     |      |                                                          |
| CAM_D7_A               | P3_3     | I    | CPI pixel data from external camera sensor bit [7]       |
| CAM_D7_B               | P8_7     |      |                                                          |
| CAM_D8_A               | P3_4     | I    | CPI pixel data from external camera sensor bit [8]       |
| CAM_D8_B               | P9_0     |      |                                                          |
| CAM_D9_A               | P3_5     | I    | CPI pixel data from external camera sensor bit [9]       |
| CAM_D9_B               | P9_1     |      |                                                          |
| CAM_D10_A              | P3_6     | I    | CPI pixel data from external camera sensor bit [10]      |
| CAM_D10_B              | P9_2     |      |                                                          |
| CAM_D11_A              | P3_7     | I    | CPI pixel data from external camera sensor bit [11]      |
| CAM_D11_B              | P9_3     |      |                                                          |
| CAM_D12_A              | P4_0     | I    | CPI pixel data from external camera sensor bit [12]      |
| CAM_D12_B              | P9_4     |      |                                                          |
| CAM_D13_A              | P4_1     | I    | CPI pixel data from external camera sensor bit [13]      |
| CAM_D13_B              | P9_5     |      |                                                          |
| CAM_D14_A              | P4_2     | I    | CPI pixel data from external camera sensor bit [14]      |
| CAM_D14_B              | P9_6     |      |                                                          |
| CAM_D15_A              | P4_3     | I    | CPI pixel data from external camera sensor bit [15]      |
| CAM_D15_B              | P9_7     |      |                                                          |
| CPI Clock and Sync A/B |          |      |                                                          |
| CAM_HSYNC_A            | P0_0     | I    | CPI line valid from external camera sensor               |
| CAM_HSYNC_B            | P10_0    |      |                                                          |
| CAM_VSYNC_A            | P0_1     | I    | CPI vertical synchronization from external camera sensor |
| CAM_VSYNC_B            | P10_1    |      |                                                          |
| CAM_PCLK_A             | P0_2     | I    | CPI pixel clock from external camera sensor              |
| CAM_PCLK_B             | P10_2    |      |                                                          |
| CAM_XVCLK_A            | P0_3     | O    | CPI pixel clock to external camera sensor                |
| CAM_XVCLK_B            | P10_3    |      |                                                          |

Table 3-26 presents LPCPI interface signals and provides descriptions to their functions.

**Table 3-26 LPCPI Signal Descriptions**

| Signal Name                 | Pin Name | Type | Description                                          |
|-----------------------------|----------|------|------------------------------------------------------|
| <b>LPCPI Data Bus A/B/C</b> |          |      |                                                      |
| LPCAM_D0_A                  | P8_0     | I    | LPCPI pixel data from external camera sensor bit [0] |
| LPCAM_D0_B                  | P2_4     |      |                                                      |
| LPCAM_D0_C                  | P1_4     |      |                                                      |
| LPCAM_D1_A                  | P8_1     | I    | LPCPI pixel data from external camera sensor bit [1] |
| LPCAM_D1_B                  | P2_5     |      |                                                      |
| LPCAM_D1_C                  | P1_5     |      |                                                      |
| LPCAM_D2_A                  | P8_2     | I    | LPCPI pixel data from external camera sensor bit [2] |
| LPCAM_D2_B                  | P2_6     |      |                                                      |
| LPCAM_D2_C                  | P1_6     |      |                                                      |
| LPCAM_D3_A                  | P8_3     | I    | LPCPI pixel data from external camera sensor bit [3] |

| Signal Name                | Pin Name | Type | Description                                                |
|----------------------------|----------|------|------------------------------------------------------------|
| LPCAM_D3_B                 | P2_7     |      |                                                            |
| LPCAM_D3_C                 | P1_7     |      |                                                            |
| LPCAM_D4_A                 | P8_4     | I    | LPCPI pixel data from external camera sensor bit [4]       |
| LPCAM_D4_B                 | P3_0     |      |                                                            |
| LPCAM_D4_C                 | P2_0     |      |                                                            |
| LPCAM_D5_A                 | P8_5     | I    | LPCPI pixel data from external camera sensor bit [5]       |
| LPCAM_D5_B                 | P3_1     |      |                                                            |
| LPCAM_D5_C                 | P2_1     |      |                                                            |
| LPCAM_D6_A                 | P8_6     | I    | LPCPI pixel data from external camera sensor bit [6]       |
| LPCAM_D6_B                 | P3_2     |      |                                                            |
| LPCAM_D6_C                 | P2_2     |      |                                                            |
| LPCAM_D7_A                 | P8_7     | I    | LPCPI pixel data from external camera sensor bit [7]       |
| LPCAM_D7_B                 | P3_3     |      |                                                            |
| LPCAM_D7_C                 | P2_3     |      |                                                            |
| LPCPI Clock and Sync A/B/C |          |      |                                                            |
| LPCAM_HSYNC_A              | P10_0    | I    | LPCPI line valid from external camera sensor               |
| LPCAM_HSYNC_B              | P0_0     |      |                                                            |
| LPCAM_HSYNC_C              | P1_0     |      |                                                            |
| LPCAM_VSYNC_A              | P10_1    | I    | LPCPI vertical synchronization from external camera sensor |
| LPCAM_VSYNC_B              | P0_1     |      |                                                            |
| LPCAM_VSYNC_C              | P1_1     |      |                                                            |
| LPCAM_PCLK_A               | P10_2    | I    | LPCPI pixel clock from external camera sensor              |
| LPCAM_PCLK_B               | P0_2     |      |                                                            |
| LPCAM_PCLK_C               | P1_2     |      |                                                            |
| LPCAM_XVCLK_A              | P10_3    | O    | LPCPI pixel clock to external camera sensor                |
| LPCAM_XVCLK_B              | P0_3     |      |                                                            |
| LPCAM_XVCLK_C              | P1_3     |      |                                                            |

### 3.19.2 CSI Overview

The MIPI Camera Serial Interface (CSI) facilitates the data reception from a MIPI CSI-2 compliant camera sensor. The interface is realized through a MIPI CSI-2 host controller that implements the protocol functions defined in the MIPI CSI-2 Specification, and a MIPI D-PHY module acting as the physical layer.

The device includes a single CSI implementation.

The CSI supports the following main features:

- Conformity to MIPI standards:
  - MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 1.2, January 2014
  - MIPI Alliance Specification for D-PHY, Version 1.2, September 2014
- PHY Protocol Interface (PPI) between the CSI-2 host controller and the D-PHY receiver
- Up to two D-PHY RX data lanes
- Up to 2.5 Gbps throughput per lane
- Dynamically configurable multi-lane merging
- Long and short packet decoding
- Virtual channel extension—up to 16 interleaved virtual channels
- Timing accurate signaling of frame and line synchronization packets

- Several frame formats:
  - General frame or digital interlaced video with or without accurate sync timing
  - Data type (packet or frame level) and virtual channel interleaving
- Primary and secondary data formats:
  - YUV420: 8-bit (legacy)/8-bit/10-bit/8-bit (CSPS)/10-bit (CSPS)
  - YUV422: 8-bit/10-bit
  - RGB: RGB888/RGB666/RGB565/RGB555/RGB444
  - RAW: RAW6/RAW7/RAW8/RAW10/RAW12/RAW14/RAW16
  - Generic 8-bit long packet data types
  - User-defined byte-based data
  - Embedded data (RAW16)
- Error detection and correction at PHY, packet, line and frame level
- Up to four Data IDs (VC/DT pairs) for simultaneous error monitoring
- Data scrambling for Electromagnetic Interference (EMI) and Radio Frequency Interference (RFI) mitigation
- Configurable Image Pixel Interface (IPI) to system level that provides:
  - Conversion of CSI-2 packets data from byte to pixel format
  - 16- or 48-bit output parallel data bus, operating at pixel clock rate and delivering either one color component at a time or one pixel (or pair of pixels) per pixel clock cycle, respectively
  - Vertical and horizontal timing accurate video synchronization signals
  - 1024-entry FIFO for data storage and synchronization
- APB slave configuration interface

The CSI does not provide support for RAW data type decompression.

#### NOTE

The device provides the option for a 2<sup>nd</sup> MIPI D-PHY CSI-2 interface by using the MIPI D-PHY DSI in slave mode. This allows interleaving two image streams from two separate image sensors.

Table 3-27 presents MIPI CSI interface signals and provides descriptions to their functions.

**Table 3-27 MIPI CSI Signal Descriptions**

| Signal Name | Pin Name    | Type | Description                                      |
|-------------|-------------|------|--------------------------------------------------|
| MIPICSI_0_P | MIPICSI_0_P | I    | CSI D-PHY Rx differential data lane 0 (positive) |
| MIPICSI_0_N | MIPICSI_0_N | I    | CSI D-PHY Rx differential data lane 0 (negative) |
| MIPICSI_1_P | MIPICSI_1_P | I    | CSI D-PHY Rx differential data lane 1 (positive) |
| MIPICSI_1_N | MIPICSI_1_N | I    | CSI D-PHY Rx differential data lane 1 (negative) |
| MIPICSI_C_P | MIPICSI_C_P | I    | CSI D-PHY Rx differential clock lane (positive)  |
| MIPICSI_C_N | MIPICSI_C_N | I    | CSI D-PHY Rx differential clock lane (negative)  |

## NOTE

The CSI D-PHY Rx module shares the MIPI\_REXT signal connection to a reference resistor (200  $\Omega$ ,  $\pm 1\%$ ) with DSI D-PHY Tx module. For more details, see [Table 3-29](#) MIPI DSI Signal Descriptions.

### 3.19.3 ISP Overview

The ISP is capable of processing images received over the MIPI CSI or the CPI interface. The ISP is integrated in the data path between the camera interfaces and the memory, offering ultra-low power image processing as well as pixel processing and conversion.

The ISP is clocked at up to 400 MHz and has the following performance characteristics:

- Maximum input resolution: 2MP (1920 × 1080)
- Maximum output resolution: 2MP (1920 × 1080)
- Minimum output resolution: 64 × 64
- Maximum performance: up to 200 FPS (assuming 2MP image and 100 MHz pixel clock)

The ISP supports the following main features:

- Input color format: 8-bit, 10-bit, 12-bit Bayer; 8-bit, 10-bit YUV BT.601, BT.656
- Input monochrome format: 8-bit, 10-bit
- Frame rate control, configurable output FPS range from 60 FPS to 1 FPS
- Format conversion: drop chroma components or reduce bit depth
- Crop function: configurable Region-of-Interest (ROI) window size and offset
- Binning function with configurable step size
- Black Level Subtraction (BLS)
- Digital gain
- Demosaicing algorithm: Bayer to RGB format conversion
- Gamma correction
- Color Space Conversion (CSC) matrix transformation: RGB to YUV
- Scale function: drop pixels by down-sampling ratio
- YUV422 to YUV444 format conversion
- YUV444 to RGB format conversion
- Auto Exposure (AE) Algorithm
- Auto White Balance (AWB) Algorithm

The ISP supports the following output formats:

- 8-bit monochrome
- RAW 8/10/12-bit with raster scan
- YUV format
- Y-only format
- RGB888 planar format (R, G, B components are stored in separate memory planes)

The data path of the ISP module is connected to the system interconnect over 64-bit bus interface clocked at up to 400 MHz.

### 3.19.4 JPEG Encoder Overview

The JPEG Encoder accelerates image compression and works in tandem with the ISP to store individual images and MJPEG compressed video clips.

The JPEG module is clocked at up to 400 MHz and has the following performance characteristics:

- Maximum frame width: 16K
- Minimum resolution: 32 × 32
- Maximum performance: 2MP @ 200 FPS

The JPEG module has the following features:

- Supports JPEG ISO/IEC 10918-1, ITU-T T.81
- Baseline process (Huffman coding interleaved YUV420)
- MJPEG format (T.81 Annex H) in AVI container
- Encoding color space: YUV 4:0:0, 4:2:0, 4:2:2
- Slices mode encoding: N macroblock rows per slice
- Rate control for target bits per picture
- Encoding bit depth: 8 bits
- Output image step size: 16 pixels
- Input color formats: YUV400, YUV420, YUV422
- Input pixel layout: raster scan, tiled
- Color Space Conversion: 422 to 420
- Multi-region alpha blending

The data path of the JPEG module is connected to the system interconnect over 64-bit bus interface clocked at up to 400 MHz. It has 700+ cycles bus latency tolerance.

## 3.20 Display Interfaces

### 3.20.1 DPI Controller Overview

The Display Parallel Interface (DPI) provides a 24-bit RGB data bus either directly to LCD and TFT panels with a resolution of up to WXGA (1280 × 800) or to the MIPI DSI Controller. In addition to the 24 data lines, the interface includes pixel clock up to 50 MHz, horizontal and vertical synchronization pulses, and data enable signals with configurable polarity.

The device includes a single Configurable DPI Controller (CDC).

The CDC supports the following main features:

- Configurable resolution and refresh rate
- Two display layers
- Programmable background color
- Color Look-Up Table (CLUT) with 256 × 24-bit entries per layer for indexed pixel formats
- Flexible blending between the layers using alpha value (pixel alpha or constant alpha)
- Color keying: defining transparent color for pixel formats without alpha channel
- Windowing: blending a programmable rectangular area of one layer into the other
- Gamma correction
- Dithering (2 bits per color component): providing softer color transitions for displays with less color depth
- Multiple input pixel formats selectable per layer:
  - ARGB8888, RGBA8888, RGB888, RGB565, ARGB1555, ARGB4444
  - AL44 (4-bit alpha + 4-bit luminance) and L8 (8-bit luminance)
- RGB888 output pixel format
- Master Bus Interface (MBI): 64-bit AXI interface used for pixel data transfer
- Slave Bus Interface (SBI): 32-bit APB interface used for configuration

Table 3-28 presents DPI interface signals and provides descriptions to their functions.

Table 3-28 DPI Signal Descriptions

| Signal Name             | Pin Name | Type | Description                        |
|-------------------------|----------|------|------------------------------------|
| <b>DPI Data Bus A/B</b> |          |      |                                    |
| CDC_D0_A                | P8_0     | O    | DPI RGB pixel data output bit B[0] |
| CDC_D0_B                | P11_0    |      |                                    |
| CDC_D1_A                | P8_1     | O    | DPI RGB pixel data output bit B[1] |
| CDC_D1_B                | P11_1    |      |                                    |
| CDC_D2_A                | P8_2     | O    | DPI RGB pixel data output bit B[2] |
| CDC_D2_B                | P11_2    |      |                                    |
| CDC_D3_A                | P8_3     | O    | DPI RGB pixel data output bit B[3] |
| CDC_D3_B                | P11_3    |      |                                    |
| CDC_D4_A                | P8_4     | O    | DPI RGB pixel data output bit B[4] |
| CDC_D4_B                | P11_4    |      |                                    |
| CDC_D5_A                | P8_5     | O    | DPI RGB pixel data output bit B[5] |
| CDC_D5_B                | P11_5    |      |                                    |
| CDC_D6_A                | P8_6     | O    | DPI RGB pixel data output bit B[6] |
| CDC_D6_B                | P11_6    |      |                                    |
| CDC_D7_A                | P8_7     | O    | DPI RGB pixel data output bit B[7] |
| CDC_D7_B                | P11_7    |      |                                    |
| CDC_D8_A                | P9_0     | O    | DPI RGB pixel data output bit G[0] |
| CDC_D8_B                | P12_0    |      |                                    |
| CDC_D9_A                | P9_1     | O    | DPI RGB pixel data output bit G[1] |
| CDC_D9_B                | P12_1    |      |                                    |
| CDC_D10_A               | P9_2     | O    | DPI RGB pixel data output bit G[2] |
| CDC_D10_B               | P12_2    |      |                                    |
| CDC_D11_A               | P9_3     | O    | DPI RGB pixel data output bit G[3] |
| CDC_D11_B               | P12_3    |      |                                    |
| CDC_D12_A               | P9_4     | O    | DPI RGB pixel data output bit G[4] |
| CDC_D12_B               | P12_4    |      |                                    |
| CDC_D13_A               | P9_5     | O    | DPI RGB pixel data output bit G[5] |
| CDC_D13_B               | P12_5    |      |                                    |
| CDC_D14_A               | P9_6     | O    | DPI RGB pixel data output bit G[6] |
| CDC_D14_B               | P12_6    |      |                                    |
| CDC_D15_A               | P9_7     | O    | DPI RGB pixel data output bit G[7] |
| CDC_D15_B               | P12_7    |      |                                    |
| CDC_D16_A               | P10_0    | O    | DPI RGB pixel data output bit R[0] |
| CDC_D16_B               | P13_0    |      |                                    |
| CDC_D17_A               | P10_1    | O    | DPI RGB pixel data output bit R[1] |
| CDC_D17_B               | P13_1    |      |                                    |
| CDC_D18_A               | P10_2    | O    | DPI RGB pixel data output bit R[2] |
| CDC_D18_B               | P13_2    |      |                                    |
| CDC_D19_A               | P10_3    | O    | DPI RGB pixel data output bit R[3] |
| CDC_D19_B               | P13_3    |      |                                    |
| CDC_D20_A               | P10_4    | O    | DPI RGB pixel data output bit R[4] |
| CDC_D20_B               | P13_4    |      |                                    |
| CDC_D21_A               | P10_5    | O    | DPI RGB pixel data output bit R[5] |

| Signal Name            | Pin Name | Type | Description                        |
|------------------------|----------|------|------------------------------------|
| CDC_D21_B              | P13_5    |      |                                    |
| CDC_D22_A              | P10_6    | O    | DPI RGB pixel data output bit R[6] |
| CDC_D22_B              | P13_6    |      |                                    |
| CDC_D23_A              | P10_7    | O    | DPI RGB pixel data output bit R[7] |
| CDC_D23_B              | P13_7    |      |                                    |
| DPI Clock and Sync A/B |          |      |                                    |
| CDC_DE_A               | P5_4     | O    | DPI pixel data enable              |
| CDC_DE_B               | P0_7     |      |                                    |
| CDC_PCLK_A             | P5_3     | O    | DPI pixel clock                    |
| CDC_PCLK_B             | P2_3     |      |                                    |
| CDC_HSYNC_A            | P5_5     | O    | DPI horizontal synchronization     |
| CDC_HSYNC_B            | P4_1     |      |                                    |
| CDC_VSYNC_A            | P5_6     | O    | DPI vertical synchronization       |
| CDC_VSYNC_B            | P4_0     |      |                                    |

### 3.20.2 DSI Overview

The MIPI Display Serial Interface (DSI) facilitates the communication and data transfer to a MIPI DSI compliant display panel. The interface is realized through a MIPI DSI host controller that implements the protocol functions defined in the MIPI DSI Specification, and a MIPI D-PHY module acting as the physical layer.

The device includes a single DSI implementation.

The DSI supports the following main features:

- Conformity to MIPI standards:
  - MIPI Alliance Specification for Display Serial Interface (DSI) Version 1.2—16 June 2014
  - MIPI Alliance Standard for Display Pixel Interface v2.00 (DPI-2)—15 September 2005
  - MIPI Alliance Specification for Stereoscopic Display Formats (SDF) v1.0—22 November 2011
  - MIPI Alliance Specification for D-PHY v1.2, 01 August 2014
- PPI between the DSI host controller and the D-PHY transmitter
- Up to two D-PHY TX data lanes
- Up to 1.25 Gbps throughput per lane
- Bidirectional communication and escape mode support through data lane 0
- End of Transmission Packet (EoTp)
- ECC and checksum capabilities
- Fault recovery schemes
- Stereoscopic (3D) image data transmission
- Video mode only
- Configurable MIPI Display Pixel Interface (DPI) to system level that provides:
  - Data transfer in Video mode:
    - Real-time pixel stream
    - Shut Down Peripheral and Color Mode commands
  - 24-bit RGB color coding
  - Programmable polarity of all DPI interface signals
  - The maximum resolution and frame rate are limited by the pixel clock and the available DSI physical link bandwidth (defined by the number of lanes and the maximum speed per lane)
- Slave interface used for the transmission of generic commands
- Independently programmable virtual channel ID for the DPI and slave interfaces

- DPI payload FIFO with 1024 × 32-bit slots depth
- Generic command FIFO with 16 × 32-bit slots depth
- Generic payload FIFO with 128 × 32-bit slots depth
- Generic read FIFO with 32 × 32-bit slots depth
- Video mode pattern generator with the following capabilities:
  - Vertical and horizontal color bar generation without DPI stimuli
  - PHY Bit-Error Ratio (BER) pattern without DPI stimuli

The DSI does not support the following features:

- Command mode
- VESA® Display Stream Compression (DSC) standard

#### NOTE

The device provides the option for a 2<sup>nd</sup> MIPI D-PHY CSI-2 interface by using the MIPI D-PHY DSI in slave mode. This allows interleaving two image streams from two separate image sensors.

Table 3-29 presents MIPI DSI interface signals and provides descriptions to their functions.

**Table 3-29 MIPI DSI Signal Descriptions**

| Signal Name | Pin Name    | Type              | Description                                                                                      |
|-------------|-------------|-------------------|--------------------------------------------------------------------------------------------------|
| MIPIDSI_0_P | MIPIDSI_0_P | IO <sup>(3)</sup> | DSI D-PHY Tx / CSI D-PHY Rx differential data lane 0 (positive)                                  |
| MIPIDSI_0_N | MIPIDSI_0_N | IO <sup>(3)</sup> | DSI D-PHY Tx / CSI D-PHY Rx differential data lane 0 (negative)                                  |
| MIPIDSI_1_P | MIPIDSI_1_P | IO <sup>(2)</sup> | DSI D-PHY Tx / CSI D-PHY Rx differential data lane 1 (positive)                                  |
| MIPIDSI_1_N | MIPIDSI_1_N | IO <sup>(2)</sup> | DSI D-PHY Tx / CSI D-PHY Rx differential data lane 1 (negative)                                  |
| MIPIDSI_C_P | MIPIDSI_C_P | IO <sup>(2)</sup> | DSI D-PHY Tx / CSI D-PHY Rx differential clock lane (positive)                                   |
| MIPIDSI_C_N | MIPIDSI_C_N | IO <sup>(2)</sup> | DSI D-PHY Tx / CSI D-PHY Rx differential clock lane (negative)                                   |
| MIPI_REXT   | MIPI_REXT   | P                 | DSI D-PHY Tx and CSI D-PHY Rx external reference resistor (200 Ω, ±1%) connection <sup>(1)</sup> |

1. Shared with CSI D-PHY Rx module.

2. Output, when primary MIPI DSI function is used; Input, when secondary MIPI CSI-2 function is used.

3. Input/Output, when primary MIPI DSI function is used; Input, when secondary MIPI CSI-2 function is used.

## 3.21 Analog Peripherals

### 3.21.1 ADC Overview

The Analog-to-Digital Converter (ADC) modules are 12-bit/24-bit, multi-input units used for analog signals conversion into digital values.

The device includes three ADC12 modules and one ADC24 module.

ADC12 modules support the following main features:

- 12-bit Successive Approximation Register (SAR) ADC
- Conversion rate of up to 1.25 MSPS
- 6 external inputs and one internal input:
  - 6 external pins may be configured to 6 single-ended or 3 differential inputs
  - One input from the on-chip temperature sensor (TSENS) (valid for ADC120 and ADC122 only)

ADC24 supports the following main features:

- 24-bit Sigma-Delta ADC
- Conversion rate of up to 16 kSPS
- 4 external differential inputs

ADC12 and ADC24 common features:

- Programmable gain instrumentation amplifier (up to 38 dB gain)
- On-chip offset calibration and factory calibrated gain error
- Widely programmable sample time
- Hardware averaging option (up to 256 samples) for enhanced Signal-to-Noise Ratio (SNR)
  - ADC12 must use hardware averaging at all times, with a minimum of two samples per average
- Flexible digital user interface:
  - Programmable input scan modes:
    - Single-shot or continuous conversions
    - A sequencer can be programmed to loop over a selection of inputs
  - Conversions can be triggered also externally by UTIMER events or QEC pins
  - Conversion results can be stored into sample registers and to SRAM via DMA
  - Hardware data shift:
    - 1 to 12 bits left shift
    - 1 to 12 bits right shift (up to 8 bits for the averaging function plus 4 bits more)
  - Threshold and window detection options. A comparator logic can generate interrupts when an input signal passes programmable thresholds
- Designed for low power operation:
  - ADC sample rate is selectable via a clock divider
  - ADC power consumption decreases as sample rate decreases
- The ADC12, ADC24, as well as other analog peripherals, are powered from a dedicated internal 1.8-V LDO

For information on ADC interface signals and their descriptions, see [Section 3.21.6 Analog Signals](#).

### 3.21.2 DAC12 Overview

The Digital-to-Analog Converter (DAC12) module converts 12-bit digital values into analog voltage signals. The analog output range is between 0 V and 1.8 V in LP mode.

The device includes two DAC12 modules.

Each DAC12 module supports the following main features:

- Up to 1 kHz conversion rate at 12-bit resolution
- Accepts unsigned binary or two's complement signed digital data
- Programmable output current up to 1.5 mA
- Programmable load capacitance compensation
- Internal 1.8-V voltage reference
- Excellent high-frequency Power Supply Rejection Ratio (PSRR)
- Maximum current output up to 1.5 mA
- Software-selectable low-power (LP) or high-performance (HP) modes
  - HP mode handles larger resistive load at the expense of higher power consumption
  - LP mode handles slow sample rate and light resistive load for power savings

For information on DAC interface signals and their descriptions, see [Section 3.21.6 Analog Signals](#).

### 3.21.3 CMP Overview

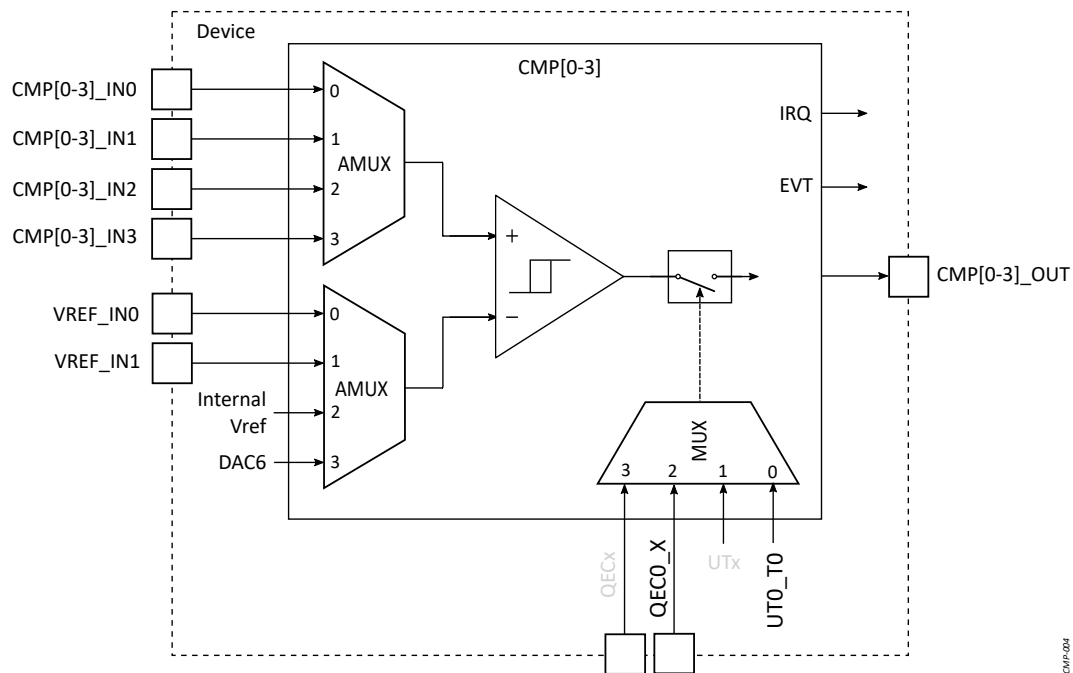
The High-Speed Comparator (CMP) module is a rail-to-rail, multi-input, analog comparator with programmable reference voltage and hysteresis.

The device includes up to four CMP modules.

Each CMP module supports the following main features:

- Reference voltage from DAC6, internal Vref, or external pins
- Programmable hysteresis
- Windowing (gating) driven by one of four events from UTIMER and QEC
- Comparator result inverter
- Configurable number of taps for filtering
- Interrupt generation after filtering
- Response time: < 5 ns
- Power supply from internal 1.8-V LDO (LDO-5)

**Figure 3-13 CMP Overview**



For information on CMP interface signals and their descriptions, see [Section 3.21.6 Analog Signals](#).

[Table 3-30](#) presents the CMP digital outputs.

**Table 3-30 CMP Signal Descriptions**

| Signal Name            | Pin Name | Type | Description                   |
|------------------------|----------|------|-------------------------------|
| <b>CMP Outputs A/B</b> |          |      |                               |
| CMP0_OUT_A             | P7_3     | O    | CMP0 comparison result output |
| CMP0_OUT_B             | P14_7    |      |                               |
| CMP1_OUT_A             | P7_2     | O    | CMP1 comparison result output |
| CMP1_OUT_B             | P14_6    |      |                               |
| CMP2_OUT_A             | P7_1     | O    | CMP2 comparison result output |
| CMP2_OUT_B             | P14_5    |      |                               |
| CMP3_OUT_A             | P7_0     | O    | CMP3 comparison result output |

| Signal Name | Pin Name | Type | Description |
|-------------|----------|------|-------------|
| CMP3_OUT_B  | P14_4    |      |             |

### 3.21.4 LPCMP Overview

The Low-Power Comparator (LPCMP) module is a low power, rail-to-rail, analog comparator with selectable reference voltage and hysteresis.

The device includes a single LPCMP module located in the PD0 domain.

The LPCMP supports the following main features:

- Up to four external pins for voltage monitoring
- Voltage reference from:
  - Internal AON 0.8-V voltage reference or
  - External VREF pins
- Programmable hysteresis
- Power supply from VDD\_IO\_1V8 pin
- Response time: < 10  $\mu$ s
- The LPCMP interrupt can be used as a wake-up source from STANDBY and STOP low-power modes

#### NOTE

All Low Power peripherals are single-master accessible, including LPCMP. Ensure that application software manages access to these LP peripherals such that no more than one bus master (CPU or DMA) attempts access at a time, using semaphores or similar techniques.

For information on LPCMP interface signals and their descriptions, see [Section 3.21.6 Analog Signals](#).

### 3.21.5 TSENS Overview

The Temperature Sensor (TSENS) generates a voltage  $V_{TEMP}$  that varies incrementally with the silicon die's temperature.

The TSENS is connected internally to input channel 6 of ADC120 and ADC122. The ADC modules can convert the sensor output voltage into a digital value. The real temperature can be translated using *temperature.h* C header file available in the Alif Ensemble CMSIS pack.

The sensor provides good linearity and accuracy of better than 2.4 °C. Additional calibration can be applied to improve accuracy.

### 3.21.6 Analog Signals

[Table 3-31](#) shows how the analog signals are mapped simultaneously to functions of the analog modules. Each signal can be used by more than one module at a time.

**Table 3-31 Analog Signal Functions Mapping**

| Signal Name | Function by Module |             |     |          |       |
|-------------|--------------------|-------------|-----|----------|-------|
|             | ADC12              | ADC24       | DAC | CMP      | LPCMP |
| ANA_S0      | ADC120_IN0         | ADC24_IN0_P |     | CMPO_IN0 |       |
| ANA_S1      | ADC120_IN1         | ADC24_IN1_P |     | CMP1_IN0 |       |
| ANA_S2      | ADC120_IN2         | ADC24_IN2_P |     | CMP2_IN0 |       |

| Signal Name | Function by Module |             |             |          |           |
|-------------|--------------------|-------------|-------------|----------|-----------|
|             | ADC12              | ADC24       | DAC         | CMP      | LPCMP     |
| ANA_S3      | ADC120_IN3         | ADC24_IN3_P |             | CMP3_IN0 |           |
| ANA_S4      | ADC120_IN4         | ADC24_IN0_N |             | CMP0_IN3 |           |
| ANA_S5      | ADC120_IN5         | ADC24_IN1_N |             | CMP1_IN3 |           |
| ANA_S6      | ADC121_IN0         | ADC24_IN2_N |             | CMP0_IN1 |           |
| ANA_S7      | ADC121_IN1         | ADC24_IN3_N |             | CMP1_IN1 |           |
| ANA_S8      | ADC121_IN2         |             |             | CMP2_IN1 |           |
| ANA_S9      | ADC121_IN3         |             |             | CMP3_IN1 |           |
| ANA_S10     | ADC121_IN4         |             |             | CMP2_IN3 |           |
| ANA_S11     | ADC121_IN5         |             |             | CMP3_IN3 |           |
| ANA_S12     | ADC122_IN0         |             |             | CMP0_IN2 |           |
| ANA_S13     | ADC122_IN1         |             |             | CMP1_IN2 |           |
| ANA_S14     | ADC122_IN2         |             |             | CMP2_IN2 |           |
| ANA_S15     | ADC122_IN3         |             |             | CMP3_IN2 |           |
| ANA_S16     | ADC122_IN4         |             |             | VREF_IN0 |           |
| ANA_S17     | ADC122_IN5         |             |             | VREF_IN1 |           |
| ANA_S18     |                    |             | DAC12_0_OUT |          | VREF_IN2  |
| ANA_S19     |                    |             | DAC12_1_OUT |          |           |
| ANA_S20     |                    |             |             |          | LPCMP_IN0 |
| ANA_S21     |                    |             |             |          | LPCMP_IN1 |
| ANA_S22     |                    |             |             |          | LPCMP_IN2 |
| ANA_S23     |                    |             |             |          | LPCMP_IN3 |

Table 3-32 presents the analog signals with the respective mapping to the analog modules and provides descriptions to their functions.

**Table 3-32 Analog Signal Descriptions**

| Signal Name | Pin Name | Type | Description                                                                                                 |
|-------------|----------|------|-------------------------------------------------------------------------------------------------------------|
| ANA_S0      | PO_0     | A    | ADC120_IN0 (ADC120 input 0)<br>ADC24_IN0_P (ADC24 differential input 0 positive)<br>CMP0_IN0 (CMP0 input 0) |
| ANA_S1      | PO_1     | A    | ADC120_IN1 (ADC120 input 1)<br>ADC24_IN1_P (ADC24 differential input 1 positive)<br>CMP1_IN0 (CMP1 input 0) |
| ANA_S2      | PO_2     | A    | ADC120_IN2 (ADC120 input 2)<br>ADC24_IN2_P (ADC24 differential input 2 positive)<br>CMP2_IN0 (CMP2 input 0) |
| ANA_S3      | PO_3     | A    | ADC120_IN3 (ADC120 input 3)<br>ADC24_IN3_P (ADC24 differential input 3 positive)<br>CMP3_IN0 (CMP3 input 0) |
| ANA_S4      | PO_4     | A    | ADC120_IN4 (ADC120 input 4)<br>ADC24_IN0_N (ADC24 differential input 0 negative)<br>CMP0_IN3 (CMP0 input 3) |
| ANA_S5      | PO_5     | A    | ADC120_IN5 (ADC120 input 5)<br>ADC24_IN1_N (ADC24 differential input 1 negative)<br>CMP1_IN3 (CMP1 input 3) |
| ANA_S6      | PO_6     | A    | ADC121_IN0 (ADC121 input 0)                                                                                 |

| Signal Name | Pin Name | Type | Description                                                                                                 |
|-------------|----------|------|-------------------------------------------------------------------------------------------------------------|
|             |          |      | ADC24_IN2_N (ADC24 differential input 2 negative)<br>CMP0_IN1 (CMP0 input 1)                                |
| ANA_S7      | P0_7     | A    | ADC121_IN1 (ADC121 input 1)<br>ADC24_IN3_N (ADC24 differential input 3 negative)<br>CMP1_IN1 (CMP1 input 1) |
| ANA_S8      | P1_0     | A    | ADC121_IN2 (ADC121 input 2)<br>CMP2_IN1 (CMP2 input 1)                                                      |
| ANA_S9      | P1_1     | A    | ADC121_IN3 (ADC121 input 3)<br>CMP3_IN1 (CMP3 input 1)                                                      |
| ANA_S10     | P1_2     | A    | ADC121_IN4 (ADC121 input 4)<br>CMP2_IN3 (CMP2 input 3)                                                      |
| ANA_S11     | P1_3     | A    | ADC121_IN5 (ADC121 input 5)<br>CMP3_IN3 (CMP3 input 3)                                                      |
| ANA_S12     | P1_4     | A    | ADC122_IN0 (ADC122 input 0)<br>CMP0_IN2 (CMP0 input 2)                                                      |
| ANA_S13     | P1_5     | A    | ADC122_IN1 (ADC122 input 1)<br>CMP1_IN2 (CMP1 input 2)                                                      |
| ANA_S14     | P1_6     | A    | ADC122_IN2 (ADC122 input 2)<br>CMP2_IN2 (CMP2 input 2)                                                      |
| ANA_S15     | P1_7     | A    | ADC122_IN3 (ADC122 input 3)<br>CMP3_IN2 (CMP3 input 2)                                                      |
| ANA_S16     | P2_0     | A    | ADC122_IN4 (ADC122 input 4)<br>VREF_IN0 (CMP0-CMP3 and LPCMP reference voltage input 0)                     |
| ANA_S17     | P2_1     | A    | ADC122_IN5 (ADC122 input 5)<br>VREF_IN1 (CMP0-CMP3 and LPCMP reference voltage input 1)                     |
| ANA_S18     | P2_2     | A    | DAC12_0_OUT (DAC120 output)<br>VREF_IN2 (LPCMP reference voltage input 2)                                   |
| ANA_S19     | P2_3     | A    | DAC12_1_OUT (DAC121 output)                                                                                 |
| ANA_S20     | P2_4     | A    | LPCMP_IN0 (LPCMP input 0)                                                                                   |
| ANA_S21     | P2_5     | A    | LPCMP_IN1 (LPCMP input 1)                                                                                   |
| ANA_S22     | P2_6     | A    | LPCMP_IN2 (LPCMP input 2)                                                                                   |
| ANA_S23     | P2_7     | A    | LPCMP_IN3 (LPCMP input 3)                                                                                   |

## 3.22 Debug Infrastructure

To support the debug of multiple cores running simultaneously, the device provides an extensive debug infrastructure, compliant with the Arm® Debug Interface Architecture Specification ADIv6.0. The debug features include:

- JTAG debug support
- Serial Wire Debug (SWD) support
- External debug of SE, APSS, RTSS-HP or RTSS-HE by an off-chip debugger
- Debug through power down for APSS, RTSS-HP and RTSS-HE
- Debug from reset for all systems
- Support for single or multi-system debug
- Trace and cross trigger capabilities

Table 3-33 presents JTAG interface signals and provides descriptions to their functions.

**Table 3-33 JTAG Signal Descriptions**

| Signal Name   | Pin Name | Type | Description                 |
|---------------|----------|------|-----------------------------|
| <b>JTAG</b>   |          |      |                             |
| JTAG_TCK      | P4_4     | I    | JTAG test clock input       |
| JTAG_TMS      | P4_5     | I    | JTAG test mode select input |
| JTAG_TDI      | P4_6     | I    | JTAG test data input        |
| JTAG_TDO      | P4_7     | O    | JTAG test data output       |
| JTAG_TDATA0   | P4_0     | O    | JTAG trace data output 0    |
| JTAG_TDATA1   | P4_1     | O    | JTAG trace data output 1    |
| JTAG_TDATA2   | P4_2     | O    | JTAG trace data output 2    |
| JTAG_TDATA3   | P4_3     | O    | JTAG trace data output 3    |
| JTAG_TRACECLK | P3_7     | O    | JTAG trace clock output     |

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**NOTE**

Code execution tracing during debug stores the resulting trace data in on-chip SRAM that can be read out of the device for formatting and post-analysis.

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## 4 Pin Assignments

### 4.1 Pin Location per Package Type

#### 4.1.1 WLCSP216 Package Pin Location Assignment

Figure 4-1 presents a simplified diagram of the WLCSP216 package pin locations.

**Figure 4-1 WLCSP216 Pin Location Assignment Diagram (Top View)**

|    | 1 | 2             | 3 | 4              | 5 | 6             | 7 | 8           | 9 | 10            | 11 | 12          | 13 | 14       | 15 | 16           | 17 | 18           |
|----|---|---------------|---|----------------|---|---------------|---|-------------|---|---------------|----|-------------|----|----------|----|--------------|----|--------------|
| A  |   | GPIO4_3       |   | GPIO13_7       |   | GPIO5_5       |   | VDD_IO_1V8  |   | GPIO12_4      |    | GPIO7_0     |    | GPIO8_2  |    | VSS          |    | VDD_ANA_0V8  |
| B  |   | VSS           |   | GPIO4_7        |   | GPIO5_2       |   | GPIO5_7     |   | VSS           |    | GPIO14_0    |    | GPIO8_0  |    | VDD_SX_0V8   |    | VSS_RF       |
| C  |   | GPIO4_1       |   | GPIO5_0        |   | GPIO5_4       |   | GPIO6_2     |   | GPIO6_6       |    | GPIO7_1     |    | GPIO8_3  |    | HFXO_N       |    | GPIO3_3      |
| D  |   | GPIO12_1      |   | GPIO4_2        |   | GPIO13_5      |   | GPIO5_6     |   | VDD_CORE_0V8  |    | GPIO6_7     |    | GPIO8_1  |    | HFXO_P       |    | GPIO3_2      |
| E  |   | GPIO12_0      |   | SEUART_TX      |   | GPIO13_6      |   | GPIO6_0     |   | GPIO6_5       |    | GPIO7_3     |    | GPIO3_4  |    | N.C.         |    | VDD_CORE_0V8 |
| F  |   | GPIO13_2      |   | GPIO4_0        |   | SEUART_RX     |   | GPIO5_3     |   | GPIO6_3       |    | GPIO12_7    |    | GPIO3_5  |    | GPIO14_2     |    | VSS          |
| G  |   | GPIO13_1      |   | GPIO13_4       |   | GPIO4_4       |   | GPIO5_1     |   | GPIO6_4       |    | GPIO8_4     |    | GPIO14_1 |    | GPIO8_5      |    | GPIO8_7      |
| H  |   | VSS           |   | GPIO13_0       |   | NSRST         |   | GPIO4_6     |   | GPIO6_1       |    | GPIO12_6    |    | GPIO8_6  |    | GPIO9_0      |    | GPIO9_1      |
| J  |   | VDD_IO_1V8    |   | GPIO13_3       |   | GPIO12_3      |   | GPIO0_2     |   | GPIO12_5      |    | GPIO3_0     |    | GPIO9_2  |    | GPIO9_5      |    | GPIO9_4      |
| K  |   | GPIO2_5       |   | VDD_CORE_0V8   |   | GPIO12_2      |   | GPIO4_5     |   | N.C.          |    | GPIO7_2     |    | GPIO9_3  |    | GPIO17_0     |    | GPIO9_6      |
| L  |   | GPIO2_6       |   | GPIO2_4        |   | GPIO2_7       |   | GPIO0_1     |   | GPIO16_0      |    | GPIO3_1     |    | GPIO17_1 |    | GPIO9_7      |    | GPIO17_2     |
| M  |   | GPIO2_0       |   | GPIO2_2        |   | GPIO2_3       |   | GPIO1_3     |   | GPIO16_1      |    | GPIO11_3    |    | GPIO10_0 |    | GPIO10_1     |    | GPIO17_3     |
| N  |   | GPIO2_1       |   | GPIO1_7        |   | GPIO1_2       |   | POR_N       |   | VREG_MIPI_0V8 |    | GPIO11_2    |    | GPIO17_4 |    | GPIO17_5     |    | GPIO10_2     |
| P  |   | GPIO1_4       |   | GPIO1_6        |   | GPIO1_1       |   | GPIO0_3     |   | GPIO16_2      |    | GPIOV_3     |    | GPIO11_0 |    | GPIO10_3     |    | GPIO17_6     |
| R  |   | GPIO1_5       |   | GPIO1_0        |   | N.C.          |   | GPIO16_6    |   | VDD_MIPI_1V8  |    | GPIOV_1     |    | GPIO10_5 |    | GPIO10_4     |    | GPIO17_7     |
| T  |   | GPIO0_7       |   | GPIO0_5        |   | GPIO0_4       |   | VDD_BATT    |   | GPIO16_5      |    | GPIOV_4     |    | GPIOV_0  |    | GPIO10_6     |    | GPIO10_7     |
| U  |   | GPIO0_6       |   | VREF_N         |   | LFXO_P        |   | GPIO16_7    |   | VSS           |    | GPIO14_3    |    | GPIO7_5  |    | GPIO7_4      |    | GPIO11_1     |
| V  |   | VREG_MIPI_1V8 |   | VREF_P         |   | VREG_CORE_0V8 |   | VREG_AON    |   | MIPI_REXT     |    | GPIO14_5    |    | GPIOV_5  |    | VDD_IO_FLEX  |    | GPIO7_6      |
| W  |   | VDD_MAIN      |   | VREG_LP_1V8    |   | VDD_IO_1V8    |   | MIPICSI_C_P |   | MIPIDSI_C_P   |    | GPIO14_4    |    | GPIOV_7  |    | VSS          |    | GPIO7_7      |
| Y  |   | VSS_ANA       |   | VREG_AUX_2_1V8 |   | LFXO_N        |   | MIPICSI_C_N |   | MIPIDSI_C_N   |    | GPIO14_6    |    | GPIO11_4 |    | GPIO3_7      |    | VDD_IO_1V8   |
| AA |   | GPIO0_0       |   | VREG_AUX_1_1V8 |   | GPIO16_4      |   | MIPICSI_0_N |   | MIPIDSI_1_P   |    | USB_IO_ID   |    | GPIO11_6 |    | GPIO3_6      |    | GPIOV_2      |
| AB |   | VDD_BUCK      |   | VSW            |   | VDD_CORE_0V8  |   | MIPICSI_1_N |   | MIPIDSI_0_P   |    | USB_VBUS    |    | USB_DM   |    | VDD_CORE_0V8 |    | VSS          |
| AC |   | VSW           |   | VSS            |   | GPIO16_3      |   | MIPICSI_0_P |   | MIPIDSI_1_N   |    | VDD_USB_3V3 |    | USB_DP   |    | GPIO11_7     |    | GPIOV_6      |
| AD |   | VSS_BUCK      |   | VREG_DIG_1V8   |   | VSS           |   | MIPICSI_1_P |   | MIPIDSI_0_N   |    | USB_REXT    |    | VSS      |    | GPIO14_7     |    | GPIO11_5     |

For detailed information about package outlines, thermal characteristics, and markings, see [Section 6.2.1 WLCSP216 Package Information](#).

## 4.1.2 FBGA194 Package Pin Location Assignment

Figure 4-2 presents a simplified diagram of the FBGA194 package pin locations.

**Figure 4-2 FBGA194 Pin Location Assignment Diagram**

|   | 1            | 2          | 3          | 4       | 5            | 6            | 7        | 8           | 9           | 10          | 11          | 12           | 13            | 14          | 15          | 16          | 17       | 18            | 19            |
|---|--------------|------------|------------|---------|--------------|--------------|----------|-------------|-------------|-------------|-------------|--------------|---------------|-------------|-------------|-------------|----------|---------------|---------------|
| A | VDD_PLL_OV8  | VDD_SX_OV8 | HFXO_N     | HFXO_P  | VDD_IO_1V8   | GPIO3_1      | GPIO8_3  | GPIO7_3     | GPIO6_7     | GPIO12_5    | GPIO6_2     | GPIO6_0      | SEUART_TX     | SEUART_RX   | GPIO13_7    | GPIO5_0     | GPIO13_5 | GPIO4_6       | GPIO4_5       |
| B | N.C.         | VSS        | GPIO7_1    | GPIO8_4 | VDD_CORE_OV8 | GPIO3_0      | GPIO8_0  | GPIO7_0     | GPIO14_0    | GPIO6_3     | GPIO5_7     | GPIO5_6      | GPIO5_3       | GPIO5_1     | GPIO13_6    | GPIO4_7     | GPIO4_4  | GPIO4_3       | GPIO4_1       |
| C | N.C.         | GPIO8_1    | GPIO8_2    |         |              |              |          |             |             |             |             |              |               |             |             |             |          | VSS           | GPIO4_2       |
| D | GPIO7_2      | GPIO12_7   |            |         |              |              |          |             |             |             |             |              |               |             |             |             |          | GPIO12_3      | VDD_IO_1V8    |
| E | VDD_CORE_OV8 | GPIO3_2    |            |         | GPIO12_6     | GPIO6_6      | GPIO6_5  | GPIO6_4     | GPIO6_1     | GPIO5_5     | GPIO5_4     | GPIO5_2      | GPIO13_3      | GPIO13_4    | GPIO12_2    |             |          | GPIO12_1      | VDD_CORE_OV8  |
| F | GPIO3_5      | GPIO3_4    |            |         | GPIO12_4     |              |          |             |             |             |             |              |               |             | GPIO13_2    |             |          | GPIO4_0       | GPIO12_0      |
| G | GPIO14_2     | GPIO3_3    |            |         | GPIO9_2      |              |          |             |             |             |             |              |               |             | GPIO13_1    |             |          | GPIO13_0      | GPIO2_4       |
| H | GPIO8_5      | GPIO14_1   |            |         | GPIO9_3      |              |          |             |             |             |             |              |               |             | GPIO2_3     |             |          | GPIO2_6       | GPIO2_5       |
| J | GPIO8_7      | GPIO8_6    |            |         | GPIO9_4      |              |          | N.C.        | GPIO11_5    | VSS         | VSS         | NSRST        |               |             | GPIO2_2     |             |          | GPIO1_7       | GPIO2_7       |
| K | GPIO9_1      | GPIO9_0    |            |         | GPIO9_6      |              |          | GPIO11_4    | VSS         | VSS         | VSS         | GPIO14_6     |               |             | GPIO1_3     |             |          | GPIO2_1       | GPIO2_0       |
| L | GPIO9_5      | VSS        |            |         | GPIO9_7      |              |          | GPIO3_7     | GPIO11_7    | VSS         | GPIO14_5    | GPIO14_7     |               |             | GPIO1_2     |             |          | GPIO1_5       | GPIO1_6       |
| M | GPIO10_1     | GPIO10_0   |            |         | GPIO10_4     |              |          |             |             |             |             |              |               |             | GPIO1_1     |             |          | N.C.          | GPIO1_4       |
| N | GPIO10_2     | GPIO10_3   |            |         | GPIO10_5     |              |          |             |             |             |             |              |               |             | GPIO0_5     |             |          | VREF_P        | VREG_MIP1_1V8 |
| P | GPIO10_7     | GPIO11_0   |            |         | GPIO10_6     |              |          |             |             |             |             |              |               |             | GPIO0_6     |             |          | VSS_ANA       | VDD_MAIN      |
| R | GPIO11_1     | GPIO11_2   |            |         | GPIO11_3     | GPIO11_6     | GPIO14_3 | GPIO14_4    | USB_IO_ID   | GPIO0_4     | GPIO0_3     | GPIO0_2      | GPIO0_1       | GPIO1_0     | GPIO0_7     |             |          | VDD_BUCK      | GPIO0_0       |
| T | GPIO7_4      | GPIO7_5    |            |         |              |              |          |             |             |             |             |              |               |             |             |             |          | VDD_BATT      | VSW           |
| U | GPIO7_7      | GPIOV_2    | GPIO7_6    |         |              |              |          |             |             |             |             |              |               |             |             |             | VREG_AON | POR_N         | VREG_DIG_1V8  |
| V | GPIOV_3      | GPIOV_0    | GPIOV_4    | GPIOV_6 | GPIO3_6      | VDD_CORE_OV8 | USB_DM   | USB_REXT    | MIPIDSI_1_N | MIPIDSI_C_N | MIPIDSI_0_N | VSS          | MIPI_REXT     | MIPICSI_0_N | MIPICSI_1_N | MIPICSI_C_N | LFXO_N   | VREG_AUX_1V8  | VSS_BUCK      |
| W | VDD_IO_FLEX  | GPIOV_1    | VDD_IO_1V8 | GPIOV_5 | GPIOV_7      | USB_VBUS     | USB_DP   | VDD_USB_3V3 | MIPIDSI_1_P | MIPIDSI_C_P | MIPIDSI_0_P | VDD_MIPI_1V8 | VREG_MIPI_OV8 | MIPICSI_0_P | MIPICSI_1_P | MIPICSI_C_P | LFXO_P   | VREG_CORE_OV8 | VREG_LP_1V8   |

For detailed information about package outlines, thermal characteristics, and markings, see [Section 6.2.2 FBGA194 Package Information](#).

## 4.2 Pin Function Options by Location

Table 4-1 describes the pin functions available as multiplexed on each pin.

### NOTE

A peripheral I/O signal can be routed to up to four different pins. In such cases, a suffix \_A, \_B, \_C, or \_D is added to the signal name for differentiation. A group of signals with the same suffix is also known as Pin Set or Pin Group.

There are no restrictions on the combination of signals from different pin groups (A, B, C, or D). However, it is user's responsibility to make sure that each peripheral I/O signal is routed to only one pin at a time through the pin multiplexing options.

### CAUTION

The following pin multiplexing options are recommended:

- TBD

Table 4-1 Pin Function Options by Location

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7)  | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|------------------|----------------|
| PO_0         | AA2                          | R19                         | GPIO0_0         | IO              | 0                          | PO_0                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D0_A      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART0_RX_A      | I               | 2                          |                               |                  |                |
|              |                              |                             | I3C_SDA_A       | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT0_T0_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_HSYNC_B   | I               | 5                          |                               |                  |                |
|              |                              |                             | CAM_HSYNC_A     | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S0          | A               | 7                          |                               |                  |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7)  | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|------------------|----------------|
| PO_1         | L8                           | R13                         | GPIO0_1         | IO              | 0                          | PO_1                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D1_A      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART0_TX_A      | O               | 2                          |                               |                  |                |
|              |                              |                             | I3C_SCL_A       | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT0_T1_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_VSYNC_B   | I               | 5                          |                               |                  |                |
|              |                              |                             | CAM_VSYNC_A     | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S1          | A               | 7                          |                               |                  |                |
| PO_2         | J8                           | R12                         | GPIO0_2         | IO              | 0                          | PO_2                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D2_A      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART0_CTS_A     | I               | 2                          |                               |                  |                |
|              |                              |                             | I2C0_SDA_A      | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT1_T0_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_PCLK_B    | I               | 5                          |                               |                  |                |
|              |                              |                             | CAM_PCLK_A      | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S2          | A               | 7                          |                               |                  |                |
| PO_3         | P7                           | R11                         | GPIO0_3         | IO              | 0                          | PO_3                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D3_A      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART0_RTS_A     | O               | 2                          |                               |                  |                |
|              |                              |                             | I2C0_SCL_A      | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT1_T1_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_XVCLK_B   | O               | 5                          |                               |                  |                |
|              |                              |                             | CAM_XVCLK_A     | O               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S3          | A               | 7                          |                               |                  |                |
| PO_4         | T5                           | R10                         | GPIO0_4         | IO              | 0                          | PO_4                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D4_A      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART1_RX_A      | I               | 2                          |                               |                  |                |
|              |                              |                             | PDM_D0_A        | I               | 3                          |                               |                  |                |
|              |                              |                             | I2C1_SDA_A      | IO              | 4                          |                               |                  |                |
|              |                              |                             | UT2_T0_A        | IO              | 5                          |                               |                  |                |
|              |                              |                             | CAN_RXD_B       | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S4          | A               | 7                          |                               |                  |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7)  | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|------------------|----------------|
| P0_5         | T3                           | N15                         | GPIO0_5         | IO              | 0                          | P0_5                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D5_A      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART1_TX_A      | O               | 2                          |                               |                  |                |
|              |                              |                             | PDM_C0_A        | O               | 3                          |                               |                  |                |
|              |                              |                             | I2C1_SCL_A      | IO              | 4                          |                               |                  |                |
|              |                              |                             | UT2_T1_A        | IO              | 5                          |                               |                  |                |
|              |                              |                             | CAN_TXD_B       | O               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S5          | A               | 7                          |                               |                  |                |
| P0_6         | U2                           | P15                         | GPIO0_6         | IO              | 0                          | P0_6                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D6_A      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART1_CTS_A     | I               | 2                          |                               |                  |                |
|              |                              |                             | PDM_D1_A        | I               | 3                          |                               |                  |                |
|              |                              |                             | I2C2_SCL_A      | IO              | 4                          |                               |                  |                |
|              |                              |                             | UT3_T0_A        | IO              | 5                          |                               |                  |                |
|              |                              |                             | CAN_STBY_B      | O               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S6          | A               | 7                          |                               |                  |                |
| P0_7         | T1                           | R15                         | GPIO0_7         | IO              | 0                          | P0_7                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D7_A      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART1_RTS_A     | O               | 2                          |                               |                  |                |
|              |                              |                             | PDM_C1_A        | O               | 3                          |                               |                  |                |
|              |                              |                             | I2C2_SDA_A      | IO              | 4                          |                               |                  |                |
|              |                              |                             | UT3_T1_A        | IO              | 5                          |                               |                  |                |
|              |                              |                             | CDC_DE_B        | O               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S7          | A               | 7                          |                               |                  |                |
| P1_0         | R4                           | R14                         | GPIO1_0         | IO              | 0                          | P1_0                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | UART2_RX_A      | I               | 1                          |                               |                  |                |
|              |                              |                             | SPI0_MISO_A     | IO              | 2                          |                               |                  |                |
|              |                              |                             | I2C3_SDA_A      | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT4_T0_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_HSYNC_C   | I               | 5                          |                               |                  |                |
|              |                              |                             | ETH_RXD0_C      | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S8          | A               | 7                          |                               |                  |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7)  | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|------------------|----------------|
| P1_1         | P5                           | M15                         | GPIO1_1         | IO              | 0                          | P1_1                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | UART2_TX_A      | O               | 1                          |                               |                  |                |
|              |                              |                             | SPI0_MOSI_A     | IO              | 2                          |                               |                  |                |
|              |                              |                             | I2C3_SCL_A      | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT4_T1_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_VSYNC_C   | I               | 5                          |                               |                  |                |
|              |                              |                             | ETH_RXD1_C      | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S9          | A               | 7                          |                               |                  |                |
| P1_2         | N6                           | L15                         | GPIO1_2         | IO              | 0                          | P1_2                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | UART3_RX_A      | I               | 1                          |                               |                  |                |
|              |                              |                             | SPI0_SCLK_A     | IO              | 2                          |                               |                  |                |
|              |                              |                             | I3C_SDA_B       | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT5_T0_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_PCLK_C    | I               | 5                          |                               |                  |                |
|              |                              |                             | ETH_RST_C       | O               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S10         | A               | 7                          |                               |                  |                |
| P1_3         | M7                           | K15                         | GPIO1_3         | IO              | 0                          | P1_3                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | UART3_TX_A      | O               | 1                          |                               |                  |                |
|              |                              |                             | SPI0_SS0_A      | IO              | 2                          |                               |                  |                |
|              |                              |                             | I3C_SCL_B       | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT5_T1_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_XVCLK_C   | O               | 5                          |                               |                  |                |
|              |                              |                             | ETH_TXD0_C      | O               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S11         | A               | 7                          |                               |                  |                |
| P1_4         | P1                           | M19                         | GPIO1_4         | IO              | 0                          | P1_4                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SS0_A     | O               | 1                          |                               |                  |                |
|              |                              |                             | UART0_RX_B      | I               | 2                          |                               |                  |                |
|              |                              |                             | SPI0_SS1_A      | O               | 3                          |                               |                  |                |
|              |                              |                             | UT6_T0_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D0_C      | I               | 5                          |                               |                  |                |
|              |                              |                             | ETH_TXD1_C      | O               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S12         | A               | 7                          |                               |                  |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7)  | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|------------------|----------------|
| P1_5         | R2                           | L18                         | GPIO1_5         | IO              | 0                          | P1_5                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SS1_A     | O               | 1                          |                               |                  |                |
|              |                              |                             | UART0_TX_B      | O               | 2                          |                               |                  |                |
|              |                              |                             | SPI0_SS2_A      | O               | 3                          |                               |                  |                |
|              |                              |                             | UT6_T1_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D1_C      | I               | 5                          |                               |                  |                |
|              |                              |                             | ETH_TXEN_C      | O               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S13         | A               | 7                          |                               |                  |                |
| P1_6         | P3                           | L19                         | GPIO1_6         | IO              | 0                          | P1_6                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_RXDS0_B   | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART1_RX_B      | I               | 2                          |                               |                  |                |
|              |                              |                             | I2S0_SDI_A      | I               | 3                          |                               |                  |                |
|              |                              |                             | UT7_T0_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D2_C      | I               | 5                          |                               |                  |                |
|              |                              |                             | ETH_IRQ_C       | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S14         | A               | 7                          |                               |                  |                |
| P1_7         | N4                           | J18                         | GPIO1_7         | IO              | 0                          | P1_7                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SCLK_A    | O               | 1                          |                               |                  |                |
|              |                              |                             | UART1_TX_B      | O               | 2                          |                               |                  |                |
|              |                              |                             | I2S0_SDO_A      | O               | 3                          |                               |                  |                |
|              |                              |                             | UT7_T1_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D3_C      | I               | 5                          |                               |                  |                |
|              |                              |                             | ETH_REFCLK_C    | IO              | 6                          |                               |                  |                |
|              |                              |                             | ANA_S15         | A               | 7                          |                               |                  |                |
| P2_0         | M1                           | K19                         | GPIO2_0         | IO              | 0                          | P2_0                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D0_B      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART2_RX_B      | I               | 2                          |                               |                  |                |
|              |                              |                             | LPPDM_D0_A      | I               | 3                          |                               |                  |                |
|              |                              |                             | UT8_T0_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D4_C      | I               | 5                          |                               |                  |                |
|              |                              |                             | ETH_MDIO_C      | IO              | 6                          |                               |                  |                |
|              |                              |                             | ANA_S16         | A               | 7                          |                               |                  |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7)  | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|------------------|----------------|
| P2_1         | N2                           | K18                         | GPIO2_1         | IO              | 0                          | P2_1                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D1_B      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART2_TX_B      | O               | 2                          |                               |                  |                |
|              |                              |                             | LPPDM_C0_A      | O               | 3                          |                               |                  |                |
|              |                              |                             | UT8_T1_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D5_C      | I               | 5                          |                               |                  |                |
|              |                              |                             | ETH_MDC_C       | O               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S17         | A               | 7                          |                               |                  |                |
| P2_2         | M3                           | J15                         | GPIO2_2         | IO              | 0                          | P2_2                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D2_B      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART3_RX_B      | I               | 2                          |                               |                  |                |
|              |                              |                             | LPPDM_D1_A      | I               | 3                          |                               |                  |                |
|              |                              |                             | UT9_T0_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D6_C      | I               | 5                          |                               |                  |                |
|              |                              |                             | ETH_CRS_DV_C    | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S18         | A               | 7                          |                               |                  |                |
| P2_3         | M5                           | H15                         | GPIO2_3         | IO              | 0                          | P2_3                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D3_B      | IO              | 1                          |                               |                  |                |
|              |                              |                             | UART3_TX_B      | O               | 2                          |                               |                  |                |
|              |                              |                             | LPPDM_C1_A      | O               | 3                          |                               |                  |                |
|              |                              |                             | UT9_T1_A        | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D7_C      | I               | 5                          |                               |                  |                |
|              |                              |                             | CDC_PCLK_B      | O               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S19         | A               | 7                          |                               |                  |                |
| P2_4         | L4                           | G19                         | GPIO2_4         | IO              | 0                          | P2_4                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D4_B      | IO              | 1                          |                               |                  |                |
|              |                              |                             | LPI2S_SDI_A     | I               | 2                          |                               |                  |                |
|              |                              |                             | SPI1_MISO_A     | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT10_T0_A       | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D0_B      | I               | 5                          |                               |                  |                |
|              |                              |                             | CAM_D0_A        | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S20         | A               | 7                          |                               |                  |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7)  | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|------------------|----------------|
| P2_5         | K1                           | H19                         | GPIO2_5         | IO              | 0                          | P2_5                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D5_B      | IO              | 1                          |                               |                  |                |
|              |                              |                             | LPI2S_SDO_A     | O               | 2                          |                               |                  |                |
|              |                              |                             | SPI1_MOSI_A     | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT10_T1_A       | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D1_B      | I               | 5                          |                               |                  |                |
|              |                              |                             | CAM_D1_A        | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S21         | A               | 7                          |                               |                  |                |
| P2_6         | L2                           | H18                         | GPIO2_6         | IO              | 0                          | P2_6                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D6_B      | IO              | 1                          |                               |                  |                |
|              |                              |                             | LPI2S_SCLK_A    | O               | 2                          |                               |                  |                |
|              |                              |                             | SPI1_SCLK_A     | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT11_T0_A       | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D2_B      | I               | 5                          |                               |                  |                |
|              |                              |                             | CAM_D2_A        | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S22         | A               | 7                          |                               |                  |                |
| P2_7         | L6                           | J19                         | GPIO2_7         | IO              | 0                          | P2_7                          | LVCMOS<br>ANALOG | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D7_B      | IO              | 1                          |                               |                  |                |
|              |                              |                             | LPI2S_WS_A      | O               | 2                          |                               |                  |                |
|              |                              |                             | SPI1_SS0_A      | IO              | 3                          |                               |                  |                |
|              |                              |                             | UT11_T1_A       | IO              | 4                          |                               |                  |                |
|              |                              |                             | LPCAM_D3_B      | I               | 5                          |                               |                  |                |
|              |                              |                             | CAM_D3_A        | I               | 6                          |                               |                  |                |
|              |                              |                             | ANA_S23         | A               | 7                          |                               |                  |                |
| P3_0         | J12                          | B6                          | GPIO3_0         | IO              | 0                          | P3_0                          | LVCMOS           | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SCLK_B    | O               | 1                          |                               |                  |                |
|              |                              |                             | UART4_RX_A      | I               | 2                          |                               |                  |                |
|              |                              |                             | PDM_D0_B        | I               | 3                          |                               |                  |                |
|              |                              |                             | I2S0_SCLK_A     | O               | 4                          |                               |                  |                |
|              |                              |                             | QECO_X_A        | I               | 5                          |                               |                  |                |
|              |                              |                             | LPCAM_D4_B      | I               | 6                          |                               |                  |                |
|              |                              |                             | CAM_D4_A        | I               | 7                          |                               |                  |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P3_1         | L12                          | A6                          | GPIO3_1         | IO              | 0                          | P3_1                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SCLKN_B   | O               | 1                          |                               |                 |                |
|              |                              |                             | UART4_TX_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | PDM_C0_B        | O               | 3                          |                               |                 |                |
|              |                              |                             | I2S0_WS_A       | O               | 4                          |                               |                 |                |
|              |                              |                             | QEC0_Y_A        | I               | 5                          |                               |                 |                |
|              |                              |                             | LPCAM_D5_B      | I               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D5_A        | I               | 7                          |                               |                 |                |
| P3_2         | D17                          | E2                          | GPIO3_2         | IO              | 0                          | P3_2                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SS0_B     | O               | 1                          |                               |                 |                |
|              |                              |                             | PDM_D1_B        | I               | 2                          |                               |                 |                |
|              |                              |                             | I2S1_SDI_A      | I               | 3                          |                               |                 |                |
|              |                              |                             | I3C_SDA_C       | IO              | 4                          |                               |                 |                |
|              |                              |                             | QEC0_Z_A        | I               | 5                          |                               |                 |                |
|              |                              |                             | LPCAM_D6_B      | I               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D6_A        | I               | 7                          |                               |                 |                |
| P3_3         | C18                          | G2                          | GPIO3_3         | IO              | 0                          | P3_3                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SS1_B     | O               | 1                          |                               |                 |                |
|              |                              |                             | PDM_C1_B        | O               | 2                          |                               |                 |                |
|              |                              |                             | I2S1_SDO_A      | O               | 3                          |                               |                 |                |
|              |                              |                             | I3C_SCL_C       | IO              | 4                          |                               |                 |                |
|              |                              |                             | QEC1_X_A        | I               | 5                          |                               |                 |                |
|              |                              |                             | LPCAM_D7_B      | I               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D7_A        | I               | 7                          |                               |                 |                |
| P3_4         | E14                          | F2                          | GPIO3_4         | IO              | 0                          | P3_4                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_RXDS0_A   | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART5_RX_A      | I               | 2                          |                               |                 |                |
|              |                              |                             | LPPDM_C0_B      | O               | 3                          |                               |                 |                |
|              |                              |                             | I2S1_SCLK_A     | O               | 4                          |                               |                 |                |
|              |                              |                             | I2C0_SCL_B      | IO              | 5                          |                               |                 |                |
|              |                              |                             | QEC1_Y_A        | I               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D8_A        | I               | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P3_5         | F13                          | F1                          | GPIO3_5         | IO              | 0                          | P3_5                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SCLKN_A   | O               | 1                          |                               |                 |                |
|              |                              |                             | UART5_TX_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | LPPDM_D0_B      | I               | 3                          |                               |                 |                |
|              |                              |                             | SPI0_SS1_B      | O               | 4                          |                               |                 |                |
|              |                              |                             | I2C0_SDA_B      | IO              | 5                          |                               |                 |                |
|              |                              |                             | QEC1_Z_A        | I               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D9_A        | I               | 7                          |                               |                 |                |
| P3_6         | AA16                         | V5                          | GPIO3_6         | IO              | 0                          | P3_6                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | HFXO_OUT_A      | O               | 1                          |                               |                 |                |
|              |                              |                             | LPUART_CTS_B    | I               | 2                          |                               |                 |                |
|              |                              |                             | LPPDM_C1_B      | O               | 3                          |                               |                 |                |
|              |                              |                             | SPI0_SS2_B      | O               | 4                          |                               |                 |                |
|              |                              |                             | I2C1_SDA_B      | IO              | 5                          |                               |                 |                |
|              |                              |                             | QEC2_X_A        | I               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D10_A       | I               | 7                          |                               |                 |                |
| P3_7         | Y15                          | L8                          | GPIO3_7         | IO              | 0                          | P3_7                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | JTAG_TRACECLK   | O               | 1                          |                               |                 |                |
|              |                              |                             | LPUART_RTS_B    | O               | 2                          |                               |                 |                |
|              |                              |                             | LPPDM_D1_B      | I               | 3                          |                               |                 |                |
|              |                              |                             | SPI1_SS1_A      | O               | 4                          |                               |                 |                |
|              |                              |                             | I2C1_SCL_B      | IO              | 5                          |                               |                 |                |
|              |                              |                             | QEC2_Y_A        | I               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D11_A       | I               | 7                          |                               |                 |                |
| P4_0         | F3                           | F18                         | GPIO4_0         | IO              | 0                          | P4_0                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | JTAG_TDATA0     | O               | 1                          |                               |                 |                |
|              |                              |                             | APLL_OUT_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | I2S1_WS_A       | O               | 3                          |                               |                 |                |
|              |                              |                             | SPI1_SS2_A      | O               | 4                          |                               |                 |                |
|              |                              |                             | QEC2_Z_A        | I               | 5                          |                               |                 |                |
|              |                              |                             | CDC_VSYNC_B     | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D12_A       | I               | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3)         | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-------------------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P4_1         | C2                           | B19                         | GPIO4_1                 | IO              | 0                          | P4_1                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | JTAG_TDATA1             | O               | 1                          |                               |                 |                |
|              |                              |                             | I2S0_SDI_B              | I               | 2                          |                               |                 |                |
|              |                              |                             | SPI1_SS3_A              | O               | 3                          |                               |                 |                |
|              |                              |                             | QEC3_X_A                | I               | 4                          |                               |                 |                |
|              |                              |                             | SD_CLK_D                | O               | 5                          |                               |                 |                |
|              |                              |                             | CDC_HSYNC_B             | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D13_A               | I               | 7                          |                               |                 |                |
| P4_2         | D3                           | C19                         | GPIO4_2                 | IO              | 0                          | P4_2                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | JTAG_TDATA2             | O               | 1                          |                               |                 |                |
|              |                              |                             | LPI2C1_SDA_A            | IO              | 2                          |                               |                 |                |
|              |                              |                             | I2S0_SDO_B              | O               | 3                          |                               |                 |                |
|              |                              |                             | SPI2_MISO_A             | IO              | 4                          |                               |                 |                |
|              |                              |                             | QEC3_Y_A                | I               | 5                          |                               |                 |                |
|              |                              |                             | SD_CMD_D                | IO              | 6                          |                               |                 |                |
|              |                              |                             | CAM_D14_A               | I               | 7                          |                               |                 |                |
| P4_3         | A2                           | B18                         | GPIO4_3                 | IO              | 0                          | P4_3                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | JTAG_TDATA3             | O               | 1                          |                               |                 |                |
|              |                              |                             | LPI2C1_SCL_A            | IO              | 2                          |                               |                 |                |
|              |                              |                             | I2S0_SCLK_B             | O               | 3                          |                               |                 |                |
|              |                              |                             | SPI2_MOSI_A             | IO              | 4                          |                               |                 |                |
|              |                              |                             | QEC3_Z_A                | I               | 5                          |                               |                 |                |
|              |                              |                             | SD_RST_D                | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D15_A               | I               | 7                          |                               |                 |                |
| P4_4         | G6                           | B17                         | GPIO4_4                 | IO              | 0                          | P4_4                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | JTAG_TCK <sup>(a)</sup> | I               | 1                          |                               |                 |                |
|              |                              |                             | I2S0_WS_B               | O               | 2                          |                               |                 |                |
|              |                              |                             | SPI2_SCLK_A             | IO              | 3                          |                               |                 |                |
|              |                              |                             | FAULT0_A                | I               | 4                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3)         | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-------------------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P4_5         | K7                           | A19                         | GPIO4_5                 | IO              | 0                          | P4_5                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | JTAG_TMS <sup>(a)</sup> | I               | 1                          |                               |                 |                |
|              |                              |                             | SPI2_SS0_A              | IO              | 2                          |                               |                 |                |
|              |                              |                             | FAULT1_A                | I               | 3                          |                               |                 |                |
| P4_6         | H7                           | A18                         | GPIO4_6                 | IO              | 0                          | P4_6                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | JTAG_TDI <sup>(a)</sup> | I               | 1                          |                               |                 |                |
|              |                              |                             | SPI2_SS1_A              | O               | 2                          |                               |                 |                |
|              |                              |                             | FAULT2_A                | I               | 3                          |                               |                 |                |
| P4_7         | B3                           | B16                         | GPIO4_7                 | IO              | 0                          | P4_7                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | JTAG_TDO <sup>(a)</sup> | O               | 1                          |                               |                 |                |
|              |                              |                             | SPI2_SS2_A              | O               | 2                          |                               |                 |                |
|              |                              |                             | FAULT3_A                | I               | 3                          |                               |                 |                |
| P5_0         | C4                           | A16                         | GPIO5_0                 | IO              | 0                          | P5_0                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_RXDS0_A           | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART4_RX_C              | I               | 2                          |                               |                 |                |
|              |                              |                             | PDM_D2_A                | I               | 3                          |                               |                 |                |
|              |                              |                             | SPI0_MISO_B             | IO              | 4                          |                               |                 |                |
|              |                              |                             | I2C2_SDA_B              | IO              | 5                          |                               |                 |                |
|              |                              |                             | UT0_T0_B                | IO              | 6                          |                               |                 |                |
|              |                              |                             | SD_D0_A                 | IO              | 7                          |                               |                 |                |
| P5_1         | G8                           | B14                         | GPIO5_1                 | IO              | 0                          | P5_1                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_SS0_A             | O               | 1                          |                               |                 |                |
|              |                              |                             | UART4_TX_C              | O               | 2                          |                               |                 |                |
|              |                              |                             | PDM_D3_A                | I               | 3                          |                               |                 |                |
|              |                              |                             | SPI0_MOSI_B             | IO              | 4                          |                               |                 |                |
|              |                              |                             | I2C2_SCL_B              | IO              | 5                          |                               |                 |                |
|              |                              |                             | UT0_T1_B                | IO              | 6                          |                               |                 |                |
|              |                              |                             | SD_D1_A                 | IO              | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P5_2         | B5                           | E12                         | GPIO5_2         | IO              | 0                          | P5_2                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_SCLKN_A   | O               | 1                          |                               |                 |                |
|              |                              |                             | UART5_RX_C      | I               | 2                          |                               |                 |                |
|              |                              |                             | PDM_C3_A        | O               | 3                          |                               |                 |                |
|              |                              |                             | SPI0_SS0_B      | IO              | 4                          |                               |                 |                |
|              |                              |                             | LPI2C0_SCL_B    | I               | 5                          |                               |                 |                |
|              |                              |                             | UT1_T0_B        | IO              | 6                          |                               |                 |                |
|              |                              |                             | SD_D2_A         | IO              | 7                          |                               |                 |                |
| P5_3         | F7                           | B13                         | GPIO5_3         | IO              | 0                          | P5_3                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_SCLK_A    | O               | 1                          |                               |                 |                |
|              |                              |                             | UART5_TX_C      | O               | 2                          |                               |                 |                |
|              |                              |                             | SPI0_SCLK_B     | IO              | 3                          |                               |                 |                |
|              |                              |                             | LPI2C0_SDA_B    | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT1_T1_B        | IO              | 5                          |                               |                 |                |
|              |                              |                             | SD_D3_A         | IO              | 6                          |                               |                 |                |
|              |                              |                             | CDC_PCLK_A      | O               | 7                          |                               |                 |                |
| P5_4         | C6                           | E11                         | GPIO5_4         | IO              | 0                          | P5_4                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_SS1_A     | O               | 1                          |                               |                 |                |
|              |                              |                             | UART3_CTS_A     | I               | 2                          |                               |                 |                |
|              |                              |                             | PDM_D2_B        | I               | 3                          |                               |                 |                |
|              |                              |                             | SPI0_SS3_A      | O               | 4                          |                               |                 |                |
|              |                              |                             | UT2_T0_B        | IO              | 5                          |                               |                 |                |
|              |                              |                             | SD_D4_A         | IO              | 6                          |                               |                 |                |
|              |                              |                             | CDC_DE_A        | O               | 7                          |                               |                 |                |
| P5_5         | A6                           | E10                         | GPIO5_5         | IO              | 0                          | P5_5                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_SCLK_C    | O               | 1                          |                               |                 |                |
|              |                              |                             | UART3_RTS_A     | O               | 2                          |                               |                 |                |
|              |                              |                             | PDM_D3_B        | I               | 3                          |                               |                 |                |
|              |                              |                             | UT2_T1_B        | IO              | 4                          |                               |                 |                |
|              |                              |                             | SD_D5_A         | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_RXD0_A      | I               | 6                          |                               |                 |                |
|              |                              |                             | CDC_HSYNC_A     | O               | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P5_6         | D7                           | B12                         | GPIO5_6         | IO              | 0                          | P5_6                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | UART1_CTS_B     | I               | 1                          |                               |                 |                |
|              |                              |                             | I2C2_SCL_C      | IO              | 2                          |                               |                 |                |
|              |                              |                             | UT3_T0_B        | IO              | 3                          |                               |                 |                |
|              |                              |                             | SD_D6_A         | IO              | 4                          |                               |                 |                |
|              |                              |                             | ETH_RXD1_A      | I               | 5                          |                               |                 |                |
|              |                              |                             | CDC_VSYNC_A     | O               | 6                          |                               |                 |                |
| P5_7         | B7                           | B11                         | GPIO5_7         | IO              | 0                          | P5_7                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_SS0_C     | O               | 1                          |                               |                 |                |
|              |                              |                             | UART1_RTS_B     | O               | 2                          |                               |                 |                |
|              |                              |                             | I2C2_SDA_C      | IO              | 3                          |                               |                 |                |
|              |                              |                             | UT3_T1_B        | IO              | 4                          |                               |                 |                |
|              |                              |                             | SD_D7_A         | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_RST_A       | O               | 6                          |                               |                 |                |
| P6_0         | E8                           | A12                         | GPIO6_0         | IO              | 0                          | P6_0                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D0_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART4_DE_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | PDM_D0_C        | I               | 3                          |                               |                 |                |
|              |                              |                             | UT4_T0_B        | IO              | 4                          |                               |                 |                |
|              |                              |                             | SD_D0_D         | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_TXD0_A      | O               | 6                          |                               |                 |                |
|              |                              |                             | LPSP1_SS1_A     | IO              | 7                          |                               |                 |                |
| P6_1         | H9                           | E9                          | GPIO6_1         | IO              | 0                          | P6_1                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D1_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART5_DE_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | PDM_C0_C        | O               | 3                          |                               |                 |                |
|              |                              |                             | UT4_T1_B        | IO              | 4                          |                               |                 |                |
|              |                              |                             | SD_D1_D         | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_TXD1_A      | O               | 6                          |                               |                 |                |
|              |                              |                             | LPSP1_SS2_A     | IO              | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P6_2         | C8                           | A11                         | GPIO6_2         | IO              | 0                          | P6_2                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D2_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART2_CTS_A     | I               | 2                          |                               |                 |                |
|              |                              |                             | LPI3C_SDA_A     | IO              | 3                          |                               |                 |                |
|              |                              |                             | PDM_D1_C        | I               | 4                          |                               |                 |                |
|              |                              |                             | UT5_T0_B        | IO              | 5                          |                               |                 |                |
|              |                              |                             | SD_D2_D         | IO              | 6                          |                               |                 |                |
|              |                              |                             | ETH_TXEN_A      | O               | 7                          |                               |                 |                |
| P6_3         | F9                           | B10                         | GPIO6_3         | IO              | 0                          | P6_3                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D3_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART2_RTS_A     | O               | 2                          |                               |                 |                |
|              |                              |                             | LPI3C_SCL_A     | IO              | 3                          |                               |                 |                |
|              |                              |                             | PDM_C1_C        | O               | 4                          |                               |                 |                |
|              |                              |                             | UT5_T1_B        | IO              | 5                          |                               |                 |                |
|              |                              |                             | SD_D3_D         | IO              | 6                          |                               |                 |                |
|              |                              |                             | ETH_IRQ_A       | I               | 7                          |                               |                 |                |
| P6_4         | G10                          | E8                          | GPIO6_4         | IO              | 0                          | P6_4                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D4_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART2_CTS_B     | I               | 2                          |                               |                 |                |
|              |                              |                             | LFRC_OUT_A      | O               | 3                          |                               |                 |                |
|              |                              |                             | SPI1_SS0_B      | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT6_T0_B        | IO              | 5                          |                               |                 |                |
|              |                              |                             | SD_D4_D         | IO              | 6                          |                               |                 |                |
|              |                              |                             | ETH_REFCLK_A    | IO              | 7                          |                               |                 |                |
| P6_5         | E10                          | E7                          | GPIO6_5         | IO              | 0                          | P6_5                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D5_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART2_RTS_B     | O               | 2                          |                               |                 |                |
|              |                              |                             | LPI2C1_SDA_B    | IO              | 3                          |                               |                 |                |
|              |                              |                             | SPI1_SS1_B      | O               | 4                          |                               |                 |                |
|              |                              |                             | UT6_T1_B        | IO              | 5                          |                               |                 |                |
|              |                              |                             | SD_D5_D         | IO              | 6                          |                               |                 |                |
|              |                              |                             | ETH_MDIO_A      | IO              | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P6_6         | C10                          | E6                          | GPIO6_6         | IO              | 0                          | P6_6                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D6_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART0_CTS_B     | I               | 2                          |                               |                 |                |
|              |                              |                             | LPI2C1_SCL_B    | IO              | 3                          |                               |                 |                |
|              |                              |                             | SPI1_SS2_B      | O               | 4                          |                               |                 |                |
|              |                              |                             | UT7_T0_B        | IO              | 5                          |                               |                 |                |
|              |                              |                             | SD_D6_D         | IO              | 6                          |                               |                 |                |
|              |                              |                             | ETH_MDC_A       | O               | 7                          |                               |                 |                |
| P6_7         | D11                          | A9                          | GPIO6_7         | IO              | 0                          | P6_7                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D7_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART0_RTS_B     | O               | 2                          |                               |                 |                |
|              |                              |                             | PDM_C2_A        | O               | 3                          |                               |                 |                |
|              |                              |                             | SPI1_SS3_B      | O               | 4                          |                               |                 |                |
|              |                              |                             | UT7_T1_B        | IO              | 5                          |                               |                 |                |
|              |                              |                             | SD_D7_D         | IO              | 6                          |                               |                 |                |
|              |                              |                             | ETH_CRS_DV_A    | I               | 7                          |                               |                 |                |
| P7_0         | A12                          | B8                          | GPIO7_0         | IO              | 0                          | P7_0                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | LPUT0_T0_A      | IO              | 1                          |                               |                 |                |
|              |                              |                             | CMP3_OUT_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | SPI0_MISO_C     | IO              | 3                          |                               |                 |                |
|              |                              |                             | I2C0_SDA_C      | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT8_T0_B        | IO              | 5                          |                               |                 |                |
|              |                              |                             | SD_CMD_A        | IO              | 6                          |                               |                 |                |
|              |                              |                             | CAN_RXD_A       | I               | 7                          |                               |                 |                |
| P7_1         | C12                          | B3                          | GPIO7_1         | IO              | 0                          | P7_1                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | LPUT0_T1_A      | IO              | 1                          |                               |                 |                |
|              |                              |                             | CMP2_OUT_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | SPI0_MOSI_C     | IO              | 3                          |                               |                 |                |
|              |                              |                             | I2C0_SCL_C      | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT8_T1_B        | IO              | 5                          |                               |                 |                |
|              |                              |                             | SD_CLK_A        | O               | 6                          |                               |                 |                |
|              |                              |                             | CAN_TXD_A       | O               | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7)        | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|------------------------|----------------|
| P7_2         | K11                          | D1                          | GPIO7_2         | IO              | 0                          | P7_2                          | LVCMOS                 | VDD_IO_1V8     |
|              |                              |                             | LPUT1_T0_A      | IO              | 1                          |                               |                        |                |
|              |                              |                             | UART3_CTS_B     | I               | 2                          |                               |                        |                |
|              |                              |                             | CMP1_OUT_A      | O               | 3                          |                               |                        |                |
|              |                              |                             | SPI0_SCLK_C     | IO              | 4                          |                               |                        |                |
|              |                              |                             | I2C1_SDA_C      | IO              | 5                          |                               |                        |                |
|              |                              |                             | UT9_T0_B        | IO              | 6                          |                               |                        |                |
|              |                              |                             | SD_RST_A        | O               | 7                          |                               |                        |                |
| P7_3         | E12                          | A8                          | GPIO7_3         | IO              | 0                          | P7_3                          | LVCMOS                 | VDD_IO_1V8     |
|              |                              |                             | LPUT1_T1_A      | IO              | 1                          |                               |                        |                |
|              |                              |                             | UART3_RTS_B     | O               | 2                          |                               |                        |                |
|              |                              |                             | CMP0_OUT_A      | O               | 3                          |                               |                        |                |
|              |                              |                             | SPI0_SS0_C      | IO              | 4                          |                               |                        |                |
|              |                              |                             | I2C1_SCL_C      | IO              | 5                          |                               |                        |                |
|              |                              |                             | UT9_T1_B        | IO              | 6                          |                               |                        |                |
|              |                              |                             | CAN_STBY_A      | O               | 7                          |                               |                        |                |
| P7_4         | U16                          | T1                          | GPIO7_4         | IO              | 0                          | P7_4                          | Dual Voltage<br>LVCMOS | VDD_IO_FLEX    |
|              |                              |                             | LPUT2_T0_A      | IO              | 1                          |                               |                        |                |
|              |                              |                             | LPUART_CTS_A    | I               | 2                          |                               |                        |                |
|              |                              |                             | LPPDM_C2_A      | O               | 3                          |                               |                        |                |
|              |                              |                             | LPSPI_MISO_A    | IO              | 4                          |                               |                        |                |
|              |                              |                             | LPI2C0_SCL_A    | I               | 5                          |                               |                        |                |
|              |                              |                             | UT10_T0_B       | IO              | 6                          |                               |                        |                |
| P7_5         | U14                          | T2                          | GPIO7_5         | IO              | 0                          | P7_5                          | Dual Voltage<br>LVCMOS | VDD_IO_FLEX    |
|              |                              |                             | LPUT2_T1_A      | IO              | 1                          |                               |                        |                |
|              |                              |                             | LPUART_RTS_A    | O               | 2                          |                               |                        |                |
|              |                              |                             | LFXO_OUT_A      | O               | 3                          |                               |                        |                |
|              |                              |                             | LPPDM_D2_A      | I               | 4                          |                               |                        |                |
|              |                              |                             | LPSPI_MOSI_A    | IO              | 5                          |                               |                        |                |
|              |                              |                             | LPI2C0_SDA_A    | IO              | 6                          |                               |                        |                |
|              |                              |                             | UT10_T1_B       | IO              | 7                          |                               |                        |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7)        | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|------------------------|----------------|
| P7_6         | V17                          | U3                          | GPIO7_6         | IO              | 0                          | P7_6                          | Dual Voltage<br>LVCMOS | VDD_IO_FLEX    |
|              |                              |                             | LPI2C1_SDA_C    | IO              | 1                          |                               |                        |                |
|              |                              |                             | LPUART_RX_A     | I               | 2                          |                               |                        |                |
|              |                              |                             | LPI3C_SDA_B     | IO              | 3                          |                               |                        |                |
|              |                              |                             | LPPDM_C3_A      | O               | 4                          |                               |                        |                |
|              |                              |                             | LPSPI_SCLK_A    | IO              | 5                          |                               |                        |                |
|              |                              |                             | I3C_SDA_D       | IO              | 6                          |                               |                        |                |
|              |                              |                             | UT11_T0_B       | IO              | 7                          |                               |                        |                |
| P7_7         | W18                          | U1                          | GPIO7_7         | IO              | 0                          | P7_7                          | Dual Voltage<br>LVCMOS | VDD_IO_FLEX    |
|              |                              |                             | LPI2C1_SCL_C    | IO              | 1                          |                               |                        |                |
|              |                              |                             | LPUART_TX_A     | O               | 2                          |                               |                        |                |
|              |                              |                             | LPI3C_SCL_B     | IO              | 3                          |                               |                        |                |
|              |                              |                             | LPPDM_D3_A      | I               | 4                          |                               |                        |                |
|              |                              |                             | LPSPI_SS0_A     | IO              | 5                          |                               |                        |                |
|              |                              |                             | I3C_SCL_D       | IO              | 6                          |                               |                        |                |
|              |                              |                             | UT11_T1_B       | IO              | 7                          |                               |                        |                |
| P8_0         | B13                          | B7                          | GPIO8_0         | IO              | 0                          | P8_0                          | LVCMOS                 | VDD_IO_1V8     |
|              |                              |                             | OSPI1_SCLKN_C   | O               | 1                          |                               |                        |                |
|              |                              |                             | AUDIO_CLK_A     | I               | 2                          |                               |                        |                |
|              |                              |                             | FAULT0_B        | I               | 3                          |                               |                        |                |
|              |                              |                             | LPCAM_D0_A      | I               | 4                          |                               |                        |                |
|              |                              |                             | SD_D0_C         | IO              | 5                          |                               |                        |                |
|              |                              |                             | CDC_D0_A        | O               | 6                          |                               |                        |                |
|              |                              |                             | CAM_D0_B        | I               | 7                          |                               |                        |                |
| P8_1         | D13                          | C2                          | GPIO8_1         | IO              | 0                          | P8_1                          | LVCMOS                 | VDD_IO_1V8     |
|              |                              |                             | I2S2_SDI_A      | I               | 1                          |                               |                        |                |
|              |                              |                             | FAULT1_B        | I               | 2                          |                               |                        |                |
|              |                              |                             | LPCAM_D1_A      | I               | 3                          |                               |                        |                |
|              |                              |                             | SD_D1_C         | IO              | 4                          |                               |                        |                |
|              |                              |                             | CDC_D1_A        | O               | 5                          |                               |                        |                |
|              |                              |                             | CAM_D1_B        | I               | 6                          |                               |                        |                |
|              |                              |                             | OSPI1_SS1_C     | O               | 7                          |                               |                        |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P8_2         | A14                          | C3                          | GPIO8_2         | IO              | 0                          | P8_2                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | I2S2_SDO_A      | O               | 1                          |                               |                 |                |
|              |                              |                             | SPI0_SS3_B      | O               | 2                          |                               |                 |                |
|              |                              |                             | FAULT2_B        | I               | 3                          |                               |                 |                |
|              |                              |                             | LPCAM_D2_A      | I               | 4                          |                               |                 |                |
|              |                              |                             | SD_D2_C         | IO              | 5                          |                               |                 |                |
|              |                              |                             | CDC_D2_A        | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D2_B        | I               | 7                          |                               |                 |                |
| P8_3         | C14                          | A7                          | GPIO8_3         | IO              | 0                          | P8_3                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | I2S2_SCLK_A     | O               | 1                          |                               |                 |                |
|              |                              |                             | SPI1_MISO_B     | IO              | 2                          |                               |                 |                |
|              |                              |                             | FAULT3_B        | I               | 3                          |                               |                 |                |
|              |                              |                             | LPCAM_D3_A      | I               | 4                          |                               |                 |                |
|              |                              |                             | SD_D3_C         | IO              | 5                          |                               |                 |                |
|              |                              |                             | CDC_D3_A        | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D3_B        | I               | 7                          |                               |                 |                |
| P8_4         | G12                          | B4                          | GPIO8_4         | IO              | 0                          | P8_4                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | I2S2_WS_A       | O               | 1                          |                               |                 |                |
|              |                              |                             | SPI1_MOSI_B     | IO              | 2                          |                               |                 |                |
|              |                              |                             | QEC0_X_B        | I               | 3                          |                               |                 |                |
|              |                              |                             | LPCAM_D4_A      | I               | 4                          |                               |                 |                |
|              |                              |                             | SD_D4_C         | IO              | 5                          |                               |                 |                |
|              |                              |                             | CDC_D4_A        | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D4_B        | I               | 7                          |                               |                 |                |
| P8_5         | G16                          | H1                          | GPIO8_5         | IO              | 0                          | P8_5                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_RXDS1_A   | IO              | 1                          |                               |                 |                |
|              |                              |                             | SPI1_SCLK_B     | IO              | 2                          |                               |                 |                |
|              |                              |                             | QEC0_Y_B        | I               | 3                          |                               |                 |                |
|              |                              |                             | LPCAM_D5_A      | I               | 4                          |                               |                 |                |
|              |                              |                             | SD_D5_C         | IO              | 5                          |                               |                 |                |
|              |                              |                             | CDC_D5_A        | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D5_B        | I               | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P8_6         | H13                          | J2                          | GPIO8_6         | IO              | 0                          | P8_6                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_RXDS1_B   | IO              | 1                          |                               |                 |                |
|              |                              |                             | I2S3_SCLK_B     | O               | 2                          |                               |                 |                |
|              |                              |                             | QEC0_Z_B        | I               | 3                          |                               |                 |                |
|              |                              |                             | LPCAM_D6_A      | I               | 4                          |                               |                 |                |
|              |                              |                             | SD_D6_C         | IO              | 5                          |                               |                 |                |
|              |                              |                             | CDC_D6_A        | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D6_B        | I               | 7                          |                               |                 |                |
| P8_7         | G18                          | J1                          | GPIO8_7         | IO              | 0                          | P8_7                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_RXDS1_C   | IO              | 1                          |                               |                 |                |
|              |                              |                             | I2S3_WS_B       | O               | 2                          |                               |                 |                |
|              |                              |                             | QEC1_X_B        | I               | 3                          |                               |                 |                |
|              |                              |                             | LPCAM_D7_A      | I               | 4                          |                               |                 |                |
|              |                              |                             | SD_D7_C         | IO              | 5                          |                               |                 |                |
|              |                              |                             | CDC_D7_A        | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D7_B        | I               | 7                          |                               |                 |                |
| P9_0         | H15                          | K2                          | GPIO9_0         | IO              | 0                          | P9_0                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_RXDS1_C   | IO              | 1                          |                               |                 |                |
|              |                              |                             | I2S3_SDI_B      | I               | 2                          |                               |                 |                |
|              |                              |                             | QEC1_Y_B        | I               | 3                          |                               |                 |                |
|              |                              |                             | SD_CMD_C        | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D8_A        | O               | 5                          |                               |                 |                |
|              |                              |                             | CAM_D8_B        | I               | 6                          |                               |                 |                |
|              |                              |                             | LPSPi_SS3_A     | IO              | 7                          |                               |                 |                |
| P9_1         | H17                          | K1                          | GPIO9_1         | IO              | 0                          | P9_1                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | LPUART_RX_B     | I               | 1                          |                               |                 |                |
|              |                              |                             | I2S3_SDO_B      | O               | 2                          |                               |                 |                |
|              |                              |                             | QEC1_Z_B        | I               | 3                          |                               |                 |                |
|              |                              |                             | SD_CLK_C        | O               | 4                          |                               |                 |                |
|              |                              |                             | CDC_D9_A        | O               | 5                          |                               |                 |                |
|              |                              |                             | CAM_D9_B        | I               | 6                          |                               |                 |                |
|              |                              |                             | LPSPi_SS4_A     | IO              | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P9_2         | J14                          | G5                          | GPIO9_2         | IO              | 0                          | P9_2                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | LPUART_TX_B     | O               | 1                          |                               |                 |                |
|              |                              |                             | I2S3_SDI_A      | I               | 2                          |                               |                 |                |
|              |                              |                             | SPI2_MISO_B     | IO              | 3                          |                               |                 |                |
|              |                              |                             | QEC2_X_B        | I               | 4                          |                               |                 |                |
|              |                              |                             | SD_RST_C        | O               | 5                          |                               |                 |                |
|              |                              |                             | CDC_D10_A       | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D10_B       | I               | 7                          |                               |                 |                |
| P9_3         | K13                          | H5                          | GPIO9_3         | IO              | 0                          | P9_3                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | HFXO_OUT_B      | O               | 1                          |                               |                 |                |
|              |                              |                             | UART7_RX_B      | I               | 2                          |                               |                 |                |
|              |                              |                             | I2S3_SDO_A      | O               | 3                          |                               |                 |                |
|              |                              |                             | SPI2_MOSI_B     | IO              | 4                          |                               |                 |                |
|              |                              |                             | QEC2_Y_B        | I               | 5                          |                               |                 |                |
|              |                              |                             | CDC_D11_A       | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D11_B       | I               | 7                          |                               |                 |                |
| P9_4         | J18                          | J5                          | GPIO9_4         | IO              | 0                          | P9_4                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | UART7_TX_B      | O               | 1                          |                               |                 |                |
|              |                              |                             | I2S3_SCLK_A     | O               | 2                          |                               |                 |                |
|              |                              |                             | SPI2_SCLK_B     | IO              | 3                          |                               |                 |                |
|              |                              |                             | I2C3_SDA_C      | IO              | 4                          |                               |                 |                |
|              |                              |                             | QEC2_Z_B        | I               | 5                          |                               |                 |                |
|              |                              |                             | CDC_D12_A       | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D12_B       | I               | 7                          |                               |                 |                |
| P9_5         | J16                          | L1                          | GPIO9_5         | IO              | 0                          | P9_5                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D0_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | I2S3_WS_A       | O               | 2                          |                               |                 |                |
|              |                              |                             | SPI2_SS0_B      | IO              | 3                          |                               |                 |                |
|              |                              |                             | I2C3_SCL_C      | IO              | 4                          |                               |                 |                |
|              |                              |                             | QEC3_X_B        | I               | 5                          |                               |                 |                |
|              |                              |                             | CDC_D13_A       | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D13_B       | I               | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P9_6         | K17                          | K5                          | GPIO9_6         | IO              | 0                          | P9_6                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D1_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | AUDIO_CLK_B     | I               | 2                          |                               |                 |                |
|              |                              |                             | SPI2_SS1_B      | O               | 3                          |                               |                 |                |
|              |                              |                             | I2C3_SDA_B      | IO              | 4                          |                               |                 |                |
|              |                              |                             | QEC3_Y_B        | I               | 5                          |                               |                 |                |
|              |                              |                             | CDC_D14_A       | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D14_B       | I               | 7                          |                               |                 |                |
| P9_7         | L16                          | L5                          | GPIO9_7         | IO              | 0                          | P9_7                          | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D2_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART7_DE_B      | O               | 2                          |                               |                 |                |
|              |                              |                             | SPI2_SS2_B      | O               | 3                          |                               |                 |                |
|              |                              |                             | I2C3_SCL_B      | IO              | 4                          |                               |                 |                |
|              |                              |                             | QEC3_Z_B        | I               | 5                          |                               |                 |                |
|              |                              |                             | CDC_D15_A       | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_D15_B       | I               | 7                          |                               |                 |                |
| P10_0        | M13                          | M2                          | GPIO10_0        | IO              | 0                          | P10_0                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D3_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART6_DE_B      | O               | 2                          |                               |                 |                |
|              |                              |                             | SPI2_SS3_B      | O               | 3                          |                               |                 |                |
|              |                              |                             | UT0_T0_C        | IO              | 4                          |                               |                 |                |
|              |                              |                             | LPCAM_HSYNC_A   | I               | 5                          |                               |                 |                |
|              |                              |                             | CDC_D16_A       | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_HSYNC_B     | I               | 7                          |                               |                 |                |
| P10_1        | M15                          | M1                          | GPIO10_1        | IO              | 0                          | P10_1                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D4_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | LPI2S_SDI_B     | I               | 3                          |                               |                 |                |
|              |                              |                             | UT0_T1_C        | IO              | 4                          |                               |                 |                |
|              |                              |                             | LPCAM_VSYNC_A   | I               | 5                          |                               |                 |                |
|              |                              |                             | CDC_D17_A       | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_VSYNC_B     | I               | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P10_2        | N18                          | N1                          | GPIO10_2        | IO              | 0                          | P10_2                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D5_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | LPI2S_SDO_B     | O               | 3                          |                               |                 |                |
|              |                              |                             | UT1_T0_C        | IO              | 4                          |                               |                 |                |
|              |                              |                             | LPCAM_PCLK_A    | I               | 5                          |                               |                 |                |
|              |                              |                             | CDC_D18_A       | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_PCLK_B      | I               | 7                          |                               |                 |                |
| P10_3        | P15                          | N2                          | GPIO10_3        | IO              | 0                          | P10_3                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D6_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | LPI2S_SCLK_B    | O               | 3                          |                               |                 |                |
|              |                              |                             | UT1_T1_C        | IO              | 4                          |                               |                 |                |
|              |                              |                             | LPCAM_XVCLK_A   | O               | 5                          |                               |                 |                |
|              |                              |                             | CDC_D19_A       | O               | 6                          |                               |                 |                |
|              |                              |                             | CAM_XVCLK_B     | O               | 7                          |                               |                 |                |
| P10_4        | R16                          | M5                          | GPIO10_4        | IO              | 0                          | P10_4                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D7_C      | IO              | 1                          |                               |                 |                |
|              |                              |                             | LPI2S_WS_B      | O               | 3                          |                               |                 |                |
|              |                              |                             | I2C0_SDA_D      | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT2_T0_C        | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_TXD0_B      | O               | 6                          |                               |                 |                |
|              |                              |                             | CDC_D20_A       | O               | 7                          |                               |                 |                |
| P10_5        | R14                          | N5                          | GPIO10_5        | IO              | 0                          | P10_5                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | UART6_RX_A      | I               | 1                          |                               |                 |                |
|              |                              |                             | I2S2_SDI_B      | I               | 2                          |                               |                 |                |
|              |                              |                             | SPI3_MISO_B     | IO              | 3                          |                               |                 |                |
|              |                              |                             | I2C0_SCL_D      | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT2_T1_C        | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_TXD1_B      | O               | 6                          |                               |                 |                |
|              |                              |                             | CDC_D21_A       | O               | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P10_6        | T15                          | P5                          | GPIO10_6        | IO              | 0                          | P10_6                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | UART6_TX_A      | O               | 1                          |                               |                 |                |
|              |                              |                             | I2S2_SDO_B      | O               | 2                          |                               |                 |                |
|              |                              |                             | SPI3_MOSI_B     | IO              | 3                          |                               |                 |                |
|              |                              |                             | I2C1_SDA_D      | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT3_T0_C        | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_TXEN_B      | O               | 6                          |                               |                 |                |
|              |                              |                             | CDC_D22_A       | O               | 7                          |                               |                 |                |
| P10_7        | T17                          | P1                          | GPIO10_7        | IO              | 0                          | P10_7                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | UART7_RX_A      | I               | 1                          |                               |                 |                |
|              |                              |                             | I2S2_SCLK_B     | O               | 2                          |                               |                 |                |
|              |                              |                             | SPI3_SCLK_B     | IO              | 3                          |                               |                 |                |
|              |                              |                             | I2C1_SCL_D      | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT3_T1_C        | IO              | 5                          |                               |                 |                |
|              |                              |                             | CDC_D23_A       | O               | 6                          |                               |                 |                |
|              |                              |                             | OSPI1_RXDS0_C   | IO              | 7                          |                               |                 |                |
| P11_0        | P13                          | P2                          | GPIO11_0        | IO              | 0                          | P11_0                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D0_A      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART7_TX_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | I2S2_WS_B       | O               | 3                          |                               |                 |                |
|              |                              |                             | SPI3_SS0_B      | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT4_T0_C        | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_REFCLK_B    | IO              | 6                          |                               |                 |                |
|              |                              |                             | CDC_D0_B        | O               | 7                          |                               |                 |                |
| P11_1        | U18                          | R1                          | GPIO11_1        | IO              | 0                          | P11_1                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D1_A      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART7_DE_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | SPI3_SS1_B      | O               | 3                          |                               |                 |                |
|              |                              |                             | UT4_T1_C        | IO              | 4                          |                               |                 |                |
|              |                              |                             | ETH_MDIO_B      | IO              | 5                          |                               |                 |                |
|              |                              |                             | CDC_D1_B        | O               | 6                          |                               |                 |                |
|              |                              |                             | LPSP1_SS5_A     | IO              | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P11_2        | N12                          | R2                          | GPIO11_2        | IO              | 0                          | P11_2                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D2_A      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART6_DE_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | LPPDM_C2_B      | O               | 3                          |                               |                 |                |
|              |                              |                             | SPI3_SS2_B      | O               | 4                          |                               |                 |                |
|              |                              |                             | UT5_T0_C        | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_MDC_B       | O               | 6                          |                               |                 |                |
|              |                              |                             | CDC_D2_B        | O               | 7                          |                               |                 |                |
| P11_3        | M11                          | R5                          | GPIO11_3        | IO              | 0                          | P11_3                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D3_A      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART5_RX_B      | I               | 2                          |                               |                 |                |
|              |                              |                             | LPPDM_C3_B      | O               | 3                          |                               |                 |                |
|              |                              |                             | SPI3_SS3_B      | O               | 4                          |                               |                 |                |
|              |                              |                             | UT5_T1_C        | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_RXD0_B      | I               | 6                          |                               |                 |                |
|              |                              |                             | CDC_D3_B        | O               | 7                          |                               |                 |                |
| P11_4        | Y13                          | K8                          | GPIO11_4        | IO              | 0                          | P11_4                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D4_A      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART5_TX_B      | O               | 2                          |                               |                 |                |
|              |                              |                             | PDM_C2_B        | O               | 3                          |                               |                 |                |
|              |                              |                             | LPSPi_MISO_B    | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT6_T0_C        | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_RXD1_B      | I               | 6                          |                               |                 |                |
|              |                              |                             | CDC_D4_B        | O               | 7                          |                               |                 |                |
| P11_5        | AD17                         | J9                          | GPIO11_5        | IO              | 0                          | P11_5                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D5_A      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART6_RX_B      | I               | 2                          |                               |                 |                |
|              |                              |                             | PDM_C3_B        | O               | 3                          |                               |                 |                |
|              |                              |                             | LPSPi_MOSI_B    | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT6_T1_C        | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_CRS_DV_B    | I               | 6                          |                               |                 |                |
|              |                              |                             | CDC_D5_B        | O               | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P11_6        | AA14                         | R6                          | GPIO11_6        | IO              | 0                          | P11_6                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D6_A      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART6_TX_B      | O               | 2                          |                               |                 |                |
|              |                              |                             | LPPDM_D2_B      | I               | 3                          |                               |                 |                |
|              |                              |                             | LPSPi_SCLK_B    | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT7_T0_C        | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_RST_B       | O               | 6                          |                               |                 |                |
|              |                              |                             | CDC_D6_B        | O               | 7                          |                               |                 |                |
| P11_7        | AC16                         | L9                          | GPIO11_7        | IO              | 0                          | P11_7                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D7_A      | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART5_DE_B      | O               | 2                          |                               |                 |                |
|              |                              |                             | LPPDM_D3_B      | I               | 3                          |                               |                 |                |
|              |                              |                             | LPSPi_SS0_B     | IO              | 4                          |                               |                 |                |
|              |                              |                             | UT7_T1_C        | IO              | 5                          |                               |                 |                |
|              |                              |                             | ETH_IRQ_B       | I               | 6                          |                               |                 |                |
|              |                              |                             | CDC_D7_B        | O               | 7                          |                               |                 |                |
| P12_0        | E2                           | F19                         | GPIO12_0        | IO              | 0                          | P12_0                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SCLK_C    | O               | 1                          |                               |                 |                |
|              |                              |                             | AUDIO_CLK_C     | I               | 2                          |                               |                 |                |
|              |                              |                             | I2S1_SDI_B      | I               | 3                          |                               |                 |                |
|              |                              |                             | UT8_T0_C        | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D8_B        | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI1_D8_B      | IO              | 6                          |                               |                 |                |
|              |                              |                             | LPUT0_T0_B      | IO              | 7                          |                               |                 |                |
| P12_1        | D1                           | E18                         | GPIO12_1        | IO              | 0                          | P12_1                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SCLKN_C   | O               | 1                          |                               |                 |                |
|              |                              |                             | UART4_RX_B      | I               | 2                          |                               |                 |                |
|              |                              |                             | I2S1_SDO_B      | O               | 3                          |                               |                 |                |
|              |                              |                             | UT8_T1_C        | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D9_B        | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI1_D9_B      | IO              | 6                          |                               |                 |                |
|              |                              |                             | LPUT0_T1_B      | IO              | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P12_2        | K5                           | E15                         | GPIO12_2        | IO              | 0                          | P12_2                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_RXDS0_C   | IO              | 1                          |                               |                 |                |
|              |                              |                             | UART4_TX_B      | O               | 2                          |                               |                 |                |
|              |                              |                             | I2S1_SCLK_B     | O               | 3                          |                               |                 |                |
|              |                              |                             | UT9_T0_C        | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D10_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI1_D10_B     | IO              | 6                          |                               |                 |                |
|              |                              |                             | LPUT1_T0_B      | IO              | 7                          |                               |                 |                |
| P12_3        | J6                           | D18                         | GPIO12_3        | IO              | 0                          | P12_3                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SS0_C     | O               | 1                          |                               |                 |                |
|              |                              |                             | UART4_DE_B      | O               | 2                          |                               |                 |                |
|              |                              |                             | I2S1_WS_B       | O               | 3                          |                               |                 |                |
|              |                              |                             | UT9_T1_C        | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D11_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI1_D11_B     | IO              | 6                          |                               |                 |                |
|              |                              |                             | LPUT1_T1_B      | IO              | 7                          |                               |                 |                |
| P12_4        | A10                          | F5                          | GPIO12_4        | IO              | 0                          | P12_4                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_SS1_C     | O               | 1                          |                               |                 |                |
|              |                              |                             | SPI3_MISO_A     | IO              | 2                          |                               |                 |                |
|              |                              |                             | UT10_T0_C       | IO              | 3                          |                               |                 |                |
|              |                              |                             | CAN_RXD_C       | I               | 4                          |                               |                 |                |
|              |                              |                             | CDC_D12_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI1_D12_B     | IO              | 6                          |                               |                 |                |
|              |                              |                             | LPUT2_T0_B      | IO              | 7                          |                               |                 |                |
| P12_5        | J10                          | A10                         | GPIO12_5        | IO              | 0                          | P12_5                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | SPI3_MOSI_A     | IO              | 2                          |                               |                 |                |
|              |                              |                             | UT10_T1_C       | IO              | 3                          |                               |                 |                |
|              |                              |                             | CAN_TXD_C       | O               | 4                          |                               |                 |                |
|              |                              |                             | CDC_D13_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI1_D13_B     | IO              | 6                          |                               |                 |                |
|              |                              |                             | LPUT2_T1_B      | IO              | 7                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P12_6        | H11                          | E5                          | GPIO12_6        | IO              | 0                          | P12_6                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | SPI3_SCLK_A     | IO              | 2                          |                               |                 |                |
|              |                              |                             | UT11_T0_C       | IO              | 3                          |                               |                 |                |
|              |                              |                             | CAN_STBY_C      | O               | 4                          |                               |                 |                |
|              |                              |                             | CDC_D14_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI1_D14_B     | IO              | 6                          |                               |                 |                |
| P12_7        | F11                          | D2                          | GPIO12_7        | IO              | 0                          | P12_7                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_RXDS0_B   | IO              | 1                          |                               |                 |                |
|              |                              |                             | SPI3_SS0_A      | IO              | 3                          |                               |                 |                |
|              |                              |                             | UT11_T1_C       | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D15_B       | O               | 5                          |                               |                 |                |
| P13_0        | H3                           | G18                         | GPIO13_0        | IO              | 0                          | P13_0                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D0_B      | IO              | 1                          |                               |                 |                |
|              |                              |                             | SPI3_SS1_A      | O               | 3                          |                               |                 |                |
|              |                              |                             | QEC0_X_C        | I               | 4                          |                               |                 |                |
|              |                              |                             | SD_D0_B         | IO              | 5                          |                               |                 |                |
|              |                              |                             | CDC_D16_B       | O               | 6                          |                               |                 |                |
|              |                              |                             | OSPI0_D8_A      | IO              | 7                          |                               |                 |                |
| P13_1        | G2                           | G15                         | GPIO13_1        | IO              | 0                          | P13_1                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D1_B      | IO              | 1                          |                               |                 |                |
|              |                              |                             | SPI3_SS2_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | QEC0_Y_C        | I               | 3                          |                               |                 |                |
|              |                              |                             | SD_D1_B         | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D17_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI0_D9_A      | IO              | 6                          |                               |                 |                |
| P13_2        | F1                           | F15                         | GPIO13_2        | IO              | 0                          | P13_2                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D2_B      | IO              | 1                          |                               |                 |                |
|              |                              |                             | SPI3_SS3_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | QEC0_Z_C        | I               | 3                          |                               |                 |                |
|              |                              |                             | SD_D2_B         | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D18_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI0_D10_A     | IO              | 6                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P13_3        | J4                           | E13                         | GPIO13_3        | IO              | 0                          | P13_3                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D3_B      | IO              | 1                          |                               |                 |                |
|              |                              |                             | SPI2_SS3_A      | O               | 2                          |                               |                 |                |
|              |                              |                             | QEC1_X_C        | I               | 3                          |                               |                 |                |
|              |                              |                             | SD_D3_B         | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D19_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI0_D11_A     | IO              | 6                          |                               |                 |                |
| P13_4        | G4                           | E14                         | GPIO13_4        | IO              | 0                          | P13_4                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D4_B      | IO              | 1                          |                               |                 |                |
|              |                              |                             | LPI2S_SDI_C     | I               | 2                          |                               |                 |                |
|              |                              |                             | QEC1_Y_C        | I               | 3                          |                               |                 |                |
|              |                              |                             | SD_D4_B         | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D20_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI0_D12_A     | IO              | 6                          |                               |                 |                |
| P13_5        | D5                           | A17                         | GPIO13_5        | IO              | 0                          | P13_5                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D5_B      | IO              | 1                          |                               |                 |                |
|              |                              |                             | LPI2S_SDO_C     | O               | 2                          |                               |                 |                |
|              |                              |                             | QEC1_Z_C        | I               | 3                          |                               |                 |                |
|              |                              |                             | SD_D5_B         | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D21_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI0_D13_A     | IO              | 6                          |                               |                 |                |
| P13_6        | E6                           | B15                         | GPIO13_6        | IO              | 0                          | P13_6                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D6_B      | IO              | 1                          |                               |                 |                |
|              |                              |                             | LPI2S_SCLK_C    | O               | 2                          |                               |                 |                |
|              |                              |                             | QEC2_X_C        | I               | 3                          |                               |                 |                |
|              |                              |                             | SD_D6_B         | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D22_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI0_D14_A     | IO              | 6                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P13_7        | A4                           | A15                         | GPIO13_7        | IO              | 0                          | P13_7                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D7_B      | IO              | 1                          |                               |                 |                |
|              |                              |                             | LPI2S_WS_C      | O               | 2                          |                               |                 |                |
|              |                              |                             | QEC2_Y_C        | I               | 3                          |                               |                 |                |
|              |                              |                             | SD_D7_B         | IO              | 4                          |                               |                 |                |
|              |                              |                             | CDC_D23_B       | O               | 5                          |                               |                 |                |
|              |                              |                             | OSPI0_D15_A     | IO              | 6                          |                               |                 |                |
| P14_0        | B11                          | B9                          | GPIO14_0        | IO              | 0                          | P14_0                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_SCLK_B    | O               | 1                          |                               |                 |                |
|              |                              |                             | UART6_RX_C      | I               | 2                          |                               |                 |                |
|              |                              |                             | QEC2_Z_C        | I               | 3                          |                               |                 |                |
|              |                              |                             | SD_CMD_B        | IO              | 4                          |                               |                 |                |
|              |                              |                             | LFRC_OUT_B      | O               | 5                          |                               |                 |                |
| P14_1        | G14                          | H2                          | GPIO14_1        | IO              | 0                          | P14_1                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_SCLKN_B   | O               | 1                          |                               |                 |                |
|              |                              |                             | UART6_TX_C      | O               | 2                          |                               |                 |                |
|              |                              |                             | APLL_OUT_C      | O               | 3                          |                               |                 |                |
|              |                              |                             | QEC3_X_C        | I               | 4                          |                               |                 |                |
|              |                              |                             | SD_CLK_B        | O               | 5                          |                               |                 |                |
|              |                              |                             | LFXO_OUT_B      | O               | 6                          |                               |                 |                |
| P14_2        | F15                          | G1                          | GPIO14_2        | IO              | 0                          | P14_2                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_SS0_B     | O               | 1                          |                               |                 |                |
|              |                              |                             | UART7_RX_C      | I               | 2                          |                               |                 |                |
|              |                              |                             | LPI3C_SDA_C     | IO              | 3                          |                               |                 |                |
|              |                              |                             | QEC3_Y_C        | I               | 4                          |                               |                 |                |
|              |                              |                             | SD_RST_B        | O               | 5                          |                               |                 |                |
|              |                              |                             | LPSPi_SS5_B     | IO              | 6                          |                               |                 |                |
| P14_3        | U12                          | R7                          | GPIO14_3        | IO              | 0                          | P14_3                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_SS1_B     | O               | 1                          |                               |                 |                |
|              |                              |                             | UART7_TX_C      | O               | 2                          |                               |                 |                |
|              |                              |                             | LPI3C_SCL_C     | IO              | 3                          |                               |                 |                |
|              |                              |                             | QEC3_Z_C        | I               | 4                          |                               |                 |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7)        | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|------------------------|----------------|
| P14_4        | W12                          | R8                          | GPIO14_4        | IO              | 0                          | P14_4                         | LVCMOS                 | VDD_IO_1V8     |
|              |                              |                             | CMP3_OUT_B      | O               | 1                          |                               |                        |                |
|              |                              |                             | SPI1_MISO_C     | IO              | 2                          |                               |                        |                |
|              |                              |                             | FAULT0_C        | I               | 3                          |                               |                        |                |
|              |                              |                             | OSPI1_RXDS1_A   | IO              | 4                          |                               |                        |                |
|              |                              |                             | LPSPI_SS1_B     | IO              | 5                          |                               |                        |                |
| P14_5        | V11                          | L11                         | GPIO14_5        | IO              | 0                          | P14_5                         | LVCMOS                 | VDD_IO_1V8     |
|              |                              |                             | CMP2_OUT_B      | O               | 1                          |                               |                        |                |
|              |                              |                             | SPI1_MOSI_C     | IO              | 2                          |                               |                        |                |
|              |                              |                             | FAULT1_C        | I               | 3                          |                               |                        |                |
|              |                              |                             | OSPI0_RXDS1_B   | IO              | 4                          |                               |                        |                |
|              |                              |                             | LPSPI_SS2_B     | IO              | 5                          |                               |                        |                |
| P14_6        | Y11                          | K12                         | GPIO14_6        | IO              | 0                          | P14_6                         | LVCMOS                 | VDD_IO_1V8     |
|              |                              |                             | CMP1_OUT_B      | O               | 1                          |                               |                        |                |
|              |                              |                             | SPI1_SCLK_C     | IO              | 2                          |                               |                        |                |
|              |                              |                             | FAULT2_C        | I               | 3                          |                               |                        |                |
|              |                              |                             | OSPI1_D15_B     | IO              | 4                          |                               |                        |                |
|              |                              |                             | LPSPI_SS3_B     | IO              | 5                          |                               |                        |                |
| P14_7        | AD15                         | L12                         | GPIO14_7        | IO              | 0                          | P14_7                         | LVCMOS                 | VDD_IO_1V8     |
|              |                              |                             | CMP0_OUT_B      | O               | 1                          |                               |                        |                |
|              |                              |                             | SPI1_SS0_C      | IO              | 2                          |                               |                        |                |
|              |                              |                             | FAULT3_C        | I               | 3                          |                               |                        |                |
|              |                              |                             | APLL_OUT_B      | O               | 4                          |                               |                        |                |
|              |                              |                             | LPSPI_SS4_B     | IO              | 5                          |                               |                        |                |
| P15_0        | T13                          | V2                          | GPIOV_0         | IO              |                            | LPGPIO_CTRL_0                 | Dual Voltage<br>LVCMOS | VDD_IO_FLEX    |
|              |                              |                             | LPTMR0_CLK_IO   | IO              |                            |                               |                        |                |
| P15_1        | R12                          | W2                          | GPIOV_1         | IO              |                            | LPGPIO_CTRL_1                 | Dual Voltage<br>LVCMOS | VDD_IO_FLEX    |
|              |                              |                             | LPTMR1_CLK_IO   | IO              |                            |                               |                        |                |
| P15_2        | AA18                         | U2                          | GPIOV_2         | IO              |                            | LPGPIO_CTRL_2                 | Dual Voltage<br>LVCMOS | VDD_IO_FLEX    |
|              |                              |                             | LPTMR2_CLK_IO   | IO              |                            |                               |                        |                |
| P15_3        | P11                          | V1                          | GPIOV_3         | IO              |                            | LPGPIO_CTRL_3                 | Dual Voltage<br>LVCMOS | VDD_IO_FLEX    |
|              |                              |                             | LPTMR3_CLK_IO   | IO              |                            |                               |                        |                |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P15_4        | T11                          | V3                          | GPIOV_4         | IO              |                            | LPGPIO_CTRL_4                 | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | LFXO_OUT_C      | O               |                            |                               |                 |                |
| P15_5        | V13                          | W4                          | GPIOV_5         | IO              |                            | LPGPIO_CTRL_5                 | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | LFRC_OUT_C      | O               |                            |                               |                 |                |
| P15_6        | AC18                         | V4                          | GPIOV_6         | IO              |                            | LPGPIO_CTRL_6                 | LVCMOS          | VDD_IO_1V8     |
| P15_7        | W14                          | W5                          | GPIOV_7         | IO              |                            | LPGPIO_CTRL_7                 | LVCMOS          | VDD_IO_1V8     |
| P16_0        | L10                          |                             | GPIO16_0        | IO              | 0                          | P16_0                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D8_B      | IO              | 1                          |                               |                 |                |
| P16_1        | M9                           |                             | GPIO16_1        | IO              | 0                          | P16_1                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D9_B      | IO              | 1                          |                               |                 |                |
| P16_2        | P9                           |                             | GPIO16_2        | IO              | 0                          | P16_2                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D10_B     | IO              | 1                          |                               |                 |                |
| P16_3        | AC6                          |                             | GPIO16_3        | IO              | 0                          | P16_3                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D11_B     | IO              | 1                          |                               |                 |                |
| P16_4        | AA6                          |                             | GPIO16_4        | IO              | 0                          | P16_4                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D12_B     | IO              | 1                          |                               |                 |                |
| P16_5        | T9                           |                             | GPIO16_5        | IO              | 0                          | P16_5                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D13_B     | IO              | 1                          |                               |                 |                |
| P16_6        | R8                           |                             | GPIO16_6        | IO              | 0                          | P16_6                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D14_B     | IO              | 1                          |                               |                 |                |
| P16_7        | U8                           |                             | GPIO16_7        | IO              | 0                          | P16_7                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI0_D15_B     | IO              | 1                          |                               |                 |                |
| P17_0        | K15                          |                             | GPIO17_0        | IO              | 0                          | P17_0                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D8_C      | IO              | 1                          |                               |                 |                |
| P17_1        | L14                          |                             | GPIO17_1        | IO              | 0                          | P17_1                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D9_C      | IO              | 1                          |                               |                 |                |
| P17_2        | L18                          |                             | GPIO17_2        | IO              | 0                          | P17_2                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D10_C     | IO              | 1                          |                               |                 |                |
| P17_3        | M17                          |                             | GPIO17_3        | IO              | 0                          | P17_3                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D11_C     | IO              | 1                          |                               |                 |                |
| P17_4        | N14                          |                             | GPIO17_4        | IO              | 0                          | P17_4                         | LVCMOS          | VDD_IO_1V8     |
|              |                              |                             | OSPI1_D12_C     | IO              | 1                          |                               |                 |                |

| Pin Name (1)   | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|----------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| P17_5          | N16                          |                             | GPIO17_5        | IO              | 0                          | P17_5                         | LVCMOS          | VDD_IO_1V8     |
|                |                              |                             | OSPI1_D13_C     | IO              | 1                          |                               |                 |                |
| P17_6          | P17                          |                             | GPIO17_6        | IO              | 0                          | P17_6                         | LVCMOS          | VDD_IO_1V8     |
|                |                              |                             | OSPI1_D14_C     | IO              | 1                          |                               |                 |                |
| P17_7          | R18                          |                             | GPIO17_7        | IO              | 0                          | P17_7                         | LVCMOS          | VDD_IO_1V8     |
|                |                              |                             | OSPI1_D15_C     | IO              | 1                          |                               |                 |                |
| VREG_AUX_1_1V8 | AA4                          |                             | VREG_AUX_1_1V8  | PWR             |                            |                               |                 |                |
| VREG_AUX_2_1V8 | Y3                           |                             | VREG_AUX_2_1V8  | PWR             |                            |                               |                 |                |
| SEUART_RX      | F5                           | A14                         | SEUART_RX       | I               |                            |                               | LVCMOS          | VDD_IO_1V8     |
| SEUART_TX      | E4                           | A13                         | SEUART_TX       | O               |                            |                               | LVCMOS          | VDD_IO_1V8     |
| N.C.           | E16, K9, R6                  | B1, C1, J8, M18             | N.C.            | N.C.            |                            |                               |                 |                |
| NSRST          | H5                           | J12                         | NSRST           | I               |                            |                               | LVCMOS          | VDD_IO_1V8     |
| POR_N          | N8                           | U18                         | POR_N           | I               |                            |                               | LVCMOS          | VDD_IO_1V8     |
| HFXO_P         | D15                          | A4                          | HFXO_P          | I               |                            |                               | LVCMOS          | VDD_IO_1V8     |
| HFXO_N         | C16                          | A3                          | HFXO_N          | O               |                            |                               | LVCMOS          | VDD_IO_1V8     |
| LFXO_P         | U6                           | W17                         | LFXO_P          | I               |                            |                               | LVCMOS          | VDD_IO_1V8     |
| LFXO_N         | Y5                           | V17                         | LFXO_N          | O               |                            |                               | LVCMOS          | VDD_IO_1V8     |
| VREF_P         | V3                           | N18                         | VREF_P          | A               |                            |                               |                 |                |
| VREF_N         | U4                           |                             | VREF_N          | A               |                            |                               |                 |                |
| VDD_MAIN       | W2                           | P19                         | VDD_MAIN        | PWR             |                            |                               |                 |                |
| VDD_BATT       | T7                           | T18                         | VDD_BATT        | PWR             |                            |                               |                 |                |
| VDD_BUCK       | AB1                          | R18                         | VDD_BUCK        | PWR             |                            |                               |                 |                |
| VDD_IO_FLEX    | V15                          | W1                          | VDD_IO_FLEX     | PWR             |                            |                               |                 |                |
| VDD_IO_1V8     | A8, J2, W6, Y17              | A5, D19, W3                 | VDD_IO_1V8      | PWR             |                            |                               |                 |                |
| VDD_CORE_0V8   | D9, E18, K3, AB5, AB15       | B5, E1, E19, V6             | VDD_CORE_0V8    | PWR             |                            |                               |                 |                |
| VREG_MIP1_0V8  | N10                          | W13                         | VREG_MIP1_0V8   | PWR             |                            |                               |                 |                |
| VDD_MIP1_1V8   | R10                          | W12                         | VDD_MIP1_1V8    | PWR             |                            |                               |                 |                |
| VDD_USB_3V3    | AC12                         | W8                          | VDD_USB_3V3     | PWR             |                            |                               |                 |                |
| VDD_SX_0V8     | B15                          | A2                          | VDD_SX_0V8      | PWR             |                            |                               |                 |                |

| Pin Name (1)  | WLCSP216<br>Pin Location (2)                                  | FBGA194<br>Pin Location (2)                            | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|---------------|---------------------------------------------------------------|--------------------------------------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| VDD_PLL_OV8   |                                                               | A1                                                     | VDD_PLL_OV8     | PWR             |                            |                               |                 |                |
| VSS_RF        | B17                                                           |                                                        | VSS_RF          | PWR             |                            |                               |                 |                |
| VDD_ANA_OV8   | A18                                                           |                                                        | VDD_ANA_OV8     | PWR             |                            |                               |                 |                |
| VSS_BUCK      | AD1                                                           | V19                                                    | VSS_BUCK        | GND             |                            |                               |                 |                |
| VSS_ANA       | Y1                                                            | P18                                                    | VSS_ANA         | GND             |                            |                               |                 |                |
| VSS           | A16, AD5, AD13,<br>B1, B9, F17, H1,<br>U10, W16,<br>AB17, AC4 | B2, C18, J10,<br>J11, K9, K10,<br>K11, L2, L10,<br>V12 | VSS             | GND             |                            |                               |                 |                |
| VREG_CORE_OV8 | V5                                                            | W18                                                    | VREG_CORE_OV8   | PWR             |                            |                               |                 |                |
| VREG_AON      | V7                                                            | U17                                                    | VREG_AON        | PWR             |                            |                               |                 |                |
| VREG_LP_1V8   | W4                                                            | W19                                                    | VREG_LP_1V8     | PWR             |                            |                               |                 |                |
| VREG_DIG_1V8  | AD3                                                           | U19                                                    | VREG_DIG_1V8    | PWR             |                            |                               |                 |                |
| VREG_AUX_1V8  |                                                               | V18                                                    | VREG_AUX_1V8    | PWR             |                            |                               |                 |                |
| VREG_MIPI_1V8 | V1                                                            | N19                                                    | VREG_MIPI_1V8   | PWR             |                            |                               |                 |                |
| VSW           | AB3, AC2                                                      | T19                                                    | VSW             | PWR             |                            |                               |                 |                |
| USB_REXT      | AD11                                                          | V8                                                     | USB_REXT        | P               |                            |                               | USBPHY          | VDD_USB_3V3    |
| USB_DP        | AC14                                                          | W7                                                     | USB_DP          | IO              |                            |                               | USBPHY          | VDD_USB_3V3    |
| USB_DM        | AB13                                                          | V7                                                     | USB_DM          | IO              |                            |                               | USBPHY          | VDD_USB_3V3    |
| USB_VBUS      | AB11                                                          | W6                                                     | USB_VBUS        | A               |                            |                               | USBPHY          | VDD_USB_3V3    |
| USB_IO_ID     | AA12                                                          | R9                                                     | USB_IO_ID       | A               |                            |                               | USBPHY          | VDD_USB_3V3    |
| MIPI_REXT     | V9                                                            | V13                                                    | MIPI_REXT       | P               |                            |                               | DSIPHY          | VDD_MIPI_1V8   |
| MIPICSI_0_P   | AC8                                                           | W14                                                    | MIPICSI_0_P     | I               |                            |                               | CSIPHY          | VDD_MIPI_1V8   |
| MIPICSI_0_N   | AA8                                                           | V14                                                    | MIPICSI_0_N     | I               |                            |                               | CSIPHY          | VDD_MIPI_1V8   |
| MIPICSI_1_P   | AD7                                                           | W15                                                    | MIPICSI_1_P     | I               |                            |                               | CSIPHY          | VDD_MIPI_1V8   |
| MIPICSI_1_N   | AB7                                                           | V15                                                    | MIPICSI_1_N     | I               |                            |                               | CSIPHY          | VDD_MIPI_1V8   |
| MIPICSI_C_P   | W8                                                            | W16                                                    | MIPICSI_C_P     | I               |                            |                               | CSIPHY          | VDD_MIPI_1V8   |
| MIPICSI_C_N   | Y7                                                            | V16                                                    | MIPICSI_C_N     | I               |                            |                               | CSIPHY          | VDD_MIPI_1V8   |
| MIPIDSI_0_P   | AB9                                                           | W11                                                    | MIPIDSI_0_P     | IO              |                            |                               | DSIPHY          | VDD_MIPI_1V8   |
| MIPIDSI_0_N   | AD9                                                           | V11                                                    | MIPIDSI_0_N     | IO              |                            |                               | DSIPHY          | VDD_MIPI_1V8   |
| MIPIDSI_1_P   | AA10                                                          | W9                                                     | MIPIDSI_1_P     | IO              |                            |                               | DSIPHY          | VDD_MIPI_1V8   |

| Pin Name (1) | WLCSP216<br>Pin Location (2) | FBGA194<br>Pin Location (2) | Signal Name (3) | Pin Type<br>(4) | Multiplexing<br>Number (5) | Configuration<br>Register (6) | Buffer Type (7) | Power Rail (8) |
|--------------|------------------------------|-----------------------------|-----------------|-----------------|----------------------------|-------------------------------|-----------------|----------------|
| MIPIDSI_1_N  | AC10                         | V9                          | MIPIDSI_1_N     | IO              |                            |                               | DSIPHY          | VDD_MIPI_1V8   |
| MIPIDSI_C_P  | W10                          | W10                         | MIPIDSI_C_P     | IO              |                            |                               | DSIPHY          | VDD_MIPI_1V8   |
| MIPIDSI_C_N  | Y9                           | V10                         | MIPIDSI_C_N     | IO              |                            |                               | DSIPHY          | VDD_MIPI_1V8   |

a. Default mode after reset.

The list below describes the column headers:

- Pin Name**—Name of the pin. Px\_y pins have several functions (mux modes) to select from. The functions of other pins are fixed.
- Pin Location**—Pad or ball number of the corresponding device package. An empty cell means that a ball does not exist on the package.
- Signal Name**—Signal(s) that can be routed to the particular pin. If a signal is routable to more than one pin, a suffix \_A, \_B, \_C, or \_D is added to the signal name for differentiation. A group of signals with the same suffix is also known as Pin Set or Pin Group.
- Pin Type**—Pin designation (for the multiplexed pins, it depends on the selected mux mode):
  - A—Analog
  - I—Digital Input
  - O—Digital Output
  - IO—Digital Bi-directional (Input/Output)
  - R—Radio frequency
  - P—Passive
  - PWR—Power
  - GND—Ground
  - N/A—Not Available. This ball does not exist on the package.
  - N.C.—No Connect
- Multiplexing Number**—Function number used in the pin configuration registers:
  - 0 is the GPIO function
  - 1 through 7 are possible alternative functions
  - An empty box means Not Applicable
- Configuration Register**—Associated pin control register. For more information, see [Section 3.10 Signal Multiplexing and I/O Buffer Configuration](#).
- Buffer Type**—Associated I/O buffer type, if applicable:
  - LVC MOS—1.8-V Low-Voltage CMOS digital I/O buffer
  - Dual-Voltage (Flex) LVC MOS—1.8-V and 3.3-V LVC MOS digital I/O buffer
  - Analog—Analog input or output
  - RF—Radio Frequency input or output
  - USBPHY—HS USB data bus PHY and I/Os
  - CSIPHY—MIPI CSI camera PHY and I/Os
  - DSIPHY—MIPI DSI display / CSI camera PHY and I/Os
- Power Rail**—I/O buffer power supply, if applicable.

### 4.3 Pin Function Multiplexing

Table 4-2 describes the pin functions multiplexing options.

**Table 4-2 Pin Function Multiplexing**

| Pin Name | 0       | 1             | 2            | 3           | 4           | 5             | 6            | 7        |
|----------|---------|---------------|--------------|-------------|-------------|---------------|--------------|----------|
| P0_0     | GPIO0_0 | OSPI0_D0_A    | UART0_RX_A   | I3C_SDA_A   | UT0_T0_A    | LPCAM_HSYNC_B | CAM_HSYNC_A  | ANA_S0   |
| P0_1     | GPIO0_1 | OSPI0_D1_A    | UART0_TX_A   | I3C_SCL_A   | UT0_T1_A    | LPCAM_VSYNC_B | CAM_VSYNC_A  | ANA_S1   |
| P0_2     | GPIO0_2 | OSPI0_D2_A    | UART0_CTS_A  | I2C0_SDA_A  | UT1_T0_A    | LPCAM_PCLK_B  | CAM_PCLK_A   | ANA_S2   |
| P0_3     | GPIO0_3 | OSPI0_D3_A    | UART0_RTS_A  | I2C0_SCL_A  | UT1_T1_A    | LPCAM_XVCLK_B | CAM_XVCLK_A  | ANA_S3   |
| P0_4     | GPIO0_4 | OSPI0_D4_A    | UART1_RX_A   | PDM_D0_A    | I2C1_SDA_A  | UT2_T0_A      | CAN_RXD_B    | ANA_S4   |
| P0_5     | GPIO0_5 | OSPI0_D5_A    | UART1_TX_A   | PDM_C0_A    | I2C1_SCL_A  | UT2_T1_A      | CAN_TXD_B    | ANA_S5   |
| P0_6     | GPIO0_6 | OSPI0_D6_A    | UART1_CTS_A  | PDM_D1_A    | I2C2_SCL_A  | UT3_T0_A      | CAN_STBY_B   | ANA_S6   |
| P0_7     | GPIO0_7 | OSPI0_D7_A    | UART1_RTS_A  | PDM_C1_A    | I2C2_SDA_A  | UT3_T1_A      | CDC_DE_B     | ANA_S7   |
| P1_0     | GPIO1_0 | UART2_RX_A    | SPI0_MISO_A  | I2C3_SDA_A  | UT4_T0_A    | LPCAM_HSYNC_C | ETH_RXD0_C   | ANA_S8   |
| P1_1     | GPIO1_1 | UART2_TX_A    | SPI0_MOSI_A  | I2C3_SCL_A  | UT4_T1_A    | LPCAM_VSYNC_C | ETH_RXD1_C   | ANA_S9   |
| P1_2     | GPIO1_2 | UART3_RX_A    | SPI0_SCLK_A  | I3C_SDA_B   | UT5_T0_A    | LPCAM_PCLK_C  | ETH_RST_C    | ANA_S10  |
| P1_3     | GPIO1_3 | UART3_TX_A    | SPI0_SS0_A   | I3C_SCL_B   | UT5_T1_A    | LPCAM_XVCLK_C | ETH_TXD0_C   | ANA_S11  |
| P1_4     | GPIO1_4 | OSPI0_SS0_A   | UART0_RX_B   | SPI0_SS1_A  | UT6_T0_A    | LPCAM_D0_C    | ETH_TXD1_C   | ANA_S12  |
| P1_5     | GPIO1_5 | OSPI0_SS1_A   | UART0_TX_B   | SPI0_SS2_A  | UT6_T1_A    | LPCAM_D1_C    | ETH_TXEN_C   | ANA_S13  |
| P1_6     | GPIO1_6 | OSPI0_RXDS0_B | UART1_RX_B   | I2S0_SDI_A  | UT7_T0_A    | LPCAM_D2_C    | ETH_IRQ_C    | ANA_S14  |
| P1_7     | GPIO1_7 | OSPI0_SCLK_A  | UART1_TX_B   | I2S0_SDO_A  | UT7_T1_A    | LPCAM_D3_C    | ETH_REFCLK_C | ANA_S15  |
| P2_0     | GPIO2_0 | OSPI0_D0_B    | UART2_RX_B   | LPPDM_D0_A  | UT8_T0_A    | LPCAM_D4_C    | ETH_MDIO_C   | ANA_S16  |
| P2_1     | GPIO2_1 | OSPI0_D1_B    | UART2_TX_B   | LPPDM_C0_A  | UT8_T1_A    | LPCAM_D5_C    | ETH_MDC_C    | ANA_S17  |
| P2_2     | GPIO2_2 | OSPI0_D2_B    | UART3_RX_B   | LPPDM_D1_A  | UT9_T0_A    | LPCAM_D6_C    | ETH_CRS_DV_C | ANA_S18  |
| P2_3     | GPIO2_3 | OSPI0_D3_B    | UART3_TX_B   | LPPDM_C1_A  | UT9_T1_A    | LPCAM_D7_C    | CDC_PCLK_B   | ANA_S19  |
| P2_4     | GPIO2_4 | OSPI0_D4_B    | LPI2S_SDI_A  | SPI1_MISO_A | UT10_T0_A   | LPCAM_D0_B    | CAM_D0_A     | ANA_S20  |
| P2_5     | GPIO2_5 | OSPI0_D5_B    | LPI2S_SDO_A  | SPI1_MOSI_A | UT10_T1_A   | LPCAM_D1_B    | CAM_D1_A     | ANA_S21  |
| P2_6     | GPIO2_6 | OSPI0_D6_B    | LPI2S_SCLK_A | SPI1_SCLK_A | UT11_T0_A   | LPCAM_D2_B    | CAM_D2_A     | ANA_S22  |
| P2_7     | GPIO2_7 | OSPI0_D7_B    | LPI2S_WS_A   | SPI1_SS0_A  | UT11_T1_A   | LPCAM_D3_B    | CAM_D3_A     | ANA_S23  |
| P3_0     | GPIO3_0 | OSPI0_SCLK_B  | UART4_RX_A   | PDM_D0_B    | I2S0_SCLK_A | QEC0_X_A      | LPCAM_D4_B   | CAM_D4_A |
| P3_1     | GPIO3_1 | OSPI0_SCLKN_B | UART4_TX_A   | PDM_C0_B    | I2S0_WS_A   | QEC0_Y_A      | LPCAM_D5_B   | CAM_D5_A |
| P3_2     | GPIO3_2 | OSPI0_SS0_B   | PDM_D1_B     | I2S1_SDI_A  | I3C_SDA_C   | QEC0_Z_A      | LPCAM_D6_B   | CAM_D6_A |
| P3_3     | GPIO3_3 | OSPI0_SS1_B   | PDM_C1_B     | I2S1_SDO_A  | I3C_SCL_C   | QEC1_X_A      | LPCAM_D7_B   | CAM_D7_A |

| Pin Name             | 0       | 1             | 2            | 3            | 4            | 5            | 6           | 7            |
|----------------------|---------|---------------|--------------|--------------|--------------|--------------|-------------|--------------|
| <a href="#">P3_4</a> | GPIO3_4 | OSPI0_RXDS0_A | UART5_RX_A   | LPPDM_C0_B   | I2S1_SCLK_A  | I2C0_SCL_B   | QEC1_Y_A    | CAM_D8_A     |
| <a href="#">P3_5</a> | GPIO3_5 | OSPI0_SCLKN_A | UART5_TX_A   | LPPDM_D0_B   | SPI0_SS1_B   | I2C0_SDA_B   | QEC1_Z_A    | CAM_D9_A     |
| <a href="#">P3_6</a> | GPIO3_6 | HFXO_OUT_A    | LPUART_CTS_B | LPPDM_C1_B   | SPI0_SS2_B   | I2C1_SDA_B   | QEC2_X_A    | CAM_D10_A    |
| <a href="#">P3_7</a> | GPIO3_7 | JTAG_TRACECLK | LPUART_RTS_B | LPPDM_D1_B   | SPI1_SS1_A   | I2C1_SCL_B   | QEC2_Y_A    | CAM_D11_A    |
| <a href="#">P4_0</a> | GPIO4_0 | JTAG_TDATA0   | APLL_OUT_A   | I2S1_WS_A    | SPI1_SS2_A   | QEC2_Z_A     | CDC_VSYNC_B | CAM_D12_A    |
| <a href="#">P4_1</a> | GPIO4_1 | JTAG_TDATA1   | I2S0_SDI_B   | SPI1_SS3_A   | QEC3_X_A     | SD_CLK_D     | CDC_HSYNC_B | CAM_D13_A    |
| <a href="#">P4_2</a> | GPIO4_2 | JTAG_TDATA2   | LPI2C1_SDA_A | I2S0_SDO_B   | SPI2_MISO_A  | QEC3_Y_A     | SD_CMD_D    | CAM_D14_A    |
| <a href="#">P4_3</a> | GPIO4_3 | JTAG_TDATA3   | LPI2C1_SCL_A | I2S0_SCLK_B  | SPI2_MOSI_A  | QEC3_Z_A     | SD_RST_D    | CAM_D15_A    |
| <a href="#">P4_4</a> | GPIO4_4 | JTAG_TCK      | I2S0_WS_B    | SPI2_SCLK_A  | FAULT0_A     |              |             |              |
| <a href="#">P4_5</a> | GPIO4_5 | JTAG_TMS      | SPI2_SS0_A   | FAULT1_A     |              |              |             |              |
| <a href="#">P4_6</a> | GPIO4_6 | JTAG_TDI      | SPI2_SS1_A   | FAULT2_A     |              |              |             |              |
| <a href="#">P4_7</a> | GPIO4_7 | JTAG_TDO      | SPI2_SS2_A   | FAULT3_A     |              |              |             |              |
| <a href="#">P5_0</a> | GPIO5_0 | OSPI1_RXDS0_A | UART4_RX_C   | PDM_D2_A     | SPI0_MISO_B  | I2C2_SDA_B   | UT0_T0_B    | SD_D0_A      |
| <a href="#">P5_1</a> | GPIO5_1 | OSPI1_SS0_A   | UART4_TX_C   | PDM_D3_A     | SPI0_MOSI_B  | I2C2_SCL_B   | UT0_T1_B    | SD_D1_A      |
| <a href="#">P5_2</a> | GPIO5_2 | OSPI1_SCLKN_A | UART5_RX_C   | PDM_C3_A     | SPI0_SS0_B   | LPI2C0_SCL_B | UT1_T0_B    | SD_D2_A      |
| <a href="#">P5_3</a> | GPIO5_3 | OSPI1_SCLK_A  | UART5_TX_C   | SPI0_SCLK_B  | LPI2C0_SDA_B | UT1_T1_B     | SD_D3_A     | CDC_PCLK_A   |
| <a href="#">P5_4</a> | GPIO5_4 | OSPI1_SS1_A   | UART3_CTS_A  | PDM_D2_B     | SPI0_SS3_A   | UT2_T0_B     | SD_D4_A     | CDC_DE_A     |
| <a href="#">P5_5</a> | GPIO5_5 | OSPI1_SCLK_C  | UART3_RTS_A  | PDM_D3_B     | UT2_T1_B     | SD_D5_A      | ETH_RXD0_A  | CDC_HSYNC_A  |
| <a href="#">P5_6</a> | GPIO5_6 | UART1_CTS_B   | I2C2_SCL_C   | UT3_T0_B     | SD_D6_A      | ETH_RXD1_A   | CDC_VSYNC_A |              |
| <a href="#">P5_7</a> | GPIO5_7 | OSPI1_SS0_C   | UART1_RTS_B  | I2C2_SDA_C   | UT3_T1_B     | SD_D7_A      | ETH_RST_A   |              |
| <a href="#">P6_0</a> | GPIO6_0 | OSPI0_D0_C    | UART4_DE_A   | PDM_D0_C     | UT4_T0_B     | SD_D0_D      | ETH_TXD0_A  | LPSPi_SS1_A  |
| <a href="#">P6_1</a> | GPIO6_1 | OSPI0_D1_C    | UART5_DE_A   | PDM_C0_C     | UT4_T1_B     | SD_D1_D      | ETH_TXD1_A  | LPSPi_SS2_A  |
| <a href="#">P6_2</a> | GPIO6_2 | OSPI0_D2_C    | UART2_CTS_A  | LPI3C_SDA_A  | PDM_D1_C     | UT5_T0_B     | SD_D2_D     | ETH_TXEN_A   |
| <a href="#">P6_3</a> | GPIO6_3 | OSPI0_D3_C    | UART2_RTS_A  | LPI3C_SCL_A  | PDM_C1_C     | UT5_T1_B     | SD_D3_D     | ETH_IRQ_A    |
| <a href="#">P6_4</a> | GPIO6_4 | OSPI0_D4_C    | UART2_CTS_B  | LFRC_OUT_A   | SPI1_SS0_B   | UT6_T0_B     | SD_D4_D     | ETH_REFCLK_A |
| <a href="#">P6_5</a> | GPIO6_5 | OSPI0_D5_C    | UART2_RTS_B  | LPI2C1_SDA_B | SPI1_SS1_B   | UT6_T1_B     | SD_D5_D     | ETH_MDIO_A   |
| <a href="#">P6_6</a> | GPIO6_6 | OSPI0_D6_C    | UART0_CTS_B  | LPI2C1_SCL_B | SPI1_SS2_B   | UT7_T0_B     | SD_D6_D     | ETH_MDC_A    |
| <a href="#">P6_7</a> | GPIO6_7 | OSPI0_D7_C    | UART0_RTS_B  | PDM_C2_A     | SPI1_SS3_B   | UT7_T1_B     | SD_D7_D     | ETH_CRS_DV_A |
| <a href="#">P7_0</a> | GPIO7_0 | LPUT0_T0_A    | CMP3_OUT_A   | SPI0_MISO_C  | I2C0_SDA_C   | UT8_T0_B     | SD_CMD_A    | CAN_RXD_A    |
| <a href="#">P7_1</a> | GPIO7_1 | LPUT0_T1_A    | CMP2_OUT_A   | SPI0_MOSI_C  | I2C0_SCL_C   | UT8_T1_B     | SD_CLK_A    | CAN_TXD_A    |
| <a href="#">P7_2</a> | GPIO7_2 | LPUT1_T0_A    | UART3_CTS_B  | CMP1_OUT_A   | SPI0_SCLK_C  | I2C1_SDA_C   | UT9_T0_B    | SD_RST_A     |
| <a href="#">P7_3</a> | GPIO7_3 | LPUT1_T1_A    | UART3_RTS_B  | CMP0_OUT_A   | SPI0_SS0_C   | I2C1_SCL_C   | UT9_T1_B    | CAN_STBY_A   |
| <a href="#">P7_4</a> | GPIO7_4 | LPUT2_T0_A    | LPUART_CTS_A | LPPDM_C2_A   | LPSPi_MISO_A | LPI2C0_SCL_A | UT10_T0_B   |              |

| Pin Name              | 0        | 1             | 2            | 3            | 4            | 5             | 6            | 7             |
|-----------------------|----------|---------------|--------------|--------------|--------------|---------------|--------------|---------------|
| <a href="#">P7_5</a>  | GPIO7_5  | LPUT2_T1_A    | LPUART_RTS_A | LFXO_OUT_A   | LPPDM_D2_A   | LPSPi_MOSI_A  | LPI2C0_SDA_A | UT10_T1_B     |
| <a href="#">P7_6</a>  | GPIO7_6  | LPI2C1_SDA_C  | LPUART_RX_A  | LPI3C_SDA_B  | LPPDM_C3_A   | LPSPi_SCLK_A  | I3C_SDA_D    | UT11_T0_B     |
| <a href="#">P7_7</a>  | GPIO7_7  | LPI2C1_SCL_C  | LPUART_TX_A  | LPI3C_SCL_B  | LPPDM_D3_A   | LPSPi_SS0_A   | I3C_SCL_D    | UT11_T1_B     |
| <a href="#">P8_0</a>  | GPIO8_0  | OSPI1_SCLKN_C | AUDIO_CLK_A  | FAULT0_B     | LPCAM_D0_A   | SD_D0_C       | CDC_D0_A     | CAM_D0_B      |
| <a href="#">P8_1</a>  | GPIO8_1  | I2S2_SDI_A    | FAULT1_B     | LPCAM_D1_A   | SD_D1_C      | CDC_D1_A      | CAM_D1_B     | OSPI1_SS1_C   |
| <a href="#">P8_2</a>  | GPIO8_2  | I2S2_SDO_A    | SPI0_SS3_B   | FAULT2_B     | LPCAM_D2_A   | SD_D2_C       | CDC_D2_A     | CAM_D2_B      |
| <a href="#">P8_3</a>  | GPIO8_3  | I2S2_SCLK_A   | SPI1_MISO_B  | FAULT3_B     | LPCAM_D3_A   | SD_D3_C       | CDC_D3_A     | CAM_D3_B      |
| <a href="#">P8_4</a>  | GPIO8_4  | I2S2_WS_A     | SPI1_MOSI_B  | QEC0_X_B     | LPCAM_D4_A   | SD_D4_C       | CDC_D4_A     | CAM_D4_B      |
| <a href="#">P8_5</a>  | GPIO8_5  | OSPI0_RXDS1_A | SPI1_SCLK_B  | QEC0_Y_B     | LPCAM_D5_A   | SD_D5_C       | CDC_D5_A     | CAM_D5_B      |
| <a href="#">P8_6</a>  | GPIO8_6  | OSPI1_RXDS1_B | I2S3_SCLK_B  | QEC0_Z_B     | LPCAM_D6_A   | SD_D6_C       | CDC_D6_A     | CAM_D6_B      |
| <a href="#">P8_7</a>  | GPIO8_7  | OSPI0_RXDS1_C | I2S3_WS_B    | QEC1_X_B     | LPCAM_D7_A   | SD_D7_C       | CDC_D7_A     | CAM_D7_B      |
| <a href="#">P9_0</a>  | GPIO9_0  | OSPI1_RXDS1_C | I2S3_SDI_B   | QEC1_Y_B     | SD_CMD_C     | CDC_D8_A      | CAM_D8_B     | LPSPi_SS3_A   |
| <a href="#">P9_1</a>  | GPIO9_1  | LPUART_RX_B   | I2S3_SDO_B   | QEC1_Z_B     | SD_CLK_C     | CDC_D9_A      | CAM_D9_B     | LPSPi_SS4_A   |
| <a href="#">P9_2</a>  | GPIO9_2  | LPUART_TX_B   | I2S3_SDI_A   | SPI2_MISO_B  | QEC2_X_B     | SD_RST_C      | CDC_D10_A    | CAM_D10_B     |
| <a href="#">P9_3</a>  | GPIO9_3  | HFXO_OUT_B    | UART7_RX_B   | I2S3_SDO_A   | SPI2_MOSI_B  | QEC2_Y_B      | CDC_D11_A    | CAM_D11_B     |
| <a href="#">P9_4</a>  | GPIO9_4  | UART7_TX_B    | I2S3_SCLK_A  | SPI2_SCLK_B  | I2C3_SDA_C   | QEC2_Z_B      | CDC_D12_A    | CAM_D12_B     |
| <a href="#">P9_5</a>  | GPIO9_5  | OSPI1_D0_C    | I2S3_WS_A    | SPI2_SS0_B   | I2C3_SCL_C   | QEC3_X_B      | CDC_D13_A    | CAM_D13_B     |
| <a href="#">P9_6</a>  | GPIO9_6  | OSPI1_D1_C    | AUDIO_CLK_B  | SPI2_SS1_B   | I2C3_SDA_B   | QEC3_Y_B      | CDC_D14_A    | CAM_D14_B     |
| <a href="#">P9_7</a>  | GPIO9_7  | OSPI1_D2_C    | UART7_DE_B   | SPI2_SS2_B   | I2C3_SCL_B   | QEC3_Z_B      | CDC_D15_A    | CAM_D15_B     |
| <a href="#">P10_0</a> | GPIO10_0 | OSPI1_D3_C    | UART6_DE_B   | SPI2_SS3_B   | UT0_T0_C     | LPCAM_HSYNC_A | CDC_D16_A    | CAM_HSYNC_B   |
| <a href="#">P10_1</a> | GPIO10_1 | OSPI1_D4_C    |              | LPI2S_SDI_B  | UT0_T1_C     | LPCAM_VSYNC_A | CDC_D17_A    | CAM_VSYNC_B   |
| <a href="#">P10_2</a> | GPIO10_2 | OSPI1_D5_C    |              | LPI2S_SDO_B  | UT1_T0_C     | LPCAM_PCLK_A  | CDC_D18_A    | CAM_PCLK_B    |
| <a href="#">P10_3</a> | GPIO10_3 | OSPI1_D6_C    |              | LPI2S_SCLK_B | UT1_T1_C     | LPCAM_XVCLK_A | CDC_D19_A    | CAM_XVCLK_B   |
| <a href="#">P10_4</a> | GPIO10_4 | OSPI1_D7_C    |              | LPI2S_WS_B   | I2C0_SDA_D   | UT2_T0_C      | ETH_TXD0_B   | CDC_D20_A     |
| <a href="#">P10_5</a> | GPIO10_5 | UART6_RX_A    | I2S2_SDI_B   | SPI3_MISO_B  | I2C0_SCL_D   | UT2_T1_C      | ETH_TXD1_B   | CDC_D21_A     |
| <a href="#">P10_6</a> | GPIO10_6 | UART6_TX_A    | I2S2_SDO_B   | SPI3_MOSI_B  | I2C1_SDA_D   | UT3_T0_C      | ETH_TXEN_B   | CDC_D22_A     |
| <a href="#">P10_7</a> | GPIO10_7 | UART7_RX_A    | I2S2_SCLK_B  | SPI3_SCLK_B  | I2C1_SCL_D   | UT3_T1_C      | CDC_D23_A    | OSPI1_RXDS0_C |
| <a href="#">P11_0</a> | GPIO11_0 | OSPI1_D0_A    | UART7_TX_A   | I2S2_WS_B    | SPI3_SS0_B   | UT4_T0_C      | ETH_REFCLK_B | CDC_D0_B      |
| <a href="#">P11_1</a> | GPIO11_1 | OSPI1_D1_A    | UART7_DE_A   | SPI3_SS1_B   | UT4_T1_C     | ETH_MDIO_B    | CDC_D1_B     | LPSPi_SS5_A   |
| <a href="#">P11_2</a> | GPIO11_2 | OSPI1_D2_A    | UART6_DE_A   | LPPDM_C2_B   | SPI3_SS2_B   | UT5_T0_C      | ETH_MDC_B    | CDC_D2_B      |
| <a href="#">P11_3</a> | GPIO11_3 | OSPI1_D3_A    | UART5_RX_B   | LPPDM_C3_B   | SPI3_SS3_B   | UT5_T1_C      | ETH_RXD0_B   | CDC_D3_B      |
| <a href="#">P11_4</a> | GPIO11_4 | OSPI1_D4_A    | UART5_TX_B   | PDM_C2_B     | LPSPi_MISO_B | UT6_T0_C      | ETH_RXD1_B   | CDC_D4_B      |
| <a href="#">P11_5</a> | GPIO11_5 | OSPI1_D5_A    | UART6_RX_B   | PDM_C3_B     | LPSPi_MOSI_B | UT6_T1_C      | ETH_CRS_DV_B | CDC_D5_B      |

| Pin Name              | 0        | 1             | 2            | 3           | 4             | 5           | 6           | 7          |
|-----------------------|----------|---------------|--------------|-------------|---------------|-------------|-------------|------------|
| <a href="#">P11_6</a> | GPIO11_6 | OSPI1_D6_A    | UART6_TX_B   | LPPDM_D2_B  | LPSPi_SCLK_B  | UT7_T0_C    | ETH_RST_B   | CDC_D6_B   |
| <a href="#">P11_7</a> | GPIO11_7 | OSPI1_D7_A    | UART5_DE_B   | LPPDM_D3_B  | LPSPi_SS0_B   | UT7_T1_C    | ETH_IRQ_B   | CDC_D7_B   |
| <a href="#">P12_0</a> | GPIO12_0 | OSPI0_SCLK_C  | AUDIO_CLK_C  | I2S1_SDI_B  | UT8_T0_C      | CDC_D8_B    | OSPI1_D8_B  | LPUT0_T0_B |
| <a href="#">P12_1</a> | GPIO12_1 | OSPI0_SCLKN_C | UART4_RX_B   | I2S1_SDO_B  | UT8_T1_C      | CDC_D9_B    | OSPI1_D9_B  | LPUT0_T1_B |
| <a href="#">P12_2</a> | GPIO12_2 | OSPI0_RXDS0_C | UART4_TX_B   | I2S1_SCLK_B | UT9_T0_C      | CDC_D10_B   | OSPI1_D10_B | LPUT1_T0_B |
| <a href="#">P12_3</a> | GPIO12_3 | OSPI0_SS0_C   | UART4_DE_B   | I2S1_WS_B   | UT9_T1_C      | CDC_D11_B   | OSPI1_D11_B | LPUT1_T1_B |
| <a href="#">P12_4</a> | GPIO12_4 | OSPI0_SS1_C   | SPI3_MISO_A  | UT10_T0_C   | CAN_RXD_C     | CDC_D12_B   | OSPI1_D12_B | LPUT2_T0_B |
| <a href="#">P12_5</a> | GPIO12_5 |               | SPI3_MOSI_A  | UT10_T1_C   | CAN_TXD_C     | CDC_D13_B   | OSPI1_D13_B | LPUT2_T1_B |
| <a href="#">P12_6</a> | GPIO12_6 |               | SPI3_SCLK_A  | UT11_T0_C   | CAN_STBY_C    | CDC_D14_B   | OSPI1_D14_B |            |
| <a href="#">P12_7</a> | GPIO12_7 | OSPI1_RXDS0_B |              | SPI3_SS0_A  | UT11_T1_C     | CDC_D15_B   |             |            |
| <a href="#">P13_0</a> | GPIO13_0 | OSPI1_D0_B    |              | SPI3_SS1_A  | QEC0_X_C      | SD_D0_B     | CDC_D16_B   | OSPI0_D8_A |
| <a href="#">P13_1</a> | GPIO13_1 | OSPI1_D1_B    | SPI3_SS2_A   | QEC0_Y_C    | SD_D1_B       | CDC_D17_B   | OSPI0_D9_A  |            |
| <a href="#">P13_2</a> | GPIO13_2 | OSPI1_D2_B    | SPI3_SS3_A   | QEC0_Z_C    | SD_D2_B       | CDC_D18_B   | OSPI0_D10_A |            |
| <a href="#">P13_3</a> | GPIO13_3 | OSPI1_D3_B    | SPI2_SS3_A   | QEC1_X_C    | SD_D3_B       | CDC_D19_B   | OSPI0_D11_A |            |
| <a href="#">P13_4</a> | GPIO13_4 | OSPI1_D4_B    | LPI2S_SDI_C  | QEC1_Y_C    | SD_D4_B       | CDC_D20_B   | OSPI0_D12_A |            |
| <a href="#">P13_5</a> | GPIO13_5 | OSPI1_D5_B    | LPI2S_SDO_C  | QEC1_Z_C    | SD_D5_B       | CDC_D21_B   | OSPI0_D13_A |            |
| <a href="#">P13_6</a> | GPIO13_6 | OSPI1_D6_B    | LPI2S_SCLK_C | QEC2_X_C    | SD_D6_B       | CDC_D22_B   | OSPI0_D14_A |            |
| <a href="#">P13_7</a> | GPIO13_7 | OSPI1_D7_B    | LPI2S_WS_C   | QEC2_Y_C    | SD_D7_B       | CDC_D23_B   | OSPI0_D15_A |            |
| <a href="#">P14_0</a> | GPIO14_0 | OSPI1_SCLK_B  | UART6_RX_C   | QEC2_Z_C    | SD_CMD_B      | LFRC_OUT_B  |             |            |
| <a href="#">P14_1</a> | GPIO14_1 | OSPI1_SCLKN_B | UART6_TX_C   | APLL_OUT_C  | QEC3_X_C      | SD_CLK_B    | LFXO_OUT_B  |            |
| <a href="#">P14_2</a> | GPIO14_2 | OSPI1_SS0_B   | UART7_RX_C   | LPI3C_SDA_C | QEC3_Y_C      | SD_RST_B    | LPSPi_SS5_B |            |
| <a href="#">P14_3</a> | GPIO14_3 | OSPI1_SS1_B   | UART7_TX_C   | LPI3C_SCL_C | QEC3_Z_C      |             |             |            |
| <a href="#">P14_4</a> | GPIO14_4 | CMP3_OUT_B    | SPI1_MISO_C  | FAULT0_C    | OSPI1_RXDS1_A | LPSPi_SS1_B |             |            |
| <a href="#">P14_5</a> | GPIO14_5 | CMP2_OUT_B    | SPI1_MOSI_C  | FAULT1_C    | OSPI0_RXDS1_B | LPSPi_SS2_B |             |            |
| <a href="#">P14_6</a> | GPIO14_6 | CMP1_OUT_B    | SPI1_SCLK_C  | FAULT2_C    | OSPI1_D15_B   | LPSPi_SS3_B |             |            |
| <a href="#">P14_7</a> | GPIO14_7 | CMP0_OUT_B    | SPI1_SS0_C   | FAULT3_C    | APLL_OUT_B    | LPSPi_SS4_B |             |            |
| <a href="#">P16_0</a> | GPIO16_0 | OSPI0_D8_B    |              |             |               |             |             |            |
| <a href="#">P16_1</a> | GPIO16_1 | OSPI0_D9_B    |              |             |               |             |             |            |
| <a href="#">P16_2</a> | GPIO16_2 | OSPI0_D10_B   |              |             |               |             |             |            |
| <a href="#">P16_3</a> | GPIO16_3 | OSPI0_D11_B   |              |             |               |             |             |            |
| <a href="#">P16_4</a> | GPIO16_4 | OSPI0_D12_B   |              |             |               |             |             |            |
| <a href="#">P16_5</a> | GPIO16_5 | OSPI0_D13_B   |              |             |               |             |             |            |
| <a href="#">P16_6</a> | GPIO16_6 | OSPI0_D14_B   |              |             |               |             |             |            |

| Pin Name              | 0        | 1           | 2 | 3 | 4 | 5 | 6 | 7 |
|-----------------------|----------|-------------|---|---|---|---|---|---|
| <a href="#">P16_7</a> | GPIO16_7 | OSPI0_D15_B |   |   |   |   |   |   |
| <a href="#">P17_0</a> | GPIO17_0 | OSPI1_D8_C  |   |   |   |   |   |   |
| <a href="#">P17_1</a> | GPIO17_1 | OSPI1_D9_C  |   |   |   |   |   |   |
| <a href="#">P17_2</a> | GPIO17_2 | OSPI1_D10_C |   |   |   |   |   |   |
| <a href="#">P17_3</a> | GPIO17_3 | OSPI1_D11_C |   |   |   |   |   |   |
| <a href="#">P17_4</a> | GPIO17_4 | OSPI1_D12_C |   |   |   |   |   |   |
| <a href="#">P17_5</a> | GPIO17_5 | OSPI1_D13_C |   |   |   |   |   |   |
| <a href="#">P17_6</a> | GPIO17_6 | OSPI1_D14_C |   |   |   |   |   |   |
| <a href="#">P17_7</a> | GPIO17_7 | OSPI1_D15_C |   |   |   |   |   |   |

## 5 Electrical Characteristics

### 5.1 Absolute Maximum Ratings

Stresses above the values listed under [Table 5-1](#) may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Table 5-1 Absolute Maximum Ratings**

| Parameter                               |             | Condition  | Min  | Max  | Unit |
|-----------------------------------------|-------------|------------|------|------|------|
| Chip power inputs                       | VDD_MAIN    |            | -0.3 | 5.0  | V    |
|                                         | VDD_IO_FLEX | 1.8-V mode | -0.3 | 1.98 | V    |
|                                         |             | 3.3-V mode | -0.3 | 3.63 | V    |
|                                         | VDD_BATT    |            | -0.3 | 5.0  | V    |
|                                         | VDD_BUCK    |            | -0.3 | 5.0  | V    |
| Input/Output voltage range (1.8 V I/Os) |             |            | 0.3  | 1.98 | V    |
| Maximum junction temperature            |             |            | -40  | 150  | °C   |

#### 5.1.1 Maximum Supply Current

[Table 5-2](#) summarizes maximum current consumption ratings at power terminals of the device.

**Table 5-2 Maximum Supply Current**

| Parameter               |                                                     | Condition | Max  | Unit |
|-------------------------|-----------------------------------------------------|-----------|------|------|
| I <sub>VDD_ALL</sub>    | Supply current into all power pins                  |           | 600  | mA   |
| I <sub>VSS_ALL</sub>    | Supply current out of all ground pin(s)             |           | 1000 | mA   |
| I <sub>VDD_MAIN</sub>   | Supply current rating for the VDD_MAIN pins         |           | 10   | mA   |
| I <sub>VDD_VBAT</sub>   | Supply current rating for the VDD_BATT pins         |           | 1    | mA   |
| I <sub>VDDIO_1.8V</sub> | Supply current rating for the VDD_IO_1V8 pins       |           | 500  | mA   |
| I <sub>VDDIO_3.3V</sub> | Supply current rating for the VDD_IO_FLEX pins      |           | 200  | mA   |
| I <sub>1V8_IO</sub>     | Current sunk, sourced by any 1.8 V I/O pin          |           | 65   | mA   |
| I <sub>3V6_IO</sub>     | Current sunk, sourced by any 3.6 V I/O pin          |           | 35   | mA   |
| I <sub>IO_ALL</sub>     | Current sunk, sourced by all pins (I/O and control) |           | 700  | mA   |

#### 5.1.2 Maximum Performance Ratings

[Table 5-3](#) lists the maximum performance per module on this device.

**Table 5-3 Maximum Performance Ratings**

| Parameter                       |           | Max | Unit |
|---------------------------------|-----------|-----|------|
| Interconnect APB bus            | SYST_PCLK | 100 | MHz  |
| Interconnect AHB bus            | SYST_HCLK | 200 | MHz  |
| Interconnect AXI bus            | SYST_ACLK | 400 | MHz  |
| Cortex-A32                      | A32       | 800 | MHz  |
| High-Performance Arm Cortex-M55 | M55-HP    | 400 | MHz  |

| Parameter                                                           |                      | Max  | Unit      |
|---------------------------------------------------------------------|----------------------|------|-----------|
| High-Efficiency Arm Cortex-M55                                      | M55-HE               | 160  | MHz       |
| Ethos-U55 Neural Processing Units                                   | NPU-HP               | 400  | MHz       |
|                                                                     | NPU-HE               | 160  | MHz       |
| Arm Ethos-U85 Neural Processing Unit                                | NPU-HG               | 400  | MHz       |
| D/AVE 2D Graphics Processing Unit                                   | GPU2D                | 400  | MHz       |
| Controller Area Network                                             | CANFD                | 10   | Mbps      |
| Ethernet 10/100 Controller                                          | ETH                  | 100  | Mbps      |
| Inter-Integrated Circuit                                            | I2C                  | 3.4  | Mbps      |
|                                                                     | LPI2C                | 400  | kbps      |
| Inter-IC Sound                                                      | I2S <sup>(1)</sup>   | 192  | kHz       |
|                                                                     | LPI2S <sup>(1)</sup> | 192  | kHz       |
| MIPI Improved Inter-Integrated Circuit                              | I3C                  | 20   | Mbps      |
|                                                                     | LPI3C                | 20   | Mbps      |
| Pulse Density Modulator                                             | PDM                  | 4.8  | MHz       |
|                                                                     | LPPDM                | 4.8  | MHz       |
| Serial Peripheral Interface                                         | SPI                  | 50   | MHz       |
|                                                                     | LPSPi                | 40   | MHz       |
| Universal Asynchronous Receiver/Transmitter                         | UART                 | 5    | Mbps      |
|                                                                     | LPUART               | 5    | Mbps      |
| Universal Serial Bus                                                | USB                  | 480  | Mbps      |
| Hex SPI                                                             | HEXSPI               | 200  | MHz       |
| Memory Card Controller                                              | SD Card              | 50   | MHz       |
|                                                                     | eMMC                 | 50   | MHz       |
|                                                                     | SDIO                 | 50   | MHz       |
| Camera Parallel Interface                                           | LPCPI                | 50   | MHz       |
|                                                                     | CPI                  | 50   | MHz       |
| MIPI Camera Serial Interface                                        | CSI                  | 2.5  | Gbps/lane |
| Display Parallel Interface                                          | DPI                  | 50   | MHz       |
| MIPI Display Serial Interface                                       | DSI                  | 1.25 | Gbps/lane |
| Image Signal Processor (assuming 2MP image and 100 MHz pixel clock) | ISP                  | 200  | FPS       |
| JPEG Encoder (assuming 2MP image)                                   | JPEG                 | 200  | FPS       |
| Analog-to-Digital Converters                                        | ADC12                | 1.25 | MSPS      |
|                                                                     | ADC24                | 16   | kSPS      |
| Digital-to-Analog Converters                                        | DAC12                | 1    | kHz       |

1. Sampling frequency

## 5.2 Operating Conditions

### 5.2.1 General Operating Conditions

Table 5-4 presents recommended operating conditions over free-air temperature range (unless otherwise noted).

Table 5-4 General Operating Conditions

| Parameter                   |                                                                            |                                                                  | Min  | Typ   | Max  | Unit |
|-----------------------------|----------------------------------------------------------------------------|------------------------------------------------------------------|------|-------|------|------|
| VDD_MAIN <sup>(1)(5)</sup>  | Main power supply                                                          | When supplied by external wide-range unregulated voltage source. | 1.75 |       | 4.8  | V    |
|                             |                                                                            | When supplied by external 1.8 V regulated source.                | 1.75 | 1.8   | 1.9  |      |
| VDD_BATT                    | Always-On domain power input                                               |                                                                  | 1.75 |       | 4.8  | V    |
| VDD_BUCK <sup>(5)</sup>     | Internal DC-DC converter power input                                       |                                                                  | 1.75 |       | 4.8  | V    |
| VDD_USB_3V3 <sup>(6)</sup>  | USB power input                                                            |                                                                  | 3.0  | 3.3   | 3.6  | V    |
| VDD_IO_FLEX                 | GPIO flex pads (1.8 V - 3.3 V) power input                                 | 1.8-V mode <sup>(2)</sup>                                        | 1.62 | 1.8   | 1.98 | V    |
|                             |                                                                            | 3.3-V mode                                                       | 3.0  | 3.3   | 4.2  | V    |
| VDD_IO_1V8                  | GPIO standard pads (1.8 V) power input                                     |                                                                  | 1.08 | 1.8   | 1.98 | V    |
| VREG_DIG_1V8 <sup>(3)</sup> | Internal 1.8 V regulator output                                            |                                                                  | 1.7  | 1.8   | 1.9  | V    |
| VREG_AUX_1V8                | Auxiliary 1.8 V regulator output                                           |                                                                  | 1.7  | 1.8   | 1.9  | V    |
| VREG_AON <sup>(4)</sup>     | Internal voltage supply – output of internal Always-On 0.8 V LDO regulator |                                                                  | 0.76 | 0.825 | 0.9  | V    |
| VREG_LP_1V8                 | Internal voltage supply – output of internal low-power LDO regulator       |                                                                  | TBD  | TBD   | TBD  | V    |
| VREF_P <sup>(8)</sup>       | External positive voltage reference input for ADC and DAC                  |                                                                  | 1.2  | 1.8   | 1.9  | V    |
| VREF_N <sup>(7)</sup>       | External negative voltage reference for ADC                                |                                                                  | 0    | 0     | 900  | mV   |
| VSS_BUCK                    | DC-DC converter ground                                                     |                                                                  | 0    |       |      | V    |
| VSS_ANA                     | Analog ground                                                              |                                                                  | 0    |       |      | V    |
| VSS                         | Digital ground                                                             |                                                                  | 0    |       |      | V    |
| t <sub>a</sub>              | Operating ambient temperature range                                        | Standard                                                         | -40  |       | 75   | °C   |
| t <sub>j</sub>              | Operating junction temperature range                                       | Standard                                                         | -40  |       | 105  | °C   |

1. When an external reset supervisor device is used, and VDD\_MAIN is less than 1.8 V, it is important that the supply voltage to the supervisor device does not dip during startup and trigger the supervisor device.
2. VDD\_IO\_FLEX should be connected to VDD\_IO\_1V8 when 1.8-V mode is used.
3. VREG\_DIG\_1V8 must be bypassed to ground through a 1-μF capacitor.
4. VREG\_AON must be bypassed to ground through a 1-μF capacitor in series with a 1.0 kΩ resistor.
5. VDD\_MAIN and VDD\_BUCK must be tied together.
6. If USB function is not used, VDD\_USB\_3V3 must be tied to ground.
7. VREF\_N should be grounded.
8. VREF\_P should be bypassed to ground through 1-uF capacitor.

#### CAUTION

The decoupling for VREG\_AON and VREG\_DIG\_1V8 pins must be present on the PCB or otherwise the device may be at risk for damage.

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**NOTE**

An external brownout supervisor must be connected to VDD\_MAIN/VDD\_BUCK. The brownout supervisor must assert before voltage input to the chip falls below 1.65V. Care (that is, sufficient decoupling) must be taken to ensure that supply noise/transients do not spuriously trigger resets. Refer to the Alif Application Note AAPN0036, *PCB Layout Guidelines for Ensemble E4, E6, E8 MCUs and Fusion Processors*, for more details and detailed information about power decoupling for all power pins.

For use of the device with external reference for VREF\_P or VREF\_N, please contact an Alif representative.

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## 5.2.2 Device Power Modes

### 5.2.2.1 Power Modes Case Definition

#### NOTE

Specifications shown in [Table 5-5 Power Modes Case Definition](#) are subject to change.

[Table 5-5](#) provides status of each module during different power modes of the device.

**Table 5-5 Power Modes Case Definition**

| Power Mode |                                                                                                     | Voltage Regulation | MRAM | SRAM      |            |            |         | Clock Source | Main Peripherals Power | LP Peripherals Power | Wake-Up Sources                         | Current Consumption at 3.3 V |       | Wake Time to Reach GO Mode |       |
|------------|-----------------------------------------------------------------------------------------------------|--------------------|------|-----------|------------|------------|---------|--------------|------------------------|----------------------|-----------------------------------------|------------------------------|-------|----------------------------|-------|
|            |                                                                                                     |                    |      | Bulk SRAM | M55-HP TCM | M55-HE TCM | Utility |              |                        |                      |                                         | Typ                          | Units | Typ                        | Units |
| GO Modes   |                                                                                                     |                    |      |           |            |            |         |              |                        |                      |                                         |                              |       |                            |       |
| GO_1       | All CPU cores running CoreMark at max frequency. All three NPUs running power indicative inference. | DC-DC              | ON   | ON        | ON         | ON         | ON      | PLL          | ON with clocks gated   | All ON               | Any interrupt from a powered peripheral | TBD <sup>(3)</sup>           | mA    | N/A                        |       |
| GO_2       | All CPU cores running CoreMark at max frequency. No NPU enabled.                                    |                    |      |           |            |            |         |              |                        |                      |                                         | 75                           | mA    |                            |       |
| GO_3       | A32-0 and A32-1 running CoreMark at 800 MHz. No NPU is enabled.                                     |                    |      |           |            |            |         |              |                        |                      |                                         | 66                           | mA    |                            |       |
| GO_4       | Only M55-HP running CoreMark at 400 MHz.                                                            |                    | 83   | µA/MHz    |            |            |         |              |                        |                      |                                         |                              |       |                            |       |
|            |                                                                                                     | OFF                | OFF  |           | OFF        |            |         |              |                        |                      |                                         | 18 <sup>(4)</sup>            | mA    |                            |       |

| Power Mode    |                                                                              | Voltage Regulation | MRAM | SRAM      |            |                  |                  | Clock Source | Main Peripherals Power | LP Peripherals Power         | Wake-Up Sources                                        | Current Consumption at 3.3 V |        | Wake Time to Reach GO Mode |       |
|---------------|------------------------------------------------------------------------------|--------------------|------|-----------|------------|------------------|------------------|--------------|------------------------|------------------------------|--------------------------------------------------------|------------------------------|--------|----------------------------|-------|
|               |                                                                              |                    |      | Bulk SRAM | M55-HP TCM | M55-HE TCM       | Utility          |              |                        |                              |                                                        | Typ                          | Units  | Typ                        | Units |
|               | No NPU is enabled.                                                           |                    |      |           |            |                  |                  |              |                        |                              |                                                        | 45                           | μA/MHz |                            |       |
| GO_5          | Only M55-HE running CoreMark at 76.8 MHz, cache disabled. No NPU is enabled. |                    |      |           |            |                  |                  | HFRC         | All OFF                |                              |                                                        | 2.1                          | mA     |                            |       |
|               |                                                                              |                    |      |           |            | OFF              |                  |              |                        |                              |                                                        |                              |        |                            |       |
| GO_6          | Only M55-HE running CoreMark at 19.2 MHz. No NPU is enabled.                 |                    |      |           |            |                  |                  | HFRC         | All OFF                |                              |                                                        | 800                          | μA     |                            |       |
|               |                                                                              |                    |      |           |            |                  |                  |              |                        |                              |                                                        |                              |        |                            |       |
| READY Modes   |                                                                              |                    |      |           |            |                  |                  |              |                        |                              |                                                        |                              |        |                            |       |
| RDY_1         | M55-HP WFI <sup>(2)</sup> at 400 MHz from PLL. M55-HE powered off.           | DC-DC              | OFF  | OFF       | ON         | OFF              | ON               | PLL          | ON with clocks gated   | All ON                       | Any interrupt from a powered peripheral                | 13 <sup>(5)</sup>            | mA     | < 40                       | ns    |
| RDY_2         | M55-HE WFI at 76.8 MHz from HFRC. M55-HP powered off.                        |                    |      |           | OFF        | ON               |                  | HFRC         | All OFF                |                              |                                                        | 1.5                          | mA     | < 200                      | ns    |
| IDLE Modes    |                                                                              |                    |      |           |            |                  |                  |              |                        |                              |                                                        |                              |        |                            |       |
| IDLE_1        | All CPU cores powered off. 76.8 MHz clock from HFXO.                         | DC-DC              | OFF  | OFF       | OFF        | OFF but retained | OFF but retained | HFXO         | ON with clocks gated   | All ON                       | Any interrupt from a powered peripheral <sup>(1)</sup> | 5.0                          | mA     | 2 - 4                      | μs    |
| IDLE_2        | All CPU cores powered off. 600 kHz clock from HFRC.                          |                    |      |           |            |                  |                  | HFRC         |                        |                              |                                                        | 4.0                          | mA     | 2 - 4                      | μs    |
| STANDBY Modes |                                                                              |                    |      |           |            |                  |                  |              |                        |                              |                                                        |                              |        |                            |       |
| STBY_1        | All CPU cores powered off. HFRC ready.                                       | DC-DC              | OFF  | OFF       | OFF        | OFF but retained | OFF but retained | HFRC         | All OFF                | LPUART, LPI2C ON + STOP Mode | Any interrupt from a                                   | 60                           | μA     | 5 <sup>(6)</sup>           | μs    |

| Power Mode |                                                                                         | Voltage Regulation | MRAM | SRAM           |            |                  |                  | Clock Source | Main Peripherals Power | LP Peripherals Power                  | Wake-Up Sources                         | Current Consumption at 3.3 V |       | Wake Time to Reach GO Mode |       |
|------------|-----------------------------------------------------------------------------------------|--------------------|------|----------------|------------|------------------|------------------|--------------|------------------------|---------------------------------------|-----------------------------------------|------------------------------|-------|----------------------------|-------|
|            |                                                                                         |                    |      | Bulk SRAM      | M55-HP TCM | M55-HE TCM       | Utility          |              |                        |                                       |                                         | Typ                          | Units | Typ                        | Units |
|            |                                                                                         |                    |      |                |            |                  |                  |              |                        | peripherals                           | powered peripheral                      |                              |       |                            |       |
| STOP Modes |                                                                                         |                    |      |                |            |                  |                  |              |                        |                                       |                                         |                              |       |                            |       |
| STOP_0     | STOP_1 plus both 4.0MB SRAM0 and 4.0MB SRAM1 are retained.                              | LDO                | OFF  | OFF            | OFF        | OFF but retained | OFF but retained | LFXO         | All OFF                | LPRTC, LPTIMER, LPCMP, BOD, LPGPIO ON | Any interrupt from a powered peripheral | TBD                          | μA    | 1.1                        | ms    |
| STOP_1     | STOP_2 plus 256KB of M55-HE TCM SRAM retained.                                          |                    |      |                |            |                  |                  |              |                        |                                       |                                         | 1050                         | nA    | 1.1                        | ms    |
| STOP_2     | STOP_3 plus 4KB Utility SRAM retained. Boot from MRAM.                                  |                    |      |                |            |                  |                  |              |                        |                                       |                                         |                              |       |                            |       |
| STOP_3     | STOP_4 plus LPTIMER, BOD, LPCMP, and LPGPIO active. Boot from MRAM.                     |                    |      |                |            | OFF              |                  |              |                        |                                       |                                         |                              |       |                            |       |
| STOP_4     | STOP_5 plus LPRTC running from 32.768 kHz LFXO. Boot from MRAM.                         |                    |      |                |            |                  |                  |              |                        |                                       |                                         |                              |       |                            |       |
| STOP_5     | 32.7 kHz LFRC running, all other functions off. Boot from MRAM.                         |                    |      |                |            |                  |                  |              |                        |                                       |                                         |                              |       |                            |       |
| SRAM0      | Adder current for optional retention of Bulk SRAM0 contents available in any Power Mode | DC-DC or LDO       | N/A  | 2MB retained   | N/A        |                  |                  |              |                        |                                       |                                         | 8.5                          | μA    | N/A                        |       |
|            |                                                                                         |                    |      | 1MB retained   |            |                  |                  |              |                        |                                       |                                         | 4.25                         | μA    |                            |       |
|            |                                                                                         |                    |      | 512KB retained |            |                  |                  |              |                        |                                       |                                         | 2.125                        | μA    |                            |       |
|            |                                                                                         |                    |      | 512KB          |            |                  |                  |              |                        |                                       |                                         | 2.125                        | μA    |                            |       |

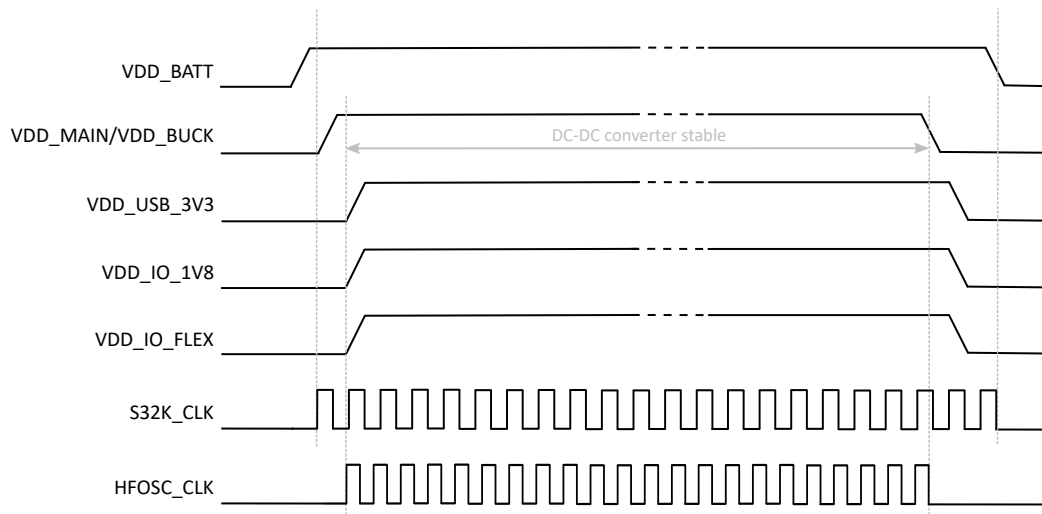
| Power Mode                             |                                                                                                  | Voltage Regulation | MRAM | SRAM                               |            |            |         | Clock Source | Main Peripherals Power | LP Peripherals Power | Wake-Up Sources | Current Consumption at 3.3 V                                            |       | Wake Time to Reach GO Mode |       |
|----------------------------------------|--------------------------------------------------------------------------------------------------|--------------------|------|------------------------------------|------------|------------|---------|--------------|------------------------|----------------------|-----------------|-------------------------------------------------------------------------|-------|----------------------------|-------|
|                                        |                                                                                                  |                    |      | Bulk SRAM                          | M55-HP TCM | M55-HE TCM | Utility |              |                        |                      |                 | Typ                                                                     | Units | Typ                        | Units |
|                                        |                                                                                                  |                    |      | retained                           |            |            |         |              |                        |                      |                 |                                                                         |       |                            |       |
| SRAM1                                  | Adder current for optional retention of Bulk SRAM1 contents available in any Power Mode          | DC-DC or LDO       | N/A  | 4MB retained                       | N/A        |            |         |              |                        |                      |                 | 17                                                                      | μA    | N/A                        |       |
| SERAM                                  | Adder current for optional retention of Secure Enclave SRAM contents available in any Power Mode | DC-DC or LDO       | N/A  | 128KB Secure Enclave SRAM retained |            |            |         | N/A          |                        |                      |                 | TBD                                                                     | nA    | N/A                        |       |
| I/O Domain Adder for STOP in all cases |                                                                                                  | N/A                |      |                                    |            |            |         |              |                        |                      |                 | STOP Mode current adder I <sub>VDD_IO_1V8</sub> when VDD_IO_1V8 = 1.8 V |       | N/A                        |       |
|                                        |                                                                                                  |                    |      |                                    |            |            |         |              |                        |                      |                 | 300                                                                     | nA    |                            |       |
| Cold boot time from Power-On Reset     |                                                                                                  | N/A                |      |                                    |            |            |         |              |                        |                      |                 |                                                                         |       | 130                        | ms    |
| Power Mode Entry                       |                                                                                                  |                    |      |                                    |            |            |         |              |                        |                      |                 |                                                                         |       | Time to Enter Mode         |       |
| Time to enter any STOP Mode            |                                                                                                  | N/A                |      |                                    |            |            |         |              |                        |                      |                 |                                                                         |       | 5.0                        | ms    |

1. If RTSS-HE is powered down, then the LPCPI, LPI2S, LPPDM, and LPSPI in the same subsystem are also powered down.
2. WFI: Wait for Interrupt.
3. At ACLK = 400 MHz, HCLK = 200 MHz.
4. At ACLK = 200 MHz, HCLK = 100 MHz.
5. At ACLK = 100 MHz, HCLK = 50 MHz, PCLK = 25 MHz.
6. Wake interrupt source is LPTIMER.

### 5.2.3 Power Sequence

Figure 5-1 shows the power-up and power-down sequencing of the device.

**Figure 5-1 Power-Up/Power-Down Sequencing**



The following restrictions and considerations apply to [Figure 5-1 Power-Up/Power-Down Sequencing](#):

- The power supply ramp-up time (10% to 90%) on all power supply inputs to the device must be between 10  $\mu$ s and 1 ms.
- During power-up phase, VDD\_BATT must come up at the same time or before the other supplies.  
**CAUTION:** VDD\_BATT must not come up after the other supplies. Failure to do so may result in damage to the device or malfunction.
- VDD\_MAIN and VDD\_BUCK must be tied together.
- VDD\_IO\_1V8 and VDD\_IO\_FLEX can come up before or after VDD\_MAIN and VDD\_BUCK. They must come up at the same time or after VDD\_BATT. VDD\_IO\_1V8 and VDD\_IO\_FLEX do not need to be tied together.
- If USB function is used, VDD\_USB\_3V3 can come up before or after VDD\_MAIN and VDD\_BUCK. VDD\_USB\_3V3 must come up at the same time or after VDD\_BATT. If USB is not used, VDD\_USB\_3V3 must be tied to ground.
- During power-down phase, VDD\_BATT must come down at the same time or after the other supplies. All other power supplies can come down in any order.
- The low-frequency S32K\_CLK comes up after VDD\_BATT.
- The high-frequency HFOSC\_CLK comes up after the internal DC-DC converter is stable.

### NOTE

Inputs to the device (for example, NSRST, POR\_N, SEUART\_RX) must not be floating after power up.

An external brownout supervisor must be connected to VDD\_MAIN/VDD\_BUCK. The brownout supervisor must assert before voltage input to the chip falls below 1.65 V. Care (that is, sufficient decoupling) must be taken to ensure that supply noise/transients do not spuriously trigger resets. Please refer to the Alif Application Note AAPN0036, *PCB Layout Guidelines for Ensemble E4, E6, E8 MCUs and Fusion Processors*, for more details.

### CAUTION

The power supply ramp up and ramp down on all device supply pins must be monotonic. Failure to do so may result in damage to the device or malfunction.

Device pins must never be back-powered, meaning power must never be applied to a device pin before VDD\_BATT, VDD\_MAIN, VDD\_BUCK, VDD\_IO\_1V8, and VDD\_IO\_FLEX have been applied and are stable. Failure to do so may result in damage to the device or malfunction.

Any connection to a GPIO pin (GPIO0\_[7:0] through GPIO17\_[7:0], and GPIOV\_[7:0]) must come from a pin whose supply is powered by the same power source as VDD\_IO\_1V8 or VDD\_IO\_FLEX (GPIOs connecting to each other must be powered by the same VDD\_IO rail). Failure to do so may result in damage to the device or malfunction.

Outputs of the device (for example, VREG\_DIG\_1V8, SEUART\_TX, VREG\_AUX\_1\_1V8, VSW, LFXO\_N) must never be driven by external voltage. Failure to do so may result in damage to the device or malfunction.

The use of current sense resistors in series with supply pins is not recommended. Doing so may result in damage to the device or malfunction.

## 5.2.4 Reference Voltage Characteristics, VREF\_P as an Output

Table 5-6 presents reference voltage characteristics when VREF\_P is used as an output for other devices to use as a precision voltage reference.

**Table 5-6 Reference Voltage Characteristics**

| Parameter                   |                                                       | Conditions               | Min | Typ | Max | Unit   |
|-----------------------------|-------------------------------------------------------|--------------------------|-----|-----|-----|--------|
| V <sub>REFP_OUT</sub>       | Voltage reference output                              |                          | 1.7 | 1.8 | 1.9 | V      |
| TRIM                        | Trim step resolution                                  |                          |     | 6   | 7   | mV     |
| C <sub>LOAD</sub>           | Load capacitor                                        |                          | 0.8 | 1   |     | μF     |
| ESR                         | Equivalent series resistor of C <sub>LOAD</sub>       |                          |     |     | 0.2 | Ω      |
| I <sub>LOAD</sub>           | Static load current                                   |                          |     |     | 10  | mA     |
| I <sub>LINE_REG</sub>       | Line regulation                                       |                          |     | 100 | 400 | ppm/V  |
| T <sub>Coeff</sub>          | Temperature coefficient                               |                          |     | 50  |     | ppm/°C |
| PSRR                        | Power supply rejection ratio                          | DC                       | 40  | 60  |     | dB     |
|                             |                                                       | 100 kHz                  | 20  | 30  |     | dB     |
| t <sub>START</sub>          | Start-up time                                         |                          |     |     | 100 | μs     |
| I <sub>DDA(VREFP_OUT)</sub> | V <sub>REFBUF</sub> consumption from V <sub>DDA</sub> | I <sub>LOAD</sub> = 0 μA |     | 200 | 250 | μA     |

| Parameter | Conditions                | Min | Typ | Max | Unit |
|-----------|---------------------------|-----|-----|-----|------|
|           | $I_{LOAD} = 1 \text{ mA}$ |     | 1.2 |     | mA   |

### 5.2.5 Electrical Sensitivity Characteristics

Table 5-7 presents Electrostatic Discharge (ESD) characteristics of the device.

**Table 5-7 ESD Characteristics**

| Parameter          | Conditions                                        | Package                        | Value      | Unit    |
|--------------------|---------------------------------------------------|--------------------------------|------------|---------|
| ESD <sub>HBM</sub> | All pins except for ones listed in <sup>(1)</sup> | ESD Human Body Model (HBM)     | WLCSP/FBGA | ±2000 V |
| ESD <sub>CDM</sub> | All pins                                          | ESD Charged Device Model (CDM) | WLCSP/FBGA | ±250 V  |

1. ESD<sub>HBM</sub> for HFXO\_P, HFXO\_N, LFXO\_P, and LFXO\_N pins: ±1000 V

Table 5-8 presents latch-up characteristics of the device.

**Table 5-8 Latch-up Characteristics**

| Parameter | Conditions                                  | Value | Unit |
|-----------|---------------------------------------------|-------|------|
| $I_{LU}$  | Latch-Up current level<br>Per JEDEC JESD 78 | ±100  | mA   |

## 5.3 Clock Characteristics

### 5.3.1 External Clock Source Characteristics

Table 5-9 presents the HFXO external clock source characteristics.

**Table 5-9 External HFXO Clock Source Characteristics**

| Parameter | Min                                                 | Typ  | Max   | Unit |
|-----------|-----------------------------------------------------|------|-------|------|
| $f_c$     | Frequency                                           | 38.4 |       | MHz  |
| $C_{CS}$  | On chip shunt capacitance (programmable by SE only) | 4    | 20    | pF   |
| $I_{CC}$  | Current consumption at 3 V                          | 75   |       | μA   |
| $t_j$     | Period jitter                                       |      | 1     | ps   |
| $t_s$     | Start-up time                                       | 200  |       | μs   |
| $t_{acr}$ | Frequency accuracy                                  | 25   |       | ppm  |
| ESR       | Equivalent Series Resistance                        |      | < 100 | Ω    |

Table 5-10 presents the LFXO external clock source characteristics.

**Table 5-10 External LFXO Clock Source Characteristics**

| Parameter | Min                                      | Typ    | Max | Unit |
|-----------|------------------------------------------|--------|-----|------|
| $f_c$     | Frequency                                | 32.768 |     | kHz  |
| $C_{CS}$  | On chip shunt capacitance (programmable) | 2      | 18  | pF   |
| $I_{CC}$  | Current consumption at 3 V               | 150    |     | nA   |
| $t_s$     | Start-up time                            | 0.1    | 0.5 | s    |
| $t_{acr}$ | Frequency accuracy                       | 250    |     | ppm  |

### 5.3.2 Internal Clock Source Characteristics

Table 5-11 presents the HFRC internal clock source characteristics.

**Table 5-11 Internal HFRC Clock Source Characteristics**

| Parameter |                                                      | Min | Typ   | Max  | Unit |
|-----------|------------------------------------------------------|-----|-------|------|------|
| $f_c$     | Frequency at 25 °C and VDD_BATT = 3 V (uncalibrated) | 65  | 76.8  | 88.8 | MHz  |
| $f_{cs}$  | Calibration step                                     |     | 0.768 |      | MHz  |
| $t_s$     | Start-up time                                        |     | 0.5   | 1    | μs   |
| $t_j$     | Frequency variation over temperature and voltage     | -2  |       | 2    | %    |
| $I_{CC}$  | Current consumption                                  |     | 1.1   |      | μA   |
| $t_{pj}$  | RMS period jitter                                    |     | 42    |      | ps   |

Table 5-12 presents the LFRC internal clock source characteristics.

**Table 5-12 Internal LFRC Clock Source Characteristics**

| Parameter |                                                         | Min | Typ  | Max | Unit |
|-----------|---------------------------------------------------------|-----|------|-----|------|
| $f_c$     | Frequency at 25 °C and VDD_BATT = 3 V (factory trimmed) |     | 32.7 |     | kHz  |
| $t_j$     | Frequency variation over temperature and voltage        | -4  |      | 4   | %    |

### 5.3.3 PLL Characteristics

Table 5-13 presents the PLL characteristics.

**Table 5-13 PLL Characteristics**

| Parameter         |                                     | Min | Typ  | Max | Unit |
|-------------------|-------------------------------------|-----|------|-----|------|
| $f_{C\_IN}$       | Input clock frequency (HFXO only)   |     | 38.4 |     | MHz  |
| $f_{C\_OUT}$      | Output clock frequency              |     | 800  |     | MHz  |
| $t_{SET}$         | Settling time                       |     | 20   |     | μs   |
| $f_{DC}$          | Output clock duty cycle             |     | 50   |     | %    |
| $t_j(CLK)$        | Output clock jitter (period jitter) |     |      | 2   | ps   |
| $I_{CC}$          | Current consumption at 3 V supply   |     | 0.6  |     | mA   |
| $I_{CC}(PWR-DWN)$ | Power-down current consumption      |     |      | 0.1 | μA   |

### 5.3.4 Audio PLL Characteristics

Table 5-14 presents the Audio PLL characteristics.

**Table 5-14 Audio PLL Characteristics**

| Parameter    |                                   | Min | Typ | Max | Unit |
|--------------|-----------------------------------|-----|-----|-----|------|
| $f_{C\_IN}$  | Input clock frequency (HFXO only) |     |     |     | MHz  |
| $f_{C\_OUT}$ | Output clock frequency            |     |     |     | MHz  |
| $t_{SET}$    | Settling time                     |     |     |     | μs   |
| $f_{DC}$     | Output clock duty cycle           |     |     |     | %    |

| Parameter         |                                     | Min | Typ | Max | Unit    |
|-------------------|-------------------------------------|-----|-----|-----|---------|
| $t_{j(CLK)}$      | Output clock jitter (period jitter) |     |     |     | ps      |
| $I_{CC}$          | Current consumption at 3 V supply   |     |     |     | mA      |
| $I_{CC(PWR-DWN)}$ | Power-down current consumption      |     |     |     | $\mu$ A |

## 5.4 Memory Characteristics

Table 5-15 presents MRAM characteristics.

**Table 5-15 MRAM Characteristics**

| Parameter      |                          | Conditions                                                                                     | Min | Typ   | Max       | Unit    |
|----------------|--------------------------|------------------------------------------------------------------------------------------------|-----|-------|-----------|---------|
| $I_{MRAM}$     | MRAM current consumption | Write                                                                                          |     | 25.2  |           | mA      |
|                |                          | Read at 40 MHz                                                                                 |     | 10.4  |           | mA      |
|                |                          | Erase                                                                                          |     | 38.2  |           | mA      |
|                |                          | Power down                                                                                     |     | 19.19 |           | $\mu$ A |
| $N_{MRAMR}$    | Number of read cycles    |                                                                                                |     |       | Unlimited | Cycles  |
| $N_{MRAME}$    | Number of erase cycles   |                                                                                                |     |       | 100000    | Cycles  |
| $t_{MRAMW16}$  | Write time, non-DMA      | Write operation, 16 bytes (minimum number of bytes that can be written in one write operation) |     |       |           | $\mu$ s |
|                |                          | Effective write time and rate                                                                  |     |       |           | $\mu$ s |
|                |                          |                                                                                                |     |       |           | MB/s    |
| $t_{MRAMWDMA}$ | Write time, DMA          | DMA write operation, 128 bytes (maximum DMA cycle payload)                                     |     |       |           | $\mu$ s |
|                |                          | Effective write time and rate                                                                  |     |       |           | ns      |
|                |                          |                                                                                                |     |       |           | MB/s    |
| $t_{MRAMR16}$  | Read time                | Read operation, 16 bytes                                                                       |     |       |           | ns      |
|                |                          |                                                                                                |     |       |           | MB/s    |

Table 5-16 presents SRAM throughput characteristics.

**Table 5-16 SRAM Throughput Characteristics**

| Memory Block        | Achievable Read Throughput (MB/s) |                         |                         |                         |                         |                         | Achievable Write Throughput (MB/s) |                         |                         |                         |                         |                         |
|---------------------|-----------------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|------------------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|
|                     | Read Originating from:            |                         |                         |                         |                         |                         | Write Originating from:            |                         |                         |                         |                         |                         |
|                     | A32-0 or<br>A32-1 at<br>800 MHz   | M55-HP<br>at 400<br>MHz | M55-HE<br>at 160<br>MHz | NPU-HG<br>at 400<br>MHz | NPU-HP<br>at 400<br>MHz | NPU-HE<br>at 160<br>MHz | A32-0 or<br>A32-1 at<br>800 MHz    | M55-HP<br>at 400<br>MHz | M55-HE<br>at 160<br>MHz | NPU-HG<br>at 400<br>MHz | NPU-HP<br>at 400<br>MHz | NPU-HE<br>at 160<br>MHz |
| SRAM0 (Bulk)        | 3,066                             | 1,350                   | 558                     | 6,400 <sup>(1)</sup>    | 3,200                   | 1,280                   | 2,872                              | 1,824                   | 731                     | 6,400                   | 3,200                   | 1,280                   |
| SRAM1 (Bulk)        | 3,083                             | 1,350                   | 558                     | 6,400 <sup>(1)</sup>    | 3,200                   | 1,280                   | 2,587                              | 1,824                   | 731                     | 6,400                   | 3,200                   | 1,280                   |
| SRAM2 (M55-HP ITCM) | 1,420                             | 1,600                   | 545                     | 1,550                   | 1,500                   | 1,280                   | 1,600                              | 1,600                   | 731                     | 1,600                   | 1,600                   | 1,280                   |
| SRAM3 (M55-HP DTCM) | 2,486                             | 3,200                   | 553                     | 3,000                   | 2,840                   | 1,280                   | 2,551                              | 3,184                   | 731                     | 3,200                   | 3,200                   | 1,280                   |
| SRAM4 (M55-HE ITCM) | 569                               | 494                     | 640                     | 620                     | 600                     | 600                     | 640                                | 640                     | 640                     | 640                     | 640                     | 640                     |
| SRAM5 (M55-HE DTCM) | 1,022                             | 800                     | 1,280                   | 1,200                   | 1,130                   | 1,130                   | 1,280                              | 1,280                   | 1,278                   | 1,280                   | 1,280                   | 1,280                   |

1. Ethos-U85 can achieve up to 12,800 MB/s when reading SRAM0 and SRAM1 with memory striping enabled. Does not apply to writes.

## 5.5 I/O Buffer Characteristics

### 5.5.1 I/O Parameter Test Conditions

Unless otherwise specified, typical values are taken at  $t_a = 25^\circ\text{C}$  and typical supply voltages as specified in [Table 5-4 General Operating Conditions](#). Where statistical variation is relevant and unless otherwise specified, typical values represent parts at the mean of the distribution.

Unless otherwise specified the minimum and maximum values are taken across the full temperature and voltage range. Where statistical variation is relevant and unless otherwise specified, minimum and maximum values represent parts that are three standard deviations away from the mean of the distribution.

All values are based on laboratory characterization.

### 5.5.2 LVCMOS DC Specifications

[Table 5-17](#) presents the LVCMOS I/O DC specifications.

**Table 5-17 LVCMOS DC Specifications (1.8 V Logic)**

| Parameter     |                                     | Min                           | Typ | Max                           | Unit       |
|---------------|-------------------------------------|-------------------------------|-----|-------------------------------|------------|
| <b>Input</b>  |                                     |                               |     |                               |            |
| $V_{IH}$      | Input logic high voltage            | $0.65 \times V_{DD\_IO\_1V8}$ |     | $V_{DD\_IO\_1V8} + 0.3$       | V          |
| $V_{IL}$      | Input logic low voltage             | -0.3                          |     | $0.35 \times V_{DD\_IO\_1V8}$ | V          |
| $R_{pu}$      | Input pull-up resistance            |                               | 50  |                               | k $\Omega$ |
| $R_{pd}$      | Input pull-down resistance          |                               | 50  |                               | k $\Omega$ |
| <b>Output</b> |                                     |                               |     |                               |            |
| $V_{OH(DC)}$  | DC Output logic high voltage        | $V_{DD\_IO\_1V8} - 0.4$       |     |                               | V          |
| $V_{OL(DC)}$  | DC Output logic low voltage         |                               |     | 0.4                           | V          |
| $I_{OL}$      | Output drive current (programmable) |                               |     | 2, 4, 8, or 12                | mA         |

### 5.5.3 Dual-Voltage (Flex) LVCMOS DC Specifications

[Table 5-18](#) presents the dual-voltage (Flex) LVCMOS I/O DC specifications.

**Table 5-18 Dual-Voltage (Flex) LVCMOS DC Specifications (1.8 V / 3.3 V Logic)**

| Parameter     |                              | Min                                  | Typ | Max                                  | Unit       |
|---------------|------------------------------|--------------------------------------|-----|--------------------------------------|------------|
| <b>Input</b>  |                              |                                      |     |                                      |            |
| $V_{IH}$      | Input logic high voltage     | $0.65 \times V_{DD\_IO\_FLEX}^{(1)}$ |     | $V_{DD\_IO\_FLEX}^{(1)} + 0.3$       | V          |
| $V_{IL}$      | Input logic low voltage      | -0.3                                 |     | $0.35 \times V_{DD\_IO\_FLEX}^{(1)}$ | V          |
| $R_{pu}$      | Input pull-up resistance     |                                      | 50  |                                      | k $\Omega$ |
| $R_{pd}$      | Input pull-down resistance   |                                      | 50  |                                      | k $\Omega$ |
| <b>Output</b> |                              |                                      |     |                                      |            |
| $V_{OH(DC)}$  | DC Output logic high voltage | $V_{DD\_IO\_FLEX}^{(1)} - 0.4$       |     |                                      | V          |
| $V_{OL(DC)}$  | DC Output logic low voltage  |                                      |     | 0.4                                  | V          |

| Parameter |                                     | Min | Typ | Max            | Unit |
|-----------|-------------------------------------|-----|-----|----------------|------|
| $I_{OL}$  | Output drive current (programmable) |     |     | 2, 4, 8, or 12 | mA   |

1. The voltage supply can be 1.8 V or 3.3 V.

#### 5.5.4 MIPI CSI DC Specifications

The CSI interface (CSIPHY port type) electrical characteristics are compliant with MIPI Alliance Specification for D-PHY, Version 1.2.

#### 5.5.5 MIPI DSI DC Specifications

The DSI interface (DSIPHY port type) electrical characteristics are compliant with MIPI Alliance Specification for D-PHY v1.2.

#### 5.5.6 USB DC Specifications

The USB interface (USBPHY port type) electrical characteristics are compliant with Universal Serial Bus Specification Revision 2.0.

### 5.6 Analog Peripherals Characteristics

#### 5.6.1 ADC Characteristics

Table 5-19 presents the ADC12 electrical characteristics.

**Table 5-19 ADC12 Electrical Characteristics**

| Parameter |                           | Conditions                                                             |              | Min                                         | Typ  | Max   | Unit |
|-----------|---------------------------|------------------------------------------------------------------------|--------------|---------------------------------------------|------|-------|------|
| RES       | Resolution                | Internal ADC voltage supply = 1.8 V from external 3.3 V supply (DC-DC) |              |                                             | 12   |       | Bits |
| $f_s$     | Operational speed         |                                                                        |              | 312                                         |      | 5000  | kHz  |
| $E_G$     | Gain error (calibrated)   |                                                                        |              |                                             | 6.1  |       | LSB  |
| $E_O$     | Offset error              |                                                                        |              |                                             | 0.41 |       | LSB  |
| $E_L$     | Integral nonlinearity     |                                                                        |              |                                             |      | 3     | LSB  |
| $E_D$     | Differential nonlinearity |                                                                        |              |                                             |      | 2     | LSB  |
| ENOB      | Effective number of bits  | Internal ADC voltage reference = 1.8 V                                 | Single-ended | 1.25 MSPS (2.5 MHz, Ave <sup>(1)</sup> = 2) |      | 9.25  | Bits |
|           |                           |                                                                        |              | 0.5 MSPS (1 MHz, Ave = 2)                   |      | 9.65  |      |
|           |                           |                                                                        |              | 1.0 MSPS (5 MHz, Ave = 4)                   |      | 10.00 |      |
|           |                           |                                                                        |              | 0.625 MSPS (2.5 MHz, Ave = 4)               |      | 10.00 |      |
|           |                           |                                                                        |              | 0.25 MSPS (1 MHz, Ave = 4)                  |      | 10.15 |      |
|           |                           | Ambient temperature = 25 °C                                            | Differential | 1.25 MSPS (2.5 MHz, Ave = 2)                |      | 10.25 |      |
|           |                           |                                                                        |              | 0.5 MSPS (1 MHz, Ave = 2)                   |      | 10.50 |      |
|           |                           |                                                                        |              | 1.0 MSPS (5 MHz, Ave = 4)                   |      | 11.00 |      |
|           |                           |                                                                        |              | 0.625 MSPS (2.5 MHz, Ave = 4)               |      | 11.00 |      |
|           |                           |                                                                        |              | 0.25 MSPS (1 MHz, Ave = 4)                  |      | 11.25 |      |
| SNR       | Signal-to-noise ratio     |                                                                        | Single-ended | 1.25 MSPS (2.5 MHz, Ave = 2)                |      | 58.8  | dB   |

| Parameter | Conditions                | Min             | Typ   | Max  | Unit |
|-----------|---------------------------|-----------------|-------|------|------|
| $T_{HD}$  | Total harmonic distortion | Differential    | 64.8  |      | dB   |
|           |                           | Single-ended    | -63.3 |      |      |
|           |                           | Differential    | -68.8 |      |      |
| $I_{DDA}$ | Current consumption       | $f_s = 5$ MHz   | 0.50  | 0.80 | mA   |
|           |                           | $f_s = 2.5$ MHz | 0.30  | 0.47 |      |

1. Ave: Averaging factor

Table 5-20 presents the ADC24 electrical characteristics.

**Table 5-20 ADC24 Electrical Characteristics**

| Parameter | Conditions                | Min     | Typ  | Max | Unit     |
|-----------|---------------------------|---------|------|-----|----------|
| RES       | Resolution                |         | 24   |     | Bits     |
| $f_s$     | Sampling rate             | 1       |      | 16  | kSPS     |
| $E_G$     | Gain error                |         | 1.5  |     | % of FSR |
| $E_O$     | Offset error              |         | 50   |     | $\mu$ V  |
| $T_{HD}$  | Total harmonic distortion | 1 kSPS  | -80  |     | dB       |
|           |                           | 16 kSPS | -74  |     |          |
| SNR       | Signal to noise ratio     | 1 kSPS  | 106  |     | dB       |
|           |                           | 16 kSPS | 93.5 |     |          |
| $I_{DDA}$ | Current consumption       |         | 0.45 | 1.0 | mA       |

## 5.6.2 DAC12 Characteristics

Table 5-21 presents the DAC12 electrical characteristics.

**Table 5-21 DAC12 Electrical Characteristics**

| Parameter | Conditions                | Min                   | Typ  | Max | Unit     |
|-----------|---------------------------|-----------------------|------|-----|----------|
| RES       | Resolution                |                       | 12   |     | Bits     |
| $f_c$     | Conversion rate           |                       |      | 1.0 | kHz      |
| $I_{OUT}$ | Output drive current      | High-performance mode |      | 1.5 | mA       |
| $E_G$     | Gain error                | High-performance mode | 1.5  |     | % of FSR |
|           |                           | Low-power mode        | 1.5  |     |          |
| $E_{Off}$ | Offset error              | High-performance mode | 0.14 |     | % of FSR |
|           |                           | Low-power mode        | 0.01 |     |          |
| $I_{DDA}$ | Current consumption       | High-performance mode | 2.0  |     | mA       |
|           |                           | Low-power mode        | 150  |     | $\mu$ A  |
| INL       | Integral nonlinearity     | High-performance mode | -2   | 3.2 | LSB      |
|           |                           | Low-power mode        | -1.5 | 2.6 |          |
| DNL       | Differential nonlinearity | High-performance mode | -2.2 | 1.5 | LSB      |
|           |                           | Low-power mode        | -1.1 | 1.8 |          |

### 5.6.3 CMP Characteristics

Table 5-22 presents the high-speed comparator electrical characteristics.

**Table 5-22 CMP Electrical Characteristics**

| Parameter        | Conditions                     | Min                                                         | Typ | Max                  | Unit    |
|------------------|--------------------------------|-------------------------------------------------------------|-----|----------------------|---------|
| $V_{IN}$         | Comparator input voltage range | -0.3                                                        |     | $V_{DD}^{(1)} + 0.3$ | V       |
| $V_{OFFSET\_IN}$ | Input offset                   | Full common mode range                                      |     | 20                   | mV      |
| $I_{CC}$         | Current consumption            | High-speed mode                                             |     | 200                  | $\mu A$ |
| $V_{HYS}$        | Hysteresis                     | $0.7\text{ V} \leq V_{in} \leq V_{DD}^{(1)} - 0.7\text{ V}$ | 5   | 30                   | mV      |
| $I_{bias}$       | Comparator input bias current  |                                                             |     | 10                   | nA      |
| $t_{RES}$        | Response time                  | High-speed mode                                             |     | 5                    | ns      |

1. Power supply from LDO-5. For more information on configuration, refer to the CMP\_COMP\_REG2[ANA\_PERIPH\_LDO\_CONT] register field in the corresponding series-specific Hardware Reference Manual.

### 5.6.4 LPCMP Characteristics

Table 5-23 presents the low power comparator electrical characteristics.

**Table 5-23 LPCMP Electrical Characteristics**

| Parameter        | Conditions                              | Min                                                    | Typ | Max             | Unit    |
|------------------|-----------------------------------------|--------------------------------------------------------|-----|-----------------|---------|
| $V_{DDA}$        | Analog supply voltage (from VDD_IO_1V8) | 1.62                                                   | 1.8 | 1.98            | V       |
| $V_{IN}$         | Comparator input voltage range          | -0.3                                                   |     | $V_{DDA} + 0.3$ | V       |
| $V_{OFFSET\_IN}$ | Input offset                            | Full common mode range                                 |     | 20              | mV      |
| $I_{CC}$         | Current consumption                     | Low power mode                                         |     | 20              | $\mu A$ |
| $V_{HYS}$        | Hysteresis                              | $0.7\text{ V} \leq V_{in} \leq V_{DDA} - 0.7\text{ V}$ | 5   | 30              | mV      |
| $I_{bias}$       | Comparator input bias current           |                                                        |     | 10              | nA      |
| $t_{RES}$        | Response time                           | Low power mode                                         |     | 10              | $\mu s$ |

## 5.7 Timing Characteristics

### 5.7.1 Timing Test Conditions

Table 5-24 shows general description of used symbols, adopted standards, terminology, and test process. Unless otherwise specified, all timing parameters are characterized assuming load capacitance of 10 pF.

**Table 5-24 Timing Test Conditions**

| Parameter        | Description                                                     |
|------------------|-----------------------------------------------------------------|
| $f_{op}$         | Operating frequency                                             |
| $t_c$            | Cycle time (period)                                             |
| $t_d$            | Delay time                                                      |
| $t_{dsbl}$       | Disable time                                                    |
| $t_{en}$         | Enable time                                                     |
| $t_h$            | Hold time                                                       |
| $t_s$            | Setup time                                                      |
| $t_{tr}$         | Transition time                                                 |
| $t_v$            | Valid time                                                      |
| $t_{pd}$         | Pulse duration                                                  |
| $t_F$            | Fall time                                                       |
| $t_R$            | Rise time                                                       |
| $V_{OH}$         | High-level output voltage                                       |
| $V_{OL}$         | Low-level output voltage                                        |
| $V_{IH}$         | High-level input voltage                                        |
| $V_{IL}$         | Low-level input voltage                                         |
| $V_{REF}$        | Reference voltage                                               |
| $t_{RES}$        | Timer resolution time                                           |
| RES              | Timer resolution                                                |
| $t_{P\_COUNTER}$ | Counter clock period                                            |
| $t_{MAX\_COUNT}$ | Maximum possible count                                          |
| $f_{(baud)}$     | Maximum programmable baud rate                                  |
| $t_{(BUF)}$      | Bus free time                                                   |
| start            | Start bit                                                       |
| $C_b$            | Capacitive load                                                 |
| Dc               | Duty cycle                                                      |
| JIT              | Jitter                                                          |
| $t_{CAS}$        | Clock after START condition                                     |
| $t_{CBT}$        | Clock before STOP condition                                     |
| $t_{CASr}$       | Clock after repeated START                                      |
| $t_{CBSr}$       | Clock before repeated START                                     |
| $t_{MMOvrLAP}$   | Current master to secondary master overlap time during hand off |
| $t_{MMLOCK}$     | Time interval where new master not driving SDA low              |
| $t_{BAC}$        | Bus available condition                                         |
| $T_{BIC}$        | Bus idle condition                                              |

## 5.7.2 Timers and Counters

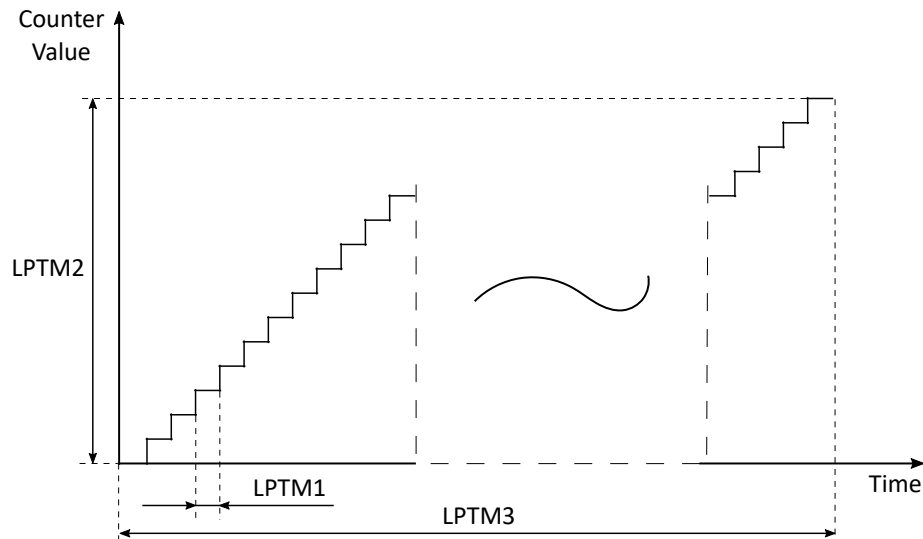
### 5.7.2.1 LPTIMER Timing Characteristics

Table 5-25 and Figure 5-2 present the LPTIMER timing characteristics.

**Table 5-25 LPTIMER Timing Characteristics**

| No                                                                                                                            | Parameter        | Min | Typ  | Max          | Unit          |
|-------------------------------------------------------------------------------------------------------------------------------|------------------|-----|------|--------------|---------------|
| <b>Condition: <math>f_{LPTIM\_CLK} = 128\text{ kHz}</math> (see Table 5-12 Internal LFRC Clock Source Characteristics)</b>    |                  |     |      |              |               |
| LPTM1                                                                                                                         | $t_{RES}$        |     | 7.8  |              | $\mu\text{s}$ |
| LPTM2                                                                                                                         | $t_{P\_COUNTER}$ | 1   |      | $2^{32} - 1$ | counts        |
| LPTM3                                                                                                                         | $t_{MAX\_COUNT}$ |     |      | 32000        | s             |
| <b>Condition: <math>f_{LPTIM\_CLK} = 32.768\text{ kHz}</math> (see Table 5-10 External LFXO Clock Source Characteristics)</b> |                  |     |      |              |               |
| LPTM1                                                                                                                         | $t_{RES}$        |     | 30.5 |              | $\mu\text{s}$ |
| LPTM2                                                                                                                         | $t_{P\_COUNTER}$ | 1   |      | $2^{32} - 1$ | counts        |
| LPTM3                                                                                                                         | $t_{MAX\_COUNT}$ |     |      | 120000       | s             |

**Figure 5-2 LPTIMER Timing Diagram**



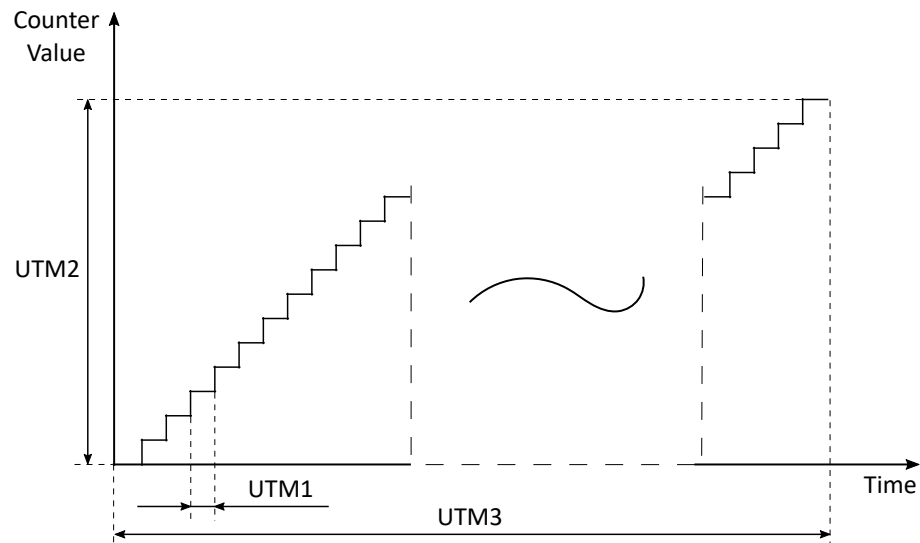
### 5.7.2.2 UTIMER Timing Characteristics

Table 5-26 and Figure 5-3 present the UTIMER timing characteristics.

**Table 5-26 UTIMER Timing Characteristics**

| No                                                            | Parameter        | Min                | Typ | Max          | Unit   |
|---------------------------------------------------------------|------------------|--------------------|-----|--------------|--------|
| <b>Condition: <math>f_{UTIM\_CLK} = 400\text{ MHz}</math></b> |                  |                    |     |              |        |
| UTM1                                                          | $t_{RES}$        |                    | 2.5 |              | ns     |
| UTM2                                                          | $t_{P\_COUNTER}$ | 1                  |     | $2^{32} - 1$ | counts |
| UTM3                                                          | $t_{PERIOD}$     | $5 \times 10^{-9}$ |     | 10.74        | s      |

Figure 5-3 UTIMER Timing Diagram



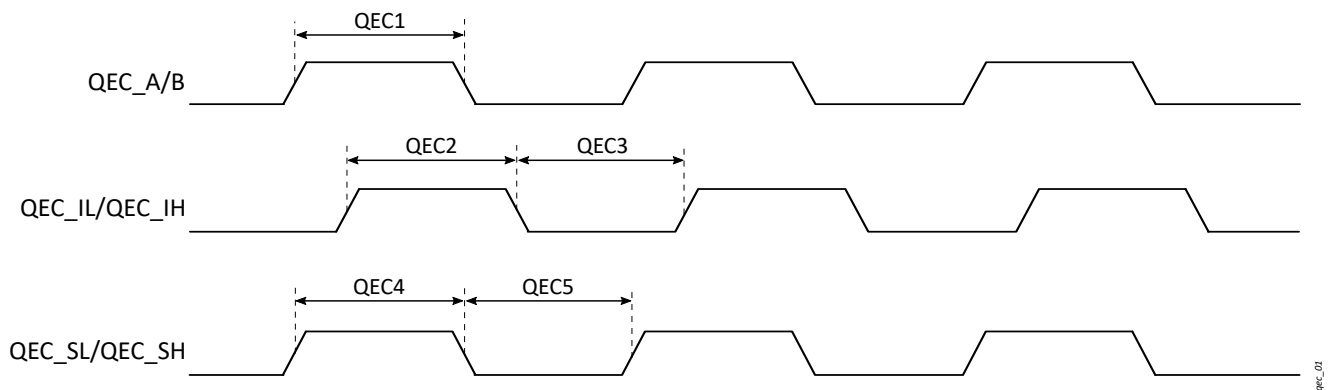
### 5.7.2.3 QEC Timing Characteristics

Table 5-27 and Figure 5-4 present the QEC timing characteristics.

Table 5-27 QEC Timing Characteristics

| No   | Parameter         |                                                 | Min | Max | Unit |
|------|-------------------|-------------------------------------------------|-----|-----|------|
| QEC1 | $t_{pd\_QEC\_in}$ | Pulse duration, QEC input                       | 10  |     | ns   |
| QEC2 | $t_{pd\_QEC-IH}$  | Pulse duration, QEC index input high            | 10  |     | ns   |
| QEC3 | $t_{pd\_QEC-IL}$  | Pulse duration, QEC index input low             | 10  |     | ns   |
| QEC4 | $t_{pd\_QEC-SH}$  | Pulse duration, QEC strobe high                 | 10  |     | ns   |
| QEC5 | $t_{pd\_QEC-SL}$  | Pulse duration, QEC strobe low                  | 10  |     | ns   |
| QEC6 | $t_{d\_QEC-CNTR}$ | Delay time, external clock to counter increment |     | 20  | ns   |

Figure 5-4 QEC Timing Diagram



### 5.7.3 Communication Peripherals

#### 5.7.3.1 CANFD Timing Characteristics

Table 5-28 presents the CANFD timing characteristics.

**Table 5-28 CANFD Timing Characteristics**

| No   | Parameter           |                                               | Min | Max | Unit |
|------|---------------------|-----------------------------------------------|-----|-----|------|
| CAN1 | $f_{(\text{baud})}$ | Maximum programmable baud rate                |     | 10  | Mbps |
| CAN2 | $t_{d\_shift\_TX}$  | Delay time, transmit shift register to Tx pin |     | 10  | ns   |
| CAN3 | $t_{d\_RX\_shift}$  | Delay time, Rx pin to receive shift register  |     | 30  | ns   |

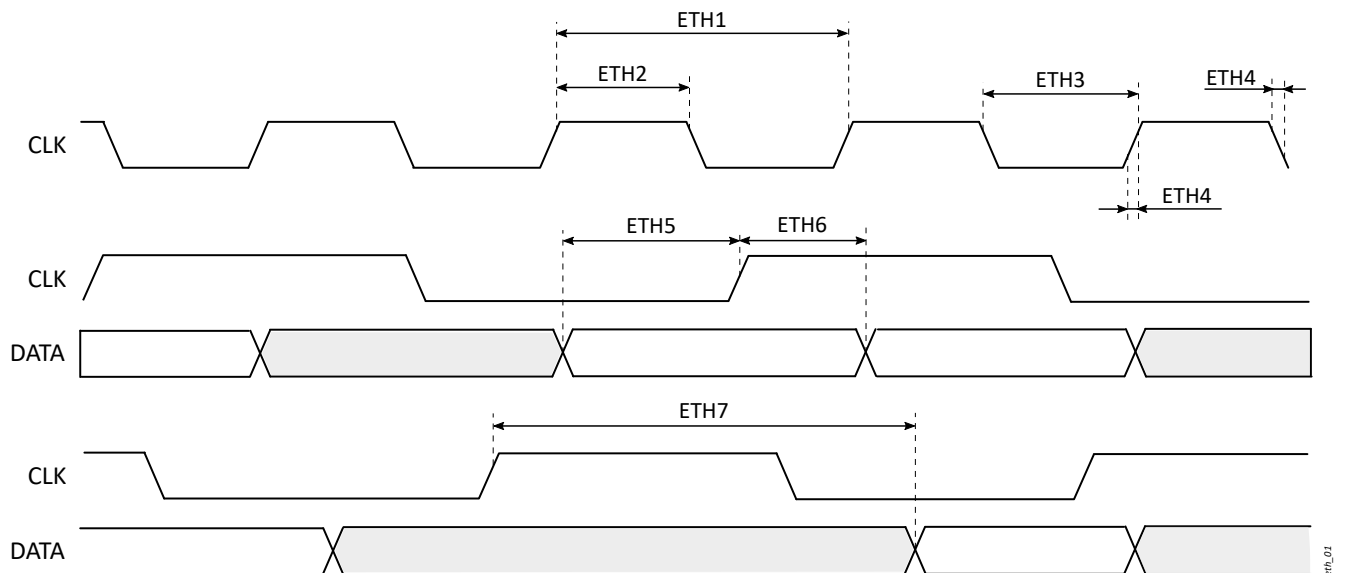
#### 5.7.3.2 ETH Timing Characteristics

Table 5-29 and Figure 5-5 present the ETH RMII timing characteristics

**Table 5-29 ETH RMII Timing Characteristics**

| No   | Parameter            |                                        | Min | Typ | Max | Unit |
|------|----------------------|----------------------------------------|-----|-----|-----|------|
| ETH1 | $t_{c\_CLK}$         | Cycle time, CLK                        |     | 20  |     | ns   |
| ETH2 | $t_{pd\_CLK-H}$      | Pulse duration, CLK high               | 9   | 10  | 11  | ns   |
| ETH3 | $t_{pd\_CLK-L}$      | Pulse duration, CLK low                | 9   | 10  | 11  | ns   |
| ETH4 | $t_{tr\_CLK}$        | Transition time, CLK                   |     |     | 1   | ns   |
| ETH5 | $t_{s\_DATA\_CLK-H}$ | Setup time, DATA valid before CLK high | 4   |     |     | ns   |
| ETH6 | $t_{h\_DATA\_CLK-H}$ | Hold time, DATA valid after CLK high   | 2   |     |     | ns   |
| ETH7 | $t_{d\_CLK-L\_DATA}$ | Delay time, CLK high to DATA valid     | 7   | 10  | 13  | ns   |

**Figure 5-5 ETH Timing Diagram**



#### 5.7.3.3 I2C Timing Characteristics

Table 5-30 and Figure 5-6 present the I2C timing characteristics.

Table 5-30 I2C Timing Characteristics

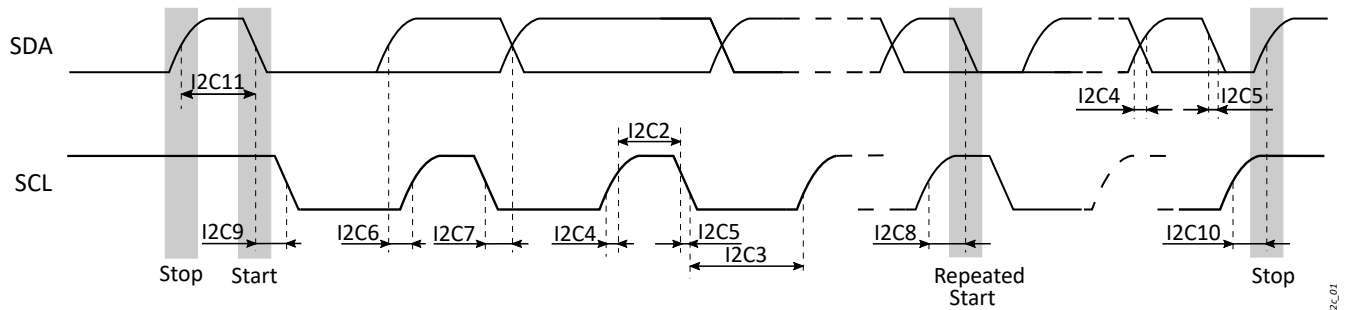
| No    | Parameter                   |                                                | SS <sup>(2)</sup>             |       | FS <sup>(2)</sup>             |       | FM+ <sup>(3)</sup>            |       | HS <sup>(3)</sup> |     | Unit |
|-------|-----------------------------|------------------------------------------------|-------------------------------|-------|-------------------------------|-------|-------------------------------|-------|-------------------|-----|------|
|       |                             |                                                | Min                           | Max   | Min                           | Max   | Min                           | Max   | Min               | Max |      |
|       | t <sub>c_SCL</sub>          | Cycle time                                     | 10                            |       | 2.5                           |       | 1                             |       |                   |     | μs   |
| I2C2  | t <sub>pd_SCL-H</sub>       | Pulse duration, SCL high                       |                               | 0.450 |                               | 1.320 |                               | 0.500 |                   |     | μs   |
| I2C3  | t <sub>pd_SCL-L</sub>       | Pulse duration, SCL low                        |                               | 0.450 |                               | 1.320 |                               | 0.500 |                   |     | μs   |
| I2C4  | t <sub>R_SDA_SCL</sub>      | Rise time of SDA and SCL signals               | 20                            | 300   | 20                            | 300   | 20                            | 120   |                   |     | ns   |
| I2C5  | t <sub>F_SDA_SCL</sub>      | Fall time of SDA and SCL signals               | See table note <sup>(1)</sup> | 300   | See table note <sup>(1)</sup> | 300   | See table note <sup>(1)</sup> | 120   |                   |     | ns   |
| I2C6  | t <sub>s_SDA_SCL</sub>      | Setup time, SDA to SCL                         |                               | 0.1   |                               | 0.1   |                               | 0.1   |                   |     | μs   |
| I2C7  | t <sub>h_SDA_SCL</sub>      | Hold time, SDA to SCL                          |                               |       |                               |       |                               |       |                   |     | μs   |
| I2C8  | t <sub>s_SCL_start</sub>    | Setup time, SCL to repeated START condition    |                               | 0.6   |                               | 0.26  |                               | 0.26  |                   |     | μs   |
| I2C9  | t <sub>h_start_SCL</sub>    | Hold time, START condition to SCL              |                               | 0.6   |                               | 0.26  |                               | 0.26  |                   |     | μs   |
| I2C10 | t <sub>h_SCL_stop</sub>     | Setup time, SCL to STOP condition              |                               | 0.6   |                               | 0.26  |                               | 0.26  |                   |     | μs   |
| I2C11 | t <sub>BUF_start_stop</sub> | Bus free time between STOP and START condition |                               | 1.3   |                               | 0.5   |                               | 0.5   |                   |     | μs   |
|       | C <sub>b_bus</sub>          | Capacitive load for each bus line              |                               | 50    |                               | 50    |                               | 50    |                   | 100 | pF   |

1.  $20 \times (VDD\_IO\_1V8 \div 5.5\text{ V})$ 

2. Supported by I2C and LPI2C modules

3. Supported only by I2C modules

Figure 5-6 I2C Timing Diagram



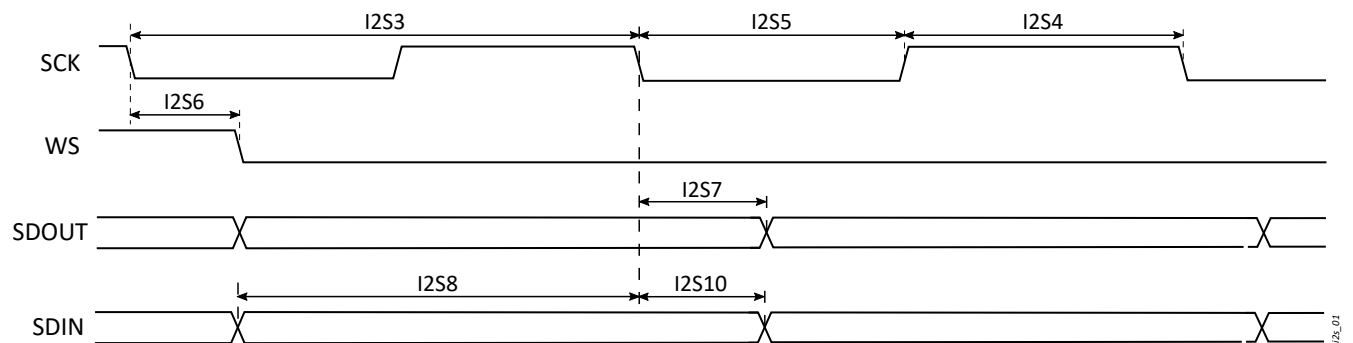
### 5.7.3.4 I2S Timing Characteristics

Table 5-31 and Figure 5-7 present the I2S timing characteristics.

Table 5-31 I2S Timing Characteristics

| No    | Parameter             |                                           | Min  | Typ | Max                     | Unit |
|-------|-----------------------|-------------------------------------------|------|-----|-------------------------|------|
|       | $f_{op\_SCK}$         | Operation frequency, SCK (serial clock)   | 2.27 | 2.5 | 2.78                    | MHz  |
| I2S3  | $t_{c\_SCK}$          | Cycle time, SCK (serial clock)            | 440  | 400 | 360                     | ns   |
| I2S4  | $t_{pd\_SCK-H}$       | Pulse duration, SCK high                  | 160  |     |                         | ns   |
| I2S5  | $t_{pd\_SCK-L}$       | Pulse duration, SCK low                   | 160  |     |                         | ns   |
| I2S6  | $t_{d\_SCK\_WS}$      | Delay time, SCK output low to WS valid    |      |     | $0.8 \times t_{c\_SCK}$ | ns   |
| I2S7  | $t_{d\_SCK\_SDOUT}$   | Delay time, SCK output low to SDOUT valid |      |     | $0.8 \times t_{c\_SCK}$ | ns   |
| I2S8  | $t_{s\_SDIN\_master}$ | Setup time, SDIN master mode              | 60   |     |                         | ns   |
| I2S9  | $t_{s\_SDIN\_slave}$  | Setup time, SDIN slave mode               | 60   |     |                         | ns   |
| I2S10 | $t_{h\_SDIN\_master}$ | Hold time, SDIN master mode               | 100  |     |                         | ns   |
| I2S11 | $t_{h\_SDIN\_slave}$  | Hold time, SDIN slave mode                | 0    |     |                         | ns   |

Figure 5-7 I2S Master Mode Timing Diagram



### 5.7.3.5 I3C Timing Characteristics

Table 5-32, Table 5-33, Figure 5-8, and Figure 5-9 present the I3C timing characteristics.

Table 5-32 I3C Open Drain Timing Characteristics

| No    | Parameter       |                                                                 | Mode   | Min    | Max | Unit |
|-------|-----------------|-----------------------------------------------------------------|--------|--------|-----|------|
| I3C1  | $t_{pd\_SCL-L}$ | Pulse duration, SCL low                                         | Master | 200    |     | ns   |
| I3C2  | $t_{pd\_SCL-H}$ | Pulse duration, SCL high                                        | Master | 200    |     | ns   |
| I3C3  | $t_{F\_SDA}$    | Fall time, SDA                                                  | Master |        | 11  | ns   |
| I3C4  | $t_{s\_SDA-OD}$ | Setup time, SDA open drain                                      | Master | 3      |     | ns   |
| I3C5  | $t_{CAS}$       | Clock after START condition                                     | Master | 38.4   |     | ns   |
| I3C6  | $t_{CBT}$       | Clock before STOP condition                                     | Master | 19.2   |     | ns   |
| I3C7  | $t_{MMOvrLAP}$  | Current master to secondary master overlap time during hand off | Master | 212    |     | ns   |
| I3C8  | $t_{BAC}$       | Bus available condition                                         | Master | 1000   |     | ns   |
| I3C9  | $T_{BIC}$       | Bus idle condition                                              | Master | 200000 |     | ns   |
| I3C10 | $t_{MMLOCK}$    | Time interval where new master not driving SDA Low              | Master | 1000   |     | ns   |

Table 5-33 I3C Push-Pull Timing Characteristics

| NO.  | PARAMETER |                 | MODE   | MIN    | MAX   | UNIT |
|------|-----------|-----------------|--------|--------|-------|------|
| I3C1 | $t_c$     | Cycle time, SCL | Master | 100000 | 77.52 | ns   |

| NO.   | PARAMETER         |                                        | MODE                | MIN  | MAX | UNIT |
|-------|-------------------|----------------------------------------|---------------------|------|-----|------|
| I3C2  | $t_{pd\_SCL-L}$   | Pulse duration, SCL low                | Master              | 32   |     | ns   |
| I3C4  | $t_{pd\_SCL-H}$   | Pulse duration, SCL high               | Master              | 32   |     | ns   |
| I3C5  | $t_{d\_SCL\_SDA}$ | Delay time, SCL to SDA out             | Master              |      | 12  | ns   |
| I3C6  | $t_{R\_SCL}$      | Rise time, SCL                         | Master              |      | 12  | ns   |
| I3C7  | $t_{F\_SCL}$      | Fall time, SCL                         | Master              |      | 12  | ns   |
| I3C8  | $t_{h\_SDA}$      | Hold time, SDA                         | Master in push-pull | 15   |     | ns   |
| I3C9  | $t_{s\_SDA}$      | Setup time, SDA                        | Master in push-pull | 15   |     | ns   |
| I3C10 | $t_{CASr}$        | Clock after repeated START             | Master              | 19.2 |     | ns   |
| I3C11 | $t_{CBSr}$        | Clock before repeated START            | Master              | 19.2 |     | ns   |
|       | $C_b$             | Capacitive load per bus line (SDA/SCL) | Master, Slave       | 50   |     | pf   |

Figure 5-8 I3C Open Drain Timing Diagram

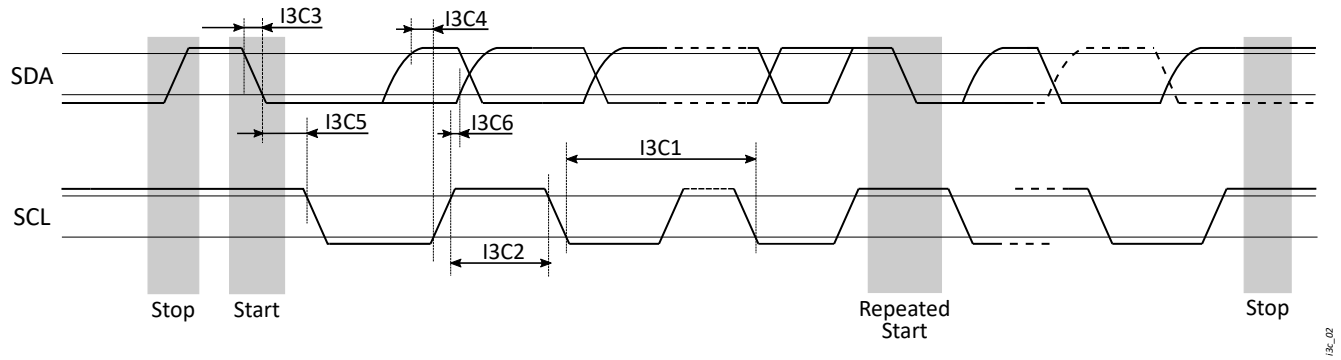
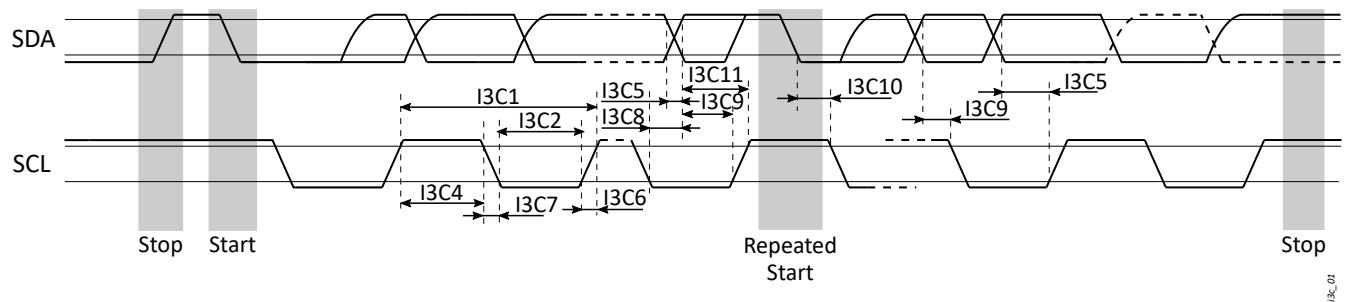


Figure 5-9 I3C Push-Pull Timing Diagram



### 5.7.3.6 PDM Timing Characteristics

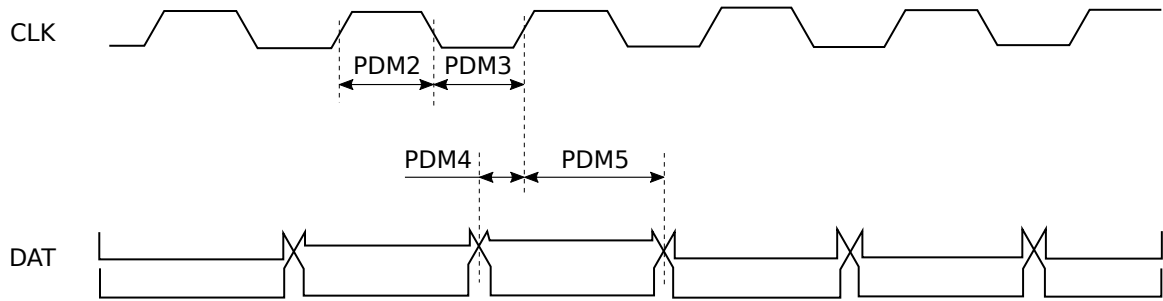
Table 5-34 and Figure 5-10 present the PDM timing characteristics.

Table 5-34 PDM Timing Characteristics

| No   | Parameter       |                              | Min   | Typ  | Max | Unit                       |
|------|-----------------|------------------------------|-------|------|-----|----------------------------|
|      | $f_{OP}$        | Operating frequency, PDM_CLK | 0.128 |      | 4.8 | MHz                        |
| PDM2 | $t_{W\_CLK\_H}$ | Pulse duration, CLK high     |       | 48.4 |     | % of total $f_{OP}$ period |

| No   | Parameter       |                         | Min | Typ  | Max | Unit                       |
|------|-----------------|-------------------------|-----|------|-----|----------------------------|
| PDM3 | $t_{W\_CLK\_L}$ | Pulse duration, CLK low |     | 48.4 |     | % of total $f_{OP}$ period |
| PDM4 | $t_{SU\_DAT}$   | Setup time, DAT         | 65  |      |     | ns                         |
| PDM5 | $t_{H\_DAT}$    | Hold time, DAT          | 0   |      |     | ns                         |

Figure 5-10 PDM Timing Diagram



### 5.7.3.7 SPI Timing Characteristics

Table 5-35, Figure 5-11, and Figure 5-12 present the SPI timing characteristics.

Table 5-35 SPI Timing Characteristics

| No   | Parameter           |                           | Min                       | Typ | Max | Unit |
|------|---------------------|---------------------------|---------------------------|-----|-----|------|
| SP1  | $t_{c\_SCLK}$       | Cycle time, SCLK          | SPI                       | 20  |     | ns   |
|      |                     |                           | LPSPi                     | 25  |     | ns   |
| SP2  | $t_{R\_SCLK}$       | Rise time, SCLK           |                           |     | 3   | ns   |
| SP3  | $t_{F\_SCLK}$       | Fall time, SCLK           |                           |     | 3   | ns   |
| SP4  | $t_{pd\_CLK-L}$     | Pulse duration, SCLK low  | $0.45 \times t_{c\_SCLK}$ |     |     | ns   |
| SP5  | $t_{pd\_CLK-H}$     | Pulse duration, SCLK high | $0.45 \times t_{c\_SCLK}$ |     |     | ns   |
| SP6  | $t_{s\_SS}$         | Setup time, SS            |                           |     | 3   | ns   |
| SP7  | $t_{h\_SS}$         | Hold time, SS             | 0.5                       | 0.6 | 0.8 | ns   |
| SP8  | $t_{s\_MISO\_SCLK}$ | Setup time, MISO to SCLK  | 3                         |     |     | ns   |
| SP9  | $t_{h\_MISO\_SCLK}$ | Hold time, MISO to SCLK   | 3                         |     |     | ns   |
| SP10 | $t_{d\_MOSI\_SS}$   | Delay time, MOSI to SS    | 3                         |     |     | ns   |
| SP11 | $t_{d\_MOSI\_SCLK}$ | Delay time, MOSI to SCLK  | 3                         |     |     | ns   |

Figure 5-11 SPI Receive Timing Diagram

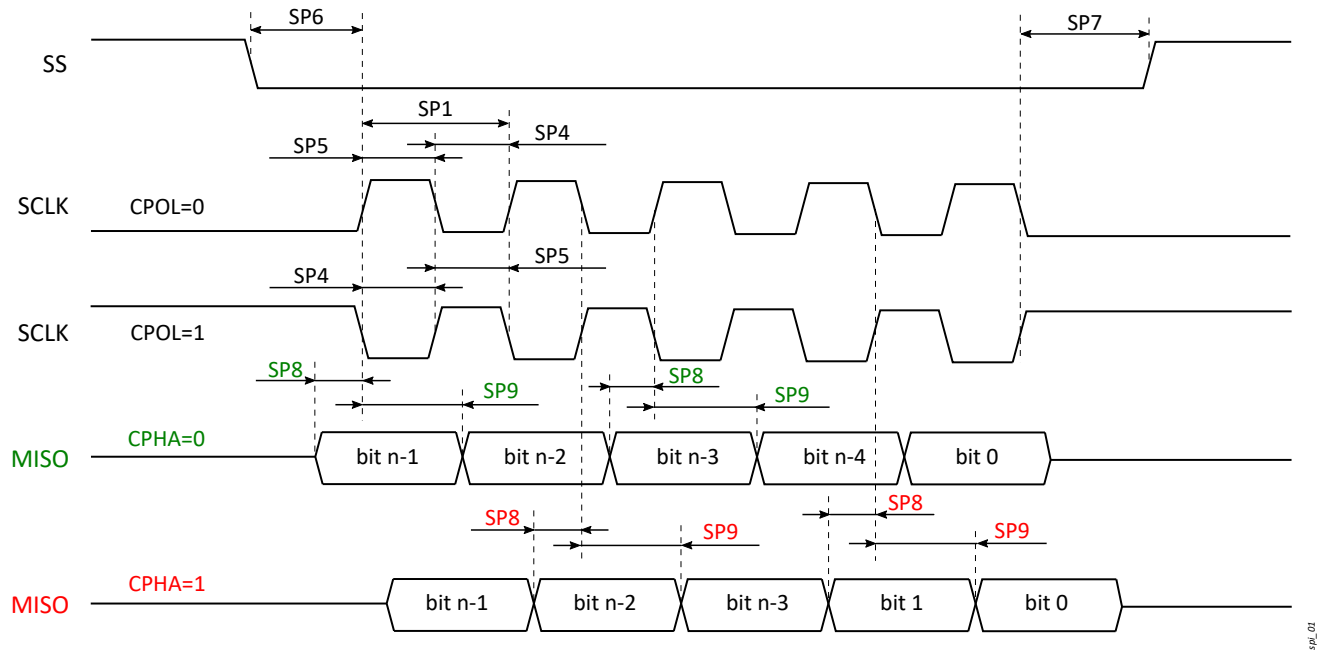
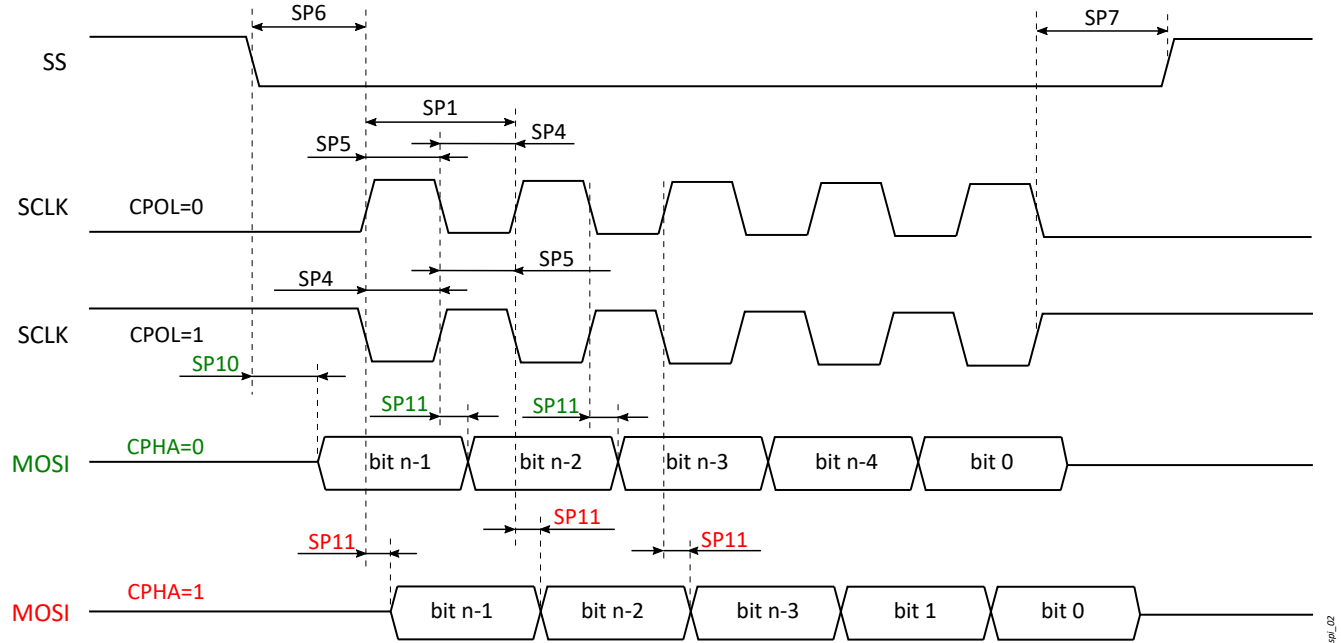


Figure 5-12 SPI Transmit Timing Diagram



### 5.7.3.8 UART Timing Characteristics

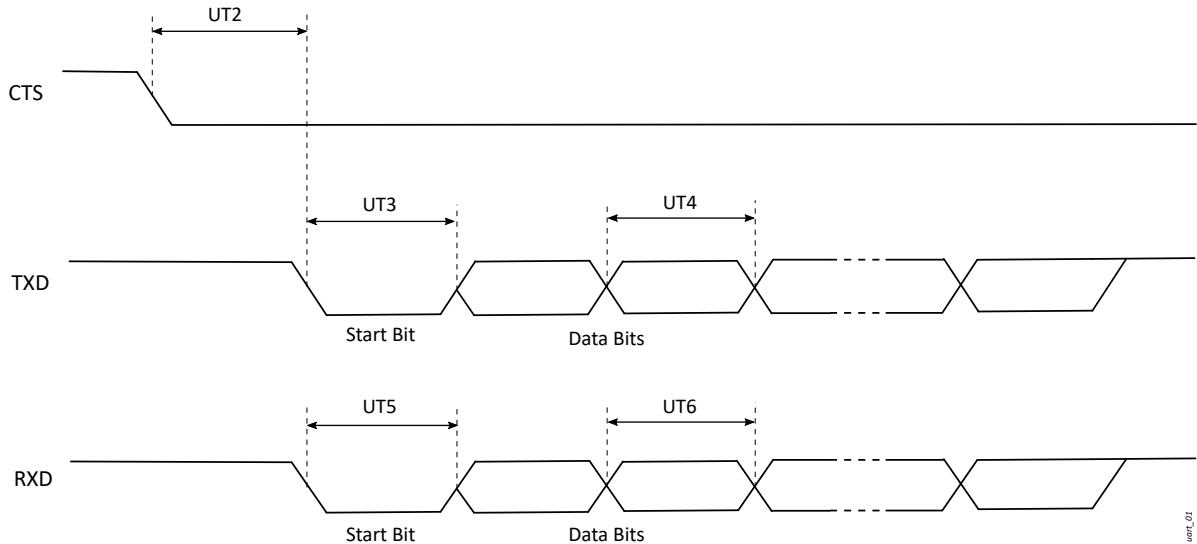
Table 5-36 and Figure 5-13 present the UART timing characteristics.

Table 5-36 UART Timing Characteristics

| No  | Parameter            |                                               | Mode | Min | Max | Unit |
|-----|----------------------|-----------------------------------------------|------|-----|-----|------|
|     | $f_{(\text{baud})}$  | Maximum programmable baud rate                |      |     | 5   | Mbps |
| UT2 | $t_{d\_CTS\_ST\_TX}$ | Delay time, receive CTSn low to start bit low |      | 100 | 200 | ns   |
| UT3 | $t_{pd\_ST\_TX}$     | Pulse duration, transmit start bit, low       |      | 400 | 400 | ns   |

| No  | Parameter         |                                                | Mode | Min | Max | Unit |
|-----|-------------------|------------------------------------------------|------|-----|-----|------|
| UT4 | $t_{pd\_DAT\_TX}$ | Pulse duration, transmit data bit, high or low |      | 400 | 400 | ns   |
| UT5 | $t_{pd\_ST\_RX}$  | Pulse duration, receive start bit, low         |      | 400 | 400 | ns   |
| UT6 | $t_{pd\_DAT\_RX}$ | Pulse duration, receive data bit, high or low  |      | 400 | 400 | ns   |

Figure 5-13 UART Timing Diagram



### 5.7.3.9 USB Timing Characteristics

The USB interface timing characteristics are compliant with Universal Serial Bus Specification Revision 2.0.

### 5.7.4 External Memory Interfaces

#### 5.7.4.1 HEXSPI Timing Characteristics

Table 5-37, Figure 5-14 and Figure 5-15 present the HEXSPI timing characteristics.

Table 5-37 HEXSPI Timing Characteristics

| No                 | Parameter        |                                    | Min                           | Typ          | Max                           | Unit |
|--------------------|------------------|------------------------------------|-------------------------------|--------------|-------------------------------|------|
|                    | $f_{op}$         | Operating frequency <sup>(1)</sup> | 50                            |              | 200                           | MHz  |
| O2                 | $t_{c\_CLK}$     | Cycle time, CLK                    | 5                             |              | 20                            | ns   |
| O3                 | $t_{pd\_CLK-H}$  | Pulse duration, CLK high           | $0.5 \times t_{c\_CLK} - 0.5$ | $t_{c\_CLK}$ | $0.5 \times t_{c\_CLK} + 0.5$ | ns   |
| O4                 | $t_{pd\_CLK-L}$  | Pulse duration, CLK low            | $0.5 \times t_{c\_CLK} - 0.5$ | $t_{c\_CLK}$ | $0.5 \times t_{c\_CLK} + 0.5$ | ns   |
| O5                 | $t_{R\_CLK}$     | Rise time, CLK                     |                               | 0.5          |                               | ns   |
| O6                 | $t_{F\_CLK}$     | Fall time, CLK                     |                               | 0.5          |                               | ns   |
| O7                 | $t_s\_DATA\_IN$  | Setup time, DATA input             |                               |              | 800                           | ps   |
| O8                 | $t_h\_DATA\_IN$  | Hold time, DATA input              |                               |              | 200                           | ps   |
| O9 <sup>(2)</sup>  | $t_d\_DATA\_OUT$ | Delay time, DATA output            | -5                            |              | 5                             | ns   |
| O10 <sup>(2)</sup> | $t_h\_DATA\_OUT$ | Hold time, DATA output             | -5                            |              | 5                             | ns   |
| O11                | $t_{EEU}$        | Edge to Edge uncertainty           |                               |              | 400                           | ps   |

1. 50 MHz, 66 MHz, 100 MHz, 133 MHz, and 200 MHz options. Lower speed options are possible.

2. On-chip programmable delays to center as needed.

Figure 5-14 HEXSPI Timing Diagram - SDR mode

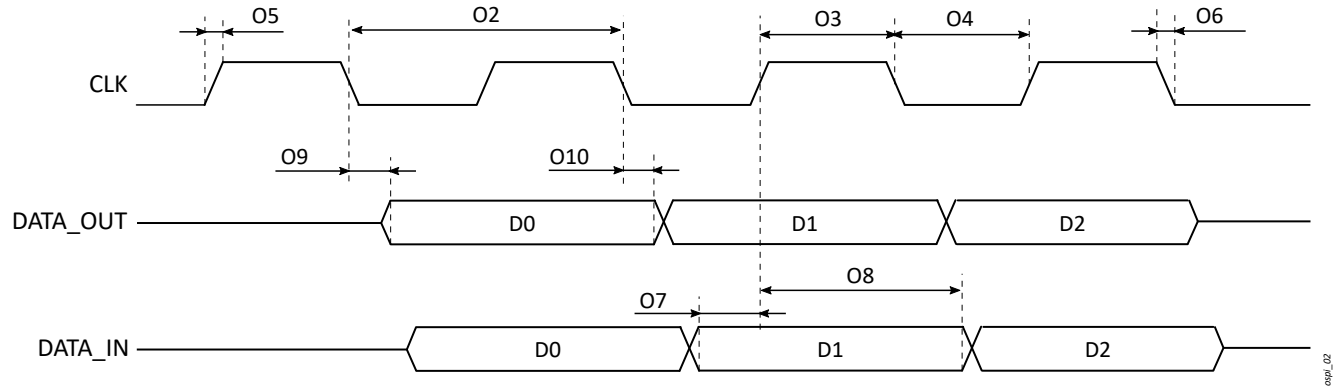
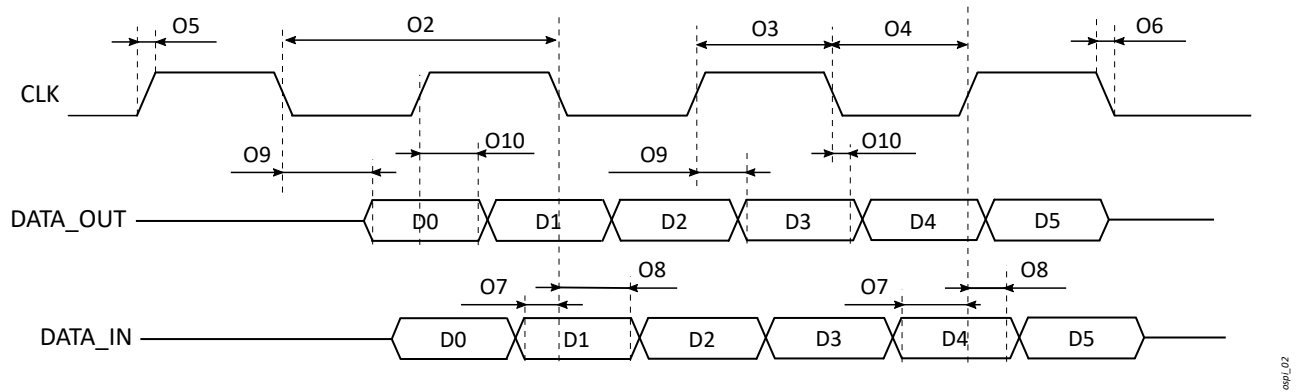


Figure 5-15 HEXSPI Timing Diagram - DDR mode



#### 5.7.4.2 SDMMC Timing Characteristics

Table 5-38 and Figure 5-16 present the SDMMC timing characteristics in DS mode.

Table 5-38 SDMMC Timing Characteristics (DS mode)

| No  | Parameter          |                                               | Min  | Max | Unit |
|-----|--------------------|-----------------------------------------------|------|-----|------|
| DS1 | $t_{c\_CLK}$       | Cycle time, CLK                               |      | 40  | ns   |
| DS2 | $t_{R\_CLK}$       | Rise time, CLK                                |      | 10  | ns   |
| DS3 | $t_{F\_CLK}$       | Fall time, CLK                                |      | 10  | ns   |
|     | $D_C\_CLK$         | Duty cycle                                    | 45   | 55  | %    |
| DS5 | $t_{s\_CMD\_CLK}$  | Setup time, CMD valid before CLK rising edge  | 11.7 |     | ns   |
| DS6 | $t_{h\_CMD\_CLK}$  | Hold time, CMD valid after CLK rising edge    | 8.3  |     | ns   |
| DS7 | $t_{s\_DATA\_CLK}$ | Setup time, DATA valid before CLK rising edge | 11.7 |     | ns   |
| DS8 | $t_{h\_DATA\_CLK}$ | Hold time, DATA valid after CLK rising edge   | 8.3  |     | ns   |

Figure 5-16 SDMMC Timing Diagram (DS mode)

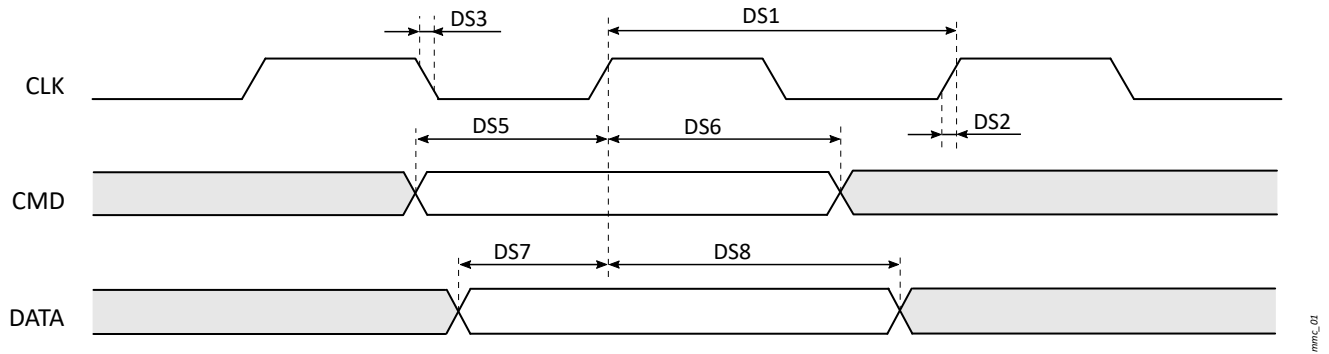


Table 5-39 and Figure 5-17 present the SDMMC timing characteristics in HS mode.

Table 5-39 SDMMC Timing Characteristics (HS mode)

| No  | Parameter          |                                               | Min | Max | Unit |
|-----|--------------------|-----------------------------------------------|-----|-----|------|
| HS1 | $t_{c\_CLK}$       | Cycle time, CLK                               |     | 20  | ns   |
| HS2 | $t_{R\_CLK}$       | Rise time, CLK                                |     | 3   | ns   |
| HS3 | $t_{F\_CLK}$       | Fall time, CLK                                |     | 3   | ns   |
|     | $D_C\_CLK$         | Duty cycle                                    | 45  | 55  | %    |
| HS5 | $t_{s\_CMD\_CLK}$  | Setup time, CMD valid before CLK rising edge  | 6.3 |     | ns   |
| HS6 | $t_{h\_CMD\_CLK}$  | Hold time, CMD valid after CLK rising edge    | 2.5 |     | ns   |
| HS7 | $t_{s\_DATA\_CLK}$ | Setup time, DATA valid before CLK rising edge | 6.3 |     | ns   |
| HS8 | $t_{h\_DATA\_CLK}$ | Hold time, DATA valid after CLK rising edge   | 2.5 |     | ns   |

Figure 5-17 SDMMC Timing Diagram (HS mode)

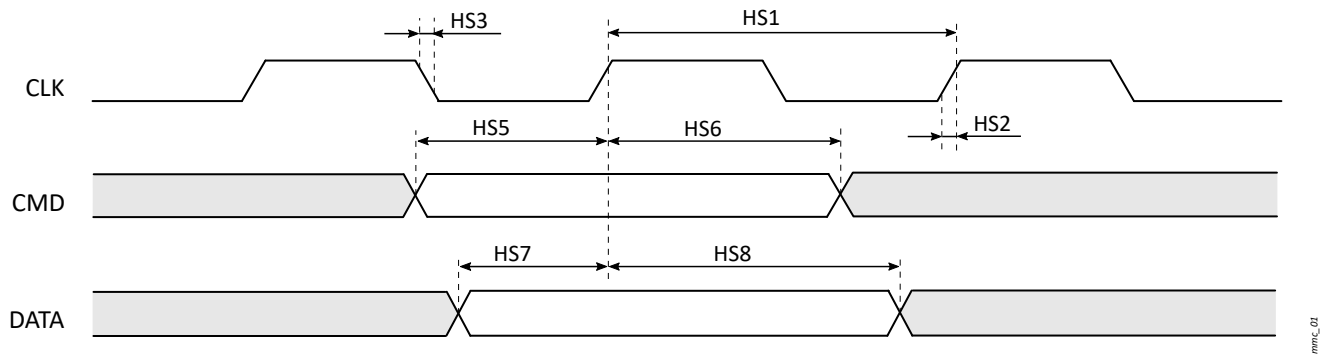
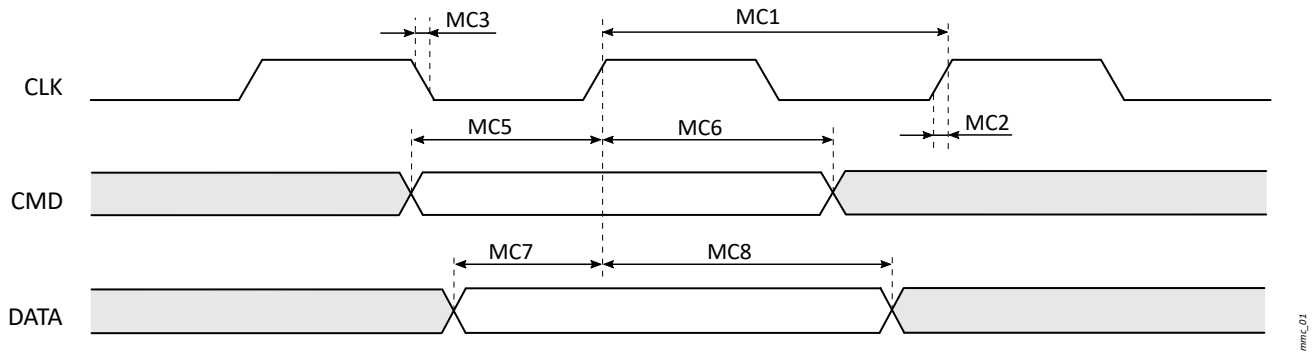


Table 5-40 and Figure 5-18 present the SDMMC timing characteristics in SDR12/SDR25 modes.

Table 5-40 SDMMC Timing Characteristics (SDR12/SDR25)

| No  | Parameter    |                 | Mode  | Min | Max | Unit |
|-----|--------------|-----------------|-------|-----|-----|------|
| MC1 | $t_{c\_CLK}$ | Cycle time, CLK | SDR12 |     | 40  | ns   |
|     |              |                 | SDR25 |     | 20  | ns   |
| MC2 | $t_{R\_CLK}$ | Rise time, CLK  |       |     | 3   | ns   |
| MC3 | $t_{F\_CLK}$ | Fall time, CLK  |       |     | 3   | ns   |
|     | $D_C\_CLK$   | Duty cycle      |       | 45  | 55  | %    |

| No  | Parameter          |                                               | Mode  | Min | Max | Unit |
|-----|--------------------|-----------------------------------------------|-------|-----|-----|------|
| MC5 | $t_{s\_CMD\_CLK}$  | Setup time, CMD valid before CLK rising edge  | SDR12 | 3   |     | ns   |
|     |                    |                                               | SDR25 | 3   |     | ns   |
| MC6 | $t_{h\_CMD\_CLK}$  | Hold time, CMD valid after CLK rising edge    | SDR12 | 0.8 |     | ns   |
|     |                    |                                               | SDR25 | 0.8 |     | ns   |
| MC7 | $t_{s\_DATA\_CLK}$ | Setup time, DATA valid before CLK rising edge | SDR12 | 3   |     | ns   |
|     |                    |                                               | SDR25 | 3   |     | ns   |
| MC8 | $t_{h\_DATA\_CLK}$ | Hold time, DATA valid after CLK rising edge   | SDR12 | 0.8 |     | ns   |
|     |                    |                                               | SDR25 | 0.8 |     | ns   |

**Figure 5-18 SDRAM Timing Diagram (SDR12/SDR25)**


## 5.7.5 Camera Interfaces

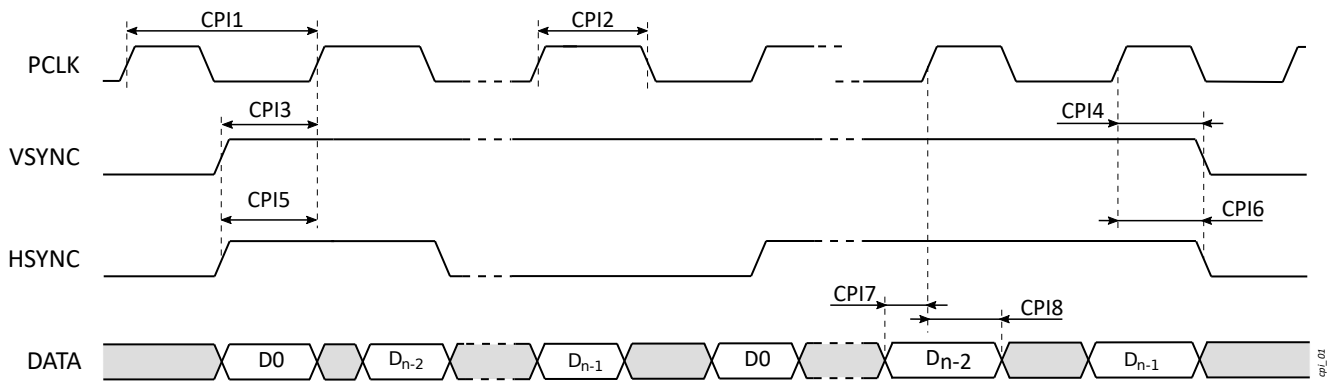
### 5.7.5.1 CPI Timing Characteristics

Table 5-41 and Figure 5-19 present the CPI timing characteristics.

**Table 5-41 CPI Timing Characteristics**

| No   | Parameter            |                                                           | Min  | Max | Unit |
|------|----------------------|-----------------------------------------------------------|------|-----|------|
| CPI1 | $t_{c\_MCLK}$        | Cycle time, PCLK                                          | 20   |     | ns   |
| CPI2 | $t_{pd\_MCLK}$       | Pulse duration, PCLK                                      | 8.33 |     | ns   |
| CPI3 | $t_{s\_VSYNC\_PCLK}$ | Setup time, input vertical sync VSYNC valid before PCLK   | 7    |     | ns   |
| CPI4 | $t_{h\_VSYNC\_PCLK}$ | Hold time, input vertical sync VSYNC valid after PCLK     | 2    |     | ns   |
| CPI5 | $t_{s\_HSYNC\_PCLK}$ | Setup time, input horizontal sync HSYNC valid before PCLK | 7    |     | ns   |
| CPI6 | $t_{h\_HSYNC\_PCLK}$ | Hold time, input horizontal sync HSYNC valid after PCLK   | 2    |     | ns   |
| CPI7 | $t_{s\_DATA\_PCLK}$  | Setup time, input DATA valid before PCLK                  | 7    |     | ns   |
| CPI8 | $t_{h\_DATA\_PCLK}$  | Hold time, input DATA valid after PCLK                    | 2    |     | ns   |

Figure 5-19 CPI Timing Diagram



### 5.7.5.2 CSI Timing Characteristics

The CSI interface timing characteristics are compliant with MIPI Alliance Specification for Camera Serial Interface 2 (CSI-2), Version 1.2, and MIPI Alliance Specification for D-PHY, Version 1.2.

## 5.7.6 Display Interfaces

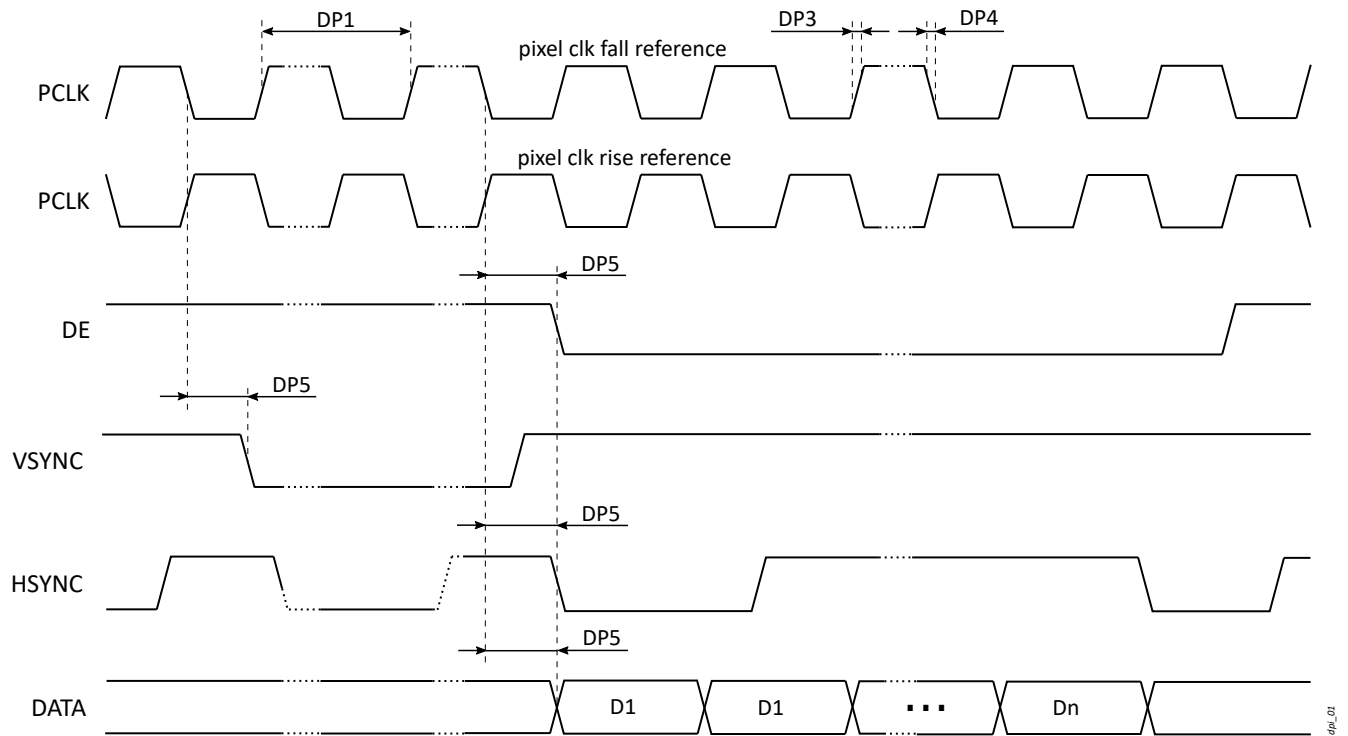
### 5.7.6.1 DPI Timing Characteristics

Table 5-42 and Figure 5-20 present the DPI timing characteristics.

Table 5-42 DPI Timing Characteristics

| No  | Parameter             |                                                    | Min | Max | Unit |
|-----|-----------------------|----------------------------------------------------|-----|-----|------|
| DP1 | $t_c$                 | Cycle time                                         | 20  |     | ns   |
|     | $D_{C\_CLK}$          | Duty cycle, PCLK                                   | 40  | 60  | %    |
| DP3 | $t_{R\_CLK}$          | Rise time, PCLK                                    |     | 1   | ns   |
| DP4 | $t_{F\_CLK}$          | Fall time, PCLK                                    |     | 1   | ns   |
| DP5 | $t_{d\_all\_to\_CLK}$ | Delay time, DE, VSYNC, HSYNC, DATA signals to PCLK | 5   |     | ns   |

Figure 5-20 DPI Timing Diagram



### 5.7.6.2 DSI Timing Characteristics

The DSI interface timing characteristics are compliant with MIPI Alliance Specification for Display Serial Interface (DSI), Version 1.2, and MIPI Alliance Specification for D-PHY, Version 1.2.

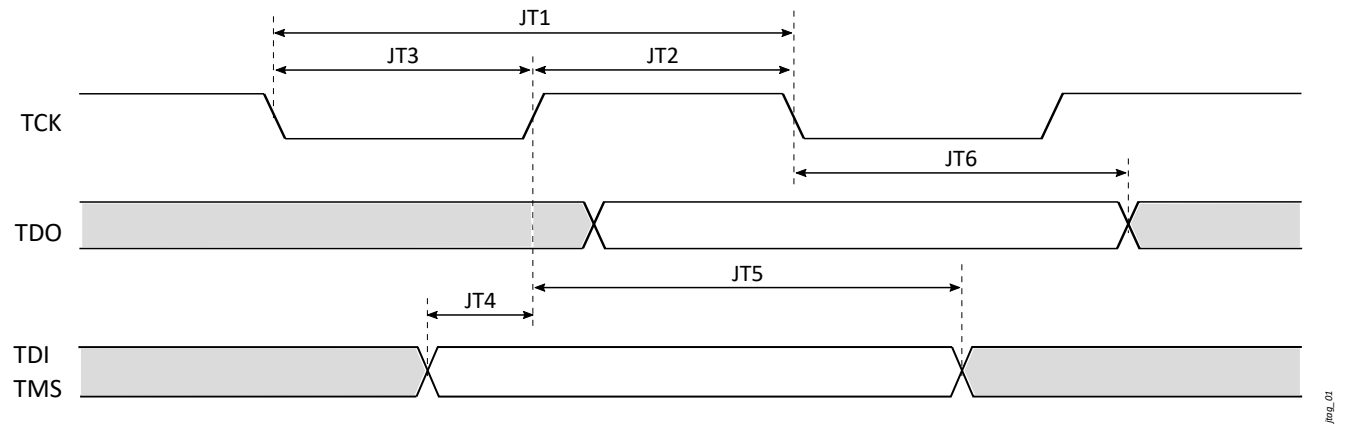
### 5.7.7 Debug Interface

Table 5-43 and Figure 5-21 present the JTAG timing characteristics.

Table 5-43 JTAG Timing Characteristics

| No  | Parameter            |                                                  | Min | Max | Unit |
|-----|----------------------|--------------------------------------------------|-----|-----|------|
| JT1 | $t_c$                | Cycle time, TCK                                  | 50  | 100 | ns   |
| JT2 | $t_{pd\_TCK-H}$      | Pulse duration, TCK high                         | 24  | 49  | ns   |
| JT3 | $t_{pd\_TCK-L}$      | Pulse duration, TCK low                          | 24  | 49  | ns   |
| JT4 | $t_{s\_TDI/TMS-TCK}$ | Setup time, TDI/TMS valid before TCK rising edge | 7   | 7   | ns   |
| JT5 | $t_{h\_TDI/TMS-TCK}$ | Hold time, TDI/TMS valid after TCK rising edge   | 7   | 7   | ns   |
| JT6 | $t_{d\_TDO}$         | Delay time, TDO valid after TCK falling edge     | 7   | 7   | ns   |

**Figure 5-21 JTAG Timing Diagram**



## 6 Package Information

### 6.1 Device Marking Definition

Figure 6-1 and Figure 6-2 present the top marking reference view.

Figure 6-1 WLCSP Device Top Marking Reference

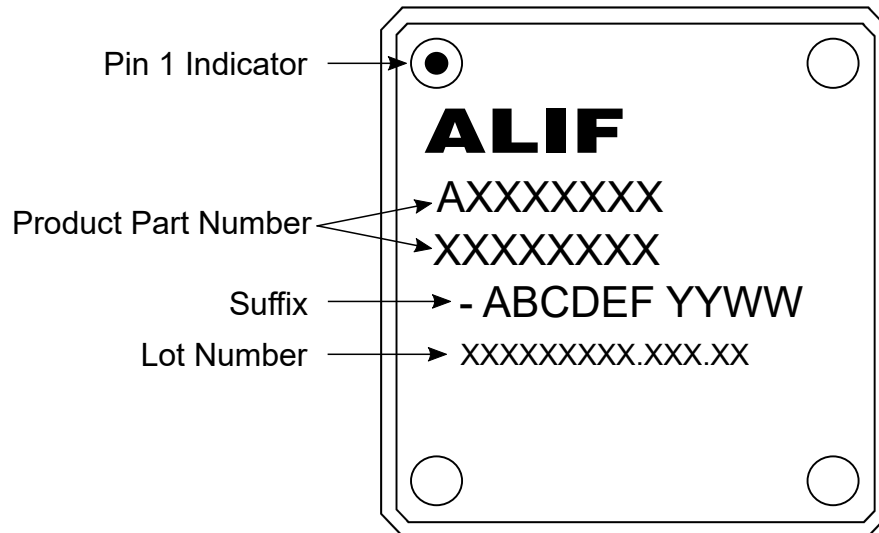


Figure 6-2 FBGA Device Top Marking Reference

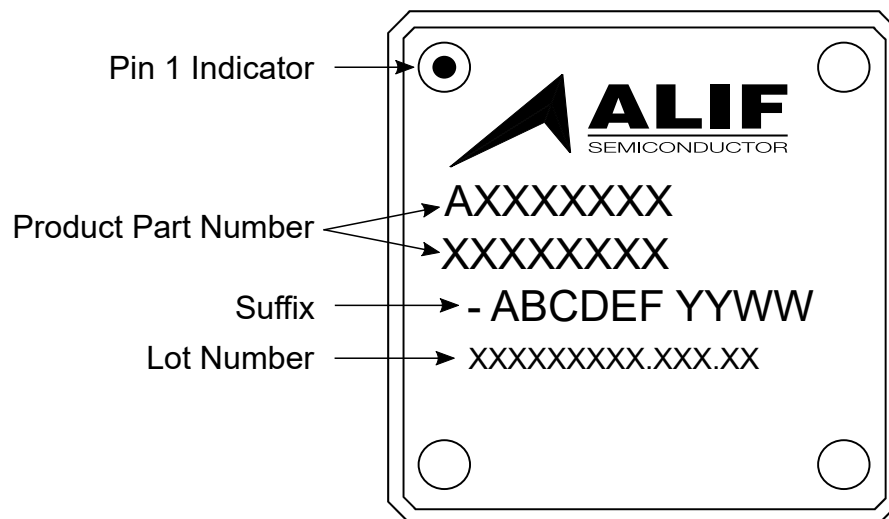


Table 6-1 presents the part number decoding for all Alif Semiconductor's product series.

**Table 6-1 Product Identification**

| Example Part Number:                                                                                       | A | E | 8 | 2 | 2 | F | A | 0 | E | 55 | 97 | B | S | 0 |
|------------------------------------------------------------------------------------------------------------|---|---|---|---|---|---|---|---|---|----|----|---|---|---|
| Device Manufacturer                                                                                        | A | E | 8 | 2 | 2 | F | A | 0 | E | 55 | 97 | B | S | 0 |
| A - Alif Semiconductor                                                                                     |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| Device Family                                                                                              |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| B - BLE-connected embedded microcontrollers                                                                |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| E - Ensemble, embedded processors                                                                          |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| Device Series                                                                                              |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 0 - Service MCU                                                                                            |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 1 - Efficiency MCU                                                                                         |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 3/4 - Performance MCU                                                                                      |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 5/6 - Fusion processor MCU/MPU                                                                             |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 7/8 - Extreme fusion processor MCU/MPU                                                                     |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| Number of Application Processing Cores /<br>Single Core Product Designator                                 |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 0 - Zero cores                                                                                             |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 1 - One cores                                                                                              |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 2 - Two cores                                                                                              |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| C - Compact                                                                                                |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| Number of Real Time Processing Cores                                                                       |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 0 - Zero cores                                                                                             |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 1 - One cores                                                                                              |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 2 - Two cores                                                                                              |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| Security Attribute                                                                                         |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| B - Basic security                                                                                         |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| F - Full security, complete life cycle management                                                          |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| Machine Learning and AI Capability                                                                         |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 0 - Hardware Acceleration for AI/ML                                                                        |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 1 - MCU Vector Extension (Helium)                                                                          |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 4 - Single Neural Processing Unit (Ethos-U55) + MCU Vector Extension (Helium)                              |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 8 - Dual Neural Processing Units (Ethos-U55) + MCU Vector Extension (Helium)                               |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 9 - Dual Neural Processing Units (Ethos-U55 and Ethos-U85) + MCU Vector<br>Extension (Helium)              |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| A - Triple Neural Processing Units (2× Ethos-U55 and Ethos-U85) + MCU Vector<br>Extension (Helium)         |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| Wireless Capability                                                                                        |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 0 - No wireless                                                                                            |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| M - BLE + IEEE 802.15.4                                                                                    |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| Peripheral Set                                                                                             |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 0 through 9, A through Z = Level of peripheral selection mix, higher is typically more<br>peripherals      |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| On-Chip Application MRAM Size                                                                              |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| MRAM memory size in MB                                                                                     |   |   |   |   |   |   |   |   |   |    |    |   |   |   |
| 1 <sup>st</sup> digit - N = None, 1 through 9 = 1MB through 9MB, A through F = 10MB through 15MB, 0 = 16MB |   |   |   |   |   |   |   |   |   |    |    |   |   |   |

|                                                                                                            |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
|------------------------------------------------------------------------------------------------------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|-----------|-----------|----------|----------|----------|
| <b>Example Part Number:</b>                                                                                | <b>A</b> | <b>E</b> | <b>8</b> | <b>2</b> | <b>2</b> | <b>F</b> | <b>A</b> | <b>0</b> | <b>E</b> | <b>55</b> | <b>97</b> | <b>B</b> | <b>S</b> | <b>0</b> |
| 2 <sup>nd</sup> digit - 0 = 0KB, 1 = 128KB, 2 = 256KB, 3 = 384KB, 5 = 512KB, 7 = 768KB                     |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| On-Chip Application SRAM Size                                                                              |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| SRAM memory size in MB                                                                                     |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| 1 <sup>st</sup> digit - N = None, 1 through 9 = 1MB through 9MB, A through F = 10MB through 15MB, 0 = 16MB |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| 2 <sup>nd</sup> digit - 0 = 0KB, 1 = 128KB, 2 = 256KB, 3 = 384KB, 5 = 512KB, 7 = 768KB                     |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| Package Type and Pin Count                                                                                 |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| A - WLCSP208, 0.5 mm pitch                                                                                 |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| B - WLCSP216, 0.4 mm pitch                                                                                 |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| H - WLCSP120, 0.35 mm pitch                                                                                |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| L - FBGA194, 0.5 mm pitch                                                                                  |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| P - FBGA120, 0.5 mm pitch                                                                                  |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| 5 - TQFP64, 0.5 mm pitch                                                                                   |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| Operating Temperature                                                                                      |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| S - Standard (see <a href="#">Section 5.2.1 General Operating Conditions</a> )                             |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| E - Extended (see <a href="#">Section 5.2.1 General Operating Conditions</a> )                             |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| H - Industrial (see <a href="#">Section 5.2.1 General Operating Conditions</a> )                           |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| Product Revision                                                                                           |          |          |          |          |          |          |          |          |          |           |           |          |          |          |
| 0 or Blank - Original version of product                                                                   |          |          |          |          |          |          |          |          |          |           |           |          |          |          |

[Table 6-2](#) presents the Suffix (characters after main part number) decoding.

**Table 6-2 Suffix Definition**

| Position | Description                                        |
|----------|----------------------------------------------------|
| A        | ID                                                 |
| B        | ID revision                                        |
| C        | Firmware version                                   |
| D        | Fab site. D = Dresden                              |
| E        | Final assembly site. M = Malaysia, K = South Korea |
| F        | Final test site. S = Singapore, E = USA            |
| Space    |                                                    |
| Y        | Calendar year of device production                 |
| Y        |                                                    |
| W        | Work week of device production                     |
| W        |                                                    |

## 6.2 Package Specifications

### 6.2.1 WLCSP216 Package Information

#### 6.2.1.1 WLCSP216 Thermal Operating Specifications

Table 6-3 provides thermal operating specifications for WLCSP216 package.

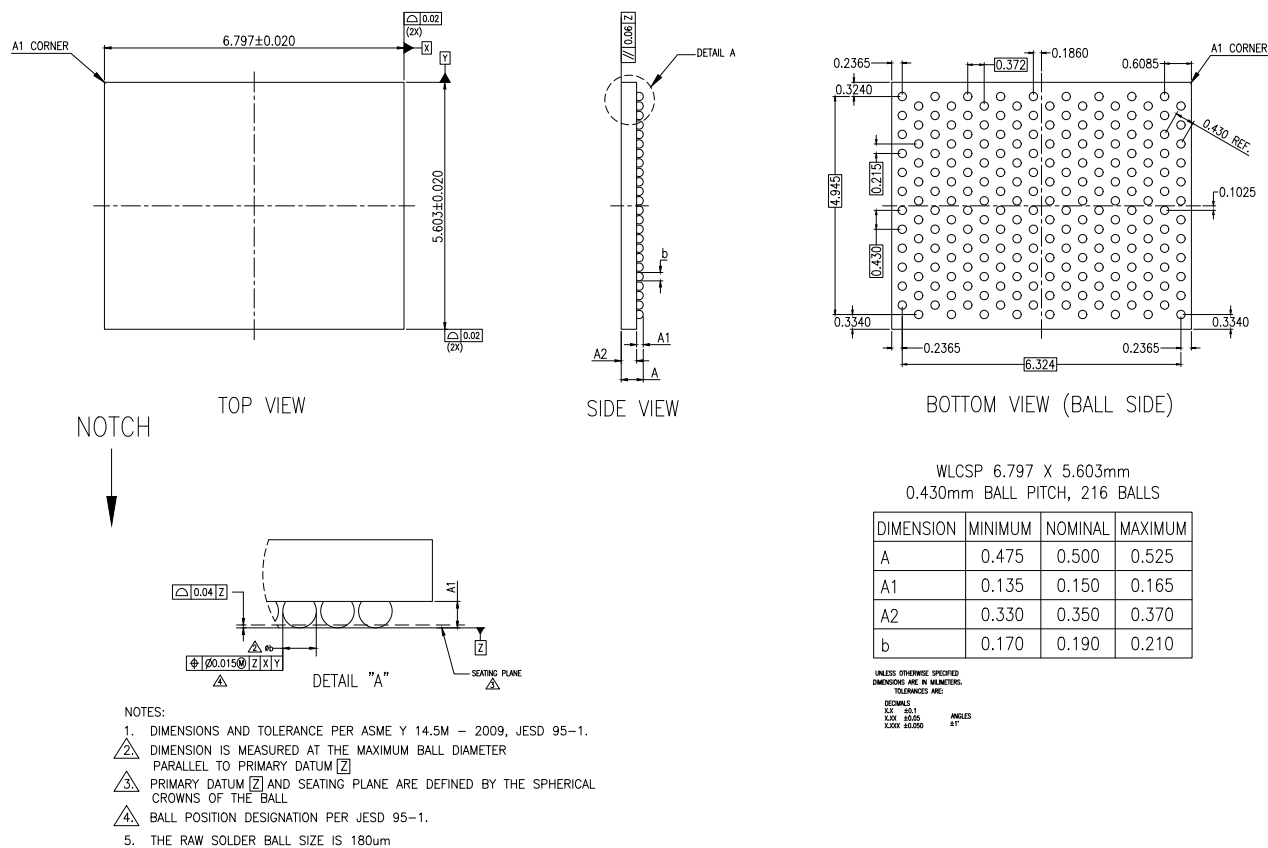
**Table 6-3 WLCSP216 Thermal Operating Specifications**

| Parameter      |                                                                 | Value | Unit |
|----------------|-----------------------------------------------------------------|-------|------|
| $R\theta_{JA}$ | Thermal resistance in natural convection (junction-to-free air) | 25.82 | °C/W |
| $R\theta_{JC}$ | Thermal resistance (junction-to-case)                           | 0.08  | °C/W |
| $\Psi_{JT}$    | Thermal characterization parameter (junction-to-package top)    | 0.03  | °C/W |

#### 6.2.1.2 WLCSP216 Package Outline

Figure 6-3 presents WLCSP216 package outline.

**Figure 6-3 WLCSP216 Package Outline (1)**



1. All linear dimensions are in millimeters.

Figure 6-4 presents the bump distances from the cut edge of the WLCSP216 package.

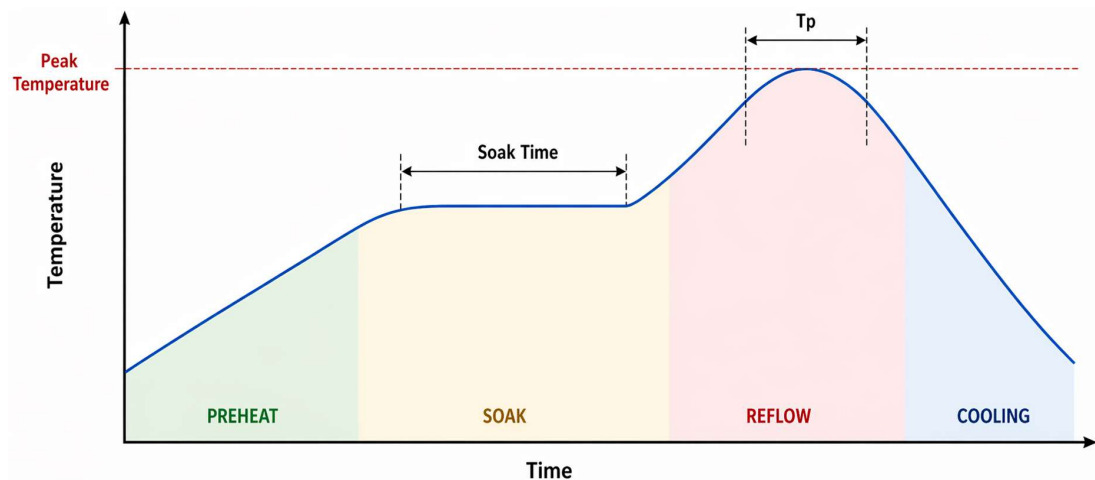
**Figure 6-4 WLCSP216 Package Bump Distances from Cut Edge**



### 6.2.1.3 WLCSP216 Solder Reflow Profile

The device is compliant with the IPC/JEDEC joint industry standard: J-STD-020F. The recommended solder reflow profile for this package is shown in Figure 6-5 and follows the guidelines defined in Section 8.6 of the standard.

**Figure 6-5 WLCSP216 Solder Reflow Profile**



| Item | Parameter                    | Setting   | Unit |
|------|------------------------------|-----------|------|
| 1    | Peak Temperature             | 235 – 255 | °C   |
| 2    | Reflow Time $T_p$ (< 217 °C) | 60 – 90   | s    |
| 3    | Soak Time (150 – 180 °C)     | 60 – 90   | s    |

## 6.2.2 FBGA194 Package Information

### 6.2.2.1 FBGA194 Thermal Operating Specifications

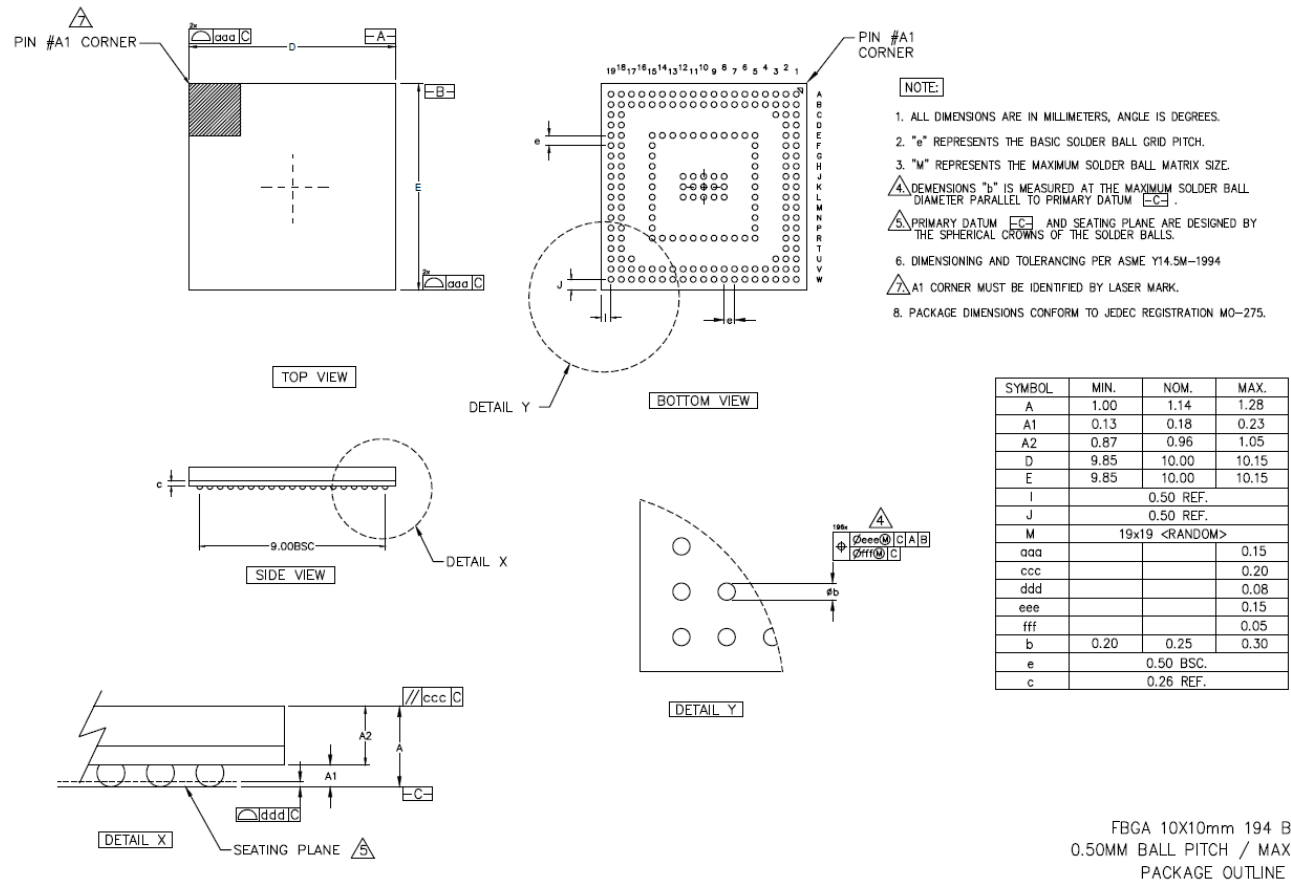
Table 6-4 provides thermal operating specifications for FBGA194 package.

**Table 6-4 FBGA194 Thermal Operating Specifications**

| Parameter     |                                                                 | Value | Unit |
|---------------|-----------------------------------------------------------------|-------|------|
| $\theta_{JA}$ | Thermal resistance in natural convection (junction-to-free air) | 21.1  | °C/W |
| $\theta_{JC}$ | Thermal resistance (junction-to-case)                           | 17.0  | °C/W |
| $\Psi_{JT}$   | Thermal characterization parameter (junction-to-package top)    | 21.0  | °C/W |

### 6.2.2.2 FBGA194 Package Outline

Figure 6-6 presents FBGA194 package outline.

**Figure 6-6 FBGA194 Package Outline (1)**


1. All linear dimensions are in millimeters.

### 6.2.2.3 FBGA194 Solder Reflow Profile

Please refer to the IPC/JEDEC joint industry standard: J-STD-020F, section 8.6 for the recommended solder reflow time and temperature profile for this package.

## 6.3 Storage Conditions

Table 6-5 defines specifics in the storage conditions.

**Table 6-5 Storage Conditions**

| Parameter        |                     |                                                  | Min | Max | Unit |
|------------------|---------------------|--------------------------------------------------|-----|-----|------|
| T <sub>STG</sub> | Storage temperature |                                                  | -40 | 150 | °C   |
| %RH              | Relative Humidity   | WLCSP package: MSL1 (Moisture Sensitivity Level) |     |     |      |
|                  |                     | FBGA package: MSL3                               |     |     |      |

## 7 Ordering Information

Table 7-1 presents the optional features for each orderable part number.

**Table 7-1 Orderable Part Numbers**

| Part Number <sup>(2)</sup> | MRAM  | SRAM   | GPIO (1.8 V)       | Package  | Operating Temperature |
|----------------------------|-------|--------|--------------------|----------|-----------------------|
| AE822FA0E5597BS0           | 5.5MB | 9.75MB | 136                | WLCSP216 | Standard              |
| AE822FA0E5597LS0           | 5.5MB | 9.75MB | 120 <sup>(1)</sup> | FBGA194  | Standard              |

1. GPIO[0-14]

2. Ordering designation for shipment packaging:

- Add the following suffix to base part number
  - -T, for Tape and Reel
  - -Y, for Tray
- Example: AE822FA0E5597BS0-T is Tape and Reel

Table 7-2 shows the user SRAM banks with their corresponding sizes (in KB) available for each part number.

**Table 7-2 Part Numbers SRAM Breakdown**

| Part Number      | Total SRAM (KB) | SRAM0 (KB) | SRAM1 (KB) | SRAM2 (M55-HP ITCM) (KB) | SRAM3 (M55-HP DTCM) (KB) | SRAM4 (M55-HE ITCM) (KB) | SRAM5 (M55-HE DTCM) (KB) |
|------------------|-----------------|------------|------------|--------------------------|--------------------------|--------------------------|--------------------------|
| AE822FA0E5597BS0 | 9984            | 4096       | 4096       | 256                      | 1024                     | 256                      | 256                      |
| AE822FA0E5597LS0 | 9984            | 4096       | 4096       | 256                      | 1024                     | 256                      | 256                      |

For complete part number decoding, see [Section 6.1 Device Marking Definition](#).

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### 8.2 Related Documents and Tools

For additional Alif Semiconductor technical documentation and software resources please visit:

- [User Guides & App Notes](#)
- [Software & Tools](#)

For managing software configurations of device resources, power, pins, clocks, DMA requests, interrupts, and various other additional settings, refer to the [Alif Conductor](#) tool.

### 8.3 Contact Information

For more information visit our website [Alif Semiconductor](#) or contact us:

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## 8.5 Acronyms

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### 3

#### **3GPP**

*3rd Generation Partnership Project*

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### A

#### **ACP**

*Accelerator Coherency Port*

#### **ADC**

*Analog to Digital Converter*

#### **AES**

*Advanced Encryption Standard*

#### **AHI**

*Application Host Interface*

#### **AI**

*Artificial Intelligence*

#### **aiPM**

*autonomous intelligent Power Management*

#### **AON**

*Always On*

#### **API**

*Application Programming Interface*

#### **APSS**

*Application Processor Subsystem*

**ATOC***Application Table of Content*

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**B****BER***Bit-Error Ratio***BLE***Bluetooth Low Energy***BLIT***Block Image Transfers***BOD***Brown-Out Detect***BOR***Brown-Out Reset***BPU***Breakpoint Unit*

---

**C****CAN***Controller Area Network***CANFD***Controller Area Network with Flexible Data rate***CCC***Common Command Code***CDC***Configurable DPI Controller***CDM***Charged Device Model***CLUT***Color Look-Up Table***CMP***Comparator*

**CMSIS***Common Microcontroller Software Interface Standard***CNN***Convolutional Neural Network***CPI***Camera Parallel Interface***CPU***Central Processing Unit***CRC***Cyclic Redundancy Check***CSI***Camera Serial Interface***D**

---

**DAC***Digital to Analog Converter***DAP***Debug Access Port***DDR***Double Data Rate***DL***Display List / Download***DLR***Display List Reader***DM***Device Manufacturer***DMA***Direct Memory Access***DMAC***Direct Memory Access Controller***DMIC***Digital Microphone*

**DPA***Differential Power Analysis***DPI***Display Parallel Interface / Display Pixel Interface***DPU***Data Processing Unit***DRD***Dual-Role Device***DSC***Display Stream Compression***DSI***Display Serial Interface***DTCM***Data Tightly-Coupled Memory***DWT***Data Watchpoint and Trace***E**

---

**ECB***Electronic Codebook***ECC***Error-Correcting Code / Elliptic-Curve Cryptography***eDRX***Extended Discontinuous Reception***EMC***Electromagnetic Compatibility***EMFI***Electromagnetic Fault Injection***EMI***Electromagnetic Interference***EMS***Electromagnetic Susceptibility*

**EOL***End of Life***EoTp***End of Transmission Packet***EPU***Extension Processing Unit***ESD***Electrostatic Discharge***eSIM***Embedded Subscriber Identity Module***ETH***Ethernet***EVTRTR***Event Router***EWIC***External Wakeup Interrupt Controller*

---

**F**

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**FC***Firewall Component***FIR***Finite Impulse Response***FSR***Full-Scale Range*

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**G**

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**GIC***Generic Interrupt Controller***GNSS***Global Navigation Satellite Subsystem***GOPS***Giga Operations Per Second*

**GPIO***General-Purpose Input/Output***GPS***Global Positioning System***GPU***Graphics Processing Unit*

---

**H**

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**HBM***Human Body Model***HCI***Host Communication Interface***HDR***High Data Rate***HE***High Efficiency***HFRC***High-Frequency Resistor-Capacitor***HFXO***High-Frequency Crystal Oscillator***HMI***Human Machine Interface***HP***High Performance***HPP***High Performance Point***HUK***Hardware Unique Key***HWRM***Hardware Reference Manual***HWSEM***Hardware Semaphore*

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**I**

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**I2C***Inter-Integrated Circuit***I2S***Inter-IC Sound***I3C***Improved Inter-Integrated Circuit***IBI***In-Band Interrupt***ICMP***Internet Control Message Protocol***ICV***Integration Circuit Vendor***IDE***Integrated Design Environment***IFG***Interframe Gap***IFU***Instruction Fetch Unit***IIR***Infinite Impulse Response***IMD***Intermodulation Distortion***IoT***Internet of Things***IPC***Inter-Process Communication***IPI***Image Pixel Interface*

**IRQRTR***Interrupt Router***iSIM***Integrated Subscriber Identity Module***ISP***In-System Programming***ITCM***Instruction Tightly-Coupled Memory***iUICC***integrated Universal Integrated Circuit Card***IWIC***Internal Wakeup Interrupt Controller***L**

---

**LCD***Liquid Crystal Display***LCS***Life Cycle State***LDE***Lockdown Extension***LDO***Low Drop-Out***LE***Low Energy***LFRC***Low-Frequency Resistor-Capacitor***LFXO***Low-Frequency Crystal Oscillator***LOM***Listen Only Mode***LP***Low-Power*

**LPCMP***Low-Power Comparator***LPGPIO***Low-Power General-Purpose Input/Output***LPI2C***Low-Power Inter-Integrated Circuit***LPI2S***Low-Power Inter-IC Sound***LPM***Link Power Management***LPP***Low Performance Point***LPPDM***Low-Power Pulse Density Modulation***LPRTC***Low-Power Real-Time Counter***LPSPi***Low-Power Serial Peripheral Interface***LPTIMER***Low-Power Timer***LSB***Least Significant Bit***LTE***Long-Term Evolution***LUT***Look-Up Table*

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**M**

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**MAC***Media Access Controller***MAU***Memory Authentication Unit*

**MBI***Master Bus Interface***MCU***Microcontroller Unit***ME***Monitor Extension***MHU***Message Handling Unit***ML***Machine Learning***MMU***Memory Management Unit***MPE***Master Permission Entry***MPU***Memory Protection Unit***MRAM***Magnetoresistive Random-Access Memory***MSL***Moisture Sensitivity Level***MTL***MAC Transaction Layer***MVE***M-profile Vector Extension***MWS***Mobile Wireless Standard*

---

**N**

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**NMI***Non-Maskable Interrupt***NPP***Nominal Performance Point*

**NPU***Neural Processing Unit***NPU-HE***Neural Processing Unit-High Efficiency***NPU-HP***Neural Processing Unit-High Performance***NRZ***Non-Return-to-Zero***NS***Non-Secure***NVIC***Nested Vectored Interrupt Controller***NVM***Non-Volatile Memory*

---

**O****OCS***OEM-signed Configuration Settings***OEM***Original Equipment Manufacturer***OPP***Operating Performance Point***OSPI***Octal Serial Peripheral Interface***OToC***OEM-signed Table of Contents***OTP***One Time Programmable*

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**P****PCB***Printed Circuit Board*

**PCM***Pulse Code Modulation***PD***Power Domain***PDM***Pulse Density Modulation***PE***Protection Extension***PLL***Phase-Locked Loop***PMU***Performance Monitoring Unit***POR***Power-On-Reset***PPI***PHY Protocol Interface / Private Peripheral Interrupt***PPS***Precise Positioning Service***PPU***Power Policy Unit***PSC***Power Sequence Controller***PSM***Power Saving Mode***PSRAM***Pseudo-Static Random-Access Memory***PSRR***Power Supply Rejection Ratio***PWM***Pulse Width Modulation*

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**Q**

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**QEC***Quadrature Encoder Counter*

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**R**

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**RAI***Release Assistance Indication***RDC***Receiver Delay Compensation***RF***Radio Frequency***RFI***Radio Frequency Interference***RLE***Run-Length Encoding***RMA***Return Merchandise Authorization***RNN***Recurrent Neural Network***RO***Read Only***ROM***Read Only Memory***RoT***Root-of-Trust***RSA***Rivest–Shamir–Adleman***RSE***Region Size Extension***RSSI***Received Signal Strength Indicator*

**RSTC***Reset Controller***RTC***Real-Time Counter***RTOS***Real-Time Operating System***RTSS***Real-Time Subsystem***RW***Read/Write*

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**S**

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**SAR***Successive Approximation Register***SAU***Security Attribution Unit***SBI***Slave Bus Interface***SCU***Snoop Control Unit***SDA***Serial Data***SDIO***Secure Digital Input/Output***SDMMC***Secure Digital / Embedded Multimedia Card***SDR***Single Data Rate***SE***Secure Enclave / Secure Enable***SESS***Secure Enclave Subsystem*

**SFD***Start of Frame Data / Start Frame Delimiter***SGI***Software Generated Interrupt***SHA***Secure Hash Algorithm***SIM***Subscriber Identity Module***SIMD***Single Instruction Multiple Data***SJW***Synchronization Jump Width***SMP***Symmetric Multi-Processing***SNR***Signal-to-Noise Ratio***SPA***Simple Power Analysis***SPI***Serial Peripheral Interface / Shared Peripheral Interrupt***SRAM***Static Random-Access Memory***SSP***Synchronous Serial Protocol***SST***Single Shot Transmission***STB***Store Buffer***STOC***System Table of Content*

**SWD***Serial Wire Debug***SWRM***Software Reference Manual***T**

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**TCM***Tightly-Coupled Memory***TCP***Transmission Control Protocol***TDC***Transmitter Delay Compensation***TE***Translation Extension***TEE***Trusted Execution Environment***TFT***Thin-Film-Translator***TGU***TCM Gate Unit***TOC***Table of Content***TRNG***True Random Number Generator***TSENS***Temperature Sensor***U**

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**UART***Universal Asynchronous Receiver/Transmitter***UDE***Unprivileged Debug Extension*

**UDP***User Datagram Protocol***UI***Unit Interval / User Interface***UL***Upload***UPP***Ultra-Low Performance Point***USB***Universal Serial Bus***UTIMER***Universal Timer***V**

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**VTOR***Vector Table Offset Register***W**

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**WDT***Watchdog Timer***WFE***Wait For Event***WFI***Wait For Interrupt***X**

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**XIP***eXecute-in-Place***XO***Execute Only*

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**Z**

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**ZI***Zero Initialized*

## 9 Revision History

[Table 9-1](#) provides the history of changes to this document.

**Table 9-1 Revision History**

| Date       | Revision | Changes                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
|------------|----------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| April 2026 | 1.0      | <p>Changes from previous revision include:</p> <ul style="list-style-type: none"> <li>■ Updated description of GO_5 and the typical current consumption at 3.3 V in <a href="#">Table 5-5 Power Modes Case Definition</a></li> <li>■ Updated the typical current consumption at 3.3 V for STOP_1, STOP_2, STOP_3, STOP_4, and STOP_5 modes in <a href="#">Table 5-5 Power Modes Case Definition</a></li> <li>■ Updated <a href="#">Figure 6-3 WLCSP216 Package Outline</a></li> <li>■ Updated <a href="#">Section 6.2.1.3 WLCSP216 Solder Reflow Profile</a></li> <li>■ Editorial enhancements</li> </ul> |

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