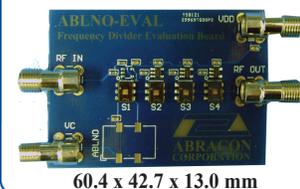


# Frequency Divider Evaluation Board

**ABLNO-EVAL**

 **RoHS Compliant**



## OVERALL CAPABILITY

**ABLNO-EVAL**; Frequency Divider Evaluation Board shown in figure (1) is designed to facilitate engineering evaluation of Abracon's Ultra Low Noise – ABLNO series of fixed clock and voltage controlled crystal oscillators. Further, there is a provision through the RF\_IN SMA Connector to supply any other oscillator signal between 10MHz and 200MHz; if ABLNO series is not being characterized.

This Evaluation Board is ideal to conduct the following measurements:

- Phase Noise and rms jitter for  $\div 1$ ,  $\div 2$ ,  $\div 4$  and  $\div 8$  frequency outputs
- Frequency Pull Characteristics of the ABLNO by using the Vc port as the control voltage
- Frequency Stability over operating temperature ( $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )



**Figure (1)**

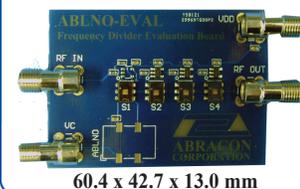
Designers who are interested in using the ABLNO as an Ultra Low Noise platform device to generate additional Low Noise frequencies will find this Evaluation Board to be of exceptional value. Abracon has implemented Ultra Low Noise  $\div 2$ ,  $\div 4$  and  $\div 8$  circuitry on this board, that can also be incorporated in end-customer solutions; please contact [tech-spport@abracon.com](mailto:tech-spport@abracon.com) for additional details.

Typical Phase Noise and jitter performance in  $\div 1$ ,  $\div 2$ ,  $\div 4$  and  $\div 8$  modes is depicted in section 2.0.

# Frequency Divider Evaluation Board

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## COMPONENT DESCRIPTION

| Component     | Description               | Functionality  |
|---------------|---------------------------|--|
| <b>RF_IN</b>  | External Oscillator Input | Input a 10MHz to 200MHz oscillator signal into this SMA connector for evaluation... <i>see Note #5</i>   |
| <b>Vc</b>     | Control Port              | When characterizing the ABLNO series of VCXO's, apply control voltage to this port to characterize frequency pull  |
| <b>VDD</b>    | Supply Voltage            | This port simultaneously biases the ABLNO Oscillator and the divider scheme (+3.3V ±5%) ..... <i>see Note #4</i>   |
| <b>RF_Out</b> | Evaluation Board Output   | Either ABLNO or RF_IN frequency is divided down by 1, 2, 4 or 8 and is present at this port  |
| <b>S1</b>     | Switch # 1                | If the tab is moved to the “up position ( <b>UP</b> )”, RF_IN signal is selected. If the tab is moved to the “down position ( <b>DN</b> )”, ABLNO signal is selected                                       |
| <b>S2</b>     | Switch # 2                | If the tab is moved to the “up position ( <b>UP</b> )”, RF_IN signal is divided down by 2 and is present at RF_Out   |
| <b>S3</b>     | Switch # 3                | If the tab is moved to the “up position ( <b>UP</b> )”, RF_IN signal is divided down by 4 and is present at RF_Out. S2 should also be in the “up position ( <b>UP</b> )”... please see truth table #1      |
| <b>S4</b>     | Switch # 4                | If the tab is moved to the “up position ( <b>UP</b> )”, RF_IN signal is divided down by 8 and is present at RF_Out. S2 & S3 should also be in the “up position ( <b>UP</b> )”... please see truth table #1 |

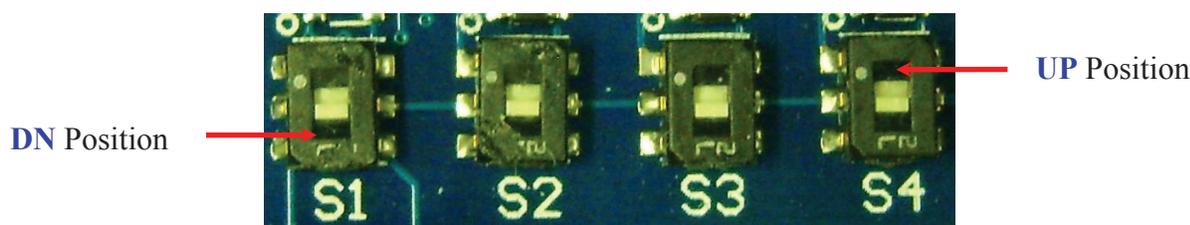
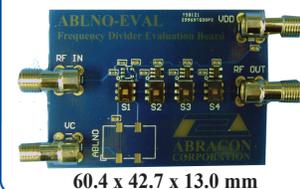


Figure (2)

# Frequency Divider Evaluation Board

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## TRUTH TABLE

Table # 1

| S1 | S2 | S3 | S4 | Description            |
|----|----|----|----|------------------------|
| DN | DN | DN | DN | ABLNO's RF Output = ÷1 |
| DN | UP | DN | DN | ABLNO's RF Output = ÷2 |
| DN | UP | UP | DN | ABLNO's RF Output = ÷4 |
| DN | UP | UP | UP | ABLNO's RF Output = ÷8 |

Table # 2

| S1 | S2 | S3 | S4 | Description                 |
|----|----|----|----|-----------------------------|
| UP | DN | DN | DN | RF_IN Port's RF Output = ÷1 |
| UP | UP | DN | DN | RF_IN Port's RF Output = ÷2 |
| UP | UP | UP | DN | RF_IN Port's RF Output = ÷4 |
| UP | UP | UP | UP | RF_IN Port's RF Output = ÷8 |

**Note # 1:** **DN** = Down Position; **UP** = Up Position

**Note # 2:** All four switches are shipped with yellow protective tape on top, please remove before use

**Note # 3:** To evaluate Abracon's ABLNO Crystal Oscillator, please solder it down in the section outlined with a rectangle and labeled ABLNO. Please follow the orientation shown in figure (3) below.



Figure (3)

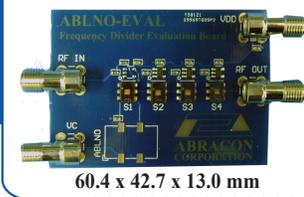
**Note # 4:** VDD Port biases both the ABLNO device, as well as the divider circuitry. Since ABLNO's VDD range is  $+3.3V \pm 5\%$ , the recommended VDD range while evaluating ABLNO oscillators is  $+3.135V$  to  $+3.465V$ . However, since the divider circuitry can be biased between  $+1.8V$  &  $+5.5V$ , while evaluating RF\_IN external signal; lower or higher biasing voltage can be used, as long as the peak-to-peak signal from the RF\_IN port does not exceed the bias voltage (VDD).

**Note # 5:** RF\_IN port expects a LVCMOS signal. If a clipped Sinewave or Sinewave signal with lower amplitude is used; it might be necessary to square-that-up. There is a provision above (S1) to add a buffer to achieve this. Please contact [tech-support@abracon.com](mailto:tech-support@abracon.com).

# Frequency Divider Evaluation Board

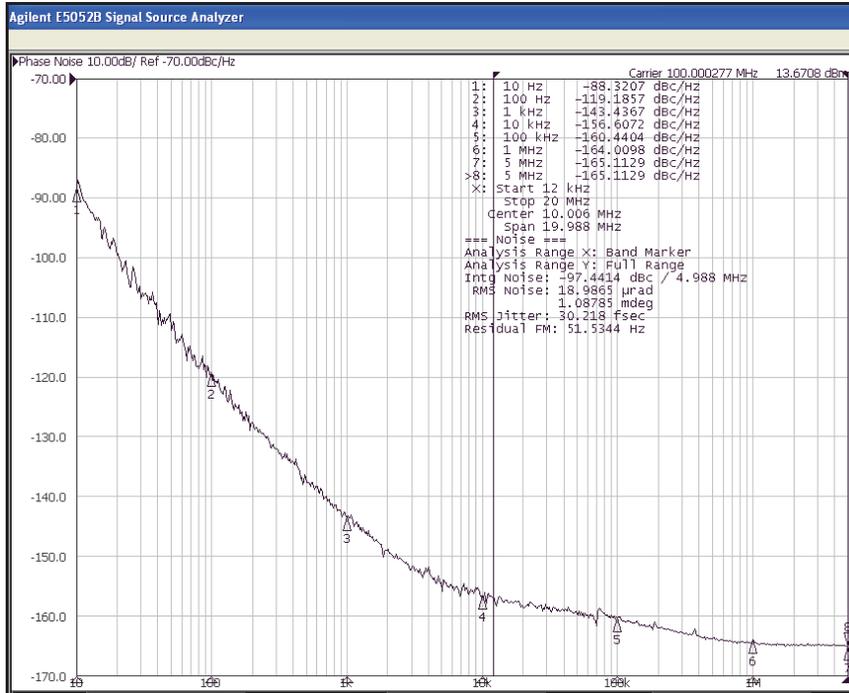
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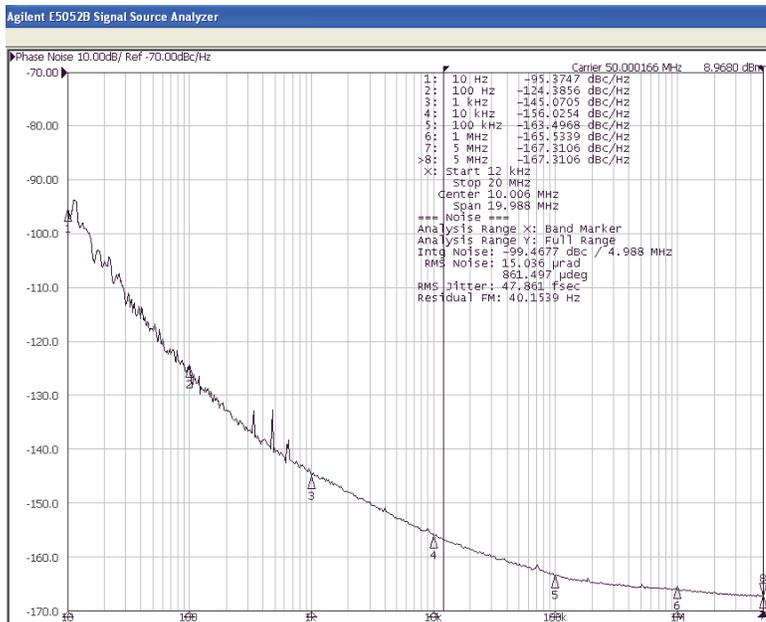
100MHz ABLNO was used to conduct  $\div 1$ ,  $\div 2$ ,  $\div 4$  and  $\div 8$  measurements

Typical Phase Noise Performance @ 100.00 MHz Carrier ( $\div 1$  Mode) @ Vdd = +3.3V (25°C±3°C)



| S1 | S2 | S3 | S4 | Description                  |
|----|----|----|----|------------------------------|
| DN | DN | DN | DN | ABLNO's RF Output = $\div 1$ |

Typical Phase Noise Performance @ 50.00 MHz Carrier ( $\div 2$  Mode) @ Vdd = +3.3V (25°C±3°C)



| S1 | S2 | S3 | S4 | Description                  |
|----|----|----|----|------------------------------|
| DN | UP | DN | DN | ABLNO's RF Output = $\div 2$ |

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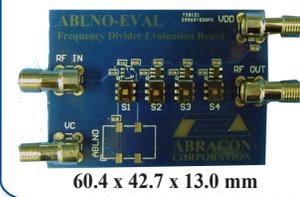
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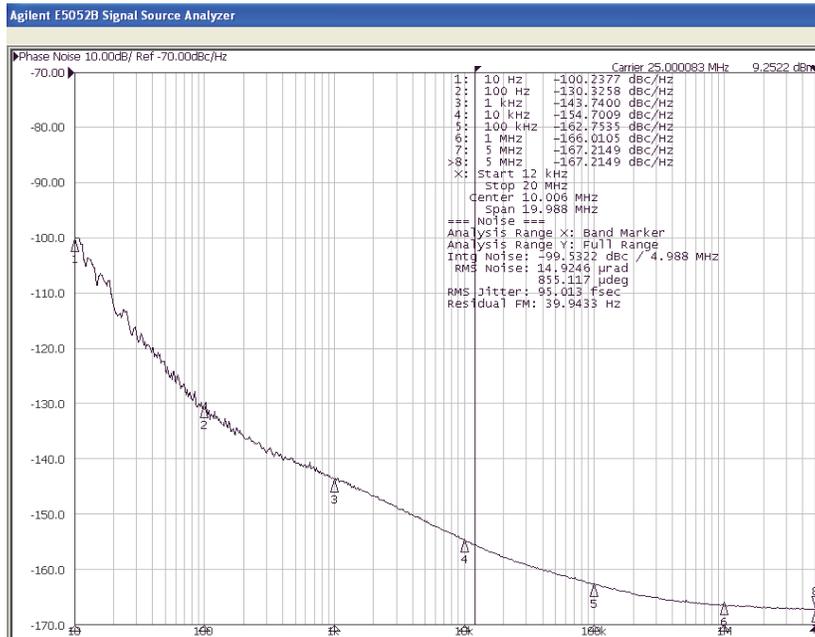
# Frequency Divider Evaluation Board

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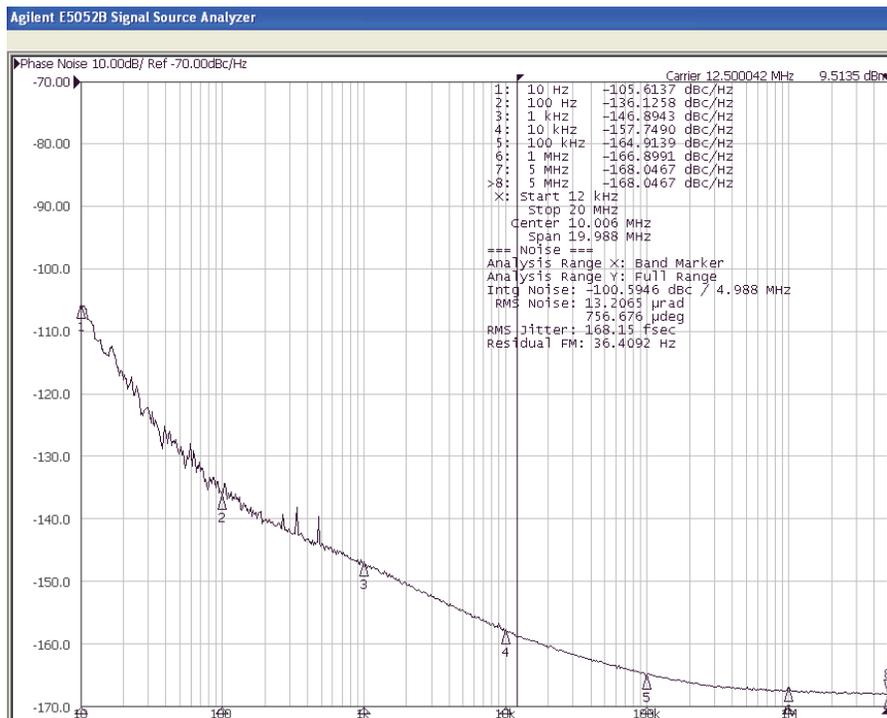


## Typical Phase Noise Performance @ 25.00 MHz Carrier ( $\div 4$ Mode) @ Vdd = +3.3V (25°C $\pm$ 3°C)



| S1 | S2 | S3 | S4 | Description                  |
|----|----|----|----|------------------------------|
| DN | UP | UP | DN | ABLNO's RF Output = $\div 4$ |

## Typical Phase Noise Performance @ 12.50 MHz Carrier ( $\div 8$ Mode) @ Vdd = +3.3V (25°C $\pm$ 3°C)



| S1 | S2 | S3 | S4 | Description                  |
|----|----|----|----|------------------------------|
| DN | UP | UP | UP | ABLNO's RF Output = $\div 8$ |

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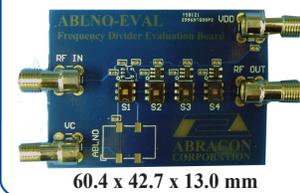
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# Frequency Divider Evaluation Board

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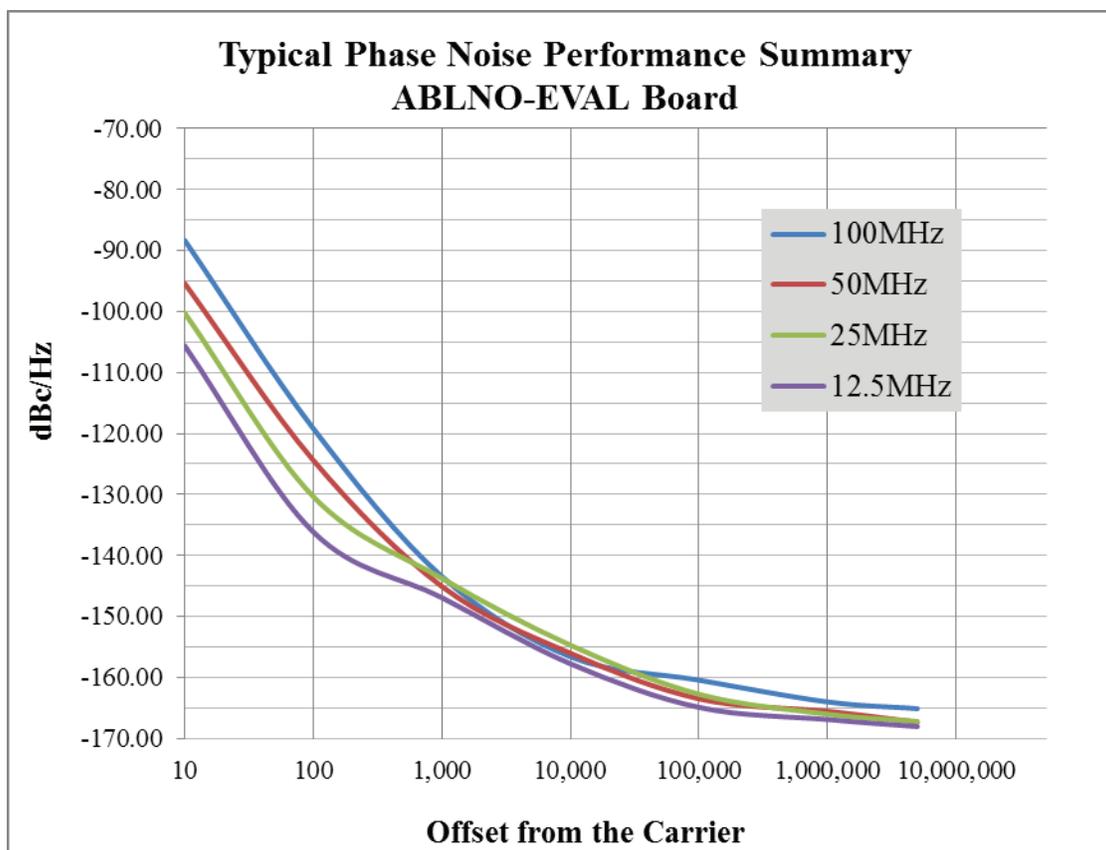
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## PHASE NOISE & RMS JITTER PERFORMANCE SUMMARY

| Offset From the Carrier | Measured Phase Noise (dBc/Hz) |         |         |         |
|-------------------------|-------------------------------|---------|---------|---------|
|                         | 100MHz                        | 50MHz   | 25MHz   | 12.5MHz |
| 10Hz                    | -88.32                        | -95.38  | -100.24 | -105.61 |
| 100Hz                   | -119.16                       | -124.38 | -130.33 | -136.13 |
| 1,000Hz                 | -143.44                       | -145.07 | -143.74 | -146.90 |
| 10,000Hz                | -156.60                       | -156.02 | -154.70 | -157.75 |
| 100,000Hz               | -160.44                       | -163.50 | -162.75 | -164.90 |
| 1,000,000Hz             | -164.00                       | -165.54 | -166.01 | -166.90 |
| 5,000,000Hz             | -165.11                       | -167.31 | -167.21 | -168.04 |

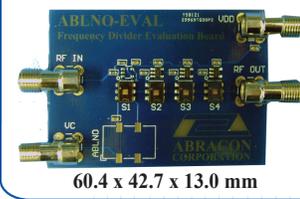
| Carrier   | 100MHz       | 50MHz | 25MHz | 12.5MHz |
|---|--------------|-------|-------|---------|
| Measured Jitter (12kHz to 20MHz) in <i>femto seconds</i>            | <b>30.22</b> | 47.86 | 95.01 | 168.15  |
| <i>Additive rms Jitter</i> (12kHz to 20MHz) in <i>femto seconds</i> |              | 17.64 | 64.80 | 137.93  |



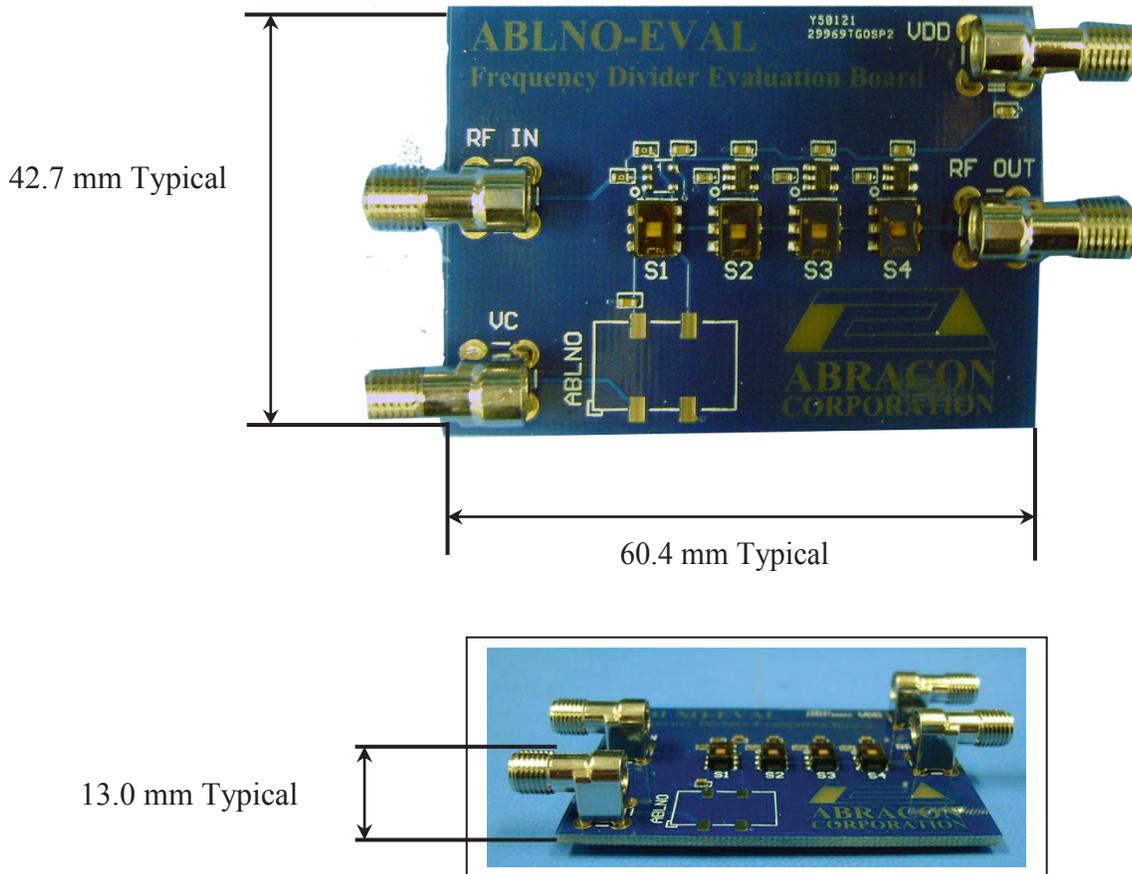
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## OUTLINE DIMENSION:



**Packaging:** Units are packaged in ESD bags, single unit per bag.

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