S-34HTS08AB

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DDR5 SPD EEPROM WITH HUB BUILT-IN TEMPERATURE SENSOR

Rev.1.1_00

This IC is a DDR5 Serial Presence Detect EEPROM with Hub function (SPD5 Hub) built in temperature sensor.
The Hub feature allows isolation of a local bus from a controller host bus. This IC contains 1024 bytes (8K-bit) of EEPROM arranged as 16 blocks of 64 bytes (512 bit) per block. Each block can be write protected via software command. Page write and sequential read are available. This IC operates with 1.8 V VDDSPD and 1.0 V VDDIO and the SidebandBus (I^2C & I3C) at 12.5 MHz maximum.

Caution **This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.**

■ Features

- JEDEC standard compliant: SPD5118
- Two-wire I^2C or I3C bus serial interface
- Operation voltage range (V_{DDSPD}): 1.7 V to 1.98 V
- Operation voltage range (V_{DDIO}): 0.95 V to 1.05 V
- Operation frequency:
  I^2C: 1.0 MHz max. (V_{DDSPD} = 1.7 V to 1.98 V)
  I3C: 12.5 MHz max. (V_{DDSPD} = 1.7 V to 1.98V)
- 1.0 V Push Pull I/O levels
- 1.0 V and 3.3 V Open Drain I/O levels
- Operation temperature range: Ta = −40°C to +125°C
- Operation temperature range (NVM Write Operation): Ta = -40°C to +95°C

EEPROM

- Page write:16 bytes / page
- Sequential read
- Write protect function during low power supply voltage
- Write protect: Individual software data protection for each of 16 blocks of 64-bytes per block
- Endurance: 10^5 cycle / word*1 (Ta = -40°C to +95°C)
- Memory capacity: 8 K-bit
- Initial delivery state: FFh

Temperature sensor

- Temperature accuracy:
  0.5°C typ. (Ta = +75°C to +95°C)
  1.0°C typ. (Ta = +40°C to +125°C)
- Temperature sample rate: 8 samples / s min.
- hysteresis width: 1.0°C

Hub Function

- Interfaces to I^2C/I3C buses which have multiple devices on a shared bus
- Uniquely addressed with fixed addressing on the same bus.
- All Hubs respond to specific predefined I^2C/I3C device select codes on a host interface bus
- Integrates a second local I^2C/I3C bus and passes through of commands from host bus onto local bus for addressing of I^2C/I3C devices on local bus

Overall

- Current consumption:
  EEPROM in standby mode and temperature sensor in active mode: 0.15 mA max.*2
  EEPROM in read operation mode and temperature sensor in active mode: 2.0 mA max.*2
  EEPROM in write operation mode and temperature sensor in active mode: 3.0 mA max.*2
- Noise suppression:
  Schmitt trigger on input pins (HSCL, HSDA, LSDA)
  Noise filter on input pins at I^2C (HSCL, HSDA)
- Packet Error Check (PEC) function
- Parity Error check function
- In Band Interrupt (IBI)
- Bus Reset function
- Up to 8 unique addressing
- 9-pin thermally enhanced DFN package

*1. For each address (Word: 8-bit)
*2. V_{DDSPD} = 1.8V

■ Block Diagram

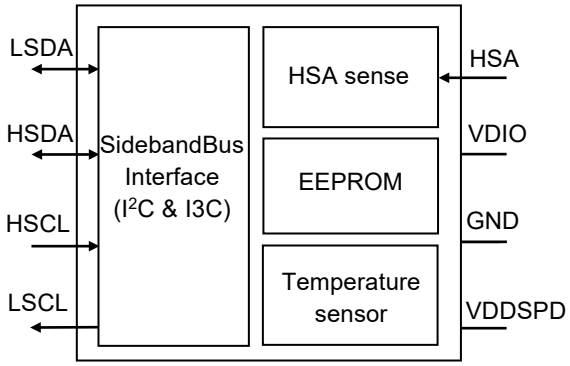

Figure 1 SPD5118 Block Diagram

■ Package

- DFN-8(2030)B

(3.0 × 2.0 × t0.8 mm)

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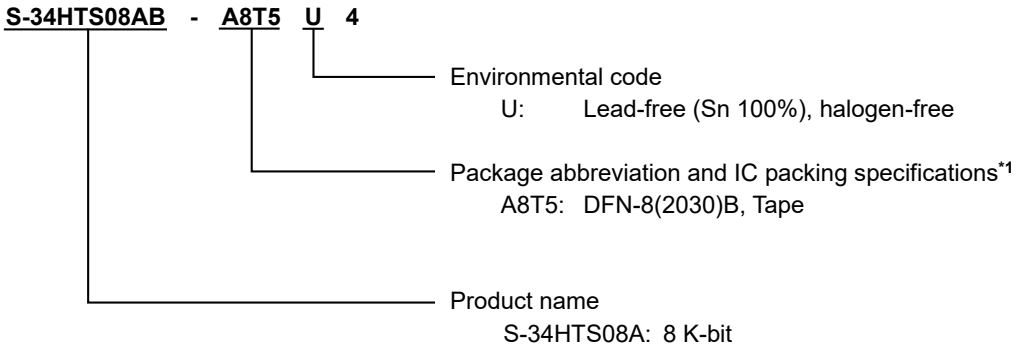
■ Product Name Structure

1. Product name



***1.** Refer to the tape drawing.

2. Product name list

Table 1 Product name list

Product Name	Capacity	Package Name
S-34HTS08AB-A8T5U4	8 K-bit	DFN-8(2030)B

3. Package

Table 2 Package

Package Name	Dimension	Tape	Reel	Land
DFN-8(2030)B	PQ008-B-P-SD	PQ008-B-C-SD	PQ008-B-R-SD	PQ008-B-L-SD

■ Pin Configuration

1. DFN-8(2030)B

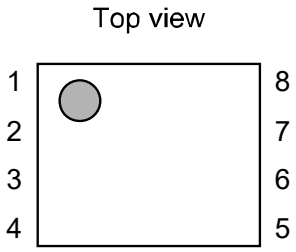


Figure 2

Table 3 Pin Configuration

Pin No.	Symbol	Pin Type	Description
1	LSDA	I/O	Local Bus - I^2C/I3C Basic Bus Data Input/Output
2	HSDA	I/O	Host Bus - I^2C/I3C Basic Bus Data Input/Output
3	HSCL	I	Host Bus - I^2C/I3C Basic Bus Input Clock
4	LSCL	O	Local Bus - I^2C/I3C Basic Bus Output Clock
5	VDDSPD	Power	1.8 V Input Power Supply. Connect minimum of 1.0 µF capacitor to GND.
6	GND	GND	Ground
7	VDDIO	Power	1.0 V Input Power Supply. Connect minimum of 1.0 µF capacitor to GND.
8	HSA	I	Host Bus - I^2C/I3C Basic Bus Address Pin. Refer to **Table 4** for HID definition.

Remark For DFN-8(2030)B package, connect the heatsink of back side to the board, and set electric potential open or GND. However, do not use it as the function of electrode.

Table 4 HSA Pin Resistor Value and Corresponding HID Values

HSA Pin Connection	3-bit HID	Comment
10.0 kΩ to GND	000	1% Resistor
15.4 kΩ to GND	001	
23.2 kΩ to GND	010	
35.7 kΩ to GND	011	
54.9 kΩ to GND	100	
84.5 kΩ to GND	101	
127 kΩ to GND	110	
196 kΩ to GND	111	
Tied directly to GND	000	Offline Mode: Write protect override enabled.

The table above shows the HSA pin resistor values and corresponding 3-bit HID for the SPD5 Hub device.

■ Function Description

1. Overview

The SPD5 Hub device S-34HTS08AB contains 1024 bytes of non-volatile memory arranged as 16 blocks of 64 bytes per block. Each block may optionally be write-protected via software command. Write protection for each block may be overridden in an offline programmer environment while overrides are prevented in normal use. The SPD5 Hub device operates from 1.8 V nominal power supply input. The SPD5 Hub device is intended to operate up to 12.5 MHz on a 1.0 V I3C Basic bus or up to 1 MHz on a 1.0 V to 3.3 V I^2C bus. It is designed to interface to I^2C/I3C Basic buses which have multiple devices on a shared bus and must be uniquely addressed with fixed addressing on the same bus. All SPD5 Hub devices respond to specific pre-defined I^2C/I3C Basic device select codes on a host interface bus. The device also incorporates a second local I^2C/I3C Basic bus and passes through of commands from the host bus onto the local bus for addressing I^2C/I3C Basic devices on the local bus (Hub function).

2. Power-up, Reset and Initialization

2. 1 Device Power Up

The SPD5 Hub device has one V_{DDSPD} power supply input.
In order to prevent inadvertent operations during power up, a Power On Reset (POR) circuit is included. On cold power on, V_{DDSPD} input supply must rise monotonically between V_{PON} and V_{DDSPD}min.
And meanwhile, V_{DDIO} input supply must rise monotonically to V_{DDIO}min without ring back to ensure proper startup.
The SPD5 Hub device uses the V_{DDIO} supply for its I/O levels and it must reach V_{DDIO}min to ensure proper operation of I^2C or I3C bus interface.
Once the V_{DDSPD} and V_{DDIO} supply is valid and stable, the SPD5 Hub device shall:

1. Once V_{DDSPD} supply is valid and stable, within t_{Sense_HSA} time, sense its HSA pin to determine if SPD5 Hub device is in application environment or in an offline tester program mode. Depending on what it senses on HSA pin, the SPD5 Hub device configures its HID code automatically based on what it detects on HSA pin at power up.
2. Enable I^2C interface within t_{INIT} time and be ready to receive the command from the host. The SPD5 Hub device is ready for operation after t_{INIT} time.

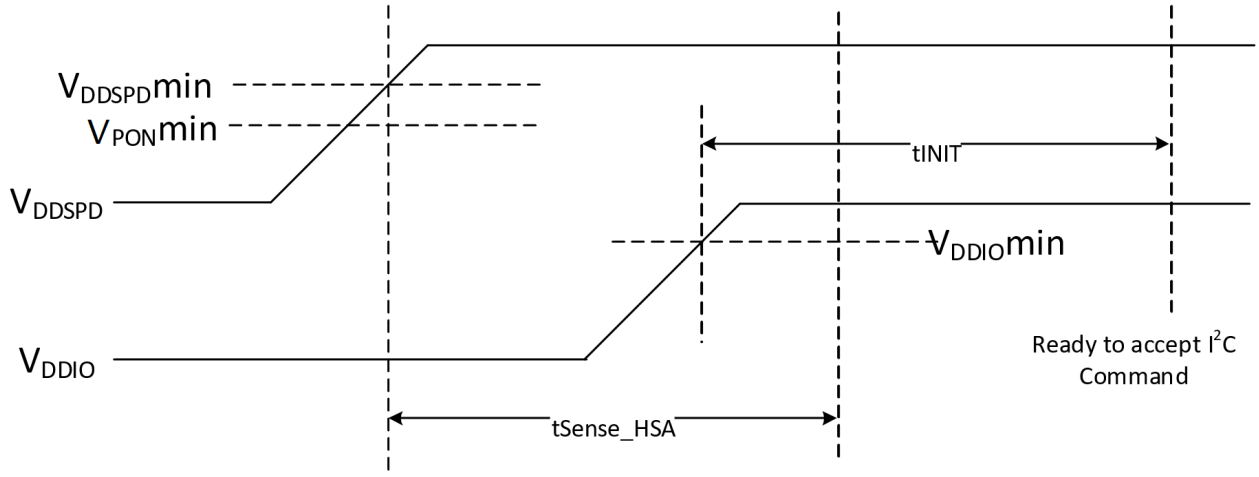


Figure 3 Device Power Up Sequence

2. 2 Device Reset and Initialization

At power down (phase during which V_{DDSPD} input supply decreases continuously), as soon as V_{DDSPD} input supply drops below the V_{DDSPD}min, the SPD5 Hub device does not guarantee the operation.
On warm power cycling, the V_{DDSPD} and V_{DDIO} input supply must remain below V_{POFF} for t_{POFF} and must meet cold power on reset timing when restoring the power.

2. 3 Bus Clear

The SPD Hub device supports the following described Bus Clear feature in I²C mode only. Any attempt by host to perform I²C Bus clear on a target device in I3C mode may result in an active drive bus contention on the SDA data line.
There may be abnormal circumstances when the host abruptly stops clocking SCL while the target device is in the middle of outputting data for read operation. For these types of events, the SDA data line may appear as stuck low as the device is expecting to receive more clock pulses from the host. Eventually when the host has control of the SCL clock, the host may optionally clear the device that is stuck low on the SDA data line by sending continuous 18 clock pulses without driving the SDA data line followed by STOP operation. The device floats the SDA line within 18 clock pulses and returns to the Idle state. The device is ready for normal new transaction with Start condition.

2. 4 Bus Reset

To prevent a malfunctioning device from locking up the I²C bus or I3C Basic bus, a bus reset mechanism is defined. It uses a timeout mechanism on HSCL as shown in **Figure 4** to force a device bus reset.
All devices (i.e., all SPD5 Hub devices and all local target devices behind the Hub) on I²C or I3C Basic bus reset simultaneously. Bus reset operation works in the same way regardless of whether the device is operating in I²C mode or I3C mode.
To guarantee the device resets the I²C or I3C Basic bus, the HSCL clock input Low time has to be greater than or equal to $t_{TIMEOUT}$ (Max).
The SPD5 Hub device will not reset I²C or I3C Basic bus if the HSCL clock input Low time is less than $t_{TIMEOUT}$ (Min). Besides, if the HSCL clock input Low time is between $t_{TIMEOUT}$ (Min) and $t_{TIMEOUT}$ (Max), the SPD5 Hub device may or may not reset the I²C / I3C Basic bus.
When RESET, the SPD5 Hub device takes the following actions:

1. Interface and any pending commands or transactions are cleared.
2. All internal register values are preserved unless noted otherwise in item # 3 below.
3. Device returns to I²C mode of operation; Register MR18[7:5] resets to '000'; MR27[4] resets to '0'; MR52[1:0] resets to '00'.
4. Device does not re-sample HSA pin.
5. Device floats HSDA such that it gets pulled High by external/other pullup. The device pulls LSDA pin High.
6. Device treats bus resets as STOP operation.

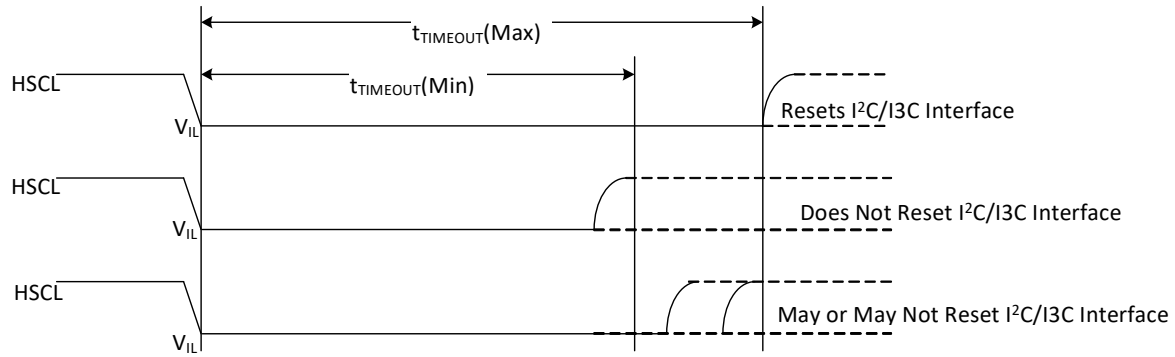


Figure 4 I²C or I3C Basic Bus Reset

3. Device Interface - IO Voltage Configuration

The SPD5 Hub device supports configurable Open Drain and Push Pull IO levels to accommodate broad range of DDR5 platform.

3. 1 Open Drain Interface

The SPD5 Hub device supports two configuration options for Open Drain interface for both Host side and Local side of the device. In this configuration, the SPD5 Hub device supports Open Drain IO levels on both Host and Local sides. However, the I/O voltage levels on Host side and Local side are independent and can be different.
On Host side, the SPD5 device can support IO levels from 1.0 V to 3.3 V depending on the supply rail Host may have pulled up the resistor to. The host side pullup resistor should be hung externally on motherboard.
On Local side, the LSCL level ranges from 1.0 V to 3.3 V depending on the supply rail Host may have pulled up the resistor to, and LSDA supports two I/O level options which depend on whether the pullup resistor selects the internal (on die) or external (on board) mode.
When register MR14[5] is configured to '0', the internal (on die) pullup resistor mode is selected (See **Figure 5**).
When register MR14[5] is configured to '1', the external (on board) pullup resistor mode is selected (See **Figure 6**).

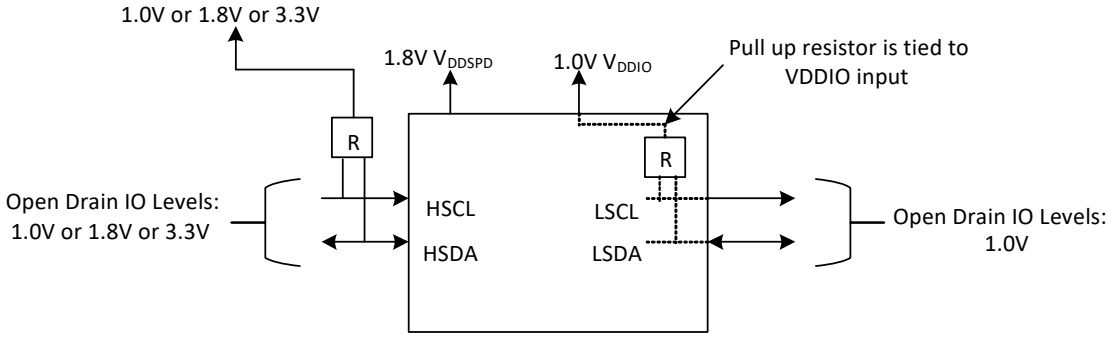


Figure 5 Open Drain Interface (Internal Pullup Resistor)

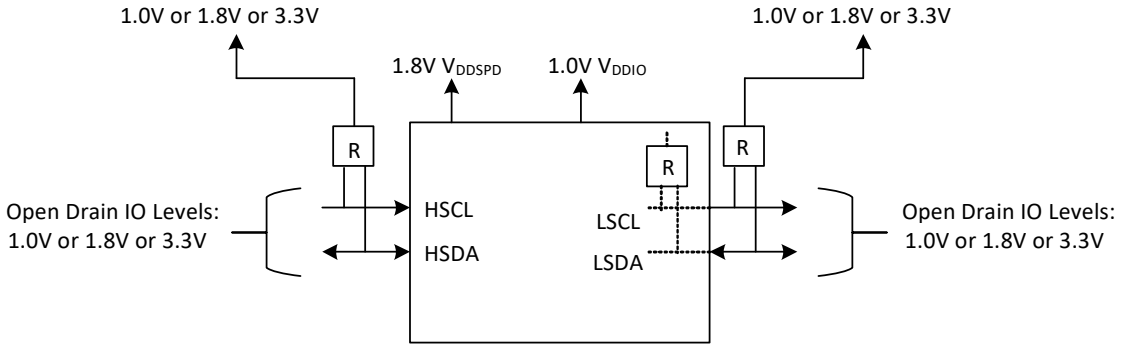


Figure 6 Open Drain Interface (External Pullup Resistor)

3. 2 Push Pull Interface

The Push Pull IO configuration is only supported when device is in I3C mode.
Figure 7 below shows the SPD5 Hub device configuration options for Push Pull interface for both Host side and local side of the device.
In this configuration, the SPD5 Hub device supports Push Pull IO levels on both Host and Local sides.

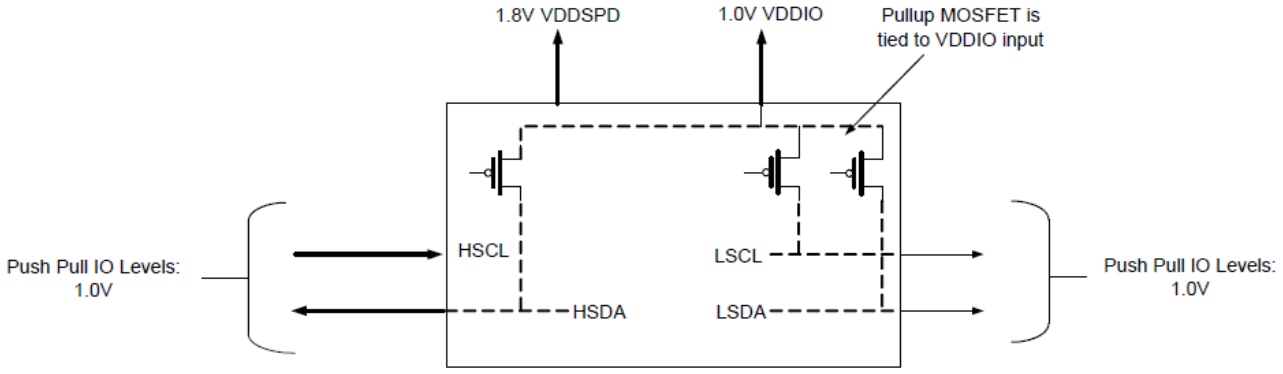


Figure 7 Push Pull Interface

3. 3 IO Operation

The SPD5 Hub device supports configurable IO operation scheme of either Open Drain or Push-Pull on its Host side of the interface (HSCL and HSDA) and Local side of the interface (LSCL and LSDA).
Further, the SPD5 Hub device supports independent IO configuration on Host side and Local side of the interface.
At power on, by default, the SPD5 Hub device comes up in legacy I^2C mode of operation with Open Drain IO for both its Host side and Local side of the interface. The maximum speed is limited to 1 MHz and supported IO voltage levels are from 1.0 V to 3.3 V.
After power on, the host may put the SPD5 Hub device in I3C mode of operation.
In I3C Basic mode, the host may drive the HSCL clock input of the SPD5 device using either Push-Pull output driver or using the open-drain output driver. It is expected that for all DDR5 DIMM family environment, the host may always drive the HSCL clock input using a Push-Pull output driver.
To support in band interrupt, the SPD5 device supports dynamic switching between Open Drain mode and Push Pull mode on its HSDA and LSDA bus for various event. **Table 5** below describes the different mode of operation by the SPD5 device for each cycle.

Table 5 SPD5 Hub Device Dynamic IO Operation Mode Switching

Supported Features	Open Drain Mode	Push Pull Mode
Start + Device Select Code	Yes	No
Start + 7'h7E IBI Header byte	Yes	No
Repeat Start + Device Select Code	No	Yes
Repeat Start + 7'h7E IBI Header byte	No	Yes
CCC Bytes	No	Yes
Stop	No	Yes
ACK/NACK Response	Yes	No
Command, Block Address, Address Operation	No	Yes
Interrupt Request by Target + Device Select Code	Yes	No
IBI Payload	No	Yes
Write Data, T-bit sequence	No	Yes
Read Data, T-bit sequence	No	Yes
PEC, T-bit sequence	No	Yes

4. Device Interface - Protocol

4. 1 I²C and I3C Protocol

This SPD5 Hub device supports both I²C and I3C interfaces. At power on, the device comes up in I²C mode of operation by default. It shall operate in I²C mode until I3C Basic mode is selected via SETAASA CCC command.

Table 6 Supported Features in I²C and I3C Basic Modes

Supported Features	I²C mode	I3C mode
Maximum operation speed	1 MHz	12.5 MHz
In-band interrupts	No	Yes
Bus reset	Yes	Yes
Parity check	No*1	Yes*2
Packet Error check	No	Yes*3

***1.** Parity check is not supported except for the supported CCCs.
***2.** Parity check is always enabled by default in I3C Basic mode.
***3.** Packet error check is supported and by default is disabled in I3C Basic mode.

4. 2 Switch from I²C Mode to I3C Basic Mode

By default, when the SPD5 Hub device first powers on, it operates in I²C mode. It shall operate in I²C mode until being put into I3C Basic mode via command.
In I²C mode, only 3 CCCs (DEVCTRL, SETHID and SETAASA) are allowed to be issued. All other CCCs are not supported. The I3C mode is selected by issuing SETAASA CCC. DEVCTRL & SETHID CCC must be issued first (if required) followed by SETAASA CCC.
When SETAASA CCC is registered by the SPD5 Hub device, it updates the register MR18[5] to '1'.
When SETHID CCC is registered by the SPD5 Hub device, it stops the 3-bit HID translation for the local Target device as explained in "**4. 5. 2 Local Device Selection (Before SETHID CCC)**".

4. 3 Switch from I3C Basic Mode to I²C Mode

The RSTDAA CCC command can put the SPD5 Hub device back in I2C mode from I3C Basic mode at any time.
When RSTDAA CCC is registered by the SPD5 Hub device, the register MR18[5] is updated to '0'.

4. 4 7-bit Serial Address

The 7-bit serial address of the SPD5 Hub device and all local devices behind the Hub applies to both I²C mode and I3C Basic mode of operation identically.
The host identifier value (HID) is merged with the SPD5 Hub Device Type ID or the local Device Type ID to establish the 7-bit address for the device on the I²C or I3C Basic bus as shown in **Table 7**.
The SPD5 Hub Device Type ID is a 4-bit binary value of 1010b. The SPD5 Hub device samples the status of the HSA pin on power up. The sampled status of the HSA pin determines the unique host ID (HID) of the device. For example, if the value sensed on HSA pin identifier is 2 (010b), then the unique 7-bit address of this device is 1010 010b.
Each local device behind the SPD5 Hub device has a unique 4-bit local device ID (LID) code. For example, the PMIC local device type ID is 1001b. The 3 HID bits of the target local device type has a default value of '111'. Thus 7-bit address of the local device, e.g., PMIC, is 1001 111b.

Table 7 7-bit Address of the SPD5 Hub Device and Local Devices

Category	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
	Device Type ID				Host ID (HID)			R/W
SPD5 Hub Device	1	0	1	0	HID[2]	HID[1]	HID[0]	Read/Write
Local Device behind the Hub	Local Device Type ID (LID)				1	1	1	Read/Write

4. 5 Device Selection on I²C / I3C Bus

4. 5. 1 SPD5 Hub Device Selection

Up to eight SPD Hub devices can be connected on a single I²C/I3C bus as shown in **Table 8**.
The host can access any SPD5 Hub device in both I²C mode and I3C Basic mode. The last 3 bits of the 7-bit address represent the HID bits.

4. 5. 2 Local Device Selection (Before SETHID CCC)

Under I²C Mode (Prior to Host issuing SETHID CCC) the host can access any local device behind the SPD5 Hub device. **Table 8** shows an example of four different local device address codes behind the SPD5 Hub device on each DIMM.
The SPD5 Hub device monitors the LID code coming from the host. When it detects the host access is for the Target device, it compares the last 3 bits of the HID information coming from the host against its own unique HID code that it has stored at power on. It compares each 3 bits one at a time. If there is a match, the SPD5 Hub device substitutes that bit with '1' and forwards it to the local device interface. If there is a mismatch, the SPD5 Hub device substitutes that bit with '0' and forwards it to the local device interface. As a result, only the targeted local device will see its last three HID bits as '111' and all non-targeted local devices will see its last three HID bits as anything other than '111' which is not a valid code.

Table 8 Device Selection on I²C / I3C Bus (Multiple Devices)

Host Access to	7-bit Address									
	SPD Hub Device		Local Devices							
			RCD		PMIC		TS0		TS1	
	LID	HID	LID	HID	LID	HID	LID	HID	LID	HID
DIMM0	1010	**000**	1011	**000**	1001	**000**	0010	**000**	0110	**000**
DIMM1		**001**		**001**		**001**		**001**		**001**
DIMM2		**010**		**010**		**010**		**010**		**010**
DIMM3		**011**		**011**		**011**		**011**		**011**
DIMM4		**100**		**100**		**100**		**100**		**100**
DIMM5		**101**		**101**		**101**		**101**		**101**
DIMM6		**110**		**110**		**110**		**110**		**110**
DIMM7		**111**		**111**		**111**		**111**		**111**

There are two exceptions where S-34HTS08AB does not substitute its own HID code when it forwards it to the Target interface:

1. Host issues Start followed by 7'h7E with W=0 (or Host issues Start followed by 0xFC).
2. After the SPD5 Hub device executes SETHID CCC command that Host issues.

Figure 8 gives an example of Host accessing Local RCD Device on DIMM0. The figure shows Host sends 7-bit address '1011 000'. Each SPD5 Hub device receives this address and then forwards the first four bits of binary address '1011' (LID) on the local device interface. Each SPD5 Hub device compares the last 3 bits of binary address '000' from the host against its own unique HID code and substitutes the bit on the local device interface.

	Hub SPD		RCD		PMIC0		PMIC1		PMIC2		TS0		TS1	
DIMM0	101 0000	50	**101 1111**	**5F**	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F	101 1111	5F
DIMM1	101 0001	51	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E	101 1110	5E
DIMM2	101 0010	52	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D	101 1101	5D
DIMM3	101 0011	53	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C	101 1100	5C
DIMM4	101 0100	54	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B	101 1011	5B
DIMM5	101 0101	55	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A	101 1010	5A
DIMM6	101 0110	56	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1001	59	101 1001	59	101 1001	59	101 1001	59	101 1001	59	101 1001	59
DIMM7	101 0111	57	101 1111	5F	100 1111	4F	100 0111	47	110 0111	67	001 0111	17	011 0111	37
Host Sends	101 1000	58												
Hub Sends			101 1000	58	101 1000	58	101 1000	58	101 1000	58	101 1000	58	101 1000	58

Figure 8 Example: Host Accessing Local Device (RCD) on DIMM0

4. 5. 3 Local Device Selection (After SETHID CCC)

When SETHID CCC is registered by the SPD5 Hub device, it stops the 3-bit HID translation for the local Target device. After Host sends SETHID CCC, the Host still accesses all the Target devices behind the SPD5 Hub device as shown in **Table 8**. There is no change in how Host access the SPD5 Hub device and all local Target devices behind the SPD Hub device before or after SETHID CCC.

4. 6 I²C Target Protocol - Host to SPD5 Hub Device

The SPD5 Hub device behaves as a Target device in the I²C Bus protocol, with all operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the Host. The START condition is followed by a 7-bit serial address (as described in **Table 7**), then a write or read bit (R/W) and terminated by an acknowledge bit (ACK). The SPD5 Hub device may NACK when it is busy performing internal write operation to EEPROM.

To allow compatibility with legacy I²C host controller, the SPD5 Hub device offers two ways to address 1024 bytes of non-volatile memory when it is operating in I²C mode only. 1 byte addressing mode is by default to access the first 128 bytes of the main array. Register MR11[2:0] is a page pointer register, which is used to configure which page to access and covers the entire 1024 bytes of the main array.

Alternatively, there is another way to access the main array, i.e., 2 bytes addressing mode. At initial power on, when register MR11[3] is set to '1', the 2 bytes addressing mode is selected to address the entire memory and hence the host is not required to go through page selection to address the entire non-volatile memory.

Moreover, 1 byte addressing mode is only applicable to the SPD5 Hub device and not applicable to the local device such as PMIC or TS or RCD device in I²C mode.

The SPD5 Hub device volatile register space does not require the page selection process as all volatile registers are within the first 128 bytes.

4. 6. 1 Write Operation – Data Packet

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = '1') or an internal register (MemReg = '0'). When MemReg = '0', there is no concept of "Block Address"; Block Address bits are treated simply as Upper Address bits.

Table 9 and **Table 10** list the write command data packet format when register MR11[3] = 0 and MR11[3] = 1 respectively.

Table 9 Write Command Data Packet, MR11[3] = 0

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr*1	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
	Data								A	
	…								A	
	Data								A	Sr or P

Table 10 Write Command Data Packet, MR11[3] = 1

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr*1	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
	0	0	0	0	Blk Addr [4:1]*2				A	
	Data								A	
	…								A	
	Data								A	Sr or P

***1.** In I²C mode, Start or Repeat Start operation followed by 7'h7E command is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered as an illegal operation.

***2.** The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.

4. 6. 2 Read Operation – Data Packet

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = '1') or an internal register (MemReg = '0'). When MemReg = '0', there is no concept of "Block Address"; Block Address bits are treated simply as Upper Address bits.

Table 11 and Table 12 show the read command data packet when MR11[3] = 0 and MR11[3] = 1 respectively.

Table 11 Read Command Data Packet, MR11[3] = 0

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr*1	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
Sr	1	0	1	0	HID			R=1	A*2	
	Data								A	
	…								A	
	Data								A	Sr or P

Table 12 Read Command Data Packet, MR11[3] = 1

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr*1	1	0	1	0	HID			W=0	A	
	MemReg	Blk Addr [0]	Address [5:0]						A	
	0	0	0	0	Blk Addr [4:1]*3				A	
Sr	1	0	1	0	HID			R=1	A*2	
	Data								A	
	…								A	
	Data								A	Sr or P

***1.** In I^2C mode, Start or Repeat Start operation followed by 7'h7E command is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered as an illegal operation.

***2.** If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. The device may eventually ACK.

***3.** The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.

4. 6. 3 Default Read Address Pointer Mode

During the normal operation of DDR5 DIMM, the host periodically may poll critical information from the same location. To help improve the efficiency of the I^2C bus protocol, the SPD5 Hub device offers a default read address pointer mode so that whenever the Hub device sees the STOP operation on its HSCL and HSDA bus, its read address pointer is always reset to default address.

The default read pointer address mode is enabled through register MR18[4] and the default starting address for read operation is selectable through register MR18[3:2]. The starting address for default read pointer address mode should be reset by Stop to the address selected through register MR18[3:2]. Compared to the standard read command data packet (shown as Table 12), the default read address pointer mode reduces the packet overhead by 3 bytes. The host typically enables this mode when the normal operation of the DDR5 DIMM begins. The default read address pointer mode is only applicable to the volatile register space.

Table 13 Read Command Data Packet with Default Address Pointer Mode

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr	1	0	1	0	HID			R=1	A	
	Data								A	
	…								A	
	Data								N	Sr or P

4. 7 I²C Target Protocol - Host to Local Device through SPD5 Hub Device

The tables below list the write and read command data packets of some typical Local Devices such as TS, PMIC, and RCD behind the SPD5 Hub device. The SPD5 Hub device simply treats all the inputs as Data and just transmits the Data to the target Local Device.

4. 7. 1 Write Operation – Data Packet

The SPD5 Hub device does not check for the PEC for its Local Devices.

Table 14 Write Command Data Packet - Local Device

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr*1	0010(TS), 1001(PMIC), 1011(RCD)				HID			W=0	A	
	Data								A	
	…								A	
	Data								A	Sr or P

***1.** In I²C mode, Start or Repeat Start operation followed by 7'h7E command is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered as an illegal operation.

4. 7. 2 Read Operation – Data Packet

Table 15 Read Command Data Packet - Local Device TS or PMIC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr*1	0010(TS), 1001(PMIC)				HID			W=0	A	
	Data (Address [7:0])								A	
Sr	0010(TS), 1001(PMIC)				HID			R=1	A*2	
	Data								A	
	Data								A	
	…								A	
	Data								A	Sr or P

***1.** In I²C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I²C mode. Any other operation including another Repeat Start is considered as an illegal operation.

***2.** If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire.

When Host makes any read request to the RCD device, the RCD protocol has PEC check for the RCD address information as well as data returned by the RCD. The SPD5 Hub simply treats the PEC information as data byte like any other data byte. The SPD5 Hub device does not check for the PEC. The RCD device requires valid stable input clock (DCK_t, DCK_c), Reset_n and DCS_n to allow any read or write access on its I²C interface.

Table 16 Read Command Data Packet - Local Device RCD (PEC Disabled, Legacy Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr*1	1	0	1	1	HID			W=0	A	
	Data (I²C Bus Command)								A	
	Data (Byte Count=4)								A	
	Data (Reserved;0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page_Num [7:0])								A	
	Data (Reg_Num [7:0])								A	P
S	1	0	1	1	HID			W=0	A	
	Data (I²C Bus Command)								A	
Sr	1	0	1	1	HID			R=1	A*2	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data [31:24])								A	
	Data (Rd Data [23:16])								A	
	Data (Rd Data [15:8])								A	
	Data (Rd Data [7:0])								A	Sr or P

Table 17 Read Command Data Packet - Local Device RCD (PEC Enabled, Legacy Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr*1	1	0	1	1	HID			W=0	A	
	Data (I^2C Bus Command)								A	
	Data (Byte Count=4)								A	
	Data (Reserved;0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page_Num [7:0])								A	
	Data (Reg_Num [7:0])								A	
	Data (PEC [7:0])								A	P
S	1	0	1	1	HID			W=0	A	
	Data (I^2C Bus Command)								A	
Sr	1	0	1	1	HID			R=1	A	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data [31:24])								A	
	Data (Rd Data [23:16])								A	
	Data (Rd Data [15:8])								A	
	Data (Rd Data [7:0])								A	
	Data (PEC [7:0])								A	Sr or P

Table 18 Read Command Data Packet - Local Device RCD (PEC Disabled, Optimized Format)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S or Sr*1	1	0	1	1	HID			W=0	A	
	Data (I^2C Bus Command)								A	
	Data (Byte Count=4)								A	
	Data (Reserved;0x00)								A	
	Data (Dev/Channel Num)								A	
	Data (Page_Num [7:0])								A	
	Data (Reg_Num [7:0])								A	
Sr	1	0	1	1	HID			R=1	A*2	
	Data (Byte Count)								A	
	Data (Status)								A	
	Data (Rd Data [31:24])								A	
	Data (Rd Data [23:16])								A	
	Data (Rd Data [15:8])								A	
	Data (Rd Data [7:0])								A	Sr or P

***1.** In I^2C mode, Start or Repeat Start operation followed by 7'h7E with W=0 is only allowed for the purpose of issuing CCCs that are allowed in I^2C mode. Any other operation including another Repeat Start is considered as an illegal operation.

***2.** If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire.

4. 8 I3C Basic Target Protocol - Host to SPD5 Hub Device

The SPD5 Hub device behaves as a Target device in the I3C Basic mode, with all operations synchronized by the serial clock. Read and Write operations are initiated by a START condition, generated by the Host. The START condition is followed by a 7-bit serial address (as described in **Table 7**), then a write or read bit (R/W) and terminated by an acknowledge bit (ACK). The SPD5 Hub device may NACK when it is busy performing internal write operation to EEPROM.

The Packet Error Code (PEC) function is disabled by default when the SPD5 Hub device is put in I3C Basic mode. The host may optionally enable this function through register MR18[7] or DEVCTRL CCC command. If PEC is enabled, the PEC field is appended at the end of all transactions and the host must complete the burst length as indicated in CMD field. In other words, the host must not interrupt the burst length pre-maturely for Write or Read operation.

The MemReg bit determines if the target of the transaction is an NVM location (MemReg = '1') or an internal register (MemReg = '0'). When MemReg = '0', there is no concept of 'Block Address'; Block Address bits are treated simply as Upper Address bits.

The 'T' bit in below table carries Parity information from the Host for each byte indicating Continuous ('1') or Stop (0') whether it is transmitting the last byte or not, prior to Repeated START. After Repeated START, 'T' bit carries information from the SPD5 Hub device.

The host may optionally allow the SPD5 Hub device to request IBI. For this case, the transactions to the SPD5 Hub device begin with the I3C Basic host issuing a START condition followed by 0xFC command. If the Hub device has a pending IBI, it transmits its 7-bit device select code followed by R=1. If no pending IBI, there is no action taken by the SPD5 Hub device.

Below tables show the I3C Basic bus write/read command data packet with optional IBI header for PEC disabled and PEC enabled cases respectively. PEC calculation does not include IBI header byte (7'h7E followed by W=0).

4. 8. 1 Write Operation – Data Packet

Table 19 Write Command Data Packet - PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr*1	1	0	1	0	HID			W=0	A*1,*2,*3	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			W=0	Blk Addr [4:1]*4				T	
	Data								T	
	…								T	
	Data								T	Sr*5 or P

Table 20 Write Command Data Packet - PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr*1	1	0	1	0	HID			W=0	A*1,*2,*3	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			W=0	Blk Addr [4:1]*4				T	
	Data								T	
	…								T	
	Data								T	
	PEC								T	Sr*5 or P

***1.** See **Figure 14** for how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
***2.** The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***3.** The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
***4.** The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
***5.** Repeat Start or Repeat Start with 7'h7E.

Table 21 Write Command Data Packet with IBI Header - PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A*1,*3	
Sr	1	0	1	0	HID			W=0	A*2,*3,*4	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			W=0	Blk Addr [4:1]*5				T	
	Data								T	
	…								T	
	Data								T	Sr*6 or P

Table 22 Write Command Data Packet with IBI Header - PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A*1,*3	
Sr	1	0	1	0	HID			W=0	A*2,*3,*4	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			W=0	Blk Addr [4:1]*5				T	
	Data								T	
	…								T	
	Data								T	
	PEC								T	Sr*6 or P

***1.** Refer to **Figure 14** to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
***2.** Refer to **Figure 15** to see how the transition occurs from Host Push Pull Operation (W=0) to Target Open Drain (ACK) and **Figure 14** to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
***3.** The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***4.** The SPD5 Hub device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
***5.** The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
***6.** Repeat Start or Repeat Start with 7'h7E.

4. 8. 2 Read Operation – Data Packet

Table 23 Read Command Data Packet - PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr*1	1	0	1	0	HID			W=0	A*1,*2,*3	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1]*4				T	
Sr	1	0	1	0	HID			R=1	A/N*5,*6	
	Data								T=1	
	…								T=1	
	Data								T=1*7,*8	Sr*9 or P

***1.** Refer to **Figure 14** for how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
***2.** The SPD5 Hub device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***3.** The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
***4.** The memory size of SPD5 hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
***5.** If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors the SPD5 Hub may eventually ACK.
***6.** Refer to **Figure 16** to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
***7.** Refer to **Figure 17** to see how Host ends Target device operation.
***8.** For NVM read memory access (i.e., MemReg = '1'), when the last byte is reached (1024 Byte) or for volatile memory access (i.e., MemReg = '0'), when the last byte (i.e., MR255) is reached (extreme rare case), the Target device sends T = '0'. Refer to **Figure 18** to see how Target device ends the operation followed by Host STOP operation.
***9.** Repeat Start or Repeat Start with 7'h7E.

Table 24 Read Command Data Packet - PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr*1	1	0	1	0	HID			W=0	A*1,*2,*3	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	CMD			R=1	Blk Addr [4:1]*4				T	
	PEC								T	
Sr	1	0	1	0	HID			R=1	A/N*5,*6	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0*7	Sr*8 or P

***1.** Refer to **Figure 14** for how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
***2.** The SPD5 Hub device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***3.** The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
***4.** The memory size of SPD5 hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
***5.** If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to PEC error parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the SPD5 Hub may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select code of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
***6.** Refer to **Figure 16** to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
***7.** Refer to **Figure 18** to see how Target device ends the operation followed by Host STOP operation.
***8.** Repeat Start or Repeat Start with 7'h7E.

Table 25 Read Command Data Packet with IBI Header - PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A*1,*3	
Sr	1	0	1	0	HID			W=0	A*2,*3,*4	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1]*5				T	
Sr	1	0	1	0	HID			R=1	A/N*6,*7	
	Data								T=1	
	…								T=1	
	Data								T=1*8,*9	Sr*10 or P

***1.** Refer to **Figure 14** for how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
***2.** Refer to **Figure 15** to see how the transition occurs from Host Push Pull Operation (W=0) to Target Open Drain (ACK) and **Figure 14** to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
***3.** The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***4.** The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
***5.** The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
***6.** Refer to **Figure 16** to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
***7.** If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors the SPD5 Hub may eventually ACK.
***8.** Refer to **Figure 17** to see how Host ends Target device operation.
***9.** For NVM read memory access (i.e., MemReg = '1'), when last byte is reached (1024 Byte) or for volatile memory access (i.e., MemReg = '0'), when last byte (i.e., MR255) is reached (extreme rare case), the Target device sends T = '0'.
***10.** Repeat Start or Repeat Start with 7'h7E.

Table 26 Read Command Data Packet with IBI Header - PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A*1,*3	
Sr	1	0	1	0	HID			W=0	A*2,*3,*4	
	MemReg	Blk Addr [0]	Address [5:0]						T	
	0	0	0	0	Blk Addr [4:1]*5				T	
	PEC								T	
Sr	1	0	1	0	HID			R=1	A/N*6,*7	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0*8	Sr*9 or P

***1.** Refer to **Figure 14** for how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
***2.** Refer to **Figure 15** to see how the transition occurs from Host Push Pull Operation (W=0) to Target Open Drain (ACK) and Figure (Handoff T to H) to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (MemReg bit).
***3.** The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***4.** The SPD5 Hub device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The SPD5 Hub device ignores the entire packet until STOP or next Repeat Start operation.
***5.** The memory size of SPD5 Hub device is limited to 1024 Bytes. SPD5 Hub device ignores Blk Addr [4] bit.
***6.** Refer to **Figure 16** to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
***7.** If Target device NACKs during Repeat Start for any reason, the host may re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity errors the SPD5 Hub may eventually ACK.
***8.** Refer to **Figure 18** to see how Target device ends the operation followed by Host STOP operation.
***9.** Repeat Start or Repeat Start with 7'h7E.

4. 8. 3 Default Read Address Pointer Mode

This mode works in the exact same way as explained in "**4. 6. 3 "Default Read Address Pointer Mode**". The tables below show the read command data packet for PEC function disabled and enabled respectively. When PEC function is enabled, register MR18[1] sets the number of bytes that the SPD5 Hub device sends out followed by the PEC calculation. If PEC is enabled, the host must complete the burst length as indicated in MR18[1] register. In other words, the host must not interrupt the burst length pre-maturely for default address pointer read operation. The default read address pointer mode is only applicable to volatile register space.

Table 27 Read Command Data Packet with Read Address Pointer Mode - PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			R=1	A*1	
	Data								T=1	
	…								T=1	
	Data								T=1*2,*3	Sr*4 or P

***1.** The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Refer to **Figure 17** to see how Host ends Target device operation.
***3.** When last byte (i.e., MR255) is reached (extreme rare case), the Targe device sends T = '0'. Refer to **Figure 18** to see how Target device ends the operation followed by Host STOP operation.
***4.** Repeat Start or Repeat Start with 7'h7E.

Table 28 Read Command Data Packet with Read Address Pointer Mode - PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	0	1	0	HID			R=1	A*1	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0*2	Sr*3 or P

***1.** The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Refer to **Figure 18** to see how Target device ends the operation followed by Host STOP operation.
***3.** Repeat Start or Repeat Start with 7'h7E.

Table 29 Read Command Data Packet with Read Address Pointer Mode & IBI Header - PEC Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A*1,*2	
Sr	1	0	1	0	HID			R=1	A*2	
	Data								T=1	
	…								T=1	
	Data								T=1*3,*4	Sr*5 or P

***1.** Refer to **Figure 14** to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).
***2.** The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***3.** Refer to **Figure 17** to see how Host ends Target device operation.
***4.** When last byte (i.e., MR255) is reached (extreme rare case), the Targe device sends T = '0'. Refer to **Figure 18** to see how Target device ends the operation followed by Host STOP operation.
***5.** Repeat Start or Repeat Start with 7'h7E.

Table 30 Read Command Data Packet with Read Address Pointer Mode & IBI Header - PEC Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A*1,*2	
Sr	1	0	1	0	HID			R=1	A*2	
	Data								T=1	
	…								T=1	
	Data								T=1	
	PEC								T=0*3	Sr*4 or P

***1.** Refer to **Figure 14** to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (Repeat Start).

***2.** The SPD5 Hub NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

***3.** Refer to **Figure 18** to see how Target device ends the operation followed by Host STOP operation.

***4.** Repeat Start or Repeat Start with 7'h7E.

4. 9 I3C Basic Target Protocol - Host to Local Device through SPD5 Hub

The tables below show examples of write and read command data packets for different types of local devices behind the SPD5 Hub device. The SPD5 Hub device simply treats all the inputs as Data and just transmits the Data to the target Local Device. These examples do not show the optional IBI header byte that Host may choose to use. All local devices behind the SPD5 Hub device also supports the IBI header byte similar to that as shown in **Table 21** and **Table 22** or **Table 25** and **Table 26**.

If PEC is enabled, the PEC Byte is appended at the end of all transactions, as shown in previous sections.

4. 9. 1 Write Operation - Data Packet

Table 31 Write Command Data Packet - Local Device (PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0010(TS), 1001(PMIC), 1011(RCD)				HID			W=0	A*1,*2,*3	
	Data								T	
	…								T	
	Data								T	Sr*4 or P

***1.** Refer to **Figure 14** to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Addr; bit [7]).
***2.** The SPD5 Hub NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***3.** The local device does not check for parity error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The local device ignores the entire packet until STOP or next Repeat Start operation.
***4.** Repeat Start or Repeat Start with 7'h7E.

4. 9. 2 Read Operation - Data Packet

Table 32 Read Command Data Packet - Local Device (PEC Disabled)

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	0010(TS), 1001(PMIC), 1011(RCD)				HID			W=0	A*1,*2,*3	
	Data								T	
	…								T	
	Data								T	
Sr	0010(TS), 1001(PMIC), 1011(RCD)				HID			R=1	A/N*4,*5	
	Data								T	
	…								T	
	Data								T=1*6	Sr*7 or P

***1.** Refer to **Figure 14** to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation (1st bit of Data).
***2.** The local device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***3.** The local device does not check for parity or PEC error in subsequent bytes when it determines 7-bit device select code issued by the host does not match with its own device code. The local device ignores the entire packet until STOP or next Repeat Start operation.
***4.** If Target device NACKs during Repeat Start for any reason, the host my re-try Repeat Start again. The host can do the Repeat Start as many times it may desire. If Target device NACKs due to parity error in previous bytes, it will always NACK regardless of how many times the Host tries Repeat Start. If there were no parity or PEC errors, the device may eventually ACK. The PEC calculation by the Target device only includes device select code of the ACK response of the Repeat start operation. In other words, if there are more than one Repeat Start operation, the Target device includes device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and all other NACK responses of the device select code of the Repeat Start are not included in PEC calculation.
***5.** Refer to **Figure 16** to see how the transition occurs from Host Push Pull Operation to Target Open Drain (ACK).
***6.** See **Figure 18** to see how Target device ends the operation followed by Host STOP operation.
***7.** Repeat Start or Repeat Start with 7'h7E.

5. Write and Read Access

5. 1 Write and Read Access - NVM Memory

Either for I^2C mode and I3C mode with PEC disabled or for I3C mode with PEC enabled, the write access to NVM memory is done within 16 byte boundary in a block. If for a given Write access to NVM memory, the address cross within the 16 byte boundary (i.e. Byte 15, Byte 31, Byte 47, Byte 63) in a block, the device stops the further operation. The write operation to remaining addresses is not executed by the SPD5 Hub device. On the other hand, the write operation to the address within the boundary is executed. The SPD5 Hub device does not loop to the first address within the 16 byte boundary in that block. It does not set any register to inform this to the host and does not generate any interrupt to the host.

Unlike write access to NVM memory, any read access to NVM memory does not impose 16 byte boundary or block boundary. The Read access to NVM memory is treated as continuous address space even if it crosses 16 byte boundary or block boundary in I^2C mode or I3C Basic mode (with or without PEC enabled). The last byte for NVM memory is the 1024th byte and when the address pointer reaches to the last byte, the SPD5 Hub device does not return any data. In I^2C mode and I3C Basic mode with PEC disabled, the host must do the STOP operation.

5. 2 Write and Read Access - Register

There is no concept of ‘Block Address’. The ‘Block Address’ is treated simply as upper address bits when MemReg = ‘0’ by the SPD5 Hub device.

For I^2C mode and I3C Basic mode with PEC disabled or PEC enabled, any access to Register memory is continuous address space even if it appears crossing 16 byte boundary or ‘Block Address’ boundary. The last byte is MR255 and when the address pointer reaches to MR255, the SPD5 Hub device does not return any data. In I^2C mode and I3C Basic mode with PEC disabled, the host must do the STOP operation.

6. Write Protection of Non Volatile Memory

6. 1 Normal Run-time Operation (HSA Pin is tied to GND via a Resistor Value)

In this mode, the SPD5 Hub device offers a write protection for its NVM memory. MR12[7:0] and MR13[7:0] registers contain a bit map for write protection status of each 64 byte block of NVM memory. MR12[7:0] and MR13[7:0] registers can be written to ‘1’ at any time. When any bit in MR12 or MR13 is set to ‘1’, further writes to that corresponding block of NVM are ignored and MR52[6] bit is set to ‘1’.

Once any bit is written to ‘1’ in registers MR12 and MR13, clearing that bit in normal run time mode is not allowed. Any attempt to clear the bit in registers MR12 and MR13 is ignored and MR52[5] bit is set to ‘1’.

6. 2 Offline Tester Operation (HSA Pin is tied directly to GND, no Resistor Value)

In this mode, the SPD5 Hub device allows to clear any bit in registers MR12 and MR13. Once cleared, the SPD5 Hub device allows to modify the corresponding block of NVM memory

6. 3 Suggested Steps to Program SPD5 Hub Device

The recommended steps to program the SPD Hub device are:

1. Connect HSA pin directly to GND (without a resistor).
2. Power up the device. The device senses HSA pin. It sets register MR48[2] = ‘1’ and enables write protection override.
3. Program registers MR12 and MR13 to enable desired NVM blocks to be written.
4. Program desired NVM blocks.
5. Program registers MR12 and MR13 to set the write protection as desired.

7. I3C Basic Common Command Codes (CCC)

The table below lists the I3C Common Command Codes (CCC) that S-34HTS08A supports.

Table 33 SPD5 Hub Supported CCC

CCC	Mode	Code	Description
ENEC	Broadcast	0x00	Enable Event Interrupts
	Direct	0x80	
DISEC	Broadcast	0x01	Disable Event Interrupts
	Direct	0x81	
RSTDAA	Broadcast	0x06	Put the device I^2C Mode (Reset Dynamic Address Assignment)
SETAASA	Broadcast	0x29	Put the device in I3C Basic Mode (Set All Addresses to Static Address)
GETSTATUS	Direct	0x90	Get Device Status
DEVCAP*1	Direct	0xE0	Get Device Capability
SETHID*1	Broadcast	0x61	SPD5 Hub updates 3-bit HID field, updates 'T' bit with updated parity calculation for all devices behind Hub and stops 3-bit HID translation.
DEVCTRL*1	Broadcast	0x62	Configure SPD5 Hub and all devices behind Hub.

***1.** JEDEC specific CCC.

The SPD5 Hub device requires STOP operation in between when switching from CCC operation to private device specific Write or Read or Default Read Address Pointer mode operation and vice versa. In other words, any CCC operation must be followed by STOP operation before continuing to any device specific Write or Read or Default Read Address Pointer mode operation. Similarly, any device specific Write or Read or Default Read Address Pointer mode operation must be followed by STOP operation before continuing to any CCC operation. The SPD5 Hub device also requires STOP operation between any direct CCC to broadcast CCC.

The SPD5 Hub device allows Repeat Start operation between any direct CCC to any other CCC or between any broadcast CCC to any other broadcast CCC or between any private Write or Read or Default Read Address Pointer mode operation to any other private Write or Read or Default Read Address Pointer mode operation.

7. 1 ENEC CCC

ENEC CCC is only supported in I3C Basic mode. It is illegal to issue this CCC in I^2C mode. When ENEC CCC is registered by the SPD5 Hub device, register MR27[4] will be updated to '1', and it will take effect at the next Start operation (after STOP condition). **Table 34** to **Table 37** show an example of a single ENEC CCC. **Table 38** shows the byte detail for ENEC CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 34 ENEC CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	Sr*2 or P

***1.** Device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Repeat Start or Repeat Start with 7'h7E.

Table 35 ENEC CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x00 (Broadcast)								T	
	0x00							ENINT	T	
	PEC								T	Sr*2 or P

***1.** Device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Repeat Start or Repeat Start with 7'h7E.

Table 36 ENEC CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x80 (Direct)								T	
Sr	DevID[6:0]							W=0	A*1,*2	
	0x00							ENINT	T	Sr*3 or P

***1.** Device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The device ignores the entire packet until STOP or next Repeat Start operation.
***3.** Repeat Start or Repeat Start with 7'h7E.

Table 37 ENEC CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x80 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A*1,*2	
	0x00							ENINT	T	
	PEC								T	Sr*3 or P

***1.** Device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The device ignores the entire packet until STOP or next Repeat Start operation.
***3.** Repeat Start or Repeat Start with 7'h7E.

Table 38 ENEC CCC Byte Detail

Bit	Detail	Notes
ENINT	0 = No Action 1 = Enable IBI Interrupt	It is illegal to issue ENEC CCC with ENINT bit = '0'

7. 2 DISEC CCC

DISEC CCC is only supported in I3C Basic mode. It is illegal to issue this CCC in I^2C mode.
When DISEC CCC is registered by the SPD5 Hub device, register MR27[4] will be updated to '0', and it will take effect at the next Start operation (after STOP condition).
Table 39 to **Table 42** show an example of a single DISEC CCC. **Table 43** shows the byte detail for DISEC CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 39 DISEC CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x01 (Broadcast)								T	
	0x00							DISINT	T	Sr*2 or P

***1.** Device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Repeat Start or Repeat Start with 7'h7E.

Table 40 DISEC CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x01 (Broadcast)								T	
	0x00							DISINT	T	
	PEC								T	Sr*2 or P

***1.** Device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Repeat Start or Repeat Start with 7'h7E.

Table 41 DISEC CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x81 (Direct)								T	
Sr	DevID[6:0]							W=0	A*1,*2	
	0x00							DISINT	T	Sr*3 or P

***1.** Device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Device does not check for parity error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The device ignores the entire packet until STOP or next Repeat Start operation.
***3.** Repeat Start or Repeat Start with 7'h7E.

Table 42 DISEC CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x81 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							W=0	A*1,*2	
	0x00							DISINT	T	
	PEC								T	Sr*3 or P

***1.** Device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Device does not check for parity or PEC error in subsequent bytes when it determines the 7-bit device select code issued by the host does not match with its own device code. The device ignores the entire packet until STOP or next Repeat Start operation.
***3.** Repeat Start or Repeat Start with 7'h7E.

Table 43 DISEC CCC Byte Detail

Bit	Detail	Notes
ENINT	0 = No Action 1 = Disable IBI Interrupt	It is illegal to issue DISEC CCC with DISINT bit = '0'

7. 3 RSTDAA CCC

RSTDAA CCC is only supported in I3C Basic mode. This CCC is ignored in I^2C mode.
When RSTDAA CCC is registered by the SPD5 Hub device, register MR18[5] will be updated to '0', and it will take effect at the next Start operation (after STOP condition). Further it disables IBI & PEC function (MR27[4] = '0' and MR18[7] = '0' respectively) and clears parity function (MR18[6] = '0').
Table 44 and **Table 45** show an example of a single RSTDAA CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 44 RSTDAA CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x06 (Broadcast)								T	Sr*2 or P

***1.** Device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Repeat Start or Repeat Start with 7'h7E.

Table 45 RSTDAA CCC - Broadcast with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x06 (Broadcast)								T	
	PEC								T	Sr*2 or P

***1.** Device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Repeat Start or Repeat Start with 7'h7E.

7. 4 SETAASA CCC

SETAASA CCC is only supported in I^2C mode. In I^2C mode, when this CCC is issued, to guarantee that this CCC is registered by the SPD5 Hub device without any error, the host shall limit the maximum speed operation for this CCC to 1 MHz. In I3C Basic mode, this CCC is ignored.

When SETAASA CCC is registered by the SPD5 Hub device, the device updates register MR18[5] = '1' and it takes in effect at the next Start operation (after STOP condition). **Table 46** shows an example of a single SETAASA CCC.

SETAASA CCC does not support PEC function as device is in I^2C mode and there is no PEC function in I^2C mode.

Table 46 SETAASA CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x29 (Broadcast)								T	P

7. 5 GETSTATUS CCC

GETSTATUS CCC is only supported in I3C Basic mode. In I^2C mode, this CCC is ignored. **Table 47** and **Table 48** show an example of a single GETSTATUS CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 47 GETSTATUS CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x90 (Direct)								T	
Sr	DevID[6:0]							R=1	A*1	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	0	P_Err	0	Pending Interrupt				T	Sr*2 or P

***1.** The device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Repeat Start or Repeat Start with 7'h7E.

Table 48 GETSTATUS CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*2	
	0x90 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A*1	
	PEC_Err	0	0	0	0	0	0	0	T	
	0	0	P_Err	0	Pending Interrupt				T	
	PEC								T	Sr*3 or P

***1.** GETSTATUS CCC with PEC check is only supported in I3C Basic mode.
***2.** The device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.
***3.** Repeat Start or Repeat Start with 7'h7E.

Table 49 GETSTATUS CCC Byte Detail

Bit	Detail	Notes
PEC_Err	0 = No Action 1 = PEC Error occurred	This register is cleared when clear command is issued to register MR20[1] for PEC error.
P_Err	0 = No Action 1 = Protocol Error, Parity Error occurred	This register is cleared when clear command is issued to register MR20[0] for Parity error.
Pending Interrupt	0000 = No Pending Interrupt 0001 = Pending Interrupt All other value is reserved	This register is cleared when clear command is issued to any appropriate device status register that causes IBI status register to get cleared.

When the SPD5 Hub device responds to GETSTATUS CCC, after it completes the response, the PEC_Err, P_Err and Pending Interrupt Bits [3:0] do not automatically get cleared. The host must explicitly clear the appropriate status register through Clear command writing '1' to corresponding register or by issuing Global Clear command. Once the device clears the appropriate status register, PEC_Err, P_Err and Pending Interrupt Bits [3:0] gets cleared. After host issues clear command, if the condition is still present, the device will again set the appropriate status register, i.e., set the IBI status register to '1' and Pending Interrupt Bits [3:0] to '0001'.

7. 6 DEVCAP CCC

DEVCAP CCC is only supported in I3C Basic mode. In I^2C mode, this CCC is ignored. **Table 50** and **Table 51** show an example of a single DEVCAP CCC.
If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 50 DEVCAP CCC - Direct

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0xE0 (Direct)								T	
Sr	DevID[6:0]							R=1	A*1	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	Sr*2 or P

***1.** The device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Repeat Start or Repeat Start with 7'h7E.

Table 51 DEVCAP CCC - Direct with PEC

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0xE0 (Direct)								T	
	PEC								T	
Sr	DevID[6:0]							R=1	A*1	
	MSB (Each bit defines capability)								T	
	LSB (Each bit defines capability)								T	
	PEC								T	Sr*2 or P

***1.** The device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.
***2.** Repeat Start or Repeat Start with 7'h7E.

Table 52 DEVCAP CCC Byte Detail

Bit	Detail	Notes
MSB[7]	RFU	Coded as '0'
MSB[6]	RFU	Coded as '0'
MSB[5]	RFU	Coded as '0'
MSB[4]	RFU	Coded as '0'
MSB[3]	RFU	Coded as '0'
MSB[2]	0 = No Support for Timer based Reset 1 = Supports Timer based Reset	SPD5 Hub hard codes to '1'
MSB[1:0]	RFU	Coded as '0'
LSB[7:0]	RFU	Coded as '0'

7. 7 SETHID CCC

SETHID CCC is only supported in I^2C mode.
In I^2C mode, when this CCC is issued, to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed operation for this CCC to 1 MHz. In I3C Basic mode, this CCC is illegal.

When SETHID CCC is registered, the device stops 3-bit HID translation. **Table 53** shows an example of a single SETHID CCC.

The host must send all '0' in the data byte followed by 'T' bit. The SPD5 Hub device forwards bits [7:4, 0] to local devices behind its Hub as it receives from the Host. The device substitutes its own 3-bit HID code in bits [3:1] and forwards it to the local devices behind the SPD5 Hub. The SPD5 Hub device also re-calculates the parity information and forwards the updated parity information in 'T' bit. As the device is in I^2C mode when SETHID CCC is issued, the PEC function is not supported.

SETHID CCC may be issued more than one time.

Table 53 SETHID CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A	
	0x61 (Broadcast)								T	
	0	0	0	0	0	0	0	0	T	P

7. 8 DEVCTRL CCC

On a typical I3C Basic bus there can be up to 120 devices. For DDR5 DIMM application environment, there are up to 8 SPD5 Hub devices, and behind each SPD5 Hub device, there are 4 local Target devices totaling up to 40 or more devices on I3C Basic bus. For certain operation such as enable or disable functions that are common to all devices (i.e., Packet Error Check), the host must go through one device at a time which takes significant amount of time at initial power up. Further, it requires additional complexity on the host because it must speak different protocol depending on how it may access the device until all devices are configured identically.

To help expedite this configuration operation and to simplify the host complexity, the device supports the DEVCTRL CCC. The DEVCTRL CCC is supported either in I^2C mode or I3C Basic mode of operation. In I^2C mode, when issuing this CCC, to guarantee that this CCC is registered by the device without any error, the host shall limit the maximum speed operation for this CCC to 1 MHz. **Table 54** and **Table 55** show an example of a single DEVCTRL CCC.

If PEC function is enabled, the PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

The host shall pay attention to DEVCTRL CCC. If DEVCTRL CCC is used to access device specific registers (i.e., RegMod = '1'), the host shall still follow any device specific register restriction. For example, if device specific register requires STOP operation for device to take in the effect of the setting, the host must also use STOP operation when using DEVCTRL CCC to access device specific register.

In I^2C mode, DEVCTRL CCC must be limited to 1 byte addressing mode for the SPD5 Hub device (i.e., MR11[3] = '0').

Table 54 DEVCTRL CCC - Broadcast

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T*2	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	Sr*3 or P

***1.** The device NACKs if there is a parity error in a previous transaction when host performs consecutive transactions with Repeat Start.

***2.** An exception is made for DEVCTRL CCC where device does report a parity error when it determines the 7-bit device select code issued by the host does not match with its own device code. The device does not check for PEC as all subsequent bytes are discarded due to parity error. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or next Repeat Start operation.

***3.** Repeat Start or Repeat Start with 7'h7E.

Table 55 DEVCTRL CCC - Broadcast with PEC*1

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S or Sr	1	1	1	1	1	1	0	W=0	A*2	
	0x62 (Broadcast)								T	
	AddrMask[2:0]			StartOffset[1:0]		PEC BL[1:0]		RegMod	T	
	DevID[6:0]							0	T*3	
	Byte 0 Data Payload								T	
	Byte 1 Data Payload								T	
	Byte 2 Data Payload								T	
	Byte 3 Data Payload								T	
	PEC								T	Sr*4 or P

***1.** DEVCTRL CCC with PEC check is only supported in I3C Basic mode.

***2.** The device NACKs if there is a parity or PEC error in a previous transaction when host performs consecutive transactions with Repeat Start.

***3.** An exception is made for DEVCTRL CCC where device does report a parity error when it determines the 7-bit device select code issued by the host does not match with its own device code. The device does not check for PEC as all subsequent bytes are discarded due to parity error. If 7-bit device select code does not match but if parity is still valid, the device does not check for parity error in subsequent bytes; ignores the entire packet and waits until STOP or next Repeat Start operation.

***4.** Repeat Start or Repeat Start with 7'h7E.

Table 56 DEVCTRL CCC Command Definition

Bit	Detail
AddrMask[2:0]	Broadcast, Unicast or Multicast Command Selection 000 = Unicast Command; SPD 5 Hub device responds if DevID[6:0] field matches with its own 7-bit address (4-bit LID + 3-bit HID) 011 = Multicast Command; SPD 5 Hub device and possible other device responds if DevID[6:3] field matches with its own 4-bit LID address 111 = Broadcast Command; All devices respond to this command Others: All other encodings are reserved.
StartOffset[1:0]	Only applicable if RegMod = '0'. Identifies the starting Byte (Byte 0 or Byte 1 or Byte 2 or Byte 3) for DEVCTRL CCC. Host can start at any Byte (from Byte 0 to Byte 3) and has continuous access to next byte until STOP operation. If Byte 3 is reached, the host is responsible for applying STOP operation. 00 = Byte 0 01 = Byte 1 10 = Byte 2 11 = Byte 3
PEC BL[1:0]	Only applicable if RegMod = '0' and PEC function is enabled. Identifies the burst length just for this DEVCTRL CCC. The device uses the setting in this field to know when the PEC byte is expected after the data bytes. 00 = 1 Byte 01 = 2 Bytes 10 = 3 Bytes 11 = 4 Bytes
RegMod	Identifies if DEVCTRL is going to be used for General Registers as identified in Byte 0 to Byte 3 or device specific address offset register. 0 = Access to General Registers in Byte 0 to Byte 3 (i.e. StartOffset[1:0] = Valid); 1 = Device Specific Offset Address (i.e. StartOffset[1:0] & PECBL[1:0] is a don't care and does not apply). The Host shall NOT use RegMod = '1' with Broadcast Command if there are different types of devices on the I3C Basic bus.
DevID[6:0]	Identifies 7-bit device address. Device responds to DEVCTRL CCC data packet depending on AddrMask[2:0]. If AddrMask[2:0] = '111', DevID[6:0] is a Don't Care and device always responds. If AddrMask[2:0] = '000', DevID[6:0] must match for device to respond. If AddrMask[2:0] = '011', DevID[6:3] must match for device to respond. DevID[2:0] is don't care. For any other codes for AddrMask[2:0], the device always NACKs.

Table 57 DEVCTRL CCC Data Payload Definition

Byte#	Bit#	Function	Definition	Comment
Byte 0	[7]	PEC Enable	0=Disable 1=Enable	MR18[7] is updated.
	[6]	Parity Disable	0=Disable 1=Enable	MR18[6] is updated.
	[5:2]	RFU	RFU	
	[1]	VR Enable	0=Disable 1=Enable	For PMIC Only SPD5 Hub device always ignores this bit.
	[0]	RFU	RFU	
Byte 1	[7:4]	RFU	RFU	
	[3]	Global & IBI Clear	0=No Action 1=Clear All event and pending IBI*1	MR27[7] is updated.
	[2:0]	RFU	RFU	
Byte 2	[7:0]	RFU	RFU	
Byte 3	[7:0]	RFU	RFU	

***1.** After Target device clears the event, the device can still have certain registers set to '1' if the event is still present in which case, the device will generate an IBI again at the next opportunity.

7. 8. 1 DEVCTRL CCC Examples - RegMod = '0'

Table 58 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTR CCC as Multicast command. Host sends Multicast command to all devices with 4-bit LID code of '1001' on I3C bus to do VR Enable followed by all devices with 4-bit LID code of '0110' to disable parity function. The host sends AddrMask = '011' to indicate Multicast command with DevID[6:3] match; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, all devices with DevID[6:3] that matches to '1001' will do the VR Enable command and DevID[6:3] that matches to '0110' will disable the parity function.

Table 58 DEVCTRL CCC Example - Multicast Command to '1001' & '0110' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A*1	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	1001 000							0	T	
	0000 0010								T	
Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	0110 000							0	T	
	0100 0000								T	P

***1.** Refer to Figure 14 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 59 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Broadcast command to enable PEC function. The host sends AddrMask = '111' to indicate Broadcast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, all devices will enable PEC function.

Table 59 DEVCTRL CCC Example - Broadcast Command to all Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A*1	
	0x62 (Broadcast)								T	
	111			00		00		0	T	
	0000 000							0	T	
	1000 0000								T	P

***1.** Refer to Figure 14 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 60 shows an example of DEVCTRL CCC data packet. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host uses DEVCTRL CCC as Unitcast command to enable VR on DIMM5. The host sends AddrMask = '000' to indicate Unicast command; StartOffset = '00' to indicate starting Byte 0 and RegMod = '0' to indicate general register. Upon receiving this command, PMIC on DIMM5 will enable its regulator.

Table 60 DEVCTRL CCC Example - Unicast Command to PMIC on DIMM5

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A*1	
	0x62 (Broadcast)								T	
	000			00		00		0	T	
	1001 101							0	T	
	0000 0010								T	P

***1.** Refer to Figure 14 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

7. 8. 2 DEVCTRL CCC Examples - RegMod = '1'

Table 61 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function enabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '0010' on the I3C Basic bus to write to address offset of 0x1C and 0x1D with data 0xFF and 0x55 respectively, followed by all devices with 4-bit LID of '1001' on the I3C bus to write to address offset of 0x15 with data 0x78.

The PEC calculation starts with Start or Repeat Start operation but does not include 7'h7E with W=0 byte in PEC calculation.

Table 61 DEVCTRL CCC Example - Multicast Command to '0010' & '1001' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	1	1	1	1	0	W=0	A*1	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	0010 000							0	T	
	0001 1100 (Address offset 0x1C)								T	
	0010 0000 (CMD field = 2 bytes of data)								T	
	1111 1111 (Data)								T	
	0001 0101 (Data)								T	
	PEC								T	
Sr	1	1	1	1	1	1	0	W=0	A*1	
	0x62 (Broadcast)								T	
	011			00		00		0	T	
	1001 000							0	T	
	0001 0101 (Address offset 0x15)								T	
	0000 0000 (CMD field = 1 byte of data)								T	
	0111 1000 (Data)								T	
	PEC								T	P

***1.** Refer to Figure 14 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

Table 62 shows an example of DEVCTRL CCC data packet for the purpose of configuring device specific address offset register. It assumes that all devices on the bus are already in I3C Basic mode with PEC function disabled and parity function enabled. In this example, the Host sends Multicast command to all devices with 4-bit LID code of '1001' on the I3C Basic bus to write to address offset of 0x13 with data 0xFF and it continues to write data 0x01 to the next address.

Table 62 DEVCTRL CCC Example - Multicast Command to '1001' Devices

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N/T	Stop
S	1	1	T	1	1	1	0	W=0	A*1	
	0x62 (Broadcast)								T	
	011			00		00		1	T	
	1001 000							0	T	
	0001 0011 (Address offset 0x13)								T	
	1111 1111 (Data)								T	
	0000 0001 (Data)								T	P

***1.** Refer to Figure 14 to see how the transition occurs from Target Open Drain (ACK) to Host Push Pull Operation.

8. Command Truth Table

The command truth table as shown in **Table 63** only applies in I3C Basic mode with PEC enabled. In I^2C mode and I3C Basic mode with PEC disabled, the command truth table does not apply.

Table 63 Command Truth Table - For I3C Basic Mode Only with PEC Enabled

Device Command	Command Name	Command Code	RW	MemReg	Block Address	Address
		2nd Byte Bits [7:5]	2nd Byte Bits [4]	1st Byte Bits [7]	2nd Byte Bits [3:0] 1st Byte Bits [6]	1st Byte Bits [5:0]
Write 1 Byte to Register	W1R	000	0	0	V	V
Read 1 Byte from Register	R1R		1	0	V	V
Write 1 Byte to NVM	W1M		0	1	V	V
Read 1 Byte from NVM	R1M		1	1	V	V
Write 2 Byte to Register	W2R	001	0	0	V	V
Read 2 Byte from Register	R2R		1	0	V	V
Write 2 Byte to NVM	W2M		0	1	V	V
Read 2 Byte from NVM	R2M		1	1	V	V
Write 2 Byte to Register	W4R	010	0	0	V	V
Read 2 Byte from Register	R4R		1	0	V	V
Write 2 Byte to NVM	W4M		0	1	V	V
Read 2 Byte from NVM	R4M		1	1	V	V
Write 16 Byte to Register	W16R	011	0	0	V	V
Read 16 Byte from Register	R16R		1	0	V	V
Write 16 Byte to NVM	W16M		0	1	V	V
Read 16 Byte from NVM	R16M		1	1	V	V
Reserved	RSVD	100 to 111	RSVD	RSVD	RSVD	RSVD

9. In Band Interrupt (IBI)

In I^2C mode, in band interrupt function is not supported. Only I3C Basic mode supports in band interrupt function.

9. 1 Enabling and Disabling IBI Function

By default, all interrupt sources are disabled. The SPD5 Hub device may enable the interrupts as described below. Once enabled, the SPD5 Hub device sends an IBI when that event occurs.

1. **Error Interrupt Enable in Table 87, "MR27" [4]:**
   a. When **Table 90**, "MR27" [4] = '1', the device sends the IBI at next available opportunity when any of the register bit in **Table 111**, "MR52" [7:5, 1:0] is set to '1' and sets **Table 107** "MR48" [7] = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.
   b. When **Table 90**, "MR27" [4] = '0', the device does not send the IBI regardless of the register bit status in **Table 111**, "MR52" [7:5, 1:0]. However, the device does set **Table 107**, "MR48" [7] = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.

2. **Temperature Sensor Interrupt Enable in Table 87, "MR27" [3:0]:**
   a. When any of the register bits in **Table 90**, "MR27" [3:0] = '1' and if **Table 90**, "MR27" [4] = '1', the device sends the IBI at next available opportunity when the corresponding register bit in **Table 110**, "MR51" [3:0] is set to '1' and sets **Table 107**, "MR48" [7] = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC.

   b. When any of the register bits in **Table 90**, "MR27" [3:0] = '0' or **Table 90**, "MR27" [4] = '0', the device does not send the interrupt regardless of the corresponding register bit status in **Table 110**, "MR51" [3:0]. However, the device does set **Table 107**, "MR48" [7] = '1' and updates Pending Interrupt Bits [3:0] = '0001' for GETSTATUS CCC if any of the bits in **Table 90**, "MR27" [3:0] = '1' and **Table 90**, "MR27" [4] = '0'.

9. 2 Mechanics of Interrupt Generation - SPD5 Hub Device

Event interrupts may be generated by the SPD5 Hub device if IBI is enabled. When there is a pending interrupt, the SPD5 Hub device requests an interrupt after detecting START condition by transmitting its 7-bit binary address followed by R/W = '1' on the SDA bus serially (synchronized by SCL falling transitions).
If the SPD5 Hub detects no START condition but if the Host to the SPD5 Hub device bus (HSDA and HSCL) has been inactive (no edges seen) for t_{AVAL} period, then the SPD5 Hub device may assert HSDA low to request an interrupt. When the SPD5 Hub device requests an interrupt, the Host toggles the HSCL. The SPD5 Hub device transmits its 7-bit binary address followed by R/W = '1'.
When the SPD5 Hub device requests an interrupt, the host may take one of the two actions below.

a. The Host sends ACK on 9th bit to accept the interrupt request. At this point, if the SPD5 Hub confirms that it has won the arbitration, the SPD5 Hub device transmits the IBI payload as shown in **Table 64** and **Table 65** for PEC disabled and PEC enabled configuration respectively. **Figure 9** just shows the first two data bits of the MDB byte to illustrate the timing. The interrupt payload contains MDB followed by 8-bit register contents of MR51 and MR52 in order. The host then issues the STOP command. Note the timing waveform in Figure 8. The host then accepts the IBI payload if it sends an ACK on 9th bit to accept the interrupt request. The host can interrupt the IBI payload at T. If host stops the IBI payload at T bit in the middle of payload, the SPD5 Hub device retains the IBI status flag MR48[7] = '1' and Pending Interrupt Bits[3:0] internally and waits for the next opportunity to request an interrupt. If the SPD5 Hub device successfully transmits the entire IBI payload, it then clears IBI status flag MR48[7] = '0' and Pending Interrupt Bits [3:0] = '0000' on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.

b. The Host sends NACK on the 9th bit as shown in **Figure 10** followed by a STOP command. In this case, the SPD5 Hub device does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, though Host sent an NACK, it does have a knowledge of which SPD5 Hub device sent the IBI request. The SPD5 Hub retains the IBI status flag MR48[7] = '1' and Pending Interrupt Bits[3:0] = '0001'. shows the first two data bits of the MDB byte to illustrate the timing.

Table 64 Read Command Data Packet w/ Default Address Pointer Mode

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	0	HID			R=1	A*1	
	MDB = 0x00								T=1	
	MR51[7:0]								T=1	
	MR52[7:0]								T=0*2	P

Table 65 Hub IBI Payload Packet - PEC is Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	1	0	1	0	HID			R=1	A*1	
	MDB = 0x00								T=1	
	MR51[7:0]								T=1	
	MR52[7:0]								T=1	
	PEC								T=0*2	P

***1.** Refer to **Figure 15** to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB, bit [7]).
***2.** Refer to **Figure 18** to see how Target device ends the operation followed by Host STOP operation.

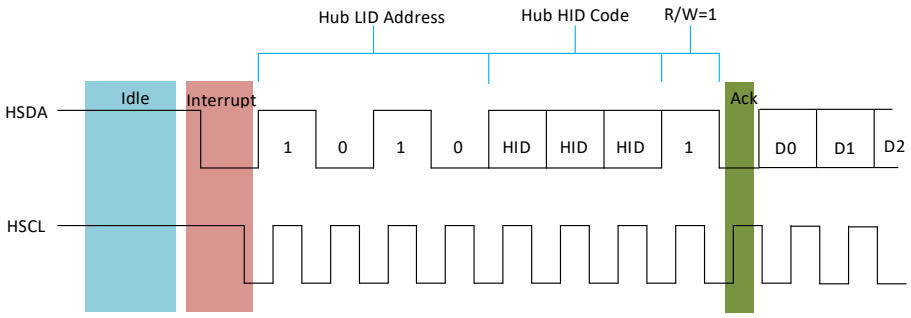


Figure 9 SPD5 Hub Interrupt - Host ACK Followed by SPD5 Hub Device IBI Payload

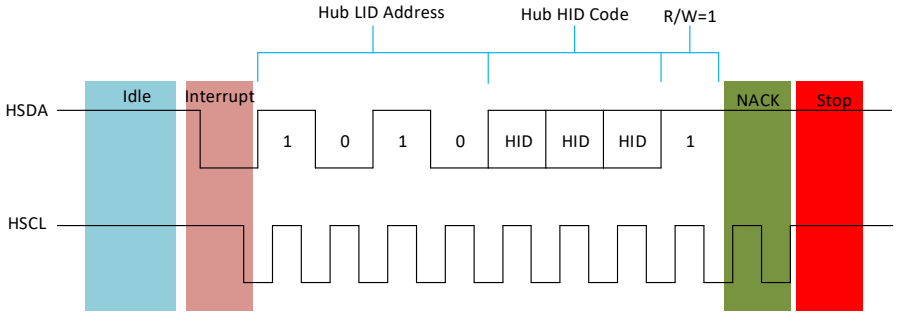


Figure 10 SPD5 Hub Interrupt - Host NACK Followed by STOP

9. 3 Mechanics of Interrupt Generation - Local Target Device

Event interrupts may be generated by the local device if IBI is enabled. When there is a pending interrupt in any local device and if IBI is enabled, the local device requests an interrupt after detecting START condition by transmitting its 7-bit binary address followed by R/W = '1' on the SDA bus serially (synchronized by SCL falling transitions).
If the local device detects no START condition but if the Host to the local target device (through the SPD5 Hub device) bus (LSDA and LSCL) has been inactive (no edges seen) for t_{AVAL} period, then any local device may assert LSDA low to request an interrupt. When the local device requests an interrupt, the SPD5 Hub device propagates the LSDA to HSDA to Host. The Host toggles the HSCL. The local device transmits its 7-bit binary address followed by R/W bit = '1' to the SPD5 Hub device. This is shown in **Figure 11** top waveform.
The SPD5 Hub device forwards LID bits it receives from the local device to the Host. The SPD5 Hub device substitutes its own HID code in place of the HID bits it receives from the local device and sends to the Host if Host has not issued SETHID CCC previously. This is shown in **Figure 11** middle waveform. The SPD5 Hub device forwards HID bits it receives from the local device to the host if Host has issued SETHID CCC previously. This is shown in **Figure 11** bottom waveform. The SPD5 Hub device forwards the R/W bit = '1' to the Host.
When the local device requests an interrupt, the host may take one of the two actions below.

a. The Host sends ACK on 9th bit to accept the interrupt request. At this point, if the local device confirms that it has won the arbitration, the local device transmits the IBI payload as shown in **Table 66** and **Table 67** for PEC disabled and PEC enabled configuration respectively. **Figure 11** just shows only first two data bits of MDB byte to illustrate the timing. The interrupt payload contains MDB followed by appropriate target device error register contents in order. The host then issues the STOP command. Note the timing waveform in **Figure 11**. The host then accepts the IBI payload if it sends an ACK on 9th bit to accept the interrupt request. The host can interrupt the IBI payload at T bit. If host stops the IBI payload at T bit in the middle of payload, the local device retains the IBI status flag and Pending Interrupt Bits [3:0] internally and waits for the next opportunity to request an interrupt. If the local device successfully transmits the entire IBI payload, it then clears IBI status flag and Pending Interrupt Bits [3:0] = '0000' on its own and does not request for an IBI again unless there is another different event occurs; for another same event, the device does not request for an IBI.

b. The Host sends NACK on the 9th bit as shown in **Figure 12** followed by a STOP command. In this case, the local device does not transmit the IBI payload and waits for the next opportunity to request an interrupt. At this point, though Host sent a NACK, it does have a knowledge of which local device sent the IBI request.
The local device retains the IBI status flag and Pending Interrupt Bits [3:0] = '0001'.

Table 66 Target Device IBI Payload Packet - PEC is Disabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	LID				HID			R=1	A*1	
	MDB = 0x00								T=1	
	First Error Code Byte								T=1	
	Second Error Code Byte								T=1	
	PEC								T=0*2	P

Table 67 Target Device IBI Payload Packet - PEC is Enabled

Start	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	A/N	Stop
S	LID				HID			R=1	A*1	
	MDB = 0x00								T=1	
	First Error Code Byte								T=1	
	Second Error Code Byte								T=1	
	…								T=1	
	PEC								T=0*2	P

***1.** Refer to **Figure 15** to see how the transition occurs from Host Open Drain (ACK) to Target Push Pull Operation (1st bit of MDB, bit [7]).
***2.** Refer to **Figure 18** to see how Target device ends the operation followed by Host STOP operation.

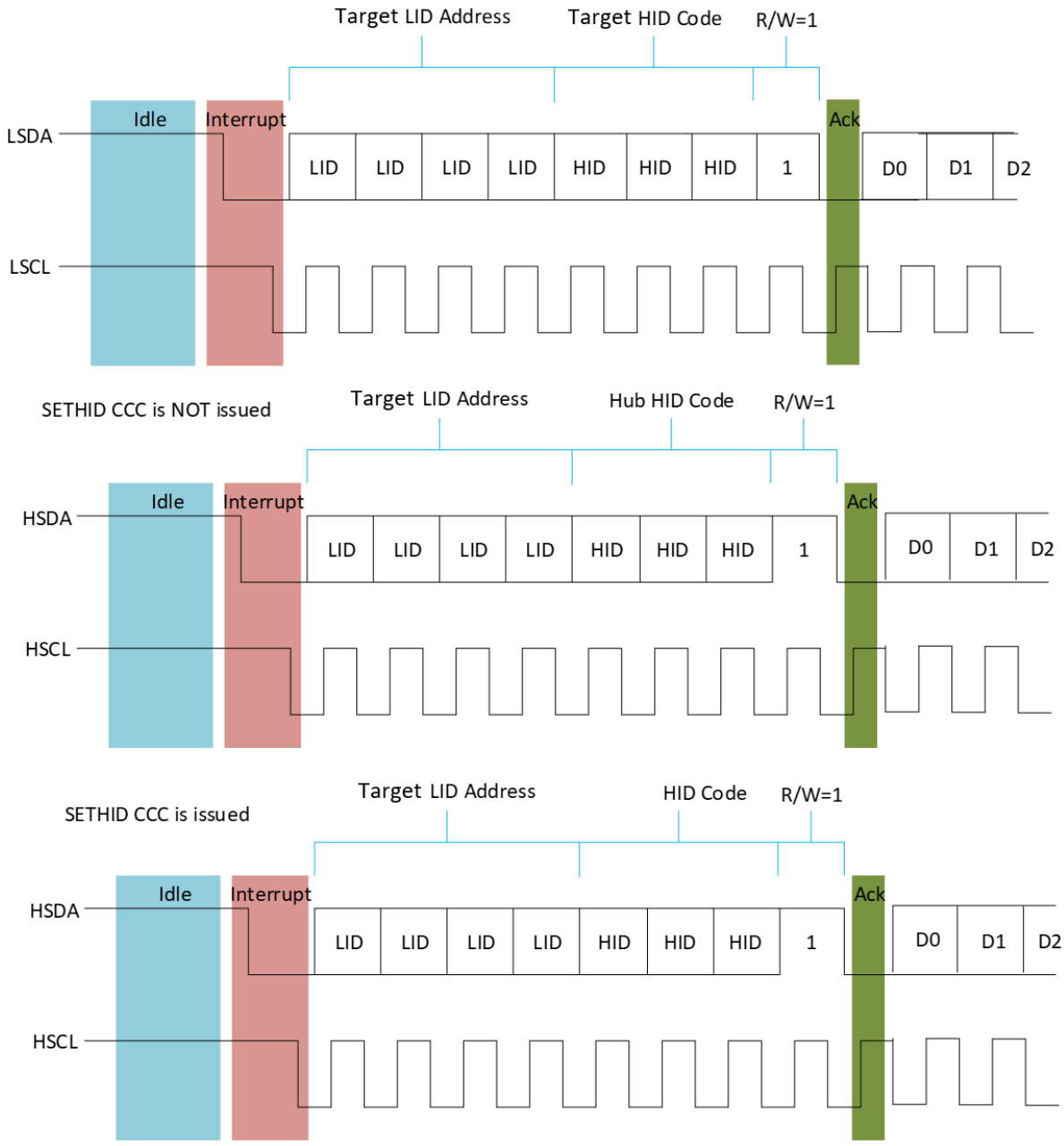


Figure 11 Local Device Interrupt - Host ACK Followed by Target Device IBI Payload

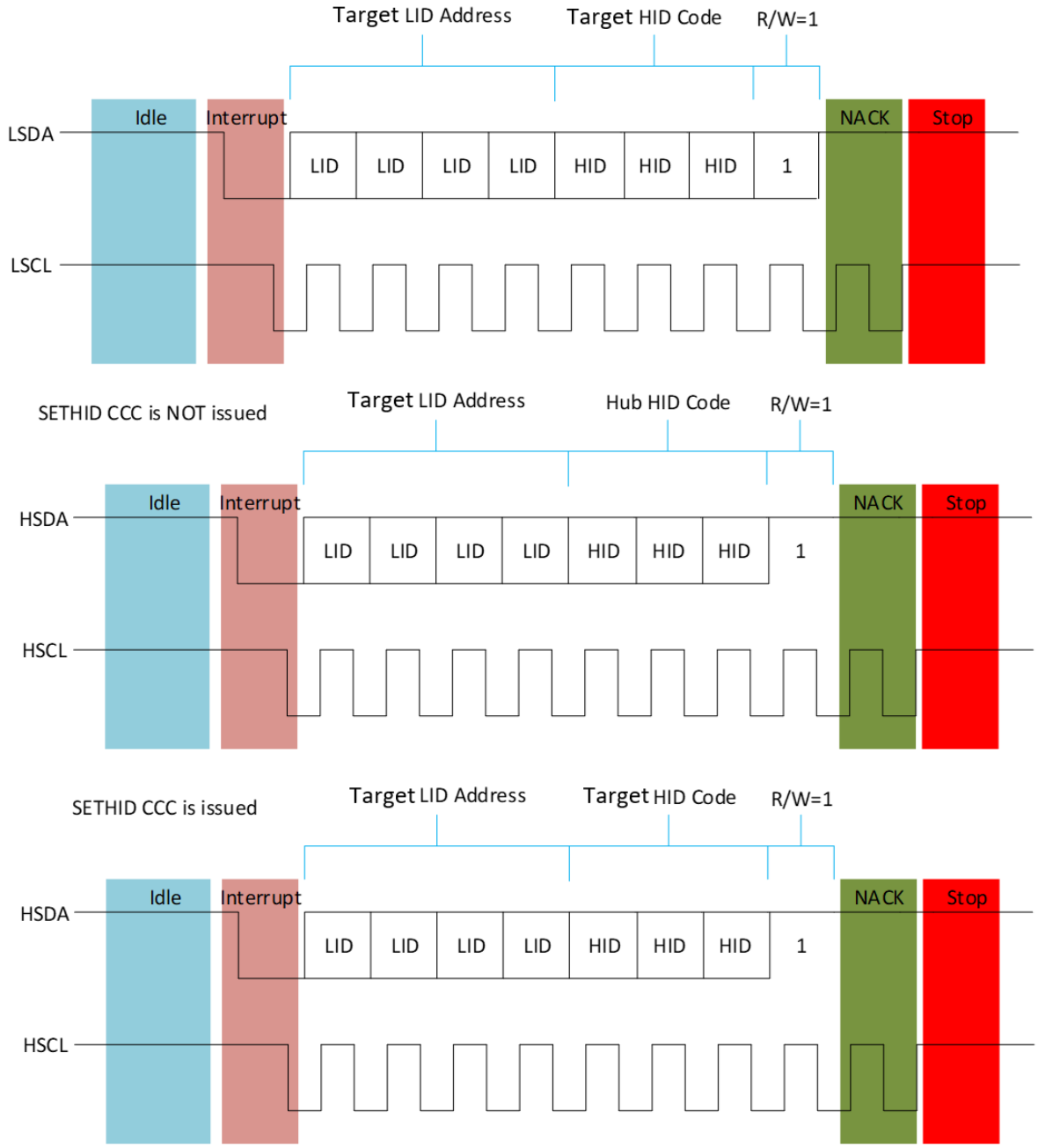


Figure 12 Local Device Interrupt - Host NACK Followed by STOP

9. 4 Interrupt Arbitration: SETHIDD CCC is not issued by Host

As there are multiple local target devices behind one SPD5 Hub device and there are multiple SPD5 Hub devices on I3C Basic bus, multiple devices may request an interrupt when the I3C Basic bus is inactive for t_{AVAL} period. Arbitration process is required.

9. 4. 1 Interrupt Arbitration - Among Multiple SPD5 Hub Devices

There are up to 8 SPD5 Hub devices on the I3C Basic bus.
As all SPD5 Hub devices have the same 4-bit LID code of '1010', the arbitration is always won by the lower HID code. For example, if one SPD5 Hub device has HID code of '000' and other SPD5 Hub device has a HID code of '011', through the arbitration process, the HID code of '000' wins. The SPD5 Hub device with a HID code of '011' must release the bus and wait for next opportunity to request an interrupt. **Table 68** shows the arbitration priority based on the HID code for the SPD5 Hub device.

Table 68 Interrupt Arbitration - Among SPD5 Hub Devices

Hub Device LID Code	Hub Device HID Code	Arbitration Priority
1010	000	1
1010	001	2
1010	010	3
1010	011	4
1010	100	5
1010	101	6
1010	110	7
1010	111	8

9. 4. 2 Interrupt Arbitration - Among Local Target Device behind one SPD5 Hub Device

There are up to 13 local devices behind one SPD5 Hub device.
As all local target devices behind the SPD5 Hub devices have the same 3-bit HID code, hence the arbitration is always won by the lower LID code. For example, if one local target device has LID code of '1001' and other local target device has a LID code of '0010', through the arbitration process, the LID code of '0010' wins. The local device with a LID code of '1001' must release the bus and wait for next opportunity to request an interrupt.
Table 69 shows the arbitration priority based on the LID code for the local devices. During the interrupt arbitration phase, the SPD5 Hub device forwards the winning 4-bit LID code one digit at a time that it receives from the local target devices to the Host.
The SPD5 Hub device discards the 3-bit '111' HID code received from the local target device. Instead the SPD5 Hub device forwards its own unique 3-bit HID code one digit at a time to the host. As a result, the Host can identify the winning device based on the 4-bit LID code (Local target device) and 3-bit HID code (the DIMM). Also, when the SPD5 Hub device substitutes its own unique 3-bit HID code to the host, its own receiver will see that at the input and it compares each 3 bits one at a time against it if the host sent those 3 bits. If there is a match, the SPD5 Hub device forwards '1' to the local device interface and if there is a mis-match, the SPD5 Hub device forwards '0' to the local device interface. Because the local target device sends '111' as its 3 bit HID code, the local device knows that it won the arbitration.

Table 69 Interrupt Arbitration - Among Local Devices

Device Local	Local Device LID Code	Local Device HID Code	Arbitration Priority
-	0001	111	1
TS0	0010	111	2
-	0011	111	3
-	0100	111	4
-	0101	111	5
TS1	0110	111	6
-	0111	111	7
PMIC1	1000	111	8
PMIC0	1001	111	9
SPD5 Hub	1010	HID	N/A
RCD	1011	111	10
PMIC2	1100	111	11
-	1101	111	12
-	1110	111	13

9. 4. 3 Interrupt Arbitration - Between SPD5 Hub Device and its Local Target Devices

There are up to 13 local devices behind each SPD5 Hub.
As the SPD5 Hub device LID code of '1010', any local target devices with a lower LID code always win the arbitration process as shown in **Table 69**. For the local target devices with a higher LID code than '1010', the SPD5 Hub device wins the arbitration process.

9. 4. 4 Interrupt Arbitration - Among Local Target Devices behind Different SPD5 Hub Devices

There are up to 8 SPD5 Hub devices on the I3C Basic bus and up to 13 local devices behind each SPD5 Hub. The arbitration process is hybrid of Section **"4. 5. 1 SPD5 Hub Device Selection" to "4. 5. 3 Local Device Selection (After SETHID CCC)"**. The device with the lowest 4 bit LID code across all local target devices and across all SPD5 Hub devices always wins the arbitration process. The HID code for that lowest LID code represents the SPD5 Hub device code.
Table 70 shows four examples. In each example, the target LID code column represents the local target device behind hub which has HID code value of '111'; the Hub HID code column represents the SPD5 Hub device which has LID code of '1010' followed by its own unique HID code; the winning device column represents the final winner among all devices (either SPD Hub device or local target devices) during the arbitration phase.

Example 1: There are total of 5 devices (4 local target devices and 1 Hub device) that are requesting an interrupt. These 5 devices are shown in the underlined text. The devices that are in the no underlined text are not requesting an interrupt. The winning device is the local device LID code of '0010' and HID code of '111'. This is because the LID code of '0010' is the lowest among three other local target device code and its HID code is '111'.

Example 2: There are total of 4 devices (2 local target devices and 2 Hub devices) that are requesting an interrupt. These 4 devices are shown in the underlined text. The devices that are in the no underlined text are not requesting an interrupt. The winning device is the local device LID code of '1001' and HID code of '100'. This is because the LID code of '1001' is the lowest among one other local target device code and its HID code is '100'.

Example 3: There are total of 3 devices (2 local target devices and 1 Hub device) that are requesting an interrupt. These 3 devices are shown in the underlined text. The devices that are in the no underlined text are not requesting an interrupt. The wining device is the Hub device on DIMM0 with LID code of '1010' and HID code of '000'. This is because LID code '1010' is lower than two other local target device codes and its HID code is '000'.

Example 4: There are total of 2 devices (2 local target devices) that are requesting an interrupt. These 2 devices are shown in the underlined text. The devices that are in the no underlined text are not requesting an interrupt. This example is unique as two identical target devices across two different DIMM device is requesting an interrupt. The winning device is the local target device on DIMM0 with LID code of '0010' and DIMM0 HID code of '000'. This is because DIMM0 HID code '000' is lower than DIMM2 HID code of '010'.

Table 70 Interrupt Arbitration - Among Local Target and SPD5 Hub Devices

Example 1			Example 2			Example 3			Example 4		
Target LID Code	Hub HID Code	Winning Device	Target LID Code	Hub HID Code	Winning Device	Target LID Code	Hub HID Code	Winning Device	Target LID Code	Hub HID Code	Winning Device
0010 0110 **1001** 1011	000		0010 0110 1001 1011	000		0010 0110 1001 **1011**	**000**	1010 000	**0010** 0110 1001 1011	000	0010 000
0010 **0110** 1001 1011	001		0010 0110 1001 1011	001		0010 0110 1001 1011	001		**0010** 0110 1001 1011	001	
0010 0110 1001 1011	010		0010 0110 1001 1011	**010**		0010 0110 1001 **1011**	010		0010 0110 1001 1011	010	
0010 0110 **1001** 1011	011		0010 0110 1001 1011	**011**		0010 0110 1001 1011	011		0010 0110 1001 1011	011	
0010 0110 1001 1011	100		0010 0110 **1001** 1011	100	1001 100	0010 0110 1001 1011	100		0010 0110 1001 1011	100	
0010 0110 1001 1011	**101**		0010 0110 1001 1011	101		0010 0110 1001 1011	101		0010 0110 1001 1011	101	
0010 0110 1001 1011	110		0010 0110 1001 **1011**	110		0010 0110 1001 1011	110		0010 0110 1001 1011	110	
0010 0110 1001 1011	111	0010 111	0010 0110 1001 1011	111		0010 0110 1001 1011	111		0010 0110 1001 1011	111	

9. 4. 5 Interrupt Arbitration - Between Host and Any SPD5 Hub or Any Local Target Devices

When the bus is idle for t_{AVAL} time, any SPD5 Hub device or any local device behind the Hub can request an interrupt by pulling the SDA bus low.
In an uncommon but possible scenario would be that at the exact same time as when the SPD5 Hub or local target devices are requesting an interrupt, the host is starting an operation to the Hub or local target devices. When this happens, Host also gets involved in the arbitration process along with the Hub or the local target devices. During the arbitration phase, there will be always only one winning device and it could be either Hub or the local target device or the Host.
If the host wins during the arbitration phase, it continues with normal operation. The losing Hub or local target device waits for next opportunity to send an interrupt.

If the host loses during the arbitration phase, it must let go of the bus. When Host loses during the arbitration, the host must let the Hub or local target device finish sending their 4-bit LID code followed by 3-bit HID code followed by R/W = '1'. At this point, during the 9th bit, the host has two options to take the action as noted below:

a. Host sends an ACK to accept the interrupt and hence accepts the IBI payload from the winning SDP5 Hub or local target device. After the IBI payload, the host issues STOP operation.
b. Host sends a NACK followed by STOP operation.

In a rare but still possible scenario would be that at the exact same time as when the Hub or local target device is requesting an interrupt, the host is starting an operation to that same exact hub or local target devices. When this happens, neither Host nor the hub or local target device knows it is a winner until the 8th bit and Host always wins. This is because, the hub or local target device sends R=1 (8th bit) during the interrupt. The host sets W=0 (8th bit) during the operation. As a result, the host wins and the hub or target device must let go of the bus and wait for the next opportunity to send an interrupt. This is shown as example 3 in **Table 71**.
Table 71 shows three examples. In each example, the Host is targeting an operation to the device cod. The target LID code column represents the local target device behind hub which has HID code value of '111'; the Hub HID code column represents the SPD5 Hub device which has LID code of '1010' followed by its own unique HID code; the winning device column represents the final winner among all devices (either Host or SPD5 Hub device or local target devices) during the arbitration phase.

Example 1, there are total of 5 devices (1 Hub device and 4 local target devices) that are requesting an interrupt at exactly same time as when the Host is starting an operation to the hub device on DIMM3 (1010 011). The winning device is local target device '0010 111' because it has the lower 4-bit LID code.

Example 2, there are total of 4 devices (2 Hub devices and 2 local target devices) that are requesting an interrupt at exactly same time as when the Host is requesting an operation to the local target device on DIMM5 (0110 101). The host is the winner because it is intended target device that has the lower 4-bit LID code than devices that are requesting an interrupt.

Example 3, there is 1 hub device on DIMM2 that is requesting an interrupt at exactly the same time as when Host is requesting an operation to the same exact Hub device on DIMM2. In this case, the host is the winner because the 8-bit will be driven low by the Host (W=0) while the Hub device drives it high (R=1) during the interrupt.

In an extreme rare but still possible scenario would be that at the exact same time as when the Hub or local target device is requesting an interrupt, the host is requesting a read operation with default read address pointer mode to the same exact hub or local target device. When this happens, there is no winning device. This is the only time there is no winning device. This is because, the hub or local target device sends R=1 (8th bit) during the interrupt and Host also sends R=1 for read request with default read address pointer mode. As a result, there is no winner because all devices, i.e. the Host or the hub or the local target device, are waiting for other device to ACK. In this case, no device will ACK. Since there is no ACK by any device, the Host must time out and repeats the read request with Repeat Start. When it repeats the read request with Repeat Start, the hub or local target device does not send an interrupt because of Repeat Start.

Table 71 Interrupt Arbitration - Best Host and Local Target and SPD5 Hub Devices

Example 1				Example 2				Example 3			
Host Target Device	Target LID Code	Hub HID Code	Winning Device	Host Target Device	Target LID Code	Hub HID Code	Winning Device	Host Target Device	Target LID Code	Hub HID Code	Winning Device
1010 011	0010 0110 **1001** 1011	000		0110 101	0010 0110 1001 1011	000		1010 010	0010 0110 1001 1011	000	
	0010 **0110** 1001 1011	001			0010 0110 1001 1011	001			0010 0110 1001 1011	001	
	0010 0110 1001 1011	010			0010 0110 1001 1011	**010**			0010 0110 1001 1011	**010**	Host operation to 1010 010
	0010 0110 **1001** 1011	011			0010 0110 1001 1011	**011**			0010 0110 1001 1011	011	
	0010 0110 1001 1011	100			0010 0110 **1001** 1011	100			0010 0110 1001 1011	100	
	0010 0110 1001 1011	**101**			0010 0110 1001 1011	101	Host operation to 0110 101		0010 0110 1001 1011	101	
	0010 0110 1001 1011	110			0010 0110 1001 **1011**	110			0010 0110 1001 1011	110	
	0010 0110 1001 1011	111	0010 111		0010 0110 1001 1011	111			0010 0110 1001 1011	111	

9. 5 Interrupt Arbitration: SETHIDD CCC is Issued by Host

The interrupt arbitration process works in similar way as defined in Section 9. 4 but with a simplification. It is assumed that in this case, all the target devices behind the Hub across all DIMMs on I3C Basic bus have a unique 7-bit device select code. Further, it assumes that all devices on a DIMM has the same 3-bit HID code.
The SPD5 Hub device forwards the 4-bit LID code and 3-bit HID code one digit at a time that it receives from the local target devices to the Host. The SPD5 Hub device's own receiver will see the same input and it forwards it back to the local device interface.

9. 5. 1 Interrupt Arbitration - Between SPD5 Hub Device and Local Target Devices

On any given DIMM, the arbitration is always won by the device that has the lowest 4-bit LID code since all devices on the DIMM has same 3-bit HID code.

9. 5. 2 Interrupt Arbitration - Between All SPD5 Hub Devices and All Local Target Devices

Across multiple DIMMs, the arbitration is always won by the device that has the lowest 7-bit address (4-bit LID + 3-bit HID).

9. 5. 3 Interrupt Arbitration - Between Host and All Devices

In an uncommon but possible scenario would be that at the exact same time as when the target device is requesting an interrupt, the host is starting an operation to the target device. When this happens, Host also gets involved in the arbitration process along with the target devices. During the arbitration phase, there will be always only one winning device and it could be either Host or the target device.
If the host wins during the arbitration phase, it continues with normal operation. The losing target device waits for next opportunity to send an interrupt.
If the host loses during the arbitration phase, it must let go of the bus. When Host loses during the arbitration, the host must let the target device finish sending their 4-bit LID code followed by 3-bit HID code followed by R/W = '1'. At this point, during the 9th bit, the host has two options to take the action as noted below:

a. Host sends an ACK to accept the interrupt and hence accepts the IBI payload from the winning target device. After the IBI payload, the host issues STOP operation.
b. Host sends an NACK followed by STOP operation.

In a rare but still possible scenario would be that at the exact same time as when the SPD5 Hub device is requesting an interrupt, the host is starting an operation to that same SPD5 Hub device. When this happens, neither Host nor the SPD5 Hub device knows it is a winner until the 8th bit and Host always wins. This is because, the SPD5 Hub device sends R=1 (8th bit) during the interrupt. The host sets W=0 (8th bit) during the operation. As a result, the host wins and the SPD5 Hub device must let go of the bus and wait for the next opportunity to send an interrupt.
In an extreme rare but still possible scenario would be that at the exact same time as when the SPD5 Hub device is requesting an interrupt, the host is requesting a read operation with default read address pointer mode to the SPD5 Hub device. When this happens, there is no winning device. This is the only time there is no winning device. This is because, the SPD5 Hub device sends R=1 (8th bit) during the interrupt and Host also sends R=1 for read request with default read address pointer mode. As a result, there is no winner because all devices, i.e. the Host or the SPD5 Hub device, are waiting for other device to ACK. In this case, no device will ACK. Since there is no ACK by any device, the Host must time out and repeats the read request with Repeat Start. When it repeats the read request with Repeat Start, the SPD5 Hub device does not send an interrupt because of Repeat Start.

9. 6 Clearing Device Status and IBI Status Register

The SPD5 Hub device provides the IBI status in register MR48[7] by setting it to '1'. The SPD5 Hub device clears the IBI status register MR48[7] to '0' automatically when it sends a complete IBI (including payload and without interruption) and it also clears Pending Interrupt Bits [3:0] to '0000'. Once IBI status register is cleared, the SPD5 Hub does not request for an IBI again unless another event occurs.
The SPD5 Hub device provides the device status in register MR52. The status information in MR52 is latched and remains set even after the SPD5 Hub device sends IBI payload and clears the IBI status register MR48[7] to '0'. The host must explicitly clear the status register through Clear command by writing '1' for appropriate status or by issuing a Global clear command.
After Host issues clear command, if the condition is no longer present, the SPD5 Hub device clears the appropriate status register, clears the IBI status register to '0' and Pending Interrupt Bits [3:0] to '0000' even if the SPD5 Hub device has not sent the IBI. After Host issues clear command, if the condition is still present, the device will again set the appropriate status register, set the IBI status register to '1' and Pending Interrupt Bits [3:0] to '0001' even if the device has already sent the IBI and entire IBI payload.

10. Error Check Function

10. 1 Packet Error Check (PEC) Function

In I^2C mode, packet error checking is not supported. Only I3C Basic mode supports packet error checking.
The SPD5 Hub device implements an 8-bit Packet Error Code (PEC) which is appended at the end of all transactions if PEC is enabled through DEVCTRL CCC or by directly writing '1' to MR18[7]. The PEC is a CRC-8 value calculated on all the message bytes except for START, REPEATED START, STOP conditions or T-bits, ACK and NACK and IBI header (7'h7E followed by W=0) bits.
The polynomial for CRC-8 calculations is:

$$C(X) = X^8 + X^2 + X^1 + 1$$

The seed value for PEC function is all zero. When Host calculates PEC for SPD5 Hub device, it includes LID and HID bits followed by R/W bit.

10. 2 Parity Error Check Function

In I^2C mode, parity error checking is not supported except for all CCCs. Only I3C Basic mode supports parity error checking.
By default, when SPD5 Hub device is put in I3C Basic mode, parity function is automatically enabled. The host can disable the function after it is enabled. Host can also disable the parity function with DEVCTRL CCC or by directly writing '1' to register MR18[6]. When parity function is disabled, the SPD5 Hub device simply ignores the 'T' bit information from the Host. The host may actually choose to compute the parity and send that information during 'T' bit or simply drive static low or high in 'T' bit.
The SPD5 Hub device implements ODD parity. If an odd number of bits in the byte are '1', the parity bit value is '0'. If even number of bits in the byte are '1', the parity bit value is '1'. The host computes the parity and sends it during T' bit.

10. 3 Packet Error Check and Parity Error Handling

There are two types of error checking done by the SPD5 Hub device: Parity error checking and Packet Error checking. By default, the parity error checking is always enabled and the packet error checking is disabled when the SPD5 Hub device is put in I3C Basic mode. The host may enable the packet error checking at any time. The parity error is calculated for each byte. The host sends the parity error information in 'T' bit.
I3C basic defines S0, S1, S2, S3, S4, S5, S6 error detection for target devices. Only S1 and S2 error detection is supported by the SPD5 Hub for parity checking. All other errors are not supported and not applicable.

10. 3. 1 Write Command Data Packet Error Handling - PEC Disabled

The SPD5 Hub device checks for the parity error for each byte in a packet except for the device select code byte that it receives from the host as shown in **Table 19**.

Write command - if no parity error:
- The SPD5 Hub device executes the command.

Write command - if there is parity error:
- The SPD5 Hub device discards the byte in the packet that had a parity error.
- The SPD5 Hub device discards all subsequent bytes in that packet until the STOP operation. The SPD5 Hub device may or may not check parity for all sub-sequent bytes in that packet.
- Note that as the packet contains more than one byte, if the first byte had no parity error but the second byte had a parity error, the SPD5 Hub device may or may not execute the first byte operation but the second byte and all subsequent bytes operations are discarded.
- The SPD5 Hub device sets the register MR52[0], MR48[7] and P_Err in GETSTATUS CCC to '1'; Updates Pending Interrupt Bits [3:0] to '0001' and waits for the next opportunity to send an in band interrupt if IBI is enabled.

Read Command Data Packet Error Handling - PEC Disabled
The SPD5 Hub device checks for parity error for each byte in a packet except for the device select code byte that it receives from the host prior to Repeat Start as shown in **Table 23**.

The SPD5 Hub device checks for the PEC error for a packet that it receives from the Host from Start condition to Repeat Start condition (from the first device select code followed by the address offset and CMD byte).
The SPD5 Hub device computes the packet error code for the entire packet starting with Repeat Start (device select code and the data SPD5 Hub device transmits back to Host).
Read command - If no parity error & no PEC error:
− The SPD5 Hub device sends ACK back to the host when Host performs a Start Repeat operation.
− The SPD5 Hub device executes the command and sends the data as shown in **Table 23**.
− The SPD5 Hub device computes PEC for the bytes (from Start condition to PEC byte prior to Repeat Start) shown in **Table 23**.
Read command - If there is parity error or PEC error:
− The SPD5 Hub device discards the byte in the packet that had a parity error.
− The SPD5 Hub device discards the second byte in that packet if a parity error occurred in the first byte. The SPD5 Hub device may or may not check parity for the second byte in that packet.
− The SPD5 Hub device discards the packet if there is a PEC error.
− The SPD5 Hub device sends NACK back to the host when Host performs a Start Repeat operation. The NACK represents either PEC error or a parity error in one of the three bytes or that SPD5 Hub is not able to start the read operation. The host may re-try Repeat Start again. The host may do the Repeat Start as many times it may desire. The PEC calculation by SPD5 Hub device only includes the device select code of the ACK responses of the Repeat Start operation. In other words, if there are more than one Repeat Start operation, the SPD5 Hub device includes the device select of only the last Repeat Start from the Host when it ACKs in PEC calculation and other NACK responses of the device select codes of the Repeat Start are not included in PEC calculation. If the SPD5 Hub device NACKs due to PEC error or a parity error in previous bytes from Host, it will always NACK regardless of how many times Host tries Repeat Start.
− The SPD5 Hub device does not send any data shown in **Table 23** and instead expects Host to perform STOP operation.
− The SPD5 Hub device sets registers MR52[0] & MR48[7] and P_Err in GETSTATUS CCC to ‘1’ for parity error and registers MR52[1] & MR48[7] and PEC_Err in GETSTATUS CCC to ‘1’ for PEC error. Further, the SPD5 Hub device updates Pending Interrupt Bits [3:0] in GETSTATUS CCC to ‘0001’ and waits for the next opportunity to send an in band interrupt if IBI is enabled.

■ Registers

The SPD5 Hub device has totally 128 volatile registers as shown in **Table 72**. The volatile register space has a continuous address. Unlike Non-Volatile memory in SPD5 Hub device, there is no concept of “Block” memory in volatile register space. When writing to and reading from volatile register space (i.e., MemReg = 0), the ’Block Address bits’ are treated simply as Upper address bits.

1. Register Map

Table 72 Register Map

Register Name	Address (hex)	Attribute	Default (hex)	Description
MR0	0x00	ROE	0x51	Device Type MSB
MR1	0x01	ROE	0x18	Device Type LSB
MR2	0x02	ROE	0x20	Device Revision
MR3	0x03	ROE	0x80	Vendor ID Byte0
MR4	0x04	ROE	0xCD	Vendor ID Byte1
MR5	0x05	ROE	0x03	Device Capability
MR6	0x06	ROE	0x52	Device Write Recovery Time Capability
MR7 to MR10	0x07 to 0x0A	RV	0x00	Reserved
MR11	0x0B	RW	0x00	I^2C Legacy Mode Device Configuration
MR12	0x0C	RWE	0x00	Write Protection for NVM Blocks [7:0]
MR13	0x0D	RWE	0x00	Write Protection for NVM Blocks [15:8]
MR14	0x0E	RWE	0x00	Device Configuration - Host & Local Interface IO; DO NOT USE [4:0]
MR15 to MR17	0x0F to 0x11	RV	0x00	Reserved
MR18	0x12	RO, RW	0x00	Device Configuration
MR19	0x13	1O	0x00	Clear Register MR51 Temperature Status Command
MR20	0x14	1O	0x00	Clear Register MR52 Error Status Command
MR21 to MR25	0x15 to 0x19	RV	0x00	Reserved
MR26	0x1A	RW	0x00	TS Configuration
MR27	0x1B	1O, RO, RW	0x00	Interrupt Configurations
MR28	0x1C	RW	0x70	TS Temperature High Limit Configuration - Low Byte
MR29	0x1D	RW	0x03	TS Temperature High Limit Configuration - High Byte
MR30	0x1E	RW	0x00	TS Temperature Low Limit Configuration - Low Byte
MR31	0x1F	RW	0x00	TS Temperature Low Limit Configuration - High Byte
MR32	0x20	RW	0x50	TS Critical Temperature High Limit Configuration - Low Byte
MR33	0x21	RW	0x05	TS Critical Temperature High Limit Configuration - High Byte
MR34	0x22	RW	0x00	TS Critical Temperature Low Limit Configuration - Low Byte
MR35	0x23	RW	0x00	TS Critical Temperature Low Limit Configuration - High Byte
MR36	0x24	RW	0x01	TS Resolution register
MR37	0x25	RW	0x01	TS Hysteresis width register
MR38 to MR47	0x26 to 0x2F	RV	0x00	Reserved
MR48	0x30	RO	0x00	Device Status
MR49	0x31	RO	0x00	TS Current Sensed Temperature - Low Byte
MR50	0x32	RO	0x00	TS Current Sensed Temperature - High Byte
MR51	0x33	RO	0x00	TS Temperature Status
MR52	0x34	RO	0x00	Hub, Thermal and NVM Error Status
MR53	0x35	RO	0x00	Program abort register
MR54 to MR127	0x36 to 0x7F	RV	0x00	Reserved

2. Register Attribute Definition

All volatile registers have Base Attributes as defined in **Table 73**. Some register attributes are further modified with Attribute Modifiers, as defined in **Table 74**.

Table 73 Register Base Attributes

Attribute	Abbreviation	Description
Read Only	RO	This bit can be read by software. Writes have no effect.
Read/Write	RW	This bit can be read or written by software.
Reserved	RV	This bit is reserved for future expansion and its value must not be modified by software. The bit will return '0' when read. When writing this bit, software must preserve the value read unless otherwise indicated.

Table 74 Register Attribute Modifier

Attribute	Abbreviation	Description
Write 1 Only	1O	This bit can only be set (i.e. write '1') but not reset (i.e. write '0').
Persistent	E	Persistent.

3. Register Description

3. 1 Register MR0 & MR1

Default: 0x5118 (SPD5118)

Table 75 Register MR0

Address: 0x00 Description: Device Type; MSB*1			
Bits	Attribute	Default	Detail
7:0	ROE	0x51	MR0[7:0]: MSB_DEV_TYPE Device Type - SPD5 Hub Device

***1.** The code in this register is used in conjunction with any device type in Register MR1.

Table 76 Register MR1

Address: 0x01 Description: Device Type; LSB*1			
Bits	Attribute	Default	Detail
7:0	ROE	0x18	MR0[7:0]: LSB_DEV_TYPE Device Type – with Temperature Sensor

***1.** The code in this register is used in conjunction with any device type in Register MR0.

3. 2 Register MR2

Default: 0x20

Table 77 Register MR2

Address: 0x02 Description: Device Revision			
Bits	Attribute	Default	Detail
7:6	RV	0	MR2[7:6]: Reserved
5:4	ROE	10	MR2[5:4]: DEV_REV_MAJOR Major Revision 00 = Revision 1 01 = Revision 2 10 = Revision 3 11 = Revision 4
3:1	ROE	000	MR2[3:1]: DEV_REV_MINOR Minor Revision: 000 = Revision 0 001 = Revision 1 010 = Revision 2 … 111 = Revision 7
0	RV	0	MR2[0]: Reserved

3. 3 Register MR3 & MR4

Default: 0x80CD

Table 78 Register MR3

Address: 0x03 Description: Vendor ID Byte0			
Bits	Attribute	Default	Detail
7:0	ROE	0x80	MR3[7:0]: VENDOR_ID_BYTE0

Table 79 Register MR4

Address: 0x04 Description: Vendor ID Byte1			
Bits	Attribute	Default	Detail
7:0	ROE	0xCD	MR4[7:0]: VENDOR_ID_BYTE1

3. 4 Register MR5

Default: 0x03

Table 80 Register MR5

Address: 0x05 Description: Device Capability			
Bits	Attribute	Default	Detail
7:2	RV	0	MR5[7:2]: Reserved
1	ROE	1	MR6[1]: TS_SUPPORT Internal Temperature Sensor Support 0 = Does not support Temperature Sensor 1 = Supports Temperature Sensor
0	ROE	1	MR6[0]: HUB_SUPPORT Hub Function Support 0 = Does not support Hub function 1 = Supports Hub function

3. 5 Register MR6

Default: 0x52

Table 81 Register MR6

Address: 0x06 Description: Write Recovery Time			
Bits	Attribute	Default	Detail
7:4	ROE	0101	MR6[7:4]: WR_REC_UNIT Write Recovery Unit 0000 = 0 0001 = 1 0010 = 2 0011 = 3 0100 = 4 0101 = 5 0110 = 6 0111 = 7 1000 = 8 1001 = 9 1010 = 10 1011 = 50 1100 = 100 1101 = 200 1110 = 500 1111 = Reserved
3:2	RV	0	MR6[3:2]:Reserved
1:0	ROE	10	MR6[1:0]: WR_REC_UNIT_TIME Write Recovery Time Unit 00 = ns 01 = µs 10 = ms 11 = Reserved

3. 6 Register MR11

Default: 0x00

Table 82 Register MR11

Address: 0x0B Description: I²C Legacy Mode Device Configuration			
Bits	Attribute	Default	Detail
7:4	RV	0	MR11[7:4]:Reserved
3	RW	0	MR11[3]: I²C_LEGACY_MODE_ADDR SPD5 Hub Device – I²C Legacy Mode Addressing 0 = 1 Byte Addressing for SPD5 Hub Device Memory 1 = 2 Bytes Addressing for SPD5 Hub Device Memory
2:0	ROE	000	MR11[2:0]: I²C_LEGACY_MODE_ADDR_POINTER SPD5 Device - Non Volatile Memory Address Page Pointer in I²CLegacy Mode*1,*2,*3 000 = Page 0 (0x00 to 0x7F) 001 = Page 1 (0x80 to 0xFF) 010 = Page 2 (0x100 to 0x17F) 011 = Page 3 (0x180 to 0x1FF) 100 = Page 4 (0x200 to 0x27F) 101 = Page 5 (0x280 to 0x2FF) 110 = Page 6 (0x300 to 0x37F) 111 = Page 7 (0x380 to 0x3FF)

***1.** This register is only applicable if bit[3] = '0' & MR18[5] = '0'. The SPD5 Hub device does not incur any delay to switch from one page to another page.

***2.** This register only applies to non-volatile memory (1024 Bytes) access of SPD5 Hub device. For volatile memory access, this register must be programmed to '000'.

***3.** See Section "**5. 1 Write and Read Access - NVM Memory**" in "**■ Function Description**" for the NVM Write and Read operation when device reaches the last byte of the 16 byte block boundary.

3. 7 Register MR12 & MR13

Default: 0x0000

Table 83 Register MR12

Address: 0x0C Description: NVM Protection Configuration For Blocks[7:0]*1,*2			
Bits	Attribute	Default	Detail
7	RWE	0	MR12[7]: WP_BLK_7 Write Protect - Block 7 0 = Not Protected 1 = Protected
6	RWE	0	MR12[6]: WP_BLK_6 Write Protect - Block 6 0 = Not Protected 1 = Protected
5	RWE	0	MR12[5]: WP_BLK_5 Write Protect - Block 5 0 = Not Protected 1 = Protected
4	RWE	0	MR12[4]: WP_BLK_4 Write Protect - Block 4 0 = Not Protected 1 = Protected
3	RWE	0	MR12[3]: WP_BLK_3 Write Protect - Block 3 0 = Not Protected 1 = Protected
2	RWE	0	MR12[2]: WP_BLK_2 Write Protect - Block 2 0 = Not Protected 1 = Protected
1	RWE	0	MR12[1]: WP_BLK_1 Write Protect - Block 1 0 = Not Protected 1 = Protected
0	RWE	0	MR12[0]: WP_BLK_0 Write Protect - Block 0 0 = Not Protected 1 = Protected

***1.** Once any register bit is set to '1', it can be cleared when the SPD5 Hub device is offline tester mode of operation.

***2.** The write (or update) transaction to this register must be followed by STOP operation to allow SPD5 Hub device to update the setting.

Table 84 Register MR13

Address: 0x0D Description: NVM Protection Configuration For Blocks[15:8]*1,*2			
Bits	Attribute	Default	Detail
7	RWE	0	MR13[7]: WP_BLK_15 Write Protect - Block 15 0 = Not Protected 1 = Protected
6	RWE	0	MR13[6]: WP_BLK_14 Write Protect - Block 14 0 = Not Protected 1 = Protected
5	RWE	0	MR13[5]: WP_BLK_13 Write Protect - Block 13 0 = Not Protected 1 = Protected
4	RWE	0	MR13[4]: WP_BLK_12 Write Protect - Block 12 0 = Not Protected 1 = Protected
3	RWE	0	MR13[3]: WP_BLK_11 Write Protect - Block 11 0 = Not Protected 1 = Protected
2	RWE	0	MR13[2]: WP_BLK_10 Write Protect - Block 10 0 = Not Protected 1 = Protected
1	RWE	0	MR13[1]: WP_BLK_9 Write Protect - Block 9 0 = Not Protected 1 = Protected
0	RWE	0	MR13[0]: WP_BLK_8 Write Protect - Block 8 0 = Not Protected 1 = Protected

***1.** Once any register bit is set to '1', it can only be cleared when the SPD5 Hub device is in offline tester mode of operation.

***2.** The write (or update) transaction to this register must be followed by STOP operation to allow SPD5 Hub device to update the setting.

3. 8 Register MR14

Default: 0x00

Table 85 Register MR14

Address: 0x0E Description: Device Configuration - Local Interface*1,*2			
Bits	Attribute	Default	Detail
7:6	RV	0	MR14[7:6]:Reserved
5	RWE	0	MR14[5]: LOCAL_INF_PULLUP_CONF Local Interface - Pull Up Resistor Configuration 0 = Internal (on die) Pullup Resistor 1 = External (board) Pullup Resistor
4:0	RV	0	MR14[4:0]: DO NOT USE

***1.** DIMM Vendor configures this register during assembly based on the DIMM design. After SPD Hub device is powered up, the Host can alter the setting through this register.

***2.** The write (or update) transaction to this register must be followed by STOP operation to allow SPD5 Hub device to update the setting.

3. 9 Register MR18

Default: 0x00

Table 86 Register MR18

Address: 0x12 Description: Device Configuration*1			
Bits	Attribute	Default	Detail
7	RW	0	MR18[7]: PEC_EN PEC Enable*2,*3 0 = Disable 1 = Enable
6	RW	0	MR18[6]: PAR_DIS Parity (T bit) Disable*3,*4 0 = Enable 1 = Disable
5	RO	0	MR18[5]: INF_SEL Interface Selection 0 = I^2C Protocol (Max speed of 1 MHz) 1 = I3C Basic Protocol*5
4	RW	0	MR18[4]: DEF_RD_ADDR_POINT_EN Default Read Address Pointer Enable 0 = Disable Default Read Address Pointer (Address pointer is set by the Host)*6 1 = Enable Default Read Address Pointer; Address selected by register bits [3:2]
3:2	RW	0	MR18[3:2]: DEF_RD_ADDR_POINT_START Default Read Pointer Starting Address*7 00 = MR49 01 = Reserved 10 = Reserved 11 = Reserved
1	RW	0	MR18[1]: DEF_RD_ADDR_POINT_BL Burst Length for Read Pointer Address for PEC Calculation*8 0 = 2 Bytes 1 = 4 Bytes
0	RV	0	MR18[0]: Reserved

***1.** The write (or update) transaction to this register must be followed by STOP operation to allow the SPD5 Hub device to update the setting.

***2.** This register is only applicable if register MR18[5] = '1'.

***3.** This register is updated when RSTDAA CCC is registered by SPD5 Hub device or when SPD5 Hub device goes through bus reset as described in **"2. 3 Bus Reset"** in **"■ Function Description"**.

***4.** This register is only applicable if register MR18 [5] = '1'. When Parity function is disabled, the SPD5 Hub device simply ignores the 'T' bit information from the Host. The host may actually choose to compute the parity and send that information in 'T' bit.

***5.** This register is automatically updated when SETAASA CCC or RSTDAA CCC is registered by the SPD5 Hub device or when SPD5 Hub device goes through bus reset as described in **"2. 3 Bus Reset"** in **"■ Function Description"**. This register can be read by the Host through normal Read operation but it cannot be written with normal write operation either in I^2C mode or I3C Basic mode of operation. When this register is updated, it takes in effect when there is a next START operation (i.e. after STOP operation).

***6.** The setting in register MR18[3:1] is don't care.

***7.** The register is only applicable if register MR18[4] = '1'.

***8.** The register is only applicable if register MR18[7,4] = '11'.

3. 10 Register MR19

Default: 0x00

Table 87 Register MR19

Address: 0x13 Description: Clear Register MR51 Temperature Status Command*1			
Bits	Attribute	Default	Detail
7:4	RV	0	MR19[7:4]: Reserved
3	1O	0	MR19 [3]: CLR_TS_CRIT_LOW Clear Temperature Sensor Critical Low Status 1 = Clear Register MR51 [3]
2	1O	0	MR19 [2]: CLR_TS_CRIT_HIGH Clear Temperature Sensor Critical High Status 1 = Clear Register MR51 [2]
1	1O	0	MR19 [1]: CLR_TS_LOW Clear Temperature Sensor Low Status 1 = Clear Register MR51 [1]
0	1O	0	MR19 [0]: CLR_TS_HIGH Clear Temperature Sensor High Status 1 = Clear Register MR51 [0]

***1.** This entire register is self clearing register after corresponding register is cleared.

3. 11 Register MR20

Default: 0x00

Table 88 Register MR20

Address: 0x14 Description: Clear Register MR52 Error Status Command*1			
Bits	Attribute	Default	Detail
7	1O	0	MR20[7]: CLR_SPD_BUSY_ERROR Clear Write or Read Attempt while SPD Device Busy Error Status 1 = Clear Register MR52 [7]
6	1O	0	MR20[6]: CLR_WR_NVM_BLK_ERROR Clear Write Attempt to Protected NVM Block Error Status 1 = Clear Register MR52 [6]
5	1O	0	MR20[5]: CLR_WR_NVM_PRO_REG_ERROR Clear Write Attempt to NVM Protection Register Error Status 1 = Clear Register MR52[5]
4:2	RV	0	MR20[4:2]: Reserved
1	1O	0	MR20[1]: CLR_PEC_ERROR Clear Packet Error Status 1 = Clear Register MR52[1]
0	1O	0	MR20[0]: CLR_PAR_ERROR Clear Parity Error Status 1 = Clear Register MR52[0]

***1.** This entire register is self clearing register after corresponding register is cleared.

3. 12 Register MR26

Default: 0x00

Table 89 Register MR26

Address: 0x1A Description: TS Configuration			
Bits	Attribute	Default	Detail
7:1	RV	0	MR26[7:1] Reserved
0	RW	0	MR26[0]: DIS_TS Disable Temperature Sensor*1 0 = Enable thermal sensor 1 = Disable thermal sensor

***1.** If this bit is set to '1' and then reset to '0', the host must wait minimum of tINIT before accessing samples on the thermal sensor.

3. 13 Register MR27

Default: 0x00

Table 90 Register MR27

Address: 0x1B Description: Interrupt Configurations			
Bits	Attribute	Default	Detail
7	1O	0	MR27[7]: CLR_GLOBAL Global Clear Event Status and In Band Interrupt Status*1,*2 1 = Clear Register MR48[7],MR51[3:0] & MR52[7:5,3,1:0]
6:5	RV	0	MR27[6:5]: Reserved
4	RO	0	MR27[4]: IBI_ERROR_EN IBI Error Enable for Register MR52 Error Log*3 0 = Disable; Errors logged in Register MR52[7:5,1:0] do not generate an IBI to Host. 1 = Enable; Errors logged in Register MR52[7:5,1:0] generate an IBI to Host.
3	RW	0	MR27[3]: IBI_TS_CRIT_LOW_EN IBI Error Enable for Temperature Sensor Critical Low 0 = Disable; Register MR51[3] = '1' does not generate an IBI to Host 1 = Enable; Register MR51[3] = '1' and Register MR27 [4] = '1' generate anIBI to Host
2	RW	0	MR27[2]: IBI_TS_CRIT_HIGH_EN IBI Error Enable for Temperature Sensor Critical High 0 = Disable; Register MR51[2] = '1' does not generate an IBI to Host 1 = Enable; Register MR51[2] = '1' and Register MR27 [4] = '1' generate anIBI to Host
1	RW	0	MR27[1]: IBI_TS_LOW_EN IBI Error Enable for Temperature Sensor Low 0 = Disable; Register MR51[1] = '1' does not generate an IBI to Host 1 = Enable; Register MR51[1] = '1' and Register MR27 [4] = '1' generate anIBI to Host
0	RV	0	MR27[0]: IBI_TS_HIGH_EN IBI Error Enable for Temperature Sensor High 0 = Disable; Register MR51[0] = '1' does not generate an IBI to Host 1 = Enable; Register MR51[0] = '1' and Register MR27 [4] = '1' generate anIBI to Host

***1.** This register is a self-clearing register after corresponding registers are cleared. Writing '0' in this register has no effect.

***2.** After this command is issued, the device does not generate an IBI for any pending event. But if new event occurs, the device does generate an IBI.

***3.** This register is automatically updated when ENEC CCC or DISEC CCC or RSTDAA CCC is registered by the SPD5 Hub device or when SPD5 Hub device goes through bus reset. This register can be read by the Host through normal read operation but cannot be written with normal write operation either in I^2C mode or in I3C Basic mode. When this register is updated, it takes effect when there is a next START operation (i.e. after STOP operation).

3. 14 Register MR28 & MR29

Default: 0x7003

Table 91 Register MR28

Address: 0x1C Description: TS Temperature High Limit Configuration - Low Byte*1			
Bits	Attribute	Default	Detail
7:0	RW	0x70	MR28[7:0]: TS_HIGH_LIMIT_LOW "MR28" and "MR29" - 16 bit thermal registers define the high limit for thermal sensor. See **Table 99**, "**Thermal Register - Low Byte and High Byte**".

Table 92 Register MR29

Address: 0x1D Description: TS Temperature High Limit Configuration - High Byte*1			
Bits	Attribute	Default	Detail
7:0	RW	0x03	MR29[7:0]: TS_HIGH_LIMIT_HIGH "MR28" and "MR29" - 16 bit thermal registers define the high limit for thermal sensor. See **Table 99**, "**Thermal Register - Low Byte and High Byte**".

***1.** Critical temperature High Limit value must have a higher value than temperature High Limit (Register MR28 [7:0] and Register MR29 [7:0].

3. 15 Register MR30 & MR31

Default: 0x0000

Table 93 Register MR30

Address: 0x1E Description: TS Temperature Low Limit Configuration - Low Byte*1			
Bits	Attribute	Default	Detail
7:0	RW	0	MR30[7:0]: TS_LOW_LIMIT_LOW "MR30" and "MR31" - 16 bit thermal registers define the low limit for thermal sensor. See **Table 99**, "**Thermal Register - Low Byte and High Byte**".

Table 94 Register MR31

Address: 0x1F Description: TS Temperature Low Limit Configuration - High Byte*1			
Bits	Attribute	Default	Detail
7:0	RW	0	MR31[7:0]: TS_LOW_LIMIT_HIGH "MR30" and "MR31" - 16 bit thermal registers define the high limit for thermal sensor. See **Table 99**, "**Thermal Register - Low Byte and High Byte**".

***1.** Critical temperature Low Limit value must have a lower value than temperature Low Limit (Register MR30 [7:0] and Register MR31 [7:0].

3. 16 Register MR32 & MR33

Default: 0x5005

Table 95 Register MR32

Address: 0x20 Description: TS Critical Temperature High Limit Configuration - Low Byte*1			
Bits	Attribute	Default	Detail
7:0	RW	0x50	MR32[7:0]: TS_CRIT_HIGH_LIMIT_LOW "MR32" and "MR33" - 16 bit thermal registers define the critical temperature high limit for thermal sensor. See **Table 99**, "**Thermal Register - Low Byte and High Byte**".

Table 96 Register MR33

Address: 0x21 Description: TS Critical Temperature High Limit Configuration - High Byte*1			
Bits	Attribute	Default	Detail
7:0	RW	0x05	MR33[7:0]: TS_CRIT_HIGH_LIMIT_HIGH "MR32" and "MR33" - 16 bit thermal registers define the critical temperature high limit for thermal sensor. See **Table 99**, "**Thermal Register - Low Byte and High Byte**".

***1.** Critical temperature High Limit value must have a higher value than temperature High Limit (Register MR28 [7:0] and Register MR29 [7:0].

3. 17 Register MR34 & MR35

Default: 0x0000

Table 97 Register MR34

Address: 0x22 Description: TS Critical Temperature Low Limit Configuration - Low Byte*1			
Bits	Attribute	Default	Detail
7:0	RW	0	MR34[7:0]: TS_CRIT_LOW_LIMIT_LOW "MR34" and "MR35" - 16 bit thermal registers define the critical temperature low limit for thermal sensor. See **Table 99**, "**Thermal Register - Low Byte and High Byte**".

Table 98 Register MR35

Address: 0x23 Description: TS Critical Temperature Low Limit Configuration - High Byte*1			
Bits	Attribute	Default	Detail
7:0	RW	0	MR35[7:0]: TS_CRIT_LOW_LIMIT_HIGH "MR34" and "MR35" - 16 bit thermal registers define the critical temperature low limit for thermal sensor. See **Table 99**, "**Thermal Register - Low Byte and High Byte**".

***1.** Critical temperature Low Limit value must have a lower value than temperature Low Limit (Register MR30 [7:0] and Register MR31 [7:0].

3. 18 Thermal Sensor Registers Read Out Mechanism

All thermal registers are sixteen bit quantities stored in two consecutive registers; low byte first and then high byte. Five bits are reserved for future use. Reserved bits are Read only bits and must be set to '0' when host writes to low and high byte. The device returns '0' in reserved bits when host reads from the low and high byte. Remaining eleven bits in these paired register form a signed value of multiples of 0.25 ranging from -256.00 to + 255.75. Unit for all thermal registers is °C.
The format of each pair of thermal registers is shown in **Table 99**.

Table 99 Thermal Register - Low Byte and High Byte

Register		B7	B6	B5	B4	B3	B2	B1	B0
MRX	Low Byte	**8**	**4**	**2**	**1**	**0.5**	**0.25**	RV	
MRX+1	High Byte	RV			**Sign**	**128**	**64**	**32**	**16**

The thermal registers examples are shown in **Table 100**.

Table 100 Thermal Register Examples

High Byte	Low Byte	Value	Unit
000 **00101**	**111100** 00	+95.00	°C
000 **00101**	**010100** 00	+85.00	°C
000 **00100**	**101100** 00	+75.00	°C
000 **00000**	**000100** 00	+1.00	°C
000 **00000**	**000011** 00	+0.75	°C
000 **00000**	**000010** 00	+0.50	°C
000 **00000**	**000001** 00	+0.25	°C
000 **00000**	**000000** 00	0.00	°C
000 **11111**	**111111** 00	-0.25	°C
000 **11111**	**111110** 00	-0.50	°C
000 **11111**	**111101** 00	-0.75	°C
000 **11111**	**111100** 00	-1.00	°C
000 **11101**	**100000** 00	-40.00	°C

3. 19 Register MR36

Default: 0x01

Table 101 Register MR36

Address: 0x24 Description: TS Resolution register			
Bits	Attribute	Default	Detail
7:2	RV	0	MR36[7:2] Reserved
1:0	RW	01	MR36[1:0]: TS_RES These bits define temperature resolution. 00 = 9-bit temperature resolution (0.5°C resolution) tCONV ≤ 34 ms max 01 = 10-bit temperature resolution (0.25°C resolution) tCONV ≤ 68 ms max 10 = 11-bit temperature resolution (0.125°C resolution) tCONV ≤ 136 ms max 11 = 12-bit temperature resolution (0.0625°C resolution) tCONV ≤ 136 ms max

3. 19. 1 Thermal Register - Low Byte and High Byte

Table 102 TS_RES[1:0]= 00, 9-bit temperature resolution (0.5°C resolution)

Register		B7	B6	B5	B4	B3	B2	B1	B0
MRX	Low Byte	8	4	2	1	0.5	RV		
MRX+1	High Byte	RV			Sign	128	64	32	16

Table 103 TS_RES[1:0]= 01, 10-bit temperature resolution (0.25°C resolution)

Register		B7	B6	B5	B4	B3	B2	B1	B0
MRX	Low Byte	8	4	2	1	0.5	0.25	RV	
MRX+1	High Byte	RV			Sign	128	64	32	16

Table 104 TS_RES[1:0]= 10, 11-bit temperature resolution (0.125°C resolution)

Register		B7	B6	B5	B4	B3	B2	B1	B0
MRX	Low Byte	8	4	2	1	0.5	0.25	0.125	RV
MRX+1	High Byte	RV			Sign	128	64	32	16

Table 105 TS_RES[1:0]=11, 12-bit temperature resolution (0.0625°C resolution)

Register		B7	B6	B5	B4	B3	B2	B1	B0
MRX	Low Byte	8	4	2	1	0.5	0.25	0.125	0.0625
MRX+1	High Byte	RV			Sign	128	64	32	16

3. 20 Register MR37

Default: 0x01

Table 106 Register MR37

Address: 0x25 Description: TS Hysteresis width register			
Bits	Attribute	Default	Detail
7:3	RV	0	MR37[7:3] Reserved
2:0	RW	001	MR37[2:0]: TS_HYS This hysteresis width applies to temperature limit, critical temperature. 001 = 1.0°C 010 = 1.5°C 011 = 3.0°C 100 = 6.0°C others = No hysteresis

3. 21 Register MR48

Default: 0x00

Table 107 Register MR48

Address: 0x30 Description: Device Status			
Bits	Attribute	Default	Detail
7	RO	0	MR48[7]: IBI_STATUS Device Event In Band Interrupt Status 0 = No pending IBI 1 = Pending IBI
6:4	RV	0	MR48[6:4]: Reserved
3	RO	0	MR48[3]: WR_OP_STATUS Write Operation Status 0 = No internal write operation is on going; 1 = Internal write operation is on going; Device ignores Host Write command if Host attempts to write when this bit is ‘1’. The device self clears this bit to ‘0’ when it completes internal write operation.
2	RO	0	MR48[2]: WP_OVERRIDE_STATUS Write Protect Override Status 0 = Override of write protect bits in Register MR12 and MR13 are blocked. 1 = Override of write protect bits in Register MR12 and MR13 are allowed. The default state of this register reflects the sensing of HSA pin during power on. This bit is set to ‘1’ if HSA pin is directly tied to GND. This bit is set to ‘0’ if HSA pin is connected to GND through a resistor.
1:0	RV	0	MR48[1:0]: Reserved

3. 22 Register MR49 & MR50

Default: 0x0000

Table 108 Register MR49

Address: 0x31 Description: TS Current Sensed Temperature - Low Byte			
Bits	Attribute	Default	Detail
7:0	RO	0	MR49[7:0]: TS_SENSE_LOW “MR49” and “MR50” - 16 bit thermal registers return the most recent conversion of the thermal sensor. See **Table 99**, “Thermal Register - Low Byte and High Byte”.

Table 109 Register MR50

Address: 0x32 Description: TS Current Sensed Temperature - High Byte			
Bits	Attribute	Default	Detail
7:0	RO	0	MR50[7:0]: TS_SENSE_HIGH “MR49” and “MR50” - 16 bit thermal registers return the most recent conversion of the thermal sensor. See **Table 99**, “Thermal Register - Low Byte and High Byte”.

3. 23 Register MR51

Default: 0x00

Table 110 Register MR51

Address: 0x33 Description: TS Temperature Status			
Bits	Attribute	Default	Detail
7:4	RV	0	MR51[7:4]: Reserved
3	RO	0	MR51[3:]: TS_CRIT_LOW_STATUS Temperature Sensor Critical Low 0 = Temperature is above the limit set Register MR34 and MR35. 1 = Temperature is below the limit set Register MR34 and MR35.
2	RO	0	MR51[2]: TS_CRIT_HIGH_STATUS Temperature Sensor Critical High 0 = Temperature is below the limit set Register MR32 and MR33. 1 = Temperature is above the limit set Register MR32 and MR33.
1	RO	0	MR51[1]: TS_LOW_STATUS Temperature Sensor Low 0 = Temperature above limit set Register MR30 and MR31. 1 = Temperature below limit set Register MR30 and MR31.
0	RO	0	MR51[0]: TS_HIGH_STATUS Temperature Sensor High 0 = Temperature is below the limit set Register MR28 and MR29. 1 = Temperature is above the limit set Register MR28 and MR29.

3. 24 Register MR52

Default: 0x00

Table 111 Register MR52

Address: 0x34 Description: Hub, Thermal and NVM Error Status			
Bits	Attribute	Default	Detail
7	RO	0	MR52[7]: BUSY_ERROR_STATUS Write or Read Attempt while SPD5 Hub Device was Busy (Write Recovery Time Violation)*1,*2 0 = No write or read attempt while SPD Hub device was busy 1 = Write or Read attempt while SPD5 Hub device was busy
6	RO	0	MR52[6]: WR_NVM_BLK_ERROR_STATUS Write Attempt to Protected NVM Block 0 = No write attempt 1 = Write attempt to protected NVM Block
5	RO	0	MR52[5]: WR_NVM_PRO_REG_ERROR_STATUS Write Attempt to NVM Protection Registers 0 = No attempt to modify write protect registers 1 = Write attempt to modify write protect registers
4:2	RV	0	MR52[4:2]: Reserved
1	RO	0	MR52[1]: PEC_ERROR_STATUS Packet Error*3,*4 0 = No PEC Error 1 = PEC Error in one or more packets
0	RO	0	MR52[0]: PAR_ERROR_STATUS Parity Check Error*4,*5 0 = No Parity Error 1 = Parity Error in one or more bytes

***1.** SPD5 Hub device busy status is only for accessing EEPROM memory. For any access to volatile register space, this bit definition does not apply

***2.** When SPD5 Hub device is busy with EEPROM write/read, it sends NACK to the host requests within write recovery time.

***3.** Only applicable in register MR18[5] = '1' and if PEC function is enabled.

***4.** This register is updated when SPD5 Hub device goes through bus reset.

***5.** Only applicable in register MR18[5] = '1' and if Parity function is not disabled or for supported CCC in I^2C mode.

3. 25 Register MR53

Default: 0x00

Table 112 Register MR53

Address: 0x35 Description: Program abort register*1,*2			
Bits	Attribute	Default	Detail
7:1	RV	0	MR37[7:1] Reserved
0	RO	0	MR37[0]: PRG_ABORT Program abort due to low supply voltage detection. 0 = Normally 1 = Error (Program abort)

***1.** The program abort register indicates write cancel due to low supply voltage detection.(See **Figure 13**)

***2.** This register is updated at every program cycle.

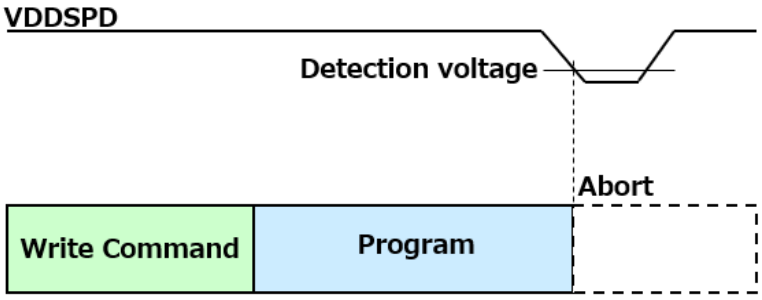


Figure 13 Program abort due to low supply voltage detection

■ AC Timing Definition

1. Open Drain to Push Pull Timing

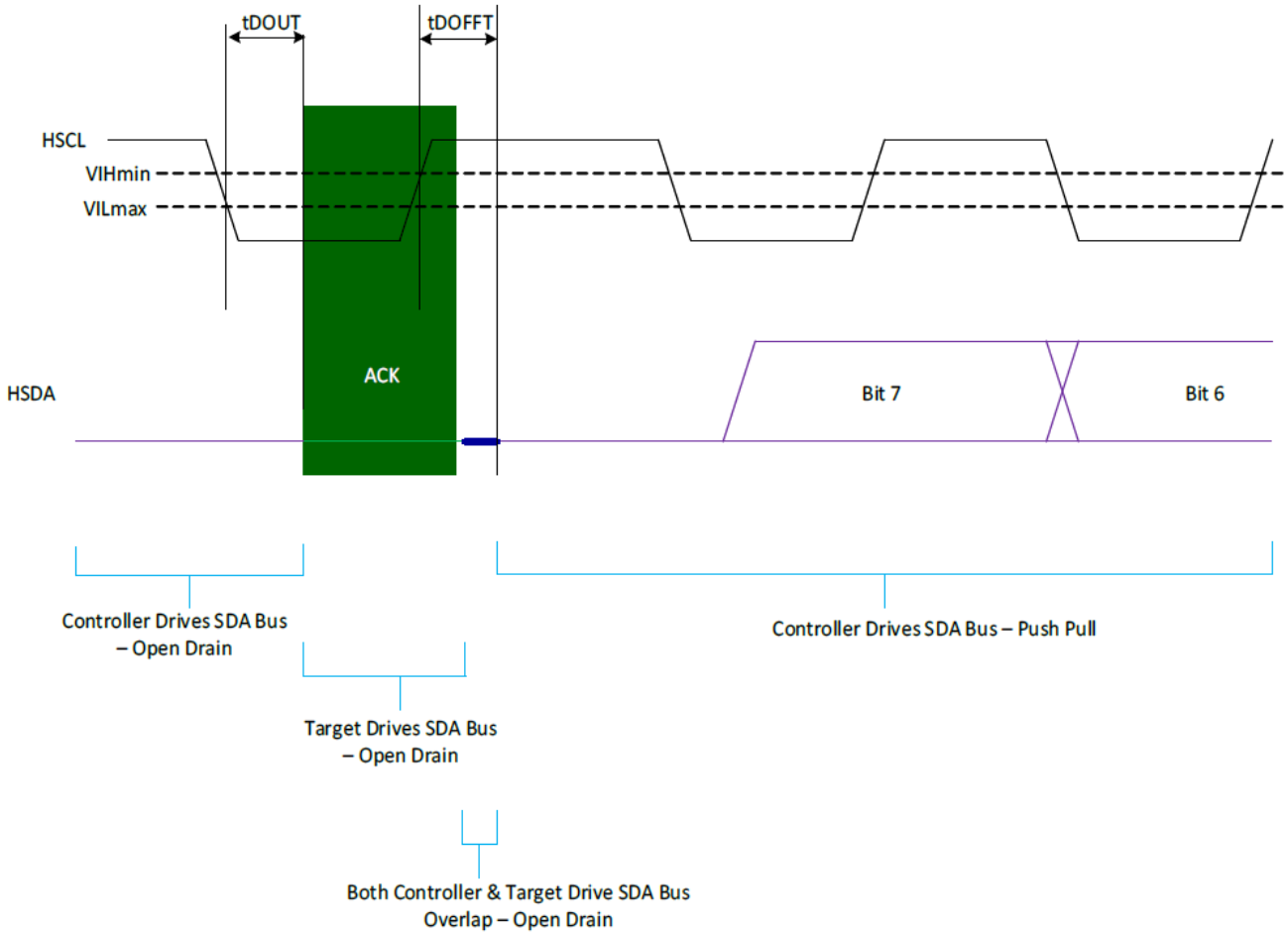


Figure 14 Target Open Drain to Host Push Pull Hand Off Operation

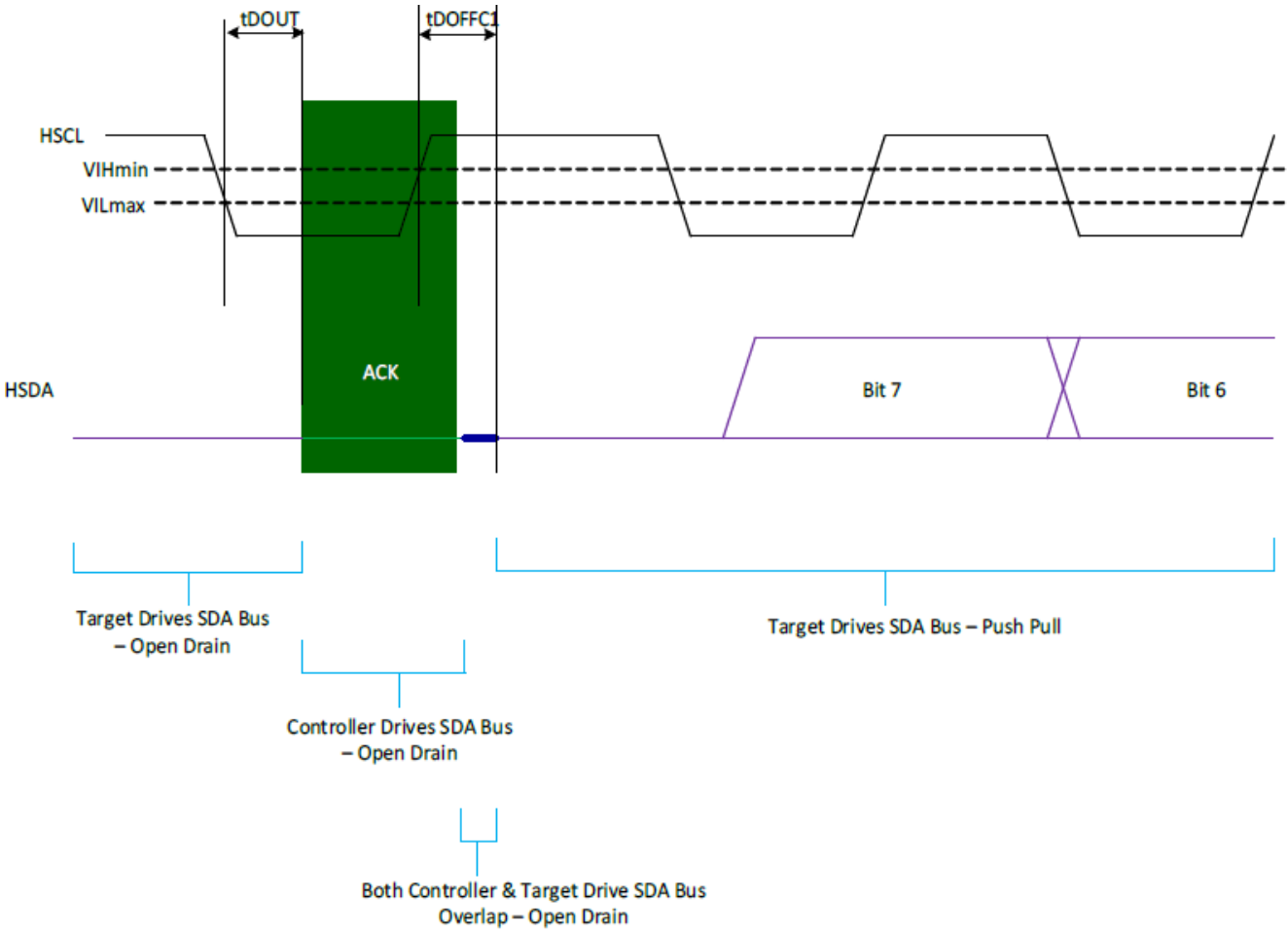


Figure 15 Controller Open Drain (ACK) to Target Push Pull Hand Off Operation

2. Push Pull to Open Drain Timing

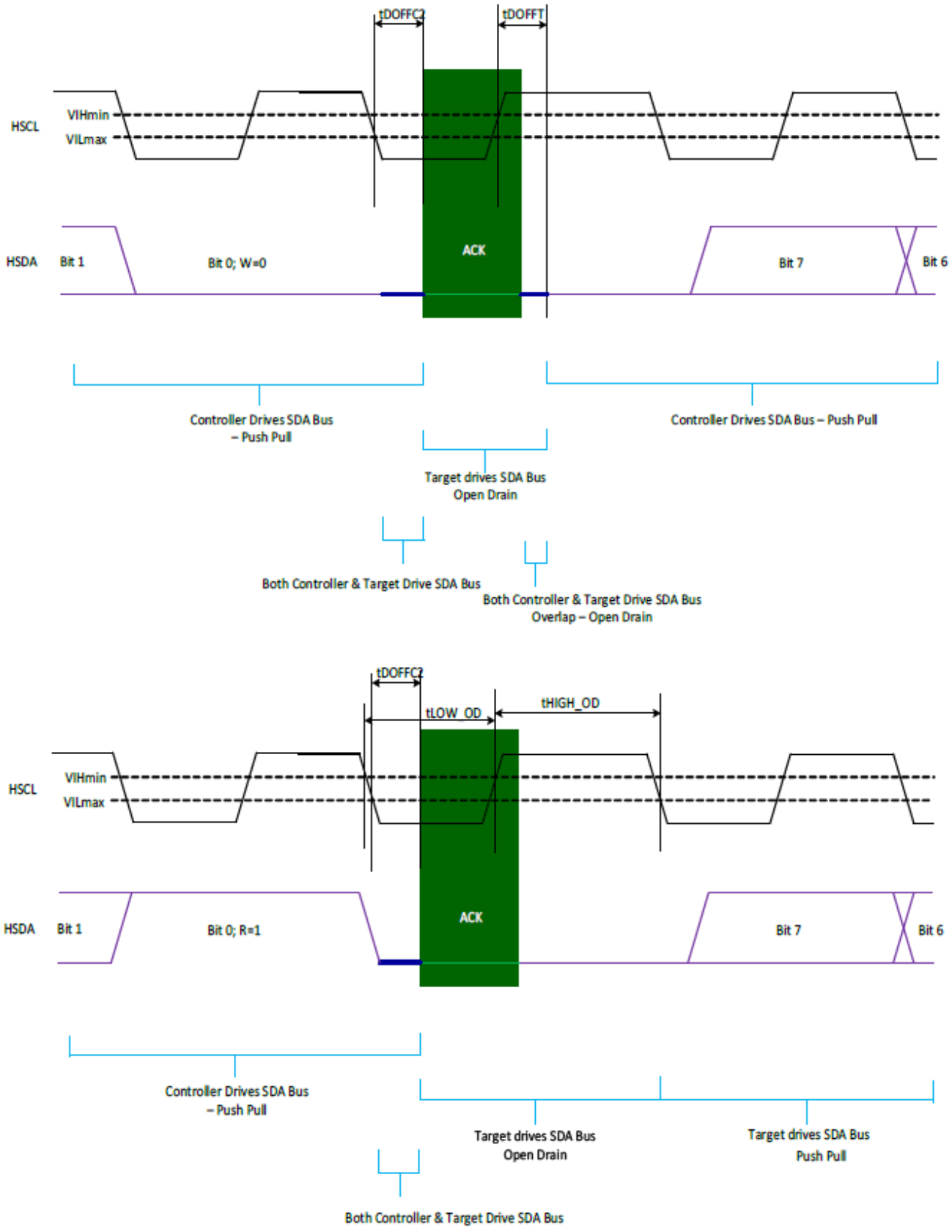


Figure 16 Controller Push Pull to Target Open Drain Hand Off Operation

3. START and STOP Timing

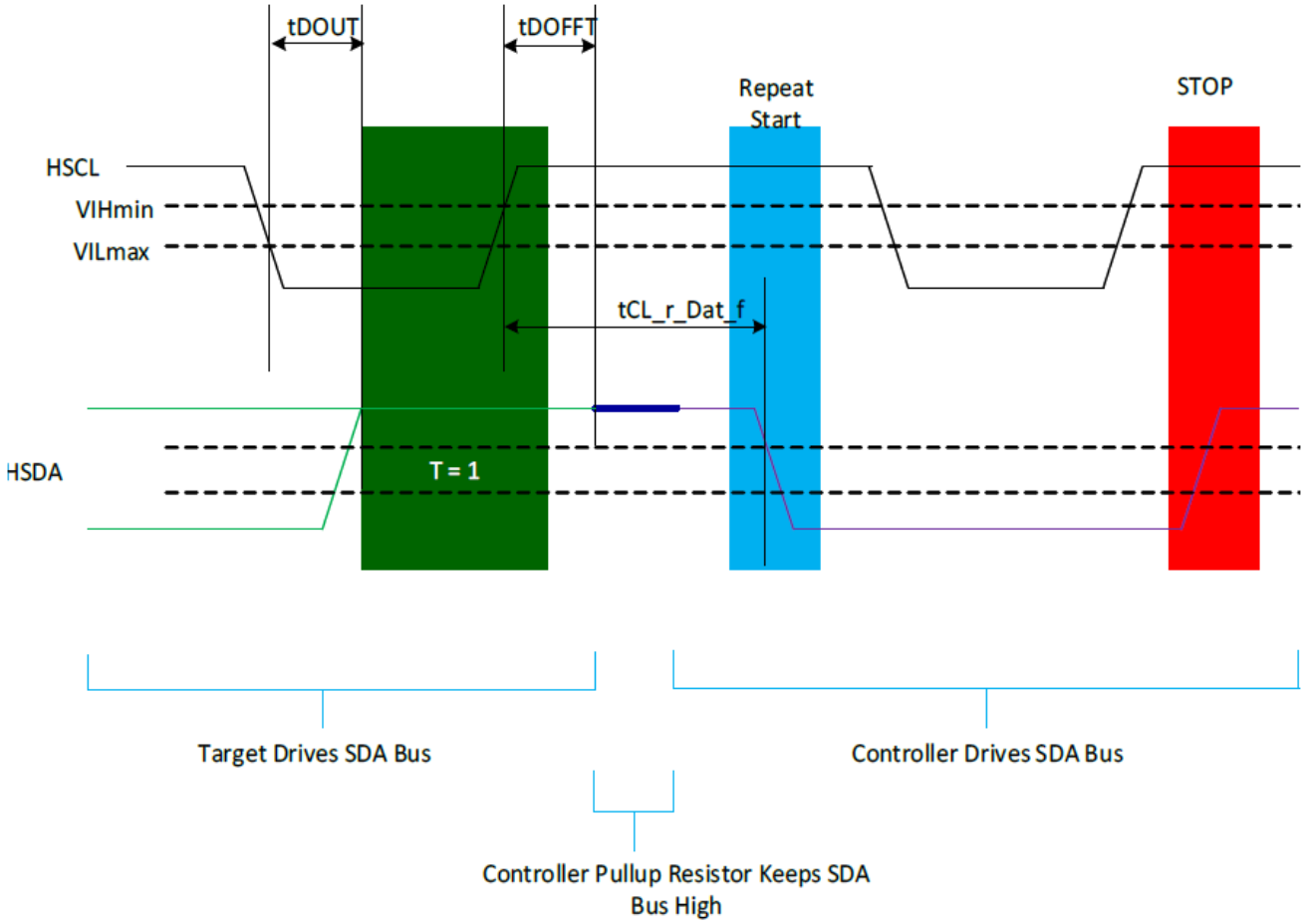


Figure 17 T=1; Host Ends Read with Repeated START and STOP Waveform

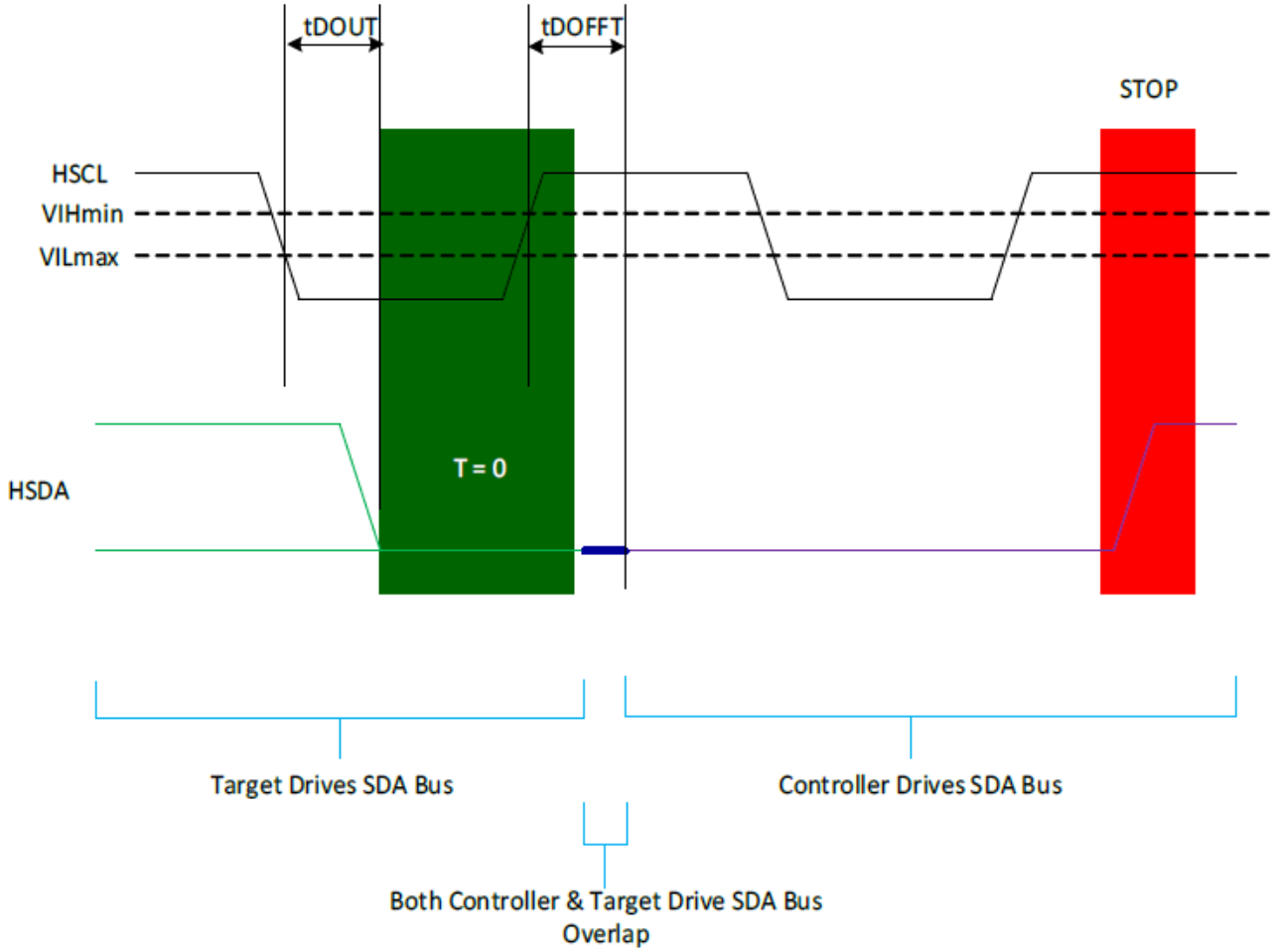


Figure 18 T=0; Target Ends Read; Host Generates STOP

4. I²C or I3C Basic Bus Timing

The SPD5 Hub device follows the I²C or I3C Basic bus timing requirements. The following tables show the timing diagrams for Data Bus Input and Data Output parameters.

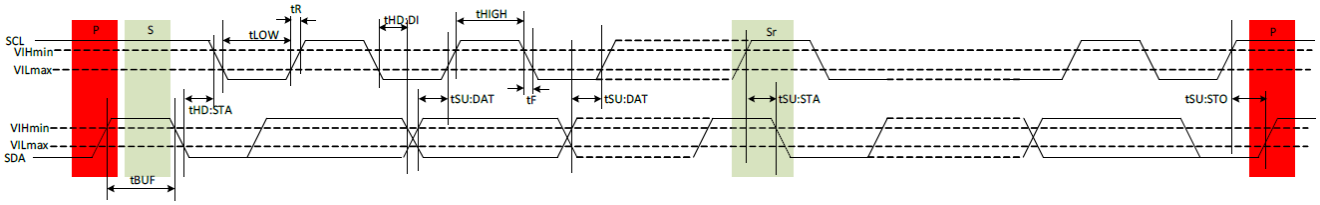


Figure 19 I²C or I3C Basic Bus AC Input Timing

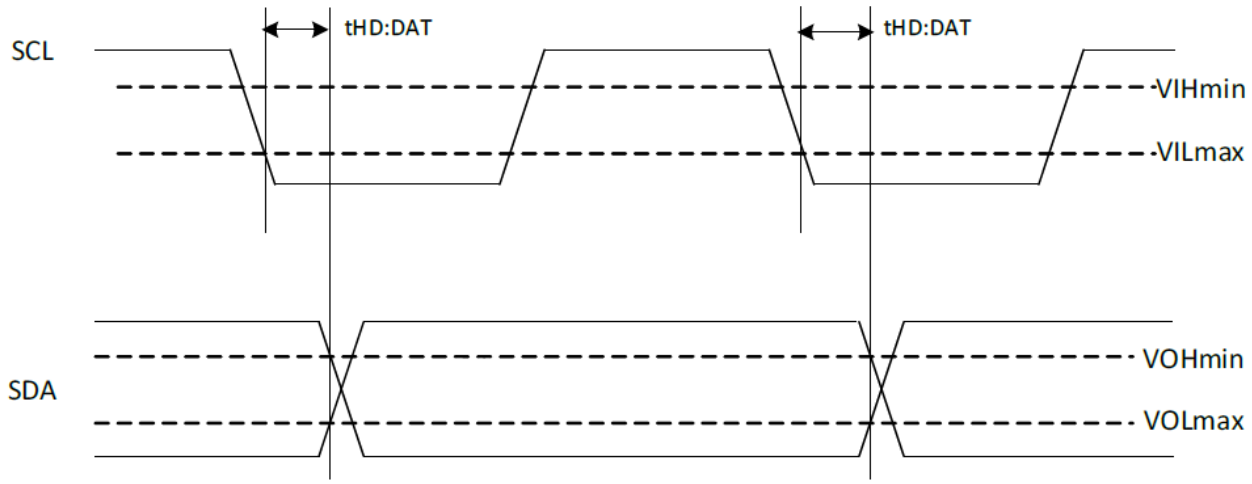


Figure 20 I^2C Bus AC Data Output Timing

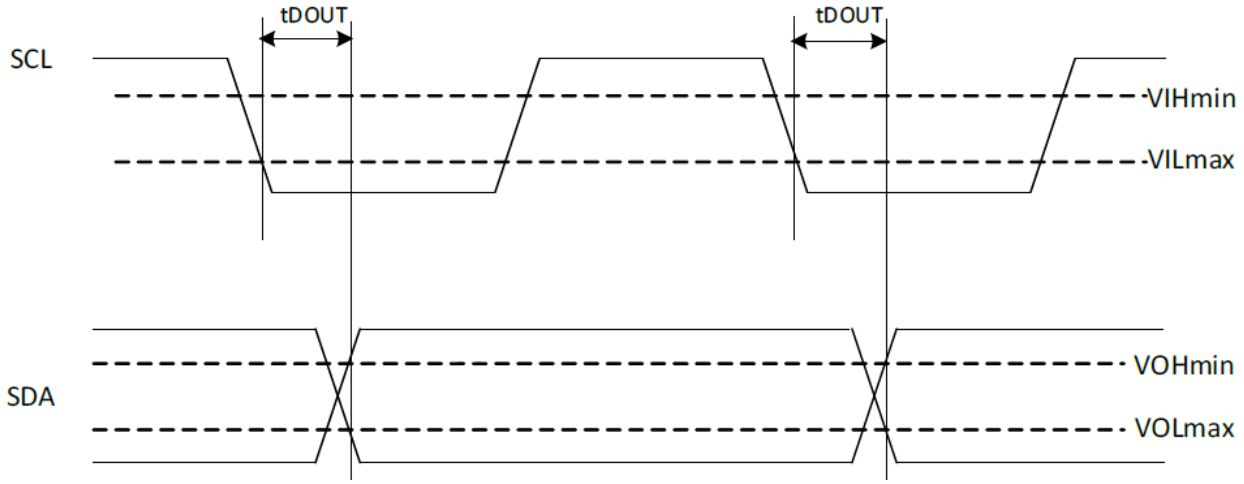


Figure 21 I3C Basic Bus AC Data Output Timing

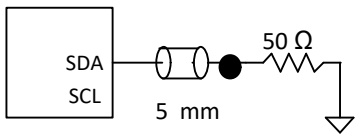


Figure 22 Output Slew Rate and Output Timing Reference Load

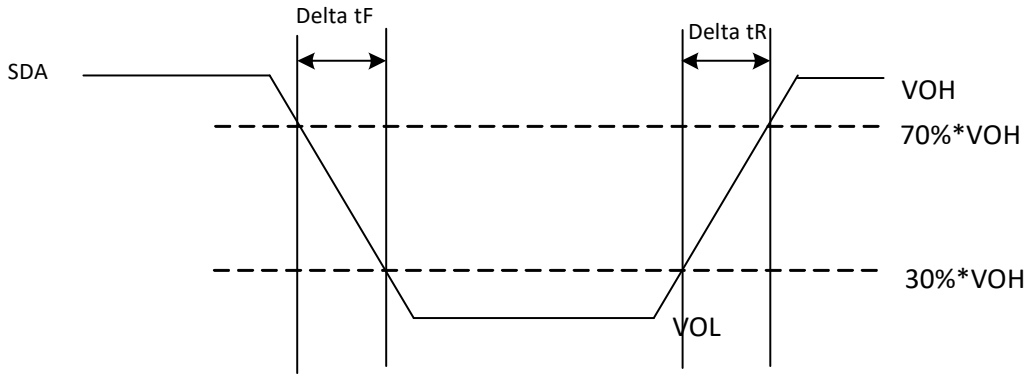


Figure 23 Output Slew Rate Measurement Points

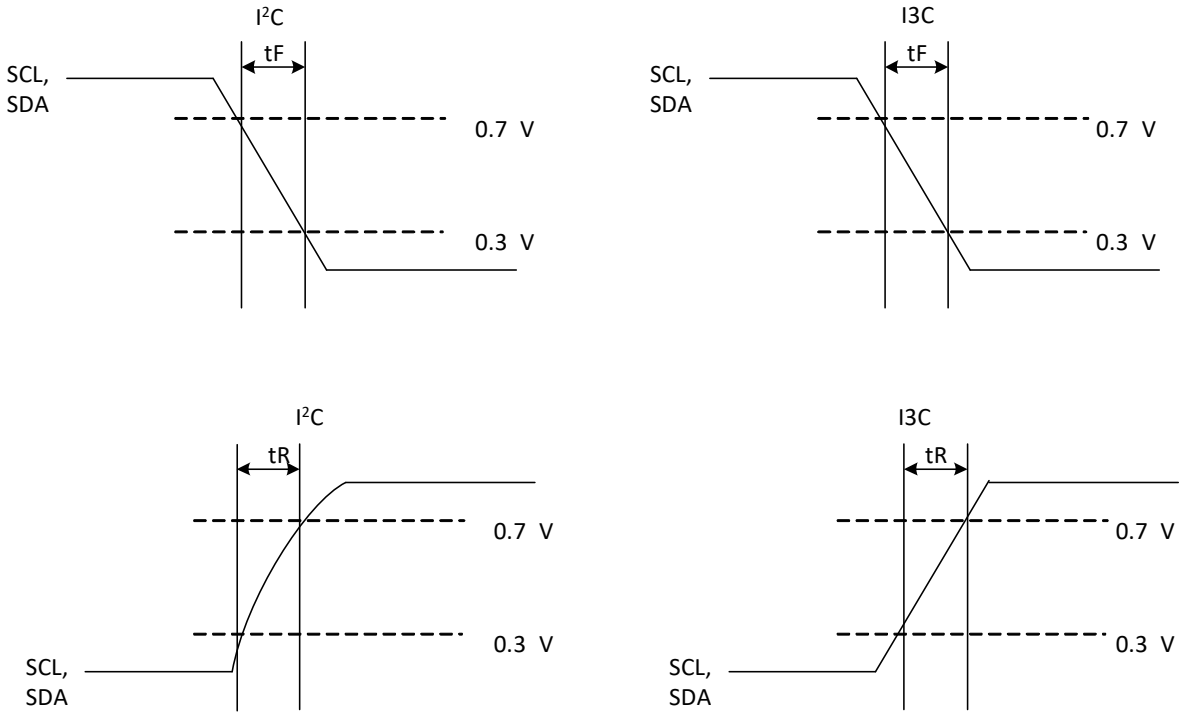


Figure 24 Rise and Fall Timing Parameter Definition

5. HSCL Non Monotonicity

Due to non-deterministic loading (number of DIMMs populated) on an unterminated bus, there can be reflections on the bus, causing slope reversal on the HSCL signal on the input receiver of the SPD5 HUB.
The SPD5 Hub device has tolerate t_{SLPR} and V_{SLPR_PK2PK} slope reversal on HSCL in I3C mode as shown in **Figure 25** through **Figure 27**. Note that t_{PDHL} is for reference only in this diagram, refer to measurement methodology for details on this parameter.

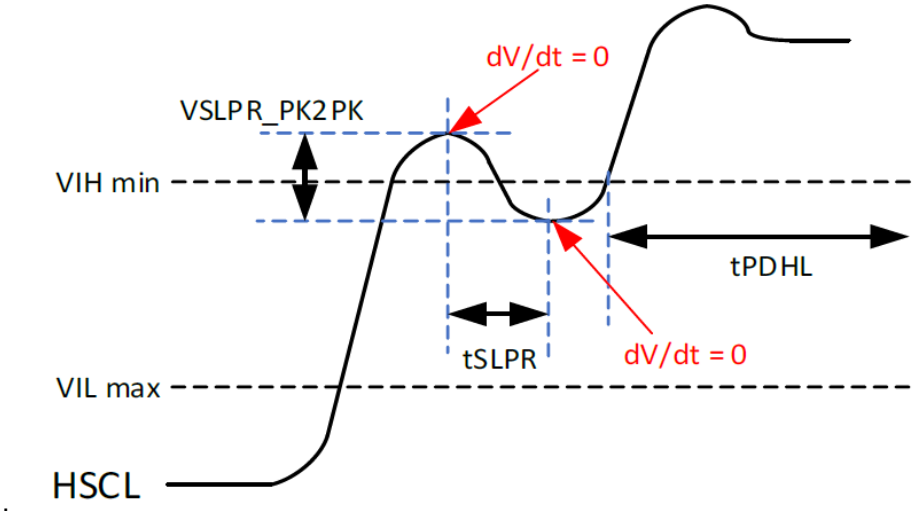


Figure 25 Slope Reversal on HSCL at VIH

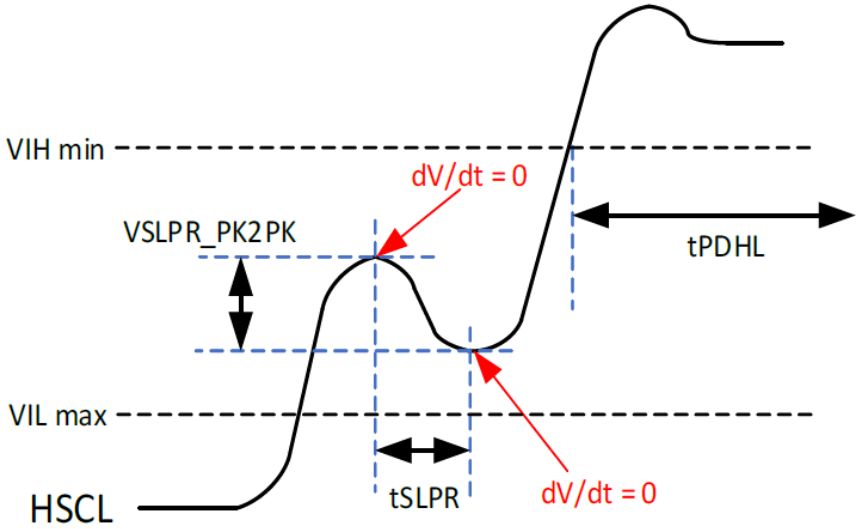


Figure 26 Slope Reversal on HSCL Between VIL and VIH

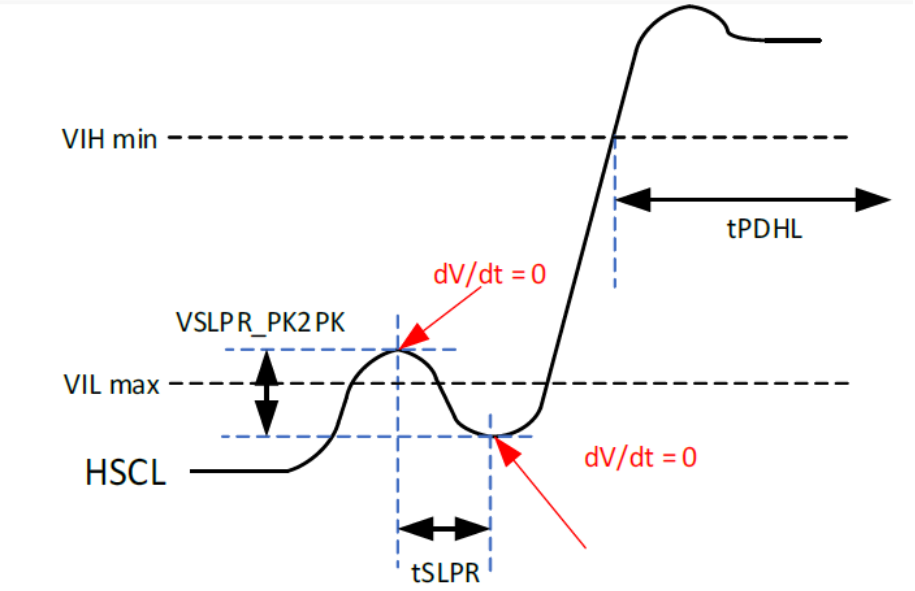


Figure 27 Slope Reversal on HSCL at VIL

Table 113

Symbol	Parameter*1,*2	Min	Max	Unit
t_{SLPR}	Pulse width of slope reversal which must be suppressed	0	2.6	ns
V_{SLPR_PK2PK}	The Peak to Peak voltage of slope reversal which must be suppressed	0	150	mV

***1.** Verified by design and characterization, not necessarily tested on all devices.
***2.** These parameters apply in I3C mode.

6. Hub Propagation Delay

The SPD5 Hub device has a propagation delay of t_{PDHL} for its host interface HSCL/HSDA input signals to the local interface LSCL/LSDA signals respectively.
Similarly, the SPD5 Hub device has a propagation delay of t_{PDLH} for its local interface LSDA input signal to the host interface HSDA signal.

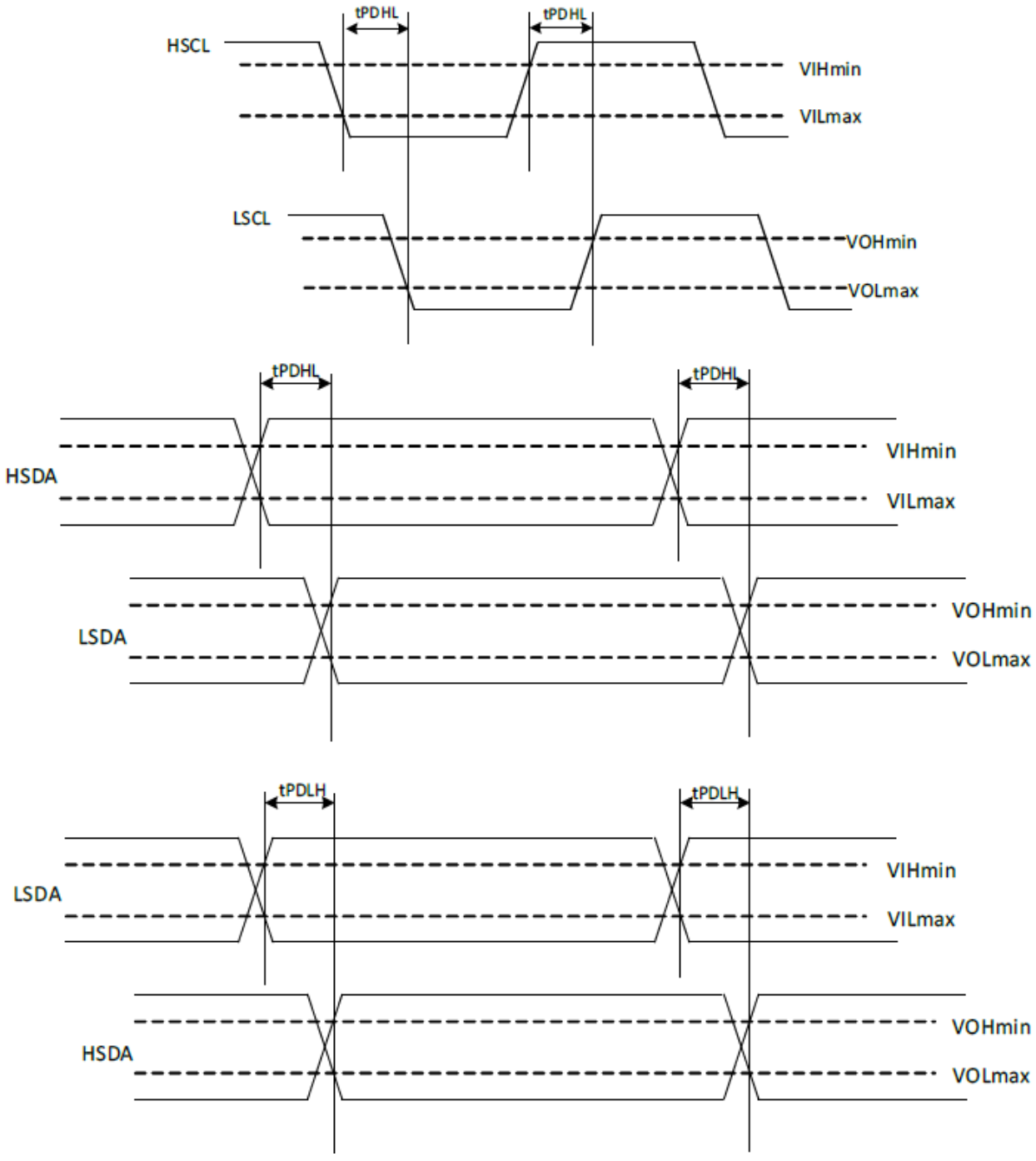


Figure 28 Propagation Delay through the SPD5 Hub Device

■ Electrical Characteristics

1. Absolute Maximum Ratings

Table 114 Absolute Maximum Ratings

Symbol	Item	Applied Pin	Absolute Maximum Rating	Unit
V_{DDIO}	Power supply voltage	VDDIO	-0.5 to +2.1	V
V_{DDSPD}		VDDSPD	-0.5 to +2.1	V
V_{HSA}	Input voltage	HSA	-0.5 to +2.1	V
V_{HSCL}		HSCL	-0.5 to +3.6	V
V_{HSDA}	I/O voltage	HSDA	-0.5 to +3.6	V
V_{LSDA}		LSDA	-0.5 to +3.6	V
V_{LSCL}	Output voltage	LSCL	-0.5 to +3.6	V
T_{opr}	Operation ambient temperature	-	-40 to +125	°C
T_{stg}	Storage temperature	-	-65 to +150	°C

Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.

2. Operating Conditions, Measurement Conditions & DC and AC Characteristics

This clause summarizes the operating and measurement conditions, and the DC and AC characteristics of the device.The parameters in the DC and AC Characteristic tables that follow are derived from tests performed under the Measurement Conditions summarized in the relevant tables.

2. 1 Operating Conditions

Table 115 Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDSPD}	Input supply voltage	1.7	1.8	1.98	V
V_{DDIO}	Input supply voltage	0.95	1.0	1.05	V
T_{CASE}	Case operating temperature	-40	-	125	°C
$T_{WRITEOK}$	Case temperature range for NVM Write operation Data writes outside this range may not meet retention requirements.	-40	-	95	°C

Table 116 Write Endurance and Data Retention Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
-	Data retention 25°C	100	-	-	Year
N_W	Write endurance cycles 25°C	10^6	-	-	Cycle
	Write endurance cycles 95°C	10^5	-	-	Cycle

2. 2 AC Measurement Conditions

Table 117 AC Measurement Conditions*1

Symbol	Parameter	Min	Max	Unit
C_L	Load capacitance	40		pF
-	Input rise and fall times - Open Drain	-	50	ns
-	Input rise and fall times - Push Pull	-	5	ns
-	Input signal swing levels	0.2 to 0.8		V
-	Input levels for timing reference	0.3 to 0.7		V

***1.** This AC measurement condition (**Table 117** & **Figure 29**) is only for the test purpose in lab.

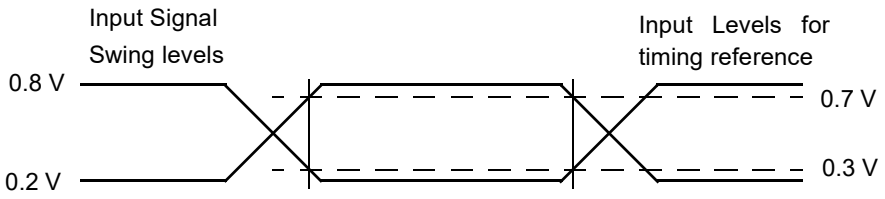


Figure 29 AC Measurement Waveform

Table 118 Input Parameters

Symbol	Parameter*1	Test Condition	Min	Max	Unit
C_{IN}	Input capacitance (HSDA, HSCL, LSDA)	Ta = 25°C, f = 400 kHz on I3C operation	-	5	pF
t_{SP}	Pulse width of spikes which must be suppressed by the input filter in I^2C mode	Single glitch, f < 100 kHz	-	-	ns
		Single glitch, f > 100 kHz	-	50	

***1.** Verified by design and characterization, not necessarily tested on all devices.

Table 119 Output R_{ON} Specification

Symbol	Parameter*1	Min	Max	Unit
R_{ON_PUH}	HSDA output pullup driver impedance	10	45	Ω
R_{ON_PDH}	HSDA output pulldown driver impedance	10	40	Ω
R_{ON_Local}	LSCL, LSDA output pullup and pulldown driver impedance	20	100	Ω

***1.** Pulldown $R_{ON} = V_{OUT} / I_{OUT}$; Pullup $R_{ON} = (V_{IO} - V_{OUT}) / I_{OUT}$.

2. 3 DC Electrical Characteristics

Table 120 DC Electrical Characteristics

Symbol	Parameter*1	Condition	Min	Max	Unit
I_{LI}	Input leakage current	-	-	±5	µA
I_{LO}	Output leakage current	-	-	±5	µA
I_{DDR}	Supply current, read operation	V_{DDSPD} = 1.8 V, f_C = 12.5 MHz*1	-	2	mA
I_{DDW}	Supply current, write operation	V_{DDSPD} = 1.8 V, f_C = 12.5 MHz*1	-	3	mA
I_{DD1}	Standby supply current	V_{DDSPD} = 1.8 V	-	150	µA
V_{IL}	Input low voltage	-	-0.35	0.3	V
V_{IH}	Input high voltage	-	0.7	3.6	V
V_{OL}	Output low voltage*2	3 mA sink current	-	0.3	V
V_{OH}	Output high voltage	3 mA source current	V_{DDIO} -0.3	-	V
I_{OL}	Output low current (HSDA, LSDA, LSCL)	V_{OL} = 0.3 V	3	-	mA
I_{OH}	Output high current (HSDA, LSDA, LSCL)	V_{OH} = V_{DDIO} - 0.3 V	-	-3	mA
Slew_Rate	Rising output slew rate (HSDA, LSDA, LSCL)*3	-	0.1	1.0	V
	Falling output slew rate (HSDA, LSDA, LSCL)*3		0.1	3.0	V
V_{PON}	Power on reset threshold	Monotonic rise between V_{PON} and V_{DDSPD}(min) without ringback	1.6	-	V
V_{POFF}	Power off threshold for warm power on cycle	No ringback above V_{POFF}	-	0.3	V

***1.** Thermal sensor is active.

***2.** Example calculation for V_{OL}= R_{ON} × (I_{LO} + I_{OUT}); where I_{OUT} = V_{DDIO} / (R_{PU} + R_{ON}); R_{PU} = Pullup resistor with typical value of 1 kΩ; Min and Max value of 750 Ω and 1.5 kΩ, respectively.

***3.** Output slew rate is guaranteed by design and/or characterization. The output slew rate reference load as shown in **Figure 22** and **Figure 23** shows the timing measurement points. For slew rate measurements, the V_{OH} level shown in **Figure 23** is a function of R_{ON} value; V_{OH} = {1.0/(R_{ON} + 50)} × 50.

2. 4 AC Electrical Characteristic

Table 121 AC Electrical Characteristic (Sheet 1 of 2)

Symbol	Parameter	I^2C Mode Open Drain		I3C Basic Push-Pull*1		Unit
		Min	Max	Min	Max	
f_{SCL}	Clock frequency	0.01	1	0.01	12.5	MHz
t_{HIGH}	Clock pulse width high time	260	-	35	-	ns
t_{LOW}	Clock pulse width low time	500	-	35	-	ns
$t_{TIMEOUT}$	Detect clock low timeout	10	50	10	50	ms
t_R	SDA rise time*2,*3	-	120	-	5	ns
t_F	SDA fall time*2,*3	-	120	-	5	ns
$t_{SU:DAT}$	Data in setup time*2	50	-	8	-	ns
$t_{HD:DI}$	Data in hold time*2	0	-	3	-	ns
$t_{SU:STA}$	Start condition setup time*2	260	-	12	-	ns
$t_{HD:STA}$	Start condition hold time*2	260	-	30	-	ns
$t_{SU:STO}$	Stop condition setup time*2	260	-	12	-	ns
t_{BUF}	Time between Stop Condition and next Start Condition*2,*4	500	-	500	-	ns
t_W	Write time	-	5	-	5	ms
t_{POFF}	Warm power cycle off time	1	-	1	-	ms
t_{Sense_HSA}	Time from valid 1.8V supply to Sense HSA pin for HID code assignment	-	5	-	5	ms
t_{INIT}	Time from power on to first command	10	-	10	-	ms
t_{AVAL}	Bus Available time (no edges seen on HSDA and HSCL)	-	-	1	-	µs
t_{IBI_ISSUE}	Time to issue IBI after an event is detected when Bus is available	-	-	-	15	µs
$t_{CLR\_I3C\_CMD\_Delay}$	Time from Clear Register Status to any I3C operation with Start condition to avoid IBI generation; PEC Disabled	-	-	4	-	µs
	Time from Clear Register Status to any I3C operation with Start condition to avoid IBI generation; PEC Enabled	-	-	15	-	µs
t_{PDHL}	Propagation Delay, HSDA to LSDA and HSCL to LSCL*5	-	200	-	6	ns
t_{PDLH}	Propagation Delay, LSDA to HSDA*5	-	200	-	6	ns
$t_{HD:DAT}$	HSCL Falling Clock In to HSDA Data Out Hold Time*6	0.5	350	N/A	N/A	ns
t_{DOUT}	HSCL Falling Clock In to HSDA Valid Data Out Time*7	N/A	N/A	0.5	12	ns
t_{DOFFT}	HSCL Rising Clock In to SDA Output Off*8	N/A	N/A	0.5	12	ns
t_{DOFFC1}	HSCL Rising Clock In to Controller SDA Output Off*9	N/A	N/A	0.5	t_{HIGH}	ns
t_{DOFFC2}	HSCL Falling Clock In to Controller SDA Output Off	N/A	N/A	0.5	12	ns

Table 122 AC Electrical Characteristic (Sheet 2 of 2)

Symbol	Parameter	I^2C Mode Open Drain		I3C Basic Push-Pull*1		Unit
		Min	Max	Min	Max	
$t_{CL\_r\_DAT\_f}$	HSCL Rising Clock In to Controller Driving HSDA Signal Low*10	N/A	N/A	40	-	ns
$t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$	DEVCTRL CCC Followed by DEVCTRL CCC or Register Read/Write Command Delay*11,*12,*13	3	-	3	-	µs
$t_{WR\_RD\_DELAY\_PEC\_EN}$	Register Write Command Followed by Register Read Command Delay in PEC Enabled Mode*14,*15,*16	N/A	N/A	8	-	µs
$t_{I2C\_CCC\_Update\_Delay}$	SETHID CCC or SETAASA CCC to any other CCC or Read/Write Command delay	2.5	-	-	-	µs
$t_{I3C\_CCC\_Update\_Delay}$	RSTDAA CCC or ENEC CCC or DISEC CCC to any other CCC or Read/Write Command delay	-	-	2.5	-	µs
t_{CCC_Delay}	Any CCC to RSTDAA CCC delay	N/A	N/A	2.5	-	µs

***1.** I3C mode with Open Drain operation follows timing values as shown in I^2C Mode - Open Drain column.

***2.** See **Figure 19** for input timing parameter definition.

***3.** See **Figure 24** for voltage threshold definition for rise and fall times.

***4.** If PEC is enabled, $t_{WR\_RD\_DELAY\_PEC\_EN}$ timing parameter also applies.

***5.** See **Figure 28** for timing definition. See **Figure 22** for output timing parameter measurement reference load.

***6.** See **Figure 20** for output timing parameter definition.

***7.** The SPD5 Hub device must be in configured in I3C Basic mode to guarantee t_{DOUT} value. See **Figure 21** for output timing parameter definition. See **Figure 22** for output timing parameter measurement reference load.

***8.** The SPD5 Hub device must be configured in I3C Basic mode to guarantee t_{DOFFT} value. See **Figure 14**. See **Figure 22** for output timing parameter measurement reference load.

***9.** The SPD5 Hub device must be configured in I3C Basic mode. The Host guarantees t_{DOFFC} value. See **Figure 15**. See **Figure 22** for output timing parameter measurement reference load. Also refer to MIPI Alliance Specification for I3C Basic Version 1.0-19 July 2018, section 5.1.2.3.2, Transition from Address ACK to Mandatory Byte during IBI. The SPD5 Hub device must be configured in I3C Basic mode. The Host guarantees t_{DOFFC} value.

***10.** See **Figure 17**.

***11.** From STOP condition of DEVCTRL CCC to START condition for Register Read or Register Write Command Data Packet delay.

***12.** The device sends NACK if Host does not satisfy $t_{DEVCTRLCCC\_DELAY\_PEC\_DIS}$ timing parameter.

***13.** This timing parameter restriction is only applicable when PEC function is disabled in SPD5 Hub. If PEC is enabled, this timing parameter does not apply.

***14.** From STOP condition for Register Write Command Data Packet to START condition for Register Read Command Data Packet delay.

***15.** This timing parameter restriction is only applicable when PEC function is enabled in SPD5 Hub. If PEC is disabled, this timing parameter does not apply.

***16.** The SPD5 Hub sends NACK if Host does not satisfy $t_{WR\_RD\_DELAY\_PEC\_EN}$ timing parameter.

3. Temperature Sensor Performance

Table 123 Temperature Sensor Performance

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{ACC1}	Temperature Sensor Accuracy (Active Range)	Ta = +75°C to +95°C	-	±0.5	±1.0	°C
T_{ACC2}	Temperature Sensor Accuracy (Monitor Range)	Ta = +40°C to +125°C	-	±1.0	±2.0	°C
T_{ACC3}	Temperature Sensor Accuracy (Industrial Temperature Range)	Ta = −40°C to +125°C	-	±2.0	±3.0	°C
T_{S_RES}	Resolution	Default value	-	0.25	-	°C
t_{CONV}	Temperature conversion time	Assumes 0.25°C accuracy	-	-	68	ms
T_{S_HYS}	Hysteresis between temperature events	Default value	1	-	-	°C

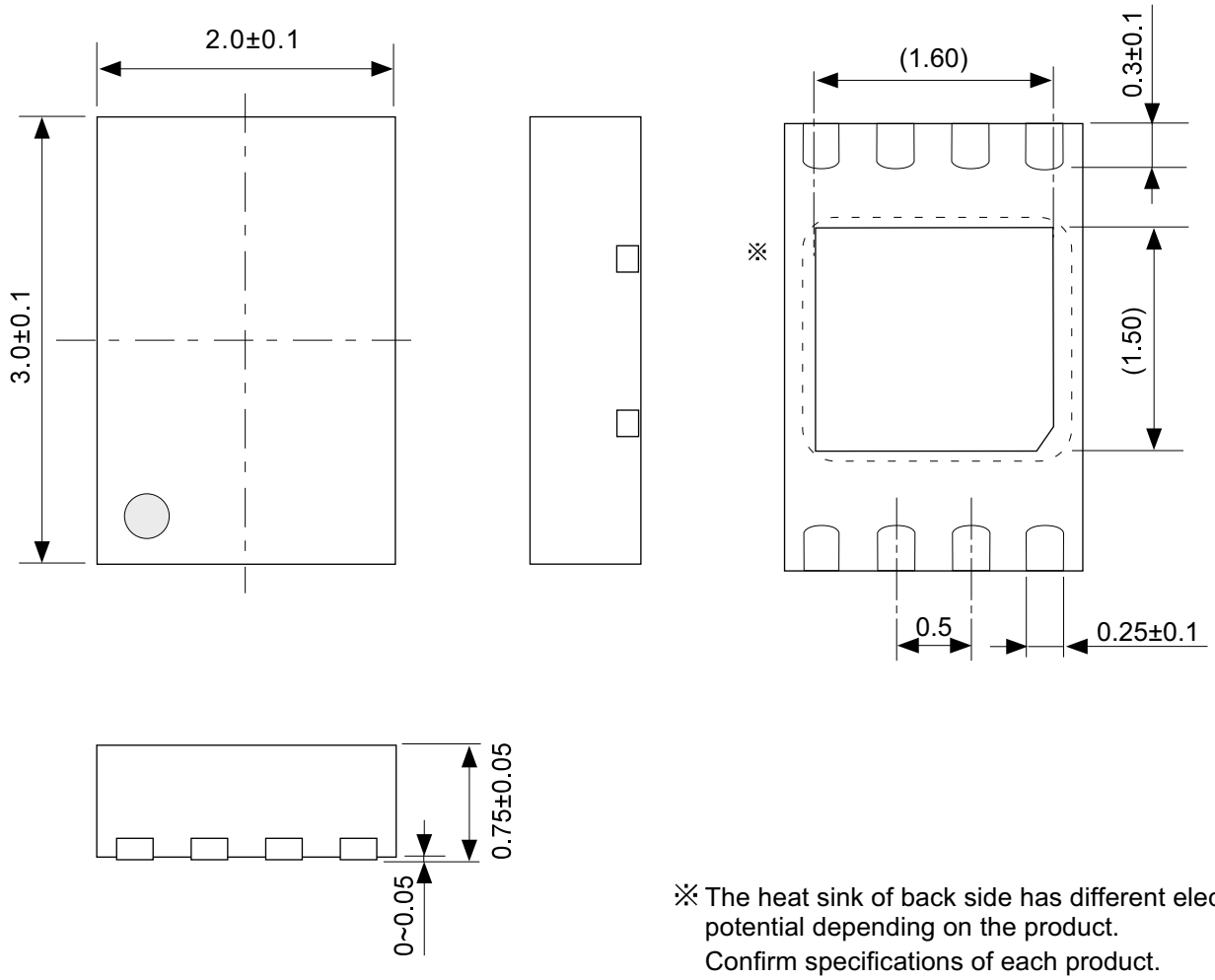
■ Precautions

- Do not operate these ICs in excess of the absolute maximum ratings. Attention should be paid to the power supply voltage, especially. The surge voltage which exceeds the absolute maximum ratings can cause latch-up and malfunction. Perform operations after confirming the detailed operation condition in the data sheet.

- Operations with moisture on this IC's pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking this IC up from low temperature tank during the evaluation. Be sure that not remain frost on this IC's pin to prevent malfunction by short-circuit.
  Also attention should be paid in using on environment, which is easy to dew for the same reason.

- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.

- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.



※ The heat sink of back side has different electric potential depending on the product.
Confirm specifications of each product.
Do not use it as the function of electrode.

No. PQ008-B-P-SD-1.0

TITLE	DFN-8-B-PKG Dimensions
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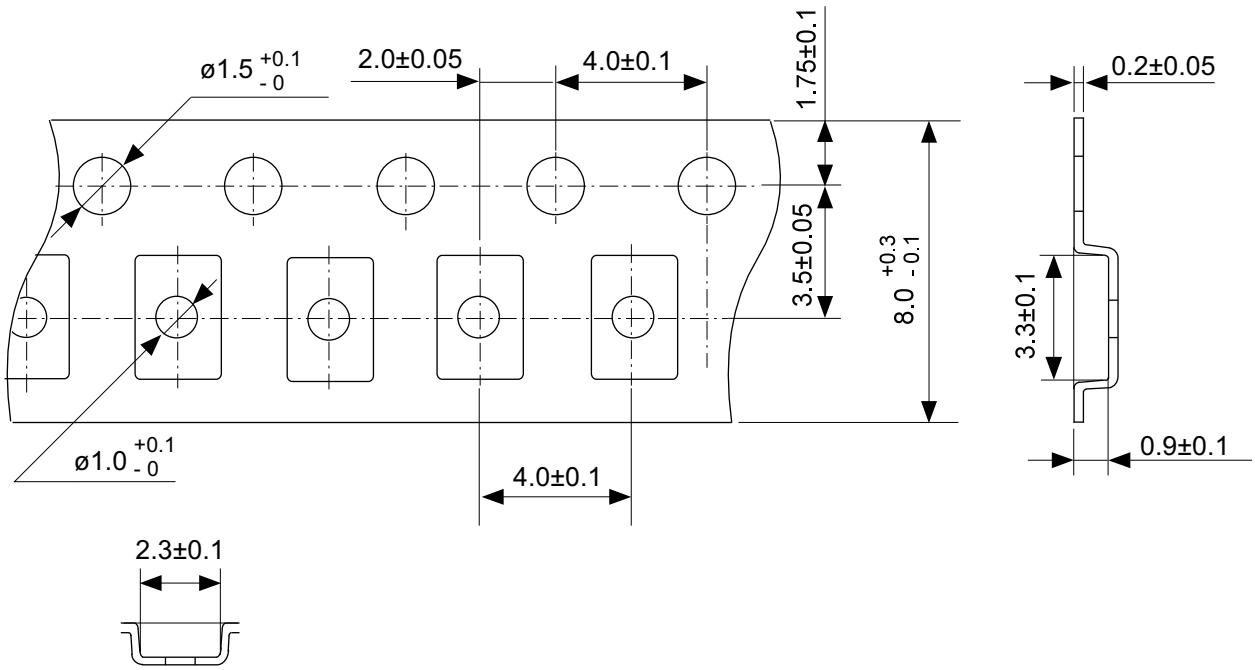
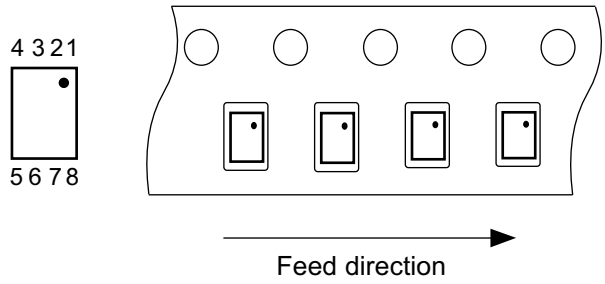
ANGLE	
UNIT	mm
ABLIC Inc.	





No. PQ008-B-C-SD-1.0

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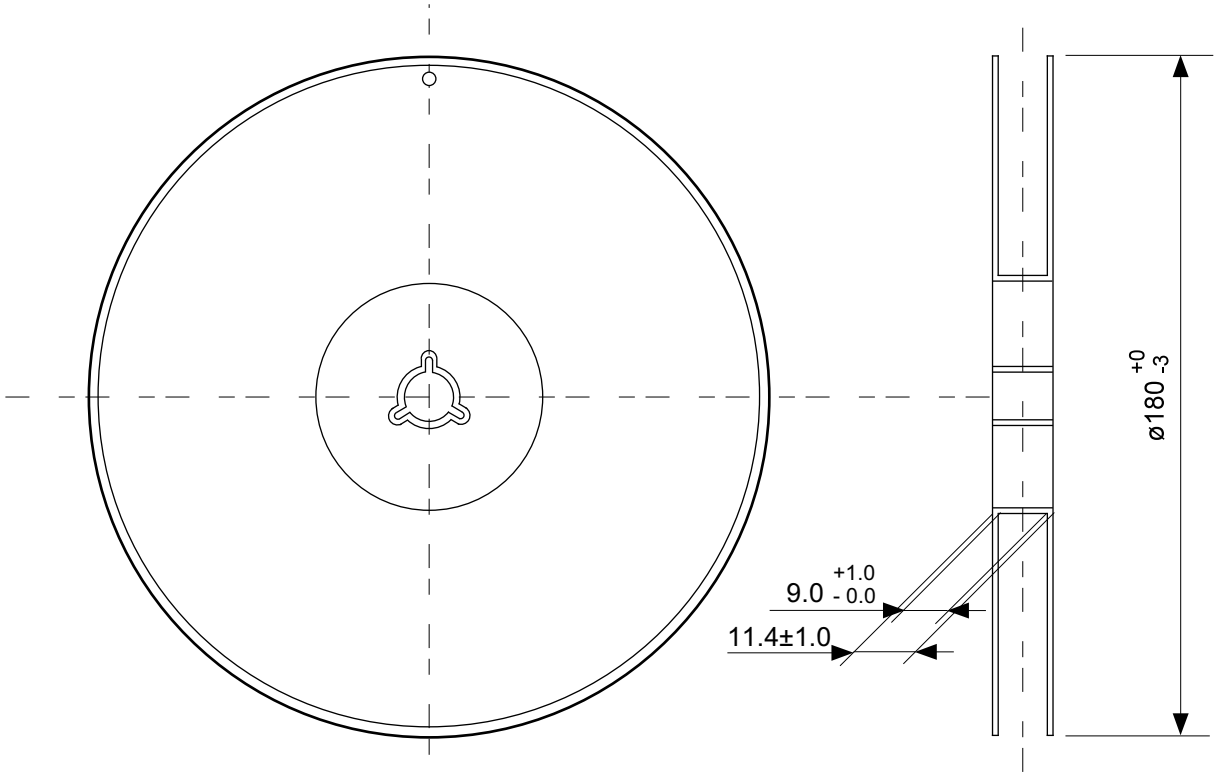
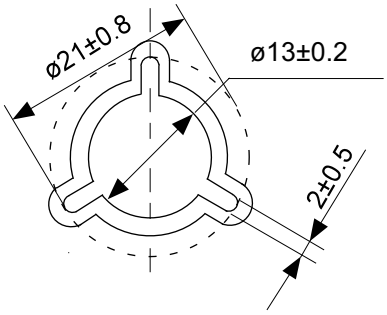
UNIT	mm
ABLIC Inc.	



Enlarged drawing in the central part



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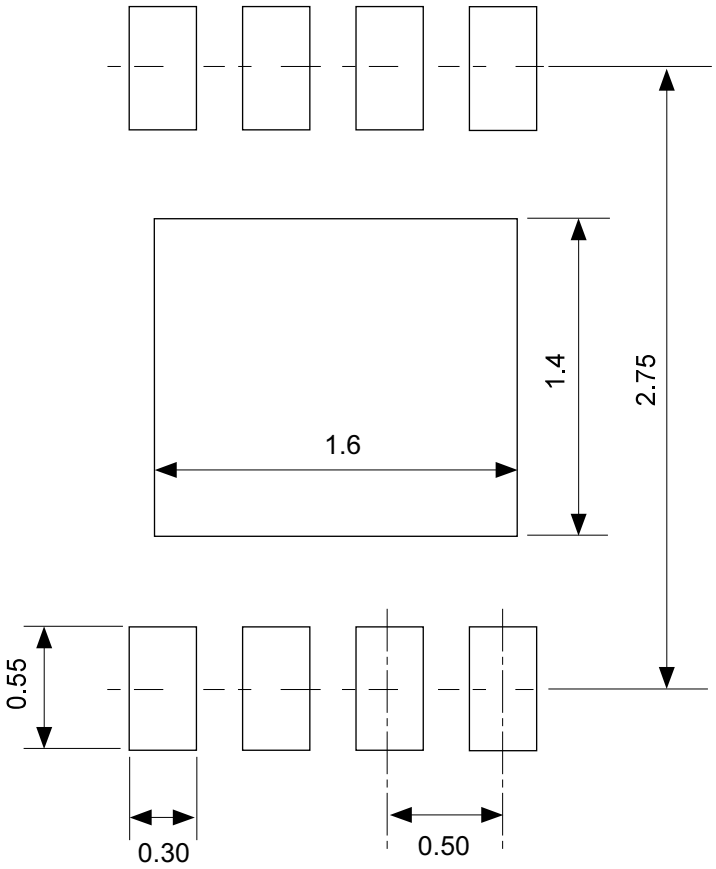
UNIT	mm		
ABLIC Inc.			



No. PQ008-B-L-SD-1.0

TITLE	DFN-8-B-Land Recommendation
No.	PQ008-B-L-SD-1.0
ANGLE	
UNIT	mm
ABLIC Inc.	

Disclaimers (Handling Precautions)

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