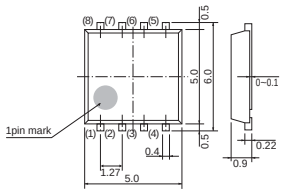
4.5V Drive Nch MOSFET

RMW180N03

● Structure
Silicon N-channel MOSFET

● Dimensions (Unit : mm)

PSOP8



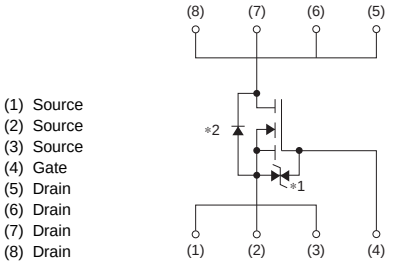
●Features
1) High Power package(PSOP8).
2) High-speed switching,Low On-resistance.
3) Low voltage drive(4.5V drive).

● Application
Switching

● Packaging specifications

Type	Package	Taping
	Code	TB
	Basic ordering unit (pieces)	2500
RMW180N03		O

● Inner circuit



*1 ESD PROTECTION DIODE
*2 BODY DIODE

● Absolute maximum ratings (Ta = 25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	30	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	Continuous	I_D	±18	A
	Pulsed	I_{DP} *1	±72	A
Source current (Body Diode)	Continuous	I_S	2.5	A
	Pulsed	I_{SP} *1	72	A
Power dissipation		P_D *2	3.0	W
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	−55 to +150	°C

*1 Pw≤10μs, Duty cycle≤1%

*2 MOUNTED ON 40mm × 40mm Cu BOARD

● Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to Ambient	Rth (ch-a)*	41.7	°C / W

* MOUNTED ON 40mm × 40mm Cu BOARD

● **Electrical characteristics** (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Gate-source leakage	I_{GSS}	-	-	±10	μA	V_{GS}=±20V, V_{DS}=0V
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	I_D=1mA, V_{GS}=0V
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	V_{DS}=30V, V_{GS}=0V
Gate threshold voltage	$V_{GS\ (th)}$	1.0	-	2.5	V	V_{DS}=10V, I_D=1mA
Static drain-source on-state resistance	$R_{DS\ (on)}$*	-	4.0	5.6	mΩ	I_D=18A, V_{GS}=10V
		-	5.5	7.7		I_D=18A, V_{GS}=4.5V
Forward transfer admittance	$\|Y_{fs}\|$*	15	-	-	S	I_D=18A, V_{DS}=10V
Input capacitance	C_{iss}	-	1250	-	pF	V_{DS}=15V
Output capacitance	C_{oss}	-	400	-	pF	V_{GS}=0V
Reverse transfer capacitance	C_{rss}	-	145	-	pF	f=1MHz
Turn-on delay time	$t_{d(on)}$*	-	14	-	ns	I_D=9A, V_{DD}≒15V
Rise time	t_r *	-	39	-	ns	V_{GS}=10V
Turn-off delay time	$t_{d(off)}$*	-	39	-	ns	R_L=1.67Ω
Fall time	t_f *	-	12	-	ns	R_G=10Ω
Total gate charge	Q_g *	-	24	-	nC	I_D=18A, V_{DD}≒15V
Gate-source charge	Q_{gs} *	-	4.4	-	nC	V_{GS}=10V
Gate-drain charge	Q_{gd} *	-	4.7	-	nC	

*Pulsed

●**Body diode characteristics** (Source-Drain) (Ta = 25°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Forward Voltage	V_{SD}*	-	-	1.2	V	I_s=2.5A, V_{GS}=0V

*Pulsed

●Electrical characteristic curves (Ta=25°C)

Fig.1 Typical Output Characteristics(Ⅰ)

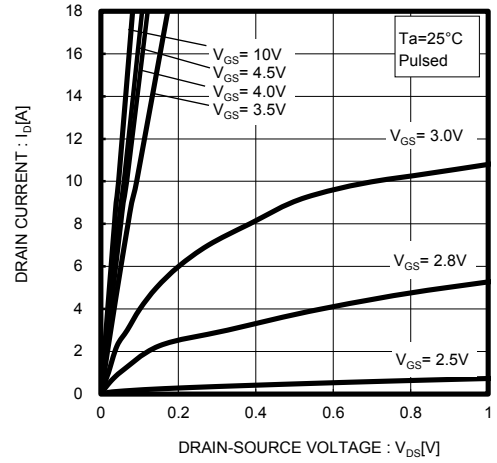


Fig.2 Typical Output Characteristics(Ⅱ)

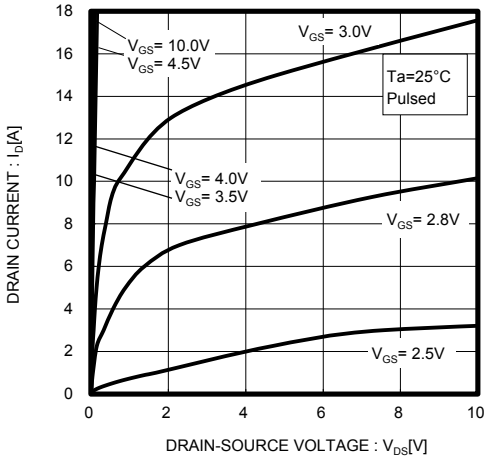


Fig.3 Typical Transfer Characteristics

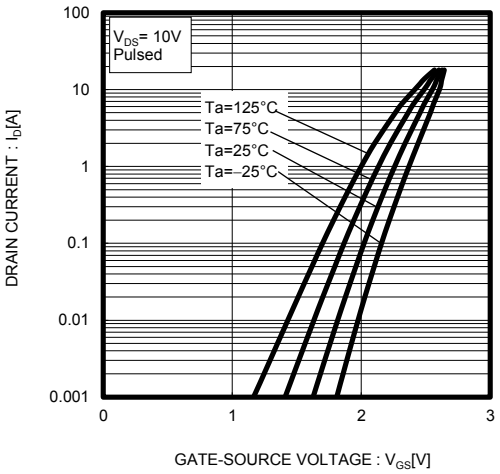


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(Ⅰ)

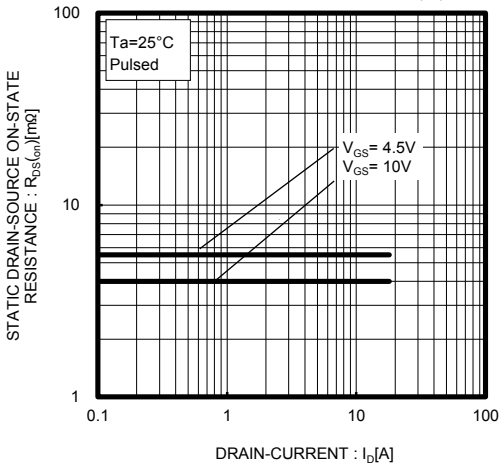


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(Ⅱ)

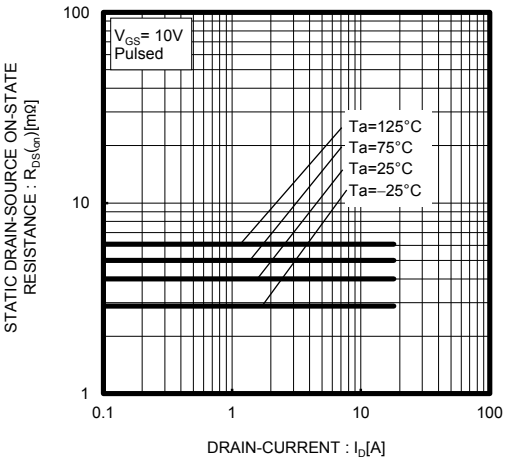


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

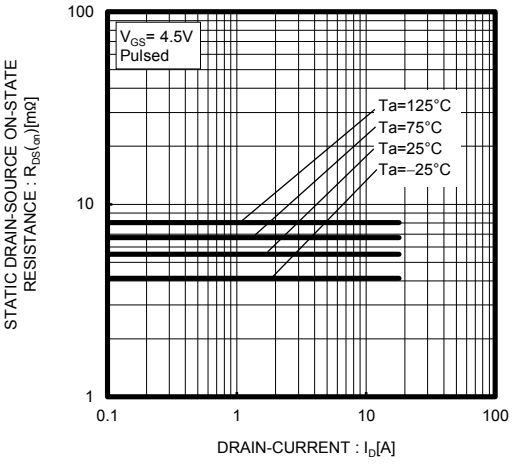


Fig.7 Forward Transfer Admittance vs. Drain Current

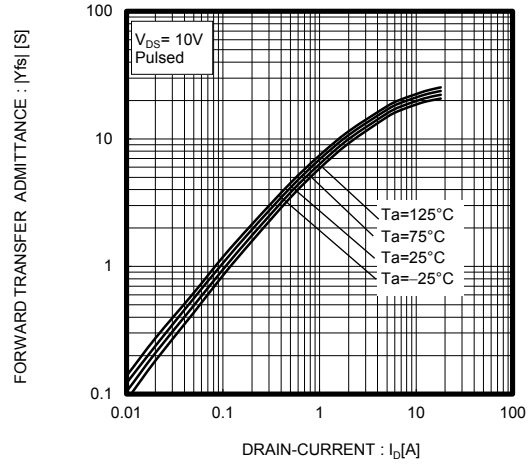


Fig.8 Reverse Drain Current vs. Sourse-Drain Voltage

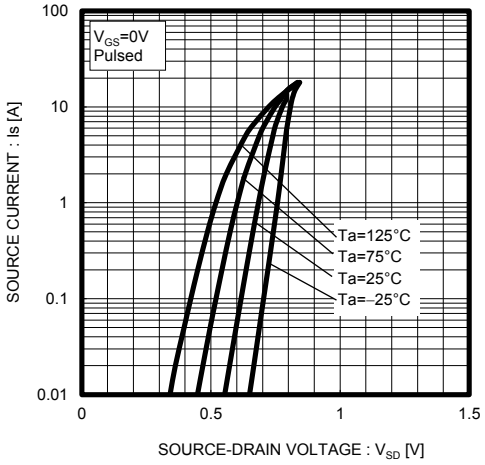


Fig.9 Static Drain-Source On-State Resistance vs. Gate Source Voltage

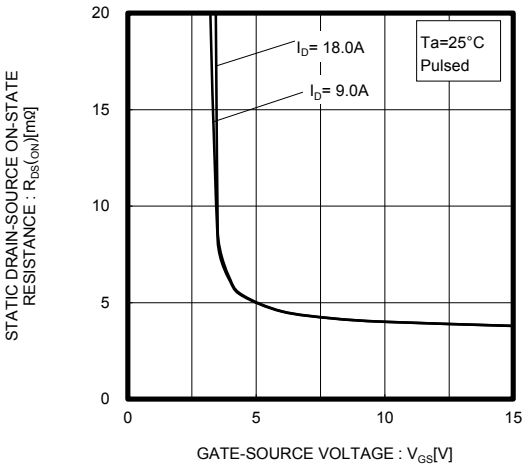


Fig.10 Switching Characteristics

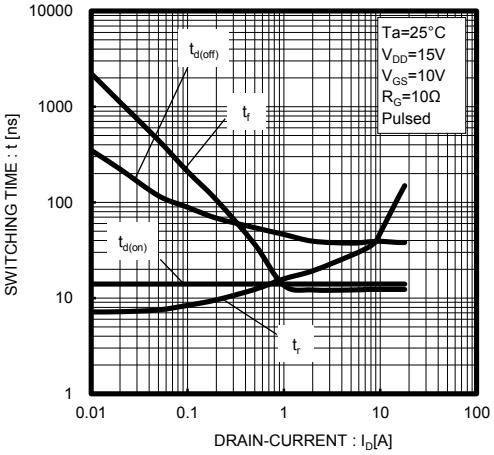


Fig.11 Dynamic Input Characteristics

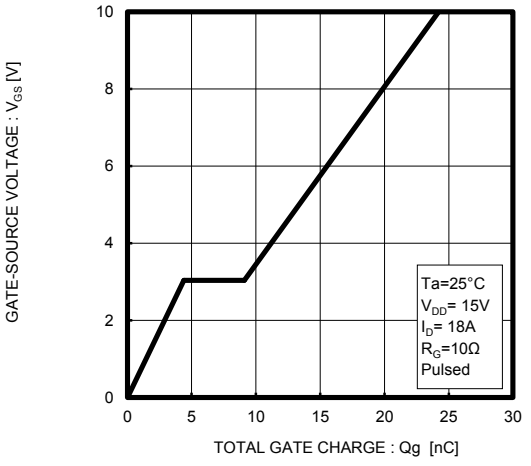


Fig.12 Typical Capacitance vs. Drain-Source Voltage

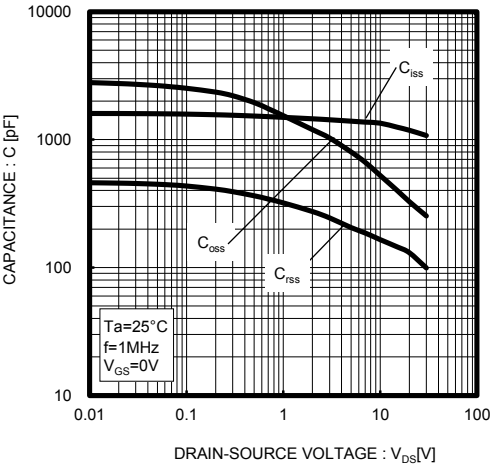


Fig.13 Maximum Safe Operating Aera

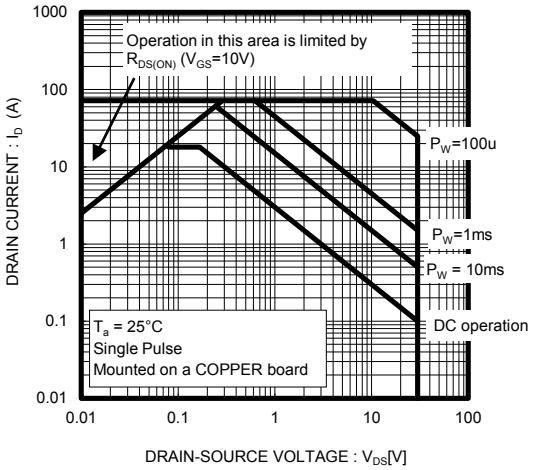
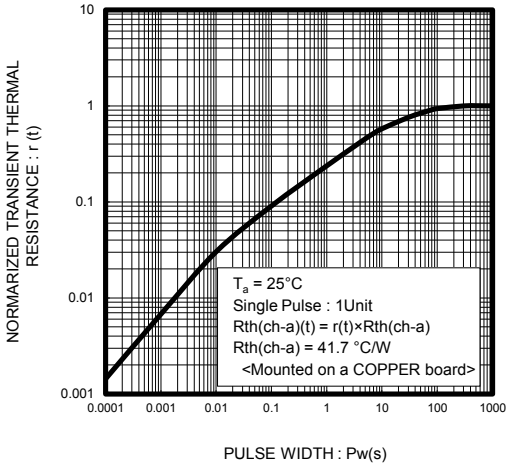


Fig.14 Normalized Transient Thermal Resistance vs. Pulse Width



● **Measurement circuits**

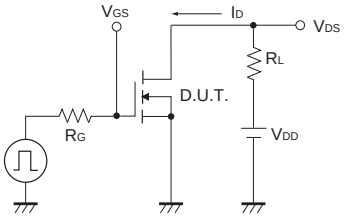


Fig.1-1 Switching Time Measurement Circuit

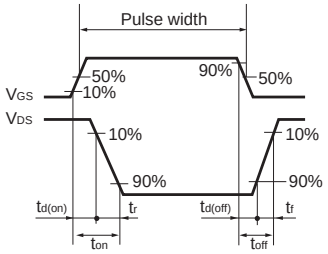


Fig.1-2 Switching Waveforms

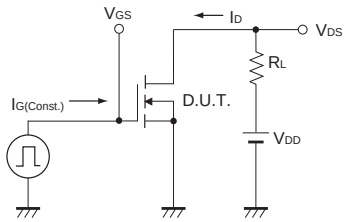


Fig.2-1 Gate Charge Measurement Circuit

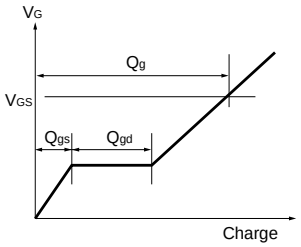


Fig.2-2 Gate Charge Waveform

● **Notice**

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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