312MHZ CLOCK & CRYSTAL MULTIPLIER WITH LVDS OUTPUTS

NOVEMBER 2003 *REV. 1.0.2*

DESCRIPTION

The XRT8010 is a monolithic analog phase locked loop that provides a high frequency LVDS clock output, using a low frequency crystal or reference clock. It is designed for SONET/SDH and other low jitter applications.The high performance of the IC provides a very low jitter LVDS clock output up to 320 MHz, while operating at 3.3 volts. The XRT8010 has a selectable 8x or 16x internal multiplier for an external crystal or signal source. The Output Enable pin provides a true disconnect for the LVDS output. The very compact (4 x 4 mm) low inductance package is ideal for high frequency operation.

APPLICATIONS

- Gigabit Ethernet
- SONET/SDH
- SPI-4 Phase 2
- 8x or 16x Clock Multiplier for
  - Computer
  - Telecommunications Sytems

FEATURES

- 156 or 320 MHz Operating Range
- Low Output Jitter:
  - 0.0009 UI_{RMS} typical @ 155.52 MHz, per Telcordia GR-253-CORE for OC-3.
- On Chip Crystal Oscillator Circuit
  - Optimized for 15 to 40 MHz crystals
  - Uses parallel fundamental mode
- Selectable 8x or 16x multiplier
- Selectable ÷1 or ÷2 LVDS output
- LVDS output meets TIA/EIA 644A Specification (2001)
- 3.3V Low power CMOS: <80 mW typical
- -40°C to +85°C operating temperature
- Extremely small 16-lead QFN package

FIGURE 1. XRT8010 BLOCK DIAGRAM

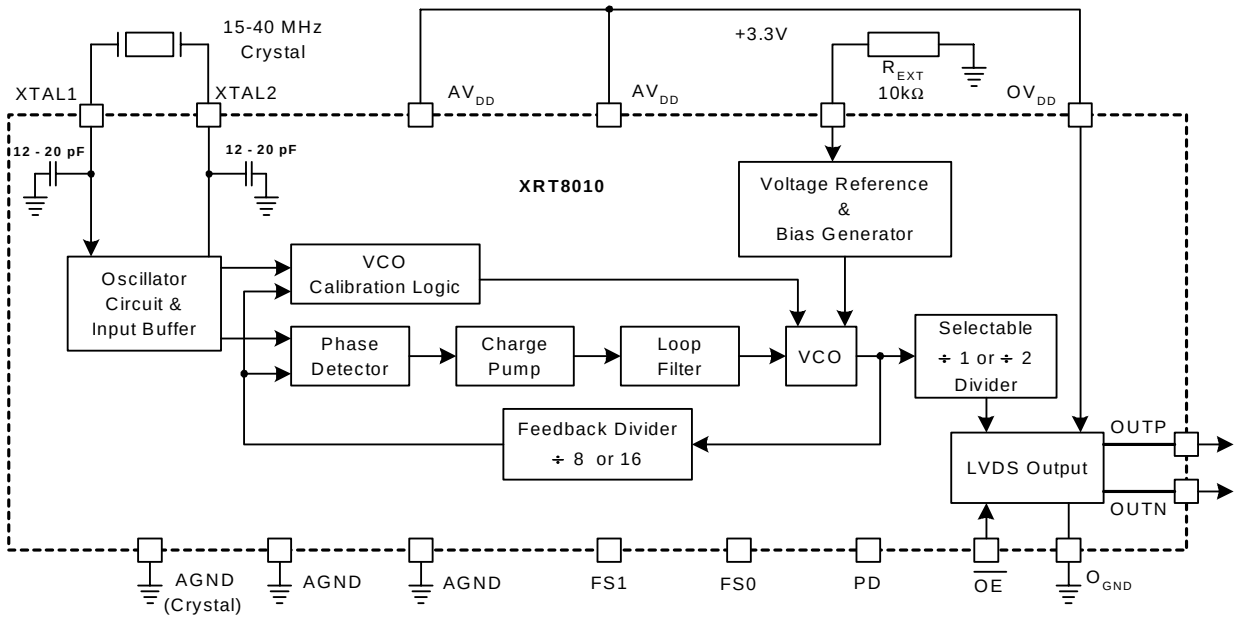
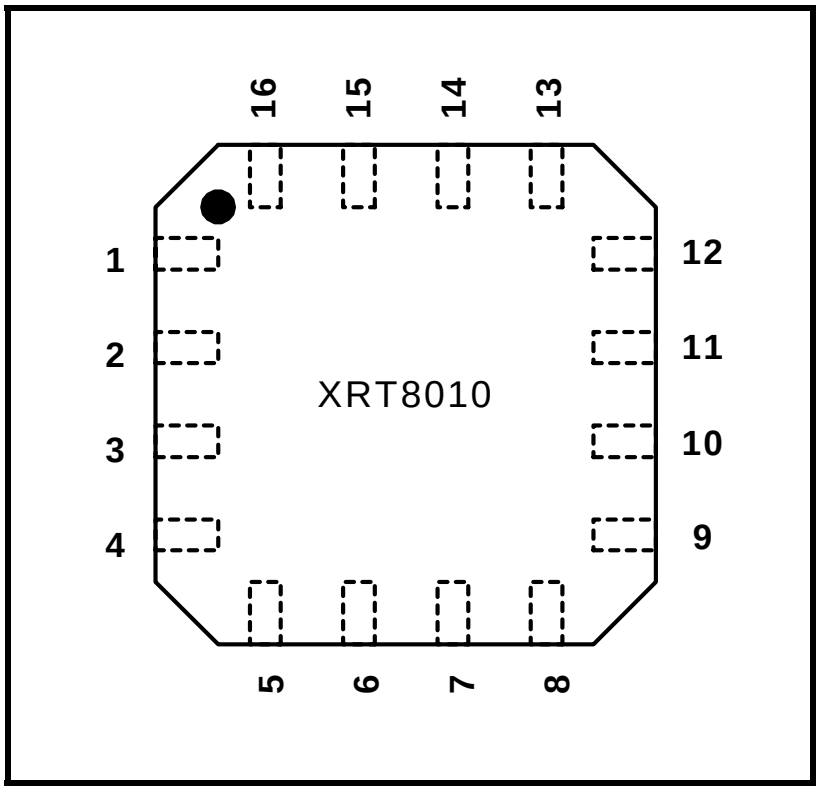


FIGURE 2. PIN-OUT OF THE XRT8010 (TOP VIEW)



ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	OPERATING TEMPERATURE RANGE
XRT8010IL	16 LEAD QUAD FLAT NO LEAD (4 mm x 4 mm, QFN)	-40°C to +85°C

TABLE OF CONTENTS

PIN DESCRIPTION

PIN	NAME	TYPE	DESCRIPTION
1	AVDD		3.3V ±10% Analog Supply for Crystal Oscillator
2	AGND		Analog Ground for Crystal Oscillator
3	XTAL1	I	Crystal pin 1 or external clock input
4	XTAL2	O	Crystal pin 2 (output drive for crystal)
5	AGND		Analog Ground
6	REXT	I	External Bias Resistor (10KΩ to ground)
7	$\overline{OE}$	I	Output Enable, Active low (*Internal 50KΩ pull-down to ground*)
8	PD	I	Power Down, Active High *(Internal 50KΩ pull-down to ground)*
9	FS1	I	Frequency select "1" *(Internal 50KΩ pull-down to ground)*
10	FS0	I	Frequency select "0" *(Internal 50KΩ pull-up to VDD)*
11	AGND		Analog Ground
12	OGND		Output Ground for LVDS outputs
13	OUTN	O	LVDS negative output for 50Ω line
14	OUTP	O	LVDS positive output for 50Ω line
15	OVDD		3.3V ±10% Digital Supply for LVDS Output buffer
16	AVDD		3.3V ±10% Analog Supply

ABSOLUTE MAXIMUM RATINGS

Supply voltage	-0.5 to 6.0 V
VIN	-0.5 to 6.0 V
Storage Temperature	-65°C to + 150°C
Operating Temperature	-40°C to + 85°C
ESD	2,000 volts

ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Supply Voltage	VDD	3.0	3.3	3.6	V	
Supply current	IDD		20	25	mA	
Input Digital High	VINH	2.0			V	
Input Digital Low	VINL			0.8	V	
Crystal Frequency		15		27	MHz	See Section 2,0 for Crystal Selection
Crystal Frequency		27		40	MHz	See Section 2,0 for Crystal Selection

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Power on Calibration time				5	ms	After VDD reaches 2.8V *NOTE: Calibration time = 16,000 clock cycles*
Max Frequency Out	FOUT	140		170	MHz	156 MHz nominal FOUT (see Table 1)
Max Frequency Out	FOUT	285		340	MHz	312 MHz nominal FOUT (see Table 1)
Rise time	TR			300	ps	CL = 5pF, RL = 100Ω (20% – 80%)
Fall Time	TF			300	ps	CL = 5pF, RL = 100Ω (20% – 80%)
Duty cycle		45		55	%	LVDS output
Differential Output Skew				10	ps	See Figure 3
Output Loading			100		Ω	
Output voltage Swing		250		450	mV	Differential (OUTP-OUTN)
Common Mode Voltage	VCM		1.2		V	
Output short circuit current			-5.7	-8	mA	Current limit to ground, VDD or Vp to Vn
Cycle-to-Cycle Jitter			3		ps	rms, at 156 MHz, Input referred
Cycle-to-Cycle Jitter			3		ps	rms, at 312 MHz, Input referred
Intinsic Jitter			16		ps	rms, over 1,000 cycles, at 156 MHz
Intinsic Jitter			16		ps	rms, over 1,000 cycles, at 312 MHz
Spectral Density of Phase Noise $L(f)$						

PARAMETER	COVERSION	TYPICAL
Single Side Band Phase Noise $L(f)$	320MHz @ 100Hz Offset	-77.75 dbc/Hz
	320MHz @ 1kHz Offset	-100.69 dbc/Hz
	320MHz @ 10kHz Offset	-95.38 dbc/Hz
	320MHz @ 100kHz Offset	-99.40 dbc/Hz
	320MHz @ 1MHz Offset	-105.05 dbc/Hz
	320MHz @ 10MHz Offset	-119.03 dbc/Hz

TABLE 1: CATEGORY II INTRINSIC JITTER PER TELCORDIA GR-253-CORE (AT 155MHZ)

JITTER BANDWIDTH	JITTER (RMS)	JITTER (UI_{RMS})
12kHz - 1.3MHz	5.74	0.0009
12kHz - 5MHz	7.89	0.0012
12kHz - 20MHz	8.99	0.0014

FIGURE 3. LVDS OUTPUT WAVEFORMS AND TEST CIRCUITS

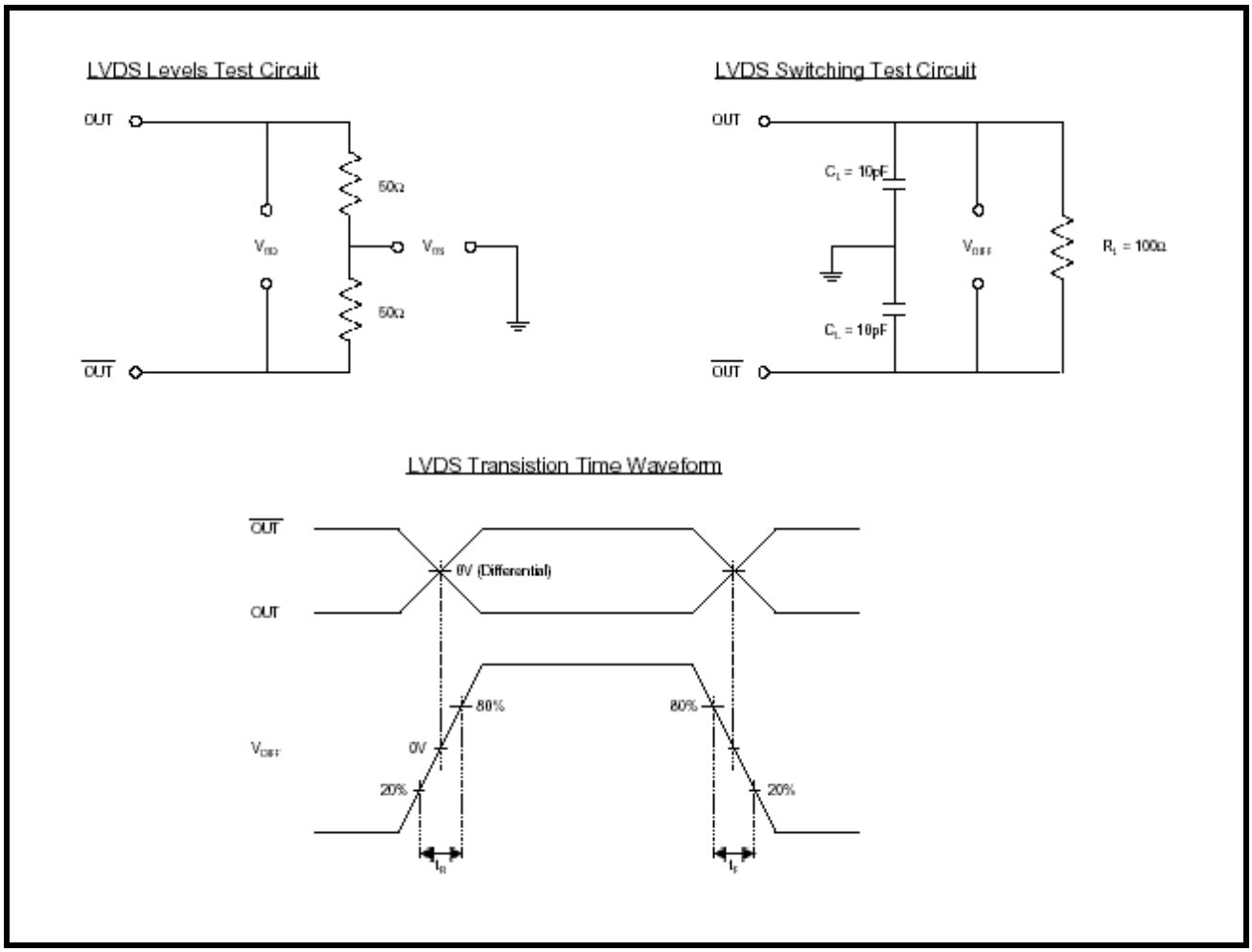


TABLE 2: FREQUENCY SELECTION TABLE

FS0PIN 10	FS1PIN 9	CRYSTAL FREQUENCY	INTERNAL CAPACITOR	MULTIPLY RATIO	OUTPUT DIVIDE	FREQUENCY OUTPUT
1	1	39.0 MHz	12 pF	8x	1	312 MHz
0	1	39.0 MHz	12 pF	8x	2	156 MHz
1	0	19.5 MHz	20 pF	16x	1	312 MHz
0	0	19.5 MHz	20 pF	16x	2	156 MHz

NOTES:

1. *Use Parallel Fundamental mode crystal*
2. *FS0 has a 50KΩ pull-up resistor to VDD on chip*
3. *FS1 has a 50KΩ pull-down resistor to ground on chip*

TABLE 3: POWER-DOWN AND OUTPUT TRI-STATE SELECTION TABLE

PD PIN 8	OE PIN 7	STATUS	NOTES
1	X	Outputs tri-stated and chip Powered-down	"X" = don't care
0	1	Output tri-stated	PD and OE have a 50KΩ pull-down resistor to ground on chip

1.0 CALIBRATION

The XRT8010 synthesizer jitter performance is optimized by calibration of its Voltage Controlled Oscillator (VCO) upon initial power application. This power ON calibration procedure is automatic and completely transparent to the user. It is initiated automatically upon first application of VDD. In order to bring the center frequency of the VCO close to the desired output frequency, the VCO bias current is adjusted via a current DAC at initial power application. The center frequency of VCO is checked against input reference frequency and calibrated internally to the desired output frequency value. These bias voltage trim bits are then held in latches for as long as the VDD is held above 2.7V (minimum specified operational value of VDD). The user should note the following important facts about this calibration procedure for proper operation of the XRT8010:

- For proper operation of the chip and to achieve lowest jitter, the user should follow layout guidelines as described in the User Guide.
- An input crystal of appropriate frequency should be connected at XTAL1 and XTAL2 pins before power is applied to the chip.
- All VDD pins should be tied to 3.3V ±10% simultaneously.
- The power supply should turn on without bouncing below 2.0V smoothly to its specified value in no more than 50msec.
- The calibration takes place during VDD ramp up between 2.6V to 3V values. Once the VDD reaches and maintains 3.0V, the chip retains the calibrated VCO bias voltages in internal latches for proper operation.
- To change a widely different value of crystal or input reference frequency, it is recommended to power down the chip by bringing VDD to 0V and restarting after the change in frequency has occurred.

2.0 CRYSTAL SELECTION

It is recommended that a Fundamental Mode Crystal be used as the timing reference of the XRT8010. The following part has been qualified by EXAR:

CITIZEN Quartz Crystals

20 MHz : HCM49-20.000MABJT

40 MHz : HCM49-40.000MABJT

3.0 DATA AND PLOTS

All plots were recorded using the following parameters and test setup:

- VDD = 3.3 V
- 2" 100Ω Differential Transmission Lines (from LVDS outputs to receiver inputs)
- Fundamental Mode Crystal of 20 MHz
- Vref = 1.5 V (PECL Receiver)

FIGURE 4. INTRINSIC JITTER CONNECTION DIAGRAM

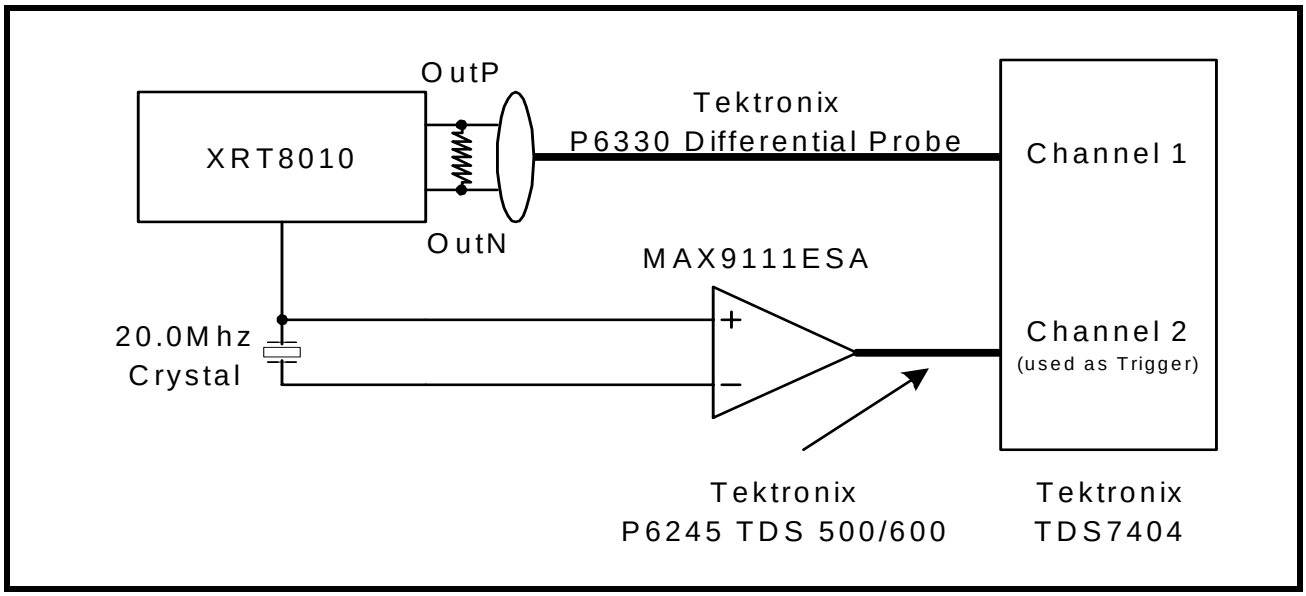


FIGURE 5. SIMPLIFIED BLOCK DIAGRAM OF THE XRT8010 AND PECL RECEIVER

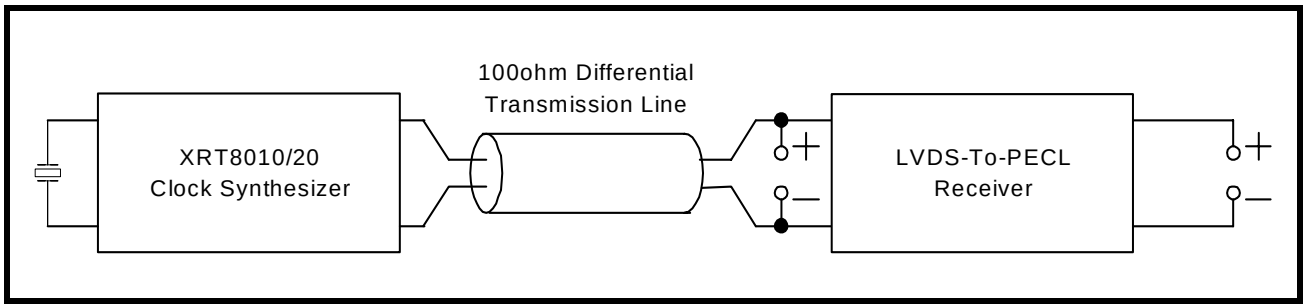


FIGURE 6. LVDS OUTPUT @160 MHZ

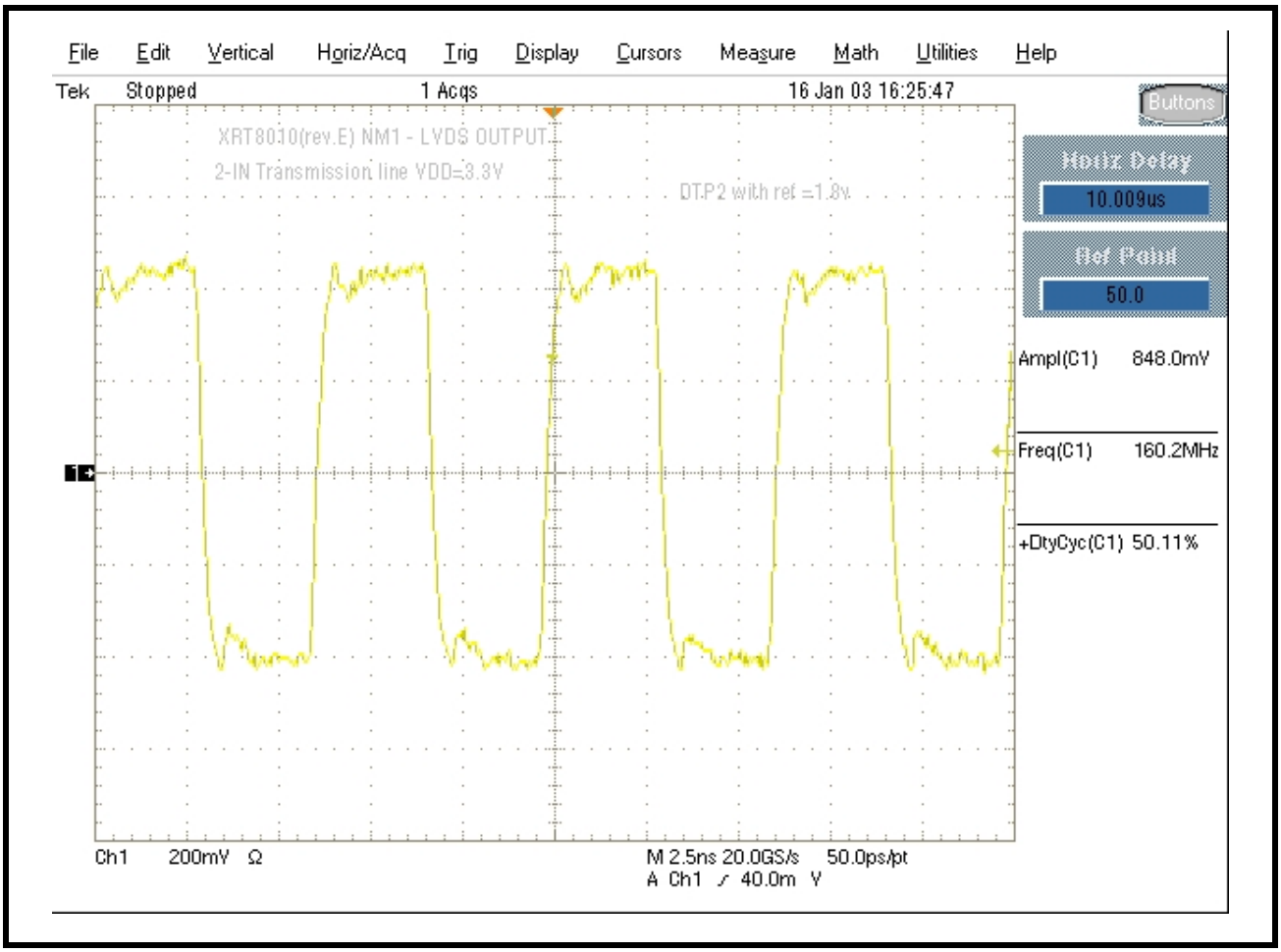


FIGURE 7. LVDS OUTPUT @ 320 MHZ

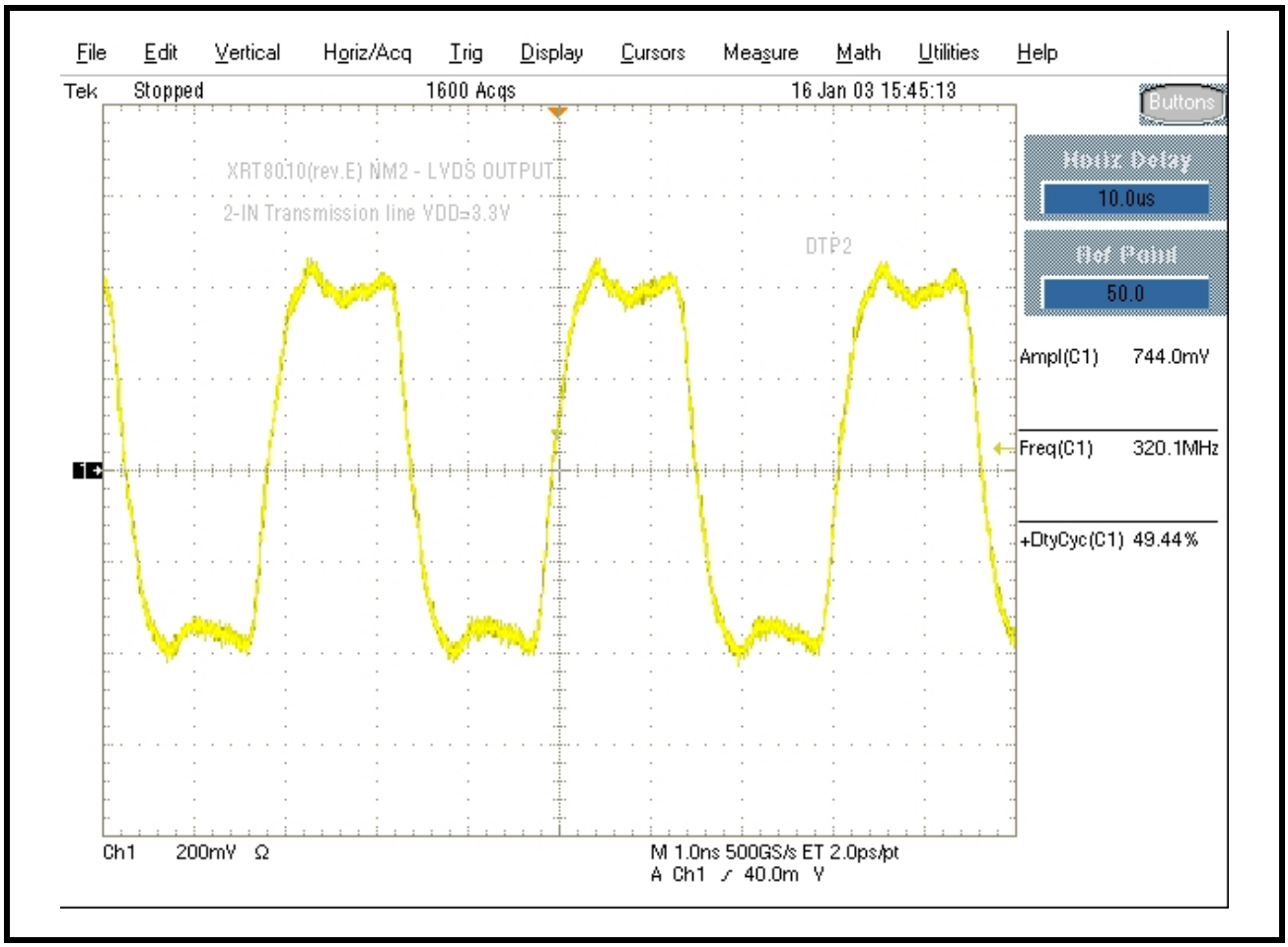
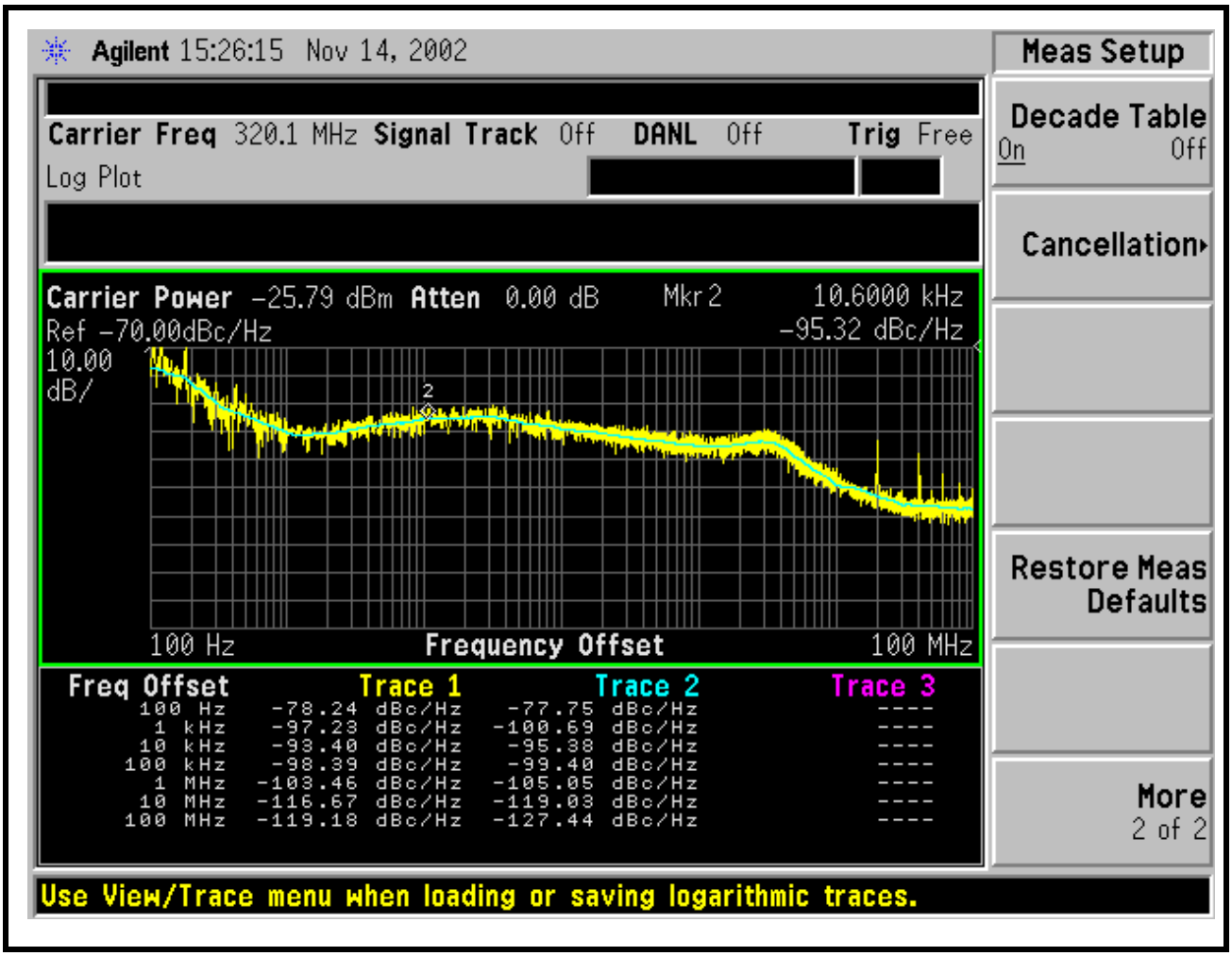


FIGURE 8. XRT8010 PHASE NOISE FOR 20 MHZ REFERENCE CRYSTAL



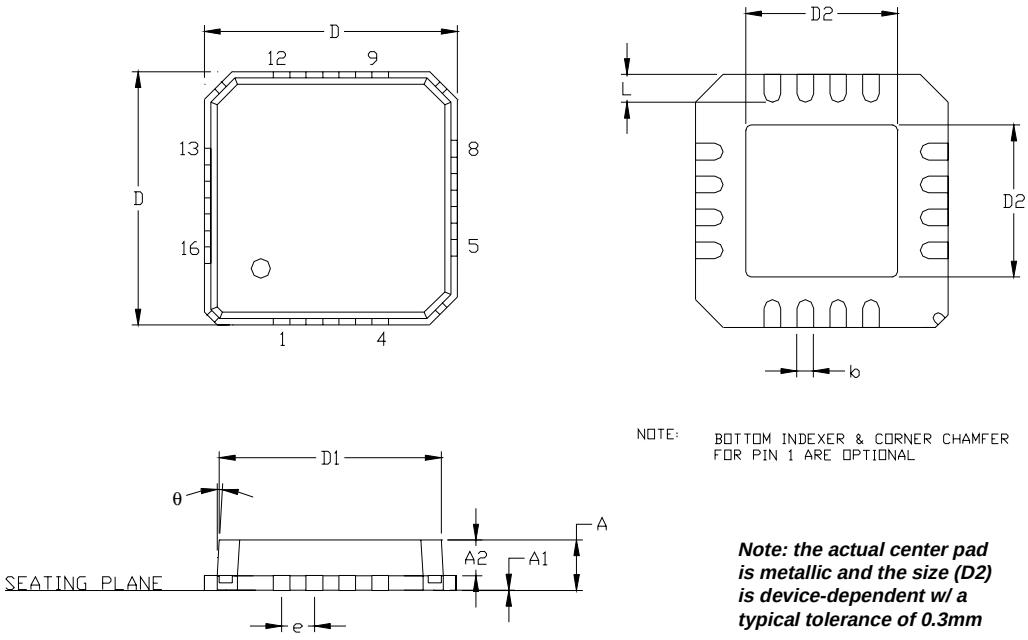
ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT8010IL	16 LEAD QUAD FLAT NO LEAD (4 mm x 4 mm, QFN)	-40°C to +85°C

PACKAGE DIMENSIONS

16 LEAD QUAD FLAT NO LEAD
(4 mm x 4 mm, 0.65 pitch QFN)

Rev. 1.01



Note: the actual center pad is metallic and the size (D2) is device-dependent w/ a typical tolerance of 0.3mm

Note: The control dimension is in millimeter.

SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.031	0.039	0.80	1.00
A1	0.000	0.002	0.00	0.05
A2	0.000	0.039	0.00	1.00
D	0.154	0.161	3.90	4.10
D1	0.144	0.152	3.65	3.85
D2	0.088	0.100	2.24	2.54
b	0.009	0.015	0.23	0.38
e	0.0256 BSC		0.65 BSC	
L	0.014	0.030	0.35	0.75
θ	0°	12°	0°	12°

REVISIONS

P1.0.0 Original issue.

P1.0.1 Modified Electrical Characteristics. Modified Figures

1.0.0 Final release. Added Category II intrinsic jitter measurements per Telcordia GR-253-CORE.

1.0.1 Changed the Page Numbering.

1.0.2 Changed the Package Drawing and Dimensions.

NOTICE

Datasheet November 2003.