

# CY7C1061G/CY7C1061GE

16-Mbit (1 M words × 16 bit) Static RAM with Error-Correcting Code (ECC)

### Features

■ High speed

□ t<sub>AA</sub> = 10 ns/15 ns

- Embedded error-correcting code (ECC) for single-bit error correction
- Low active and standby currents □ I<sub>CC</sub> = 90-mA typical at 100 MHz □ I<sub>SB2</sub> = 20-mA typical
- Operating voltage range: 1.65 V to 2.2 V, 2.2 V to 3.6 V, and 4.5 V to 5.5 V
- 1.0-V data retention
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Error indication (ERR) pin to indicate 1-bit error detection and correction
- Available in Pb-free 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages

### **Functional Description**

CY7C1061G and CY7C1061GE are high-performance CMOS fast static RAM devices with embedded ECC<sup>[1]</sup>. Both devices are offered in single and dual chip enable options and in multiple pin configurations. The CY7C1061GE device includes an ERR pin that signals a single-bit error-detection and correction event during a read cycle.

To access <u>d</u>evices with a single chip enable input, assert the chip enable (CE) input LOW. To access dual chip enable devices, assert both chip enable inputs –  $CE_1$  as LOW and  $CE_2$  as HIGH.

To perform data writes, assert the Write Enable ( $\overline{WE}$ ) input LOW, and provide the data and address on the device data pins ( $I/O_0$  through  $I/O_{15}$ ) and address pins ( $A_0$  through  $A_{19}$ ) respectively. The Byte High Enable (BHE) and Byte Low Enable (BLE) inputs control byte writes, and write data on the corresponding I/O lines to the memory location specified. BHE controls I/O<sub>8</sub> through I/O<sub>15</sub> and BLE controls I/O<sub>0</sub> through I/O<sub>7</sub>.

To perform data reads, assert the Output Enable  $(\overline{\text{OE}})$  input and provide the required address on the address lines. Read data is accessible on I/O lines (I/O<sub>0</sub> through I/O<sub>15</sub>). You can perform byte accesses by asserting the required byte enable signal (BHE or BLE) to read either the upper byte or the lower byte of data from the specified address location.

All I/Os (I/O<sub>0</sub> through I/O<sub>15</sub>) are <u>placed</u> in a high-impedance state when the device is deselected (CE HIGH for a single chip enable device and  $\overline{CE}_1$  HIGH / CE<sub>2</sub> LOW for a <u>dual chip enable</u> device), or control signals are de-asserted (OE, BLE, BHE).

On the CY7C1061GE devices, the detection and correction of a single-bit error in the accessed location is indicated by the assertion of the ERR output (ERR = High). See the Truth Table on page 16 for a complete description of read and write modes.

The logic block diagrams are on page 2.

The CY7C1061G and CY7C1061GE devices are available in 48-pin TSOP I, 54-pin TSOP II, and 48-ball VFBGA packages.

For a complete list of related documentation, click here.

### Product Portfolio

					Current Consumption				
Product	Features and Options (see "Pin Configurations" on page 4)	Range	V <sub>CC</sub> Range	Speed	Operating	ng I <sub>CC</sub> , (mA) Standby, Ico		l (mA)	
			je (V)	(ns) 10/15	f = f <sub>max</sub>		Standby, I <sub>SB2</sub> (mA)		
					<b>Typ</b> <sup>[2]</sup>	Мах	<b>Typ</b> <sup>[2]</sup>	Max	
CY7C1061G18	Single or dual chip enables	Industrial	1.65 V–2.2 V	15	70	80	20	30	
CY7C1061G(E)30		bles	2.2 V–3.6 V	10	90	110			
CY7C1061G	Optional ERR pins		4.5 V–5.5 V	10	90	110			
	Address MSB A <sub>19</sub> pin placement options compatible with Cypress and other vendors								

#### Notes

1. This device does not support automatic write-back on error detection.

2. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC}$  = 1.8 V (for a  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC}$  = 3 V (for a  $V_{CC}$  range of 2.2 V–3.6 V), and  $V_{CC}$  = 5 V (for a  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A$  = 25 °C.

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# Logic Block Diagram – CY7C1061G



### Logic Block Diagram – CY7C1061GE





# CY7C1061G/CY7C1061GE

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### **Pin Configurations**

Figure 1. 48-ball VFBGA (6 x 8 x 1.0 mm) CY7C1061G<sup>[3]</sup> Package/Grade ID: BVJXI



Figure 2. 48-ball VFBGA (6 x 8 x 1.0 mm) Dual Chip Enable without ERR, Address MSB A19 at Ball G2, Dual Chip Enable without ERR, Address MSB A19 at Ball H6, CY7C1061G<sup>[3]</sup> Package/Grade ID: BVXI



Figure 3. 48-ball VFBGA (6 × 8 × 1.0 mm) Single Chip Enable without ERR, Address MSB A19 at Ball G2, CY7C1061G<sup>[3]</sup> Package/Grade ID: BV1XI



Note 3. NC pins are not connected internally to the die.



Figure 5. 48-ball VFBGA (6 × 8 × 1.0 mm)

Dual Chip Enable with ERR, Address MSB A19 at Ball G2

### Pin Configurations (continued)

Figure 4. 48-ball VFBGA (6 x 8 x 1.0 mm) Single Chip Enable with ERR, Address MSB A19 at Ball G2 CY7C1061GE<sup>[4, 5]</sup> Package/Grade ID: BV1XI



Figure 6. 48-ball VFBGA (6 × 8 × 1.0 mm) Dual Chip Enable with ERR, Address MSB A19 at Ball H6 CY7C1061GE<sup>[4, 5]</sup> Package/Grade ID: BVXI



Notes

4. NC pins are not connected internally to the die.

5. ERR is an Output pin. If not used, this pin should be left floating.





### Pin Configurations (continued)

Figure 7. 48-pin TSOP I (12 × 18.4 × 1 mm) Single Chip Enable with ERR CY7C1061GE<sup>[6, 7]</sup> Package/Grade ID: ZXI

73		-
	Α	8 <b>-</b> A5
<sup>74</sup>		
A3 = 2		7 🗖 A <sub>6</sub>
A <sub>2</sub> = 3	4	6 🗖 A <sub>7</sub>
A <sub>1</sub> 🗖 4	4	5 🗖 🗛
A <sub>0</sub> = 5	4	4 🗖 OE
EŘR 🗖 6	4	3 BHE
CF 7	4	$5 = A_8$ $4 = OE$ $3 = BHE$ $2 = BLE$
1/0. 8	4	
1/0		
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		1  /O <sub>15</sub> 0  /O <sub>14</sub> 9  /O <sub>13</sub> 8  /O <sub>12</sub>
1/02 10	ວ ວ	9 1/0 <sub>13</sub>
I/O <sub>3</sub>	3	° = 1/0 <sub>12</sub>
V <sub>DD</sub> <u>■</u> 12 GND <b>■</b> 13	3	/ E GND
GND 🗖 13	3	6 H Vaa
I/O <sub>4</sub> 🖿 14	3	5 1/0
I/O <sub>5</sub> 🗖 15	3	4 🗖 1/010
I/O <sub>6</sub> 🗖 16		3 🗖 1/0,
I/O <sub>7</sub> 🗖 17	3	2 <b>=</b> 1/0 <sub>8</sub>
$I/O_4$ <b>1</b> $I/O_5$ <b>1</b> $I/O_5$ <b>1</b> $I/O_7$ <b>1</b> $I/O_$	3	1 ⊐ NC
NC 🗖 19	3	0 🗖 A <sub>9</sub>
A <sub>19</sub> <b>□</b> 20	2	
A <sub>19</sub> = 20 A <sub>18</sub> = 21	2	9 <b>a</b> A <sub>10</sub> 8 <b>a</b> A <sub>11</sub>
A <sub>18</sub> = 21	2	<sup>o</sup> A <sub>11</sub>
$\begin{array}{c c} A_{19} & \blacksquare & 20 \\ A_{18} & \blacksquare & 21 \\ A_{17} & \blacksquare & 22 \\ A_{16} & \blacksquare & 23 \\ A_{16} & \blacksquare & 23 \end{array}$	2	7 🗖 A <sub>12</sub>
A <sub>16</sub> 🖿 23	2	6 <b>P</b> A <sub>13</sub>
A <sub>15</sub> = 24	2	5 <b>–</b> A <sub>14</sub>

# Figure 9. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Dual Chip Enable without ERR CY7C1061G<sup>[6]</sup> Package/Grade ID: ZSXI

I/O <sub>12</sub>		1	54	þ	I/O <sub>11</sub>
$V_{CC}$		2	53		V <sub>SS</sub>
I/O <sub>13</sub>		3	52		I/O <sub>10</sub>
I/O <sub>14</sub>		4	51		I/O <sub>9</sub>
V <sub>SS</sub>		5	50		V <sub>CC</sub>
I/O <sub>15</sub>		6	49		I/O <sub>8</sub>
$A_4$		7	48		A <sub>5</sub>
$A_3$		8	47		A <sub>6</sub>
A <sub>2</sub>		9	46		A <sub>7</sub>
A <sub>1</sub>		10	45		А <sub>8</sub>
A <sub>0</sub>		11	44	6	A <sub>9</sub>
BHE		12	43		NC
CE₁		13	42	5	OE
V <sub>CC</sub>		14	41		V <sub>SS</sub>
WE		15	40		NC
$CE_2$		16	39		BLE
A <sub>19</sub>	Г	17	38		A <sub>10</sub>
A <sub>18</sub>		18	37		A <sub>11</sub>
A <sub>17</sub>		19	36		A <sub>12</sub>
A <sub>16</sub>		20	35		A <sub>13</sub>
A <sub>15</sub>		21	34		A <sub>14</sub>
I/O <sub>0</sub>		22	33		I/O <sub>7</sub>
V <sub>CC</sub>		23	32		$V_{SS}$
I/O <sub>1</sub>	Г	24	31		I/O <sub>6</sub>
I/O <sub>2</sub>		25	30		I/O <sub>5</sub>
$V_{SS}$		26	29		$V_{CC}$
I/O <sub>3</sub>		27	28	μ	I/O <sub>4</sub>

### Figure 8. 48-pin TSOP I (12 × 18.4 × 1 mm) Single Chip Enable without ERR CY7C1061G<sup>[6]</sup> Package/Grade ID: ZXI



# Figure 10. 54-pin TSOP II (22.4 $\times$ 11.84 $\times$ 1.0 mm) Dual Chip Enable with ERR CY7C1061GE $^{[6,\ 7]}$ Package/Grade ID: ZSXI

54   I/O <sub>11</sub> 53   V <sub>SS</sub> 52   I/O <sub>10</sub> 51   I/O <sub>9</sub> 50   V <sub>CC</sub> 49   I/O <sub>8</sub> 48   A <sub>5</sub> 47   A <sub>6</sub> 46   A <sub>7</sub> 45   A <sub>8</sub> 44   A <sub>9</sub>

#### Notes

NC pins are not connected internally to the die.
 ERR is an Output pin. If not used, this pin should be left floating.



# CY7C1061G/CY7C1061GE

### **Maximum Ratings**

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature	–65 °C to +150 °C
Ambient temperature with power applied	–55 °C to +125 °C
Supply voltage on V <sub>CC</sub> relative to GND	–0.5 V to V <sub>CC</sub> + 0.5 V
DC voltage applied to outputs in High Z State <sup>[8]</sup>	–0.5 V to V <sub>CC</sub> + 0.5 V

DC input voltage <sup>[8]</sup>	–0.5 V to $V_{CC}$ + 0.5 V
Current into outputs (LOW)	
Static discharge voltage (MIL-STD-883, Method 301	5)>2001 V
Latch-up current	> 140 mA

### **Operating Range**

Grade	Ambient Temperature	V <sub>CC</sub>
Industrial	–40 °C to +85 °C	1.65 V to 2.2 V, 2.2 V to 3.6 V, 4.5 V to 5.5 V

### **DC Electrical Characteristics**

Over the operating range of -40 °C to 85 °C

-	_				1	0 ns / 15 n	S	
Parameter	Desc	cription	Test Conditions		Min	<b>Typ</b> <sup>[10]</sup>	Max	Unit
V <sub>OH</sub>	OutputHIGH	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = –0.1 mA	1.4	_	_	V	
	voltage	2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -1.0 mA	2.0	_	-		
		2.7 V to 3.6 V	$V_{CC}$ = Min, $I_{OH}$ = -4.0 mA		2.2	-	_	
		4.5 V to 5.5 V	$V_{CC}$ = Min, $I_{OH}$ = -4.0 mA		2.4	-	_	
		4.5 V to 5.5 V	V <sub>CC</sub> = Min, I <sub>OH</sub> = -0.1 mA		V <sub>CC</sub> – 0.4 <sup>[11]</sup>	_	-	
V <sub>OL</sub>	Output LOW	1.65 V to 2.2 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 0.1 mA		-	_	0.2	V
	voltage	2.2 V to 2.7 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 2 mA		-	-	0.4	
		2.7 V to 3.6 V	V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA		_	_	0.4	
	4.5 V to 5.		V <sub>CC</sub> = Min, I <sub>OL</sub> = 8 mA	-	_	0.4		
V <sub>IH</sub> <sup>[8]</sup> Input HIGH voltage		1.65 V to 2.2 V			1.4	-	V <sub>CC</sub> + 0.2	V
	2.2 V to 2.7 V			2.0	_	V <sub>CC</sub> + 0.3		
		2.7 V to 3.6 V			2.0	_	V <sub>CC</sub> + 0.3	
		4.5 V to 5.5 V			2.2	_	V <sub>CC</sub> + 0.5	
V <sub>IL</sub> <sup>[8]</sup>	Input LOW	1.65 V to 2.2 V			-0.2	_	0.4	V
	voltage	2.2 V to 2.7 V			-0.3	_	0.6	
		2.7 V to 3.6 V			-0.3	-	0.8	
		4.5 V to 5.5 V			-0.5	-	0.8	
I <sub>IX</sub>	Input leakage	current	$GND \leq V_{IN} \leq V_{CC}$		-1.0	-	+1.0	μA
I <sub>OZ</sub>	Output leaka	ge current	GND <u>&lt;</u> V <sub>OUT</sub> ≤ V <sub>CC</sub> , Output	disabled	-1.0	-	+1.0	μA
I <sub>CC</sub>	Operating su	pply current	V <sub>CC</sub> = Max, I <sub>OUT</sub> = 0 mA, CMOS levels	f = 100 MHz	-	90.0	110.0	mA
			CMOS levels	f = 66.7 MHz	-	70.0	80.0	
I <sub>SB1</sub>	Automatic CE current – TTL	power down inputs	$\begin{array}{l} \text{Max V}_{\text{CC}}, \overline{\text{CE}} \geq \text{V}_{\text{IH}} ^{[9]}, \\ \text{V}_{\text{IN}} \geq \text{V}_{\text{IH}} \text{ or } \text{V}_{\text{IN}} \leq \text{V}_{\text{IL}},  \text{f} = \text{f}_{\text{MAX}} \end{array}$		-	_	40.0	mA
I <sub>SB2</sub>	Automatic CE current – CM	power down OS inputs	$\begin{array}{l} \text{Max V}_{\text{CC}}, \overline{\text{CE}} \geq \text{V}_{\text{CC}} - 0.2 \text{ V} \\ \text{V}_{\text{IN}} \geq \text{V}_{\text{CC}} - 0.2 \text{ V} \text{ or } \text{V}_{\text{IN}} \leq 0 \end{array}$	/[9], 0.2 V, f = 0	-	20.0	30.0	mA

#### Notes

10. Typical values are included only for reference and are not guaranteed or tested. Typical values are measured at  $V_{CC} = 1.8 \text{ V}$  (for a  $V_{CC}$  range of 1.65 V–2.2 V),  $V_{CC} = 3 \text{ V}$  (for a  $V_{CC}$  range of 2.2 V–3.6 V), and  $V_{CC} = 5 \text{ V}$  (for a  $V_{CC}$  range of 4.5 V–5.5 V),  $T_A = 25 \text{ °C}$ .

11. This parameter is guaranteed by design and is not tested

<sup>8.</sup>  $V_{IL(min)} = -2.0 \text{ V}$  and  $V_{IH(max)} = V_{CC} + 2 \text{ V}$  for pulse durations of less than 2 ns. 9. For all dual chip enable devices,  $\overrightarrow{CE}$  is the logical combination of  $\overrightarrow{CE}_1$  and  $CE_2$ . When  $\overrightarrow{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overrightarrow{CE}$  is LOW; when  $\overrightarrow{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overrightarrow{CE}$  is HIGH.



### Capacitance

Parameter <sup>[12]</sup>	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	48-pin TSOP I	Unit
C <sub>IN</sub>	Input capacitance	$T_A = 25 \circ C$ , f = 1 MHz, $V_{CC} = V_{CC(typ)}$	10	10	10	pF
C <sub>OUT</sub>	I/O capacitance		10	10	10	pF

### **Thermal Resistance**

Parameter <sup>[12]</sup>	Description	Test Conditions	54-pin TSOP II	48-ball VFBGA	48-pin TSOP I	Unit
$\Theta_{JA}$		Still air, soldered on a 3 × 4.5 inch, four layer printed circuit board	93.63	31.50	57.99	°C/W
- 30	Thermal resistance (junction to case)		21.58	15.75	13.42	°C/W

### **AC Test Loads and Waveforms**





Parameters	1.8 V	3.0 V	5.0 V	Unit
R1	1667	317	317	Ω
R2	1538	351	351	Ω
V <sub>TH</sub>	0.9	1.5	1.5	V
V <sub>HIGH</sub>	1.8	3	3	V

#### Notes

Tested initially and after any design or process changes that may affect these parameters.
 Full-device AC operation assumes a 100-µs ramp time from 0 to V<sub>CC</sub> (min) and 100-µs wait time after V<sub>CC</sub> stabilizes to its operational value.



### **Data Retention Characteristics**

Over the operating range of -40 °C to 85 °C

Parameter	Description	Conditions	Min	Max	Unit
V <sub>DR</sub>	V <sub>CC</sub> for data retention		1.0	-	V
I <sub>CCDR</sub>	Data retention current	$ \begin{array}{l} V_{CC} = V_{DR}, \overline{CE} \geq V_{CC} - 0.2 \; V^{[14]}, \\ V_{IN} \geq V_{CC} - 0.2 \; V \; \text{or} \; V_{IN} \leq 0.2 \; V \end{array} $	_	30.0	mA
t <sub>CDR</sub> <sup>[15]</sup>	Chip deselect to data retention time		0	-	ns
t <sub>R</sub> <sup>[15, 16]</sup>	Operation recovery time	V <sub>CC</sub> ≥ 2.2 V	10.0	-	ns
		V <sub>CC</sub> < 2.2 V	15.0	Ι	ns

### Data Retention Waveform





- 14. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 15. This parameter is guaranteed by design and is not tested

<sup>16.</sup> Full-device operation requires linear V<sub>CC</sub> ramp from V<sub>DR</sub> to V<sub>CC</sub> (min)  $\geq$  100 µs or stable at V<sub>CC</sub> (min)  $\geq$  100 µs.



### AC Switching Characteristics

Over the operating range of -40 °C to 85 °C

Parameter [17]	Description	10	ns	15 ns		l la lt
Parameter [17]	Description	Min	Мах	Min	Max	Unit
Read Cycle	•					
t <sub>POWER</sub>	V <sub>CC</sub> (stable) to the first access <sup>[18, 19]</sup>	100.0	-	100.0	-	μs
t <sub>RC</sub>	Read cycle time	10.0	-	15.0	-	ns
t <sub>AA</sub>	Address to data / ERR valid	_	10.0	-	15.0	ns
t <sub>OHA</sub>	Data / ERR hold from address change	3.0	_	3.0	_	ns
t <sub>ACE</sub>	CE LOW to data / ERR valid <sup>[20]</sup>	-	10.0	-	15.0	ns
t <sub>DOE</sub>	OE LOW to data / ERR valid	_	5.0	-	8.0	ns
t <sub>LZOE</sub>	OE LOW to low Z [21, 22, 23]	0	-	1.0	-	ns
t <sub>HZOE</sub>	OE HIGH to high Z <sup>[21, 22, 23]</sup>	-	5.0	-	8.0	ns
t <sub>LZCE</sub>	CE LOW to low Z <sup>[20, 21, 22, 23]</sup>	3.0	-	3.0	-	ns
t <sub>HZCE</sub>	CE HIGH to high Z <sup>[20, 21, 22, 23]</sup>	_	5.0	-	8.0	ns
t <sub>PU</sub>	CE LOW to power-up <sup>[19, 20]</sup>	0	-	0	-	ns
t <sub>PD</sub>	CE HIGH to power-down <sup>[19, 20]</sup>	_	10.0	-	15.0	ns
t <sub>DBE</sub>	Byte enable to data valid	_	5.0	-	8.0	ns
t <sub>LZBE</sub>	Byte enable to low Z <sup>[21, 22]</sup>	0	-	1.0	-	ns
t <sub>HZBE</sub>	Byte disable to high Z <sup>[21, 22]</sup>	_	6.0	-	8.0	ns
Write Cycle [24	, 25]					
t <sub>WC</sub>	Write cycle time	10.0	_	15.0	_	ns
t <sub>SCE</sub>	CE LOW to write end <sup>[20]</sup>	7.0	-	12.0	-	ns
t <sub>AW</sub>	Address setup to write end	7.0	-	12.0	-	ns
t <sub>HA</sub>	Address hold from write end	0	-	0	-	ns
t <sub>SA</sub>	Address setup to write start	0	-	0	-	ns
t <sub>PWE</sub>	WE pulse width	7.0	-	12.0	-	ns
t <sub>SD</sub>	Data setup to write end	5.0	-	8.0	-	ns
t <sub>HD</sub>	Data hold from write end	0	-	0	-	ns
t <sub>LZWE</sub>	WE HIGH to low Z [21, 22, 23]	3.0	-	3.0	-	ns
t <sub>HZWE</sub>	WE LOW to high Z <sup>[21, 22, 23]</sup>	-	5.0	_	8.0	ns
t <sub>BW</sub>	Byte Enable to write end	7.0	-	12.0	-	ns

#### Notes

17. Test conditions assume signal transition time (rise/fall) of 3 ns or less, timing reference levels of 1.5 V (for V<sub>CC</sub> ≥ 3 V) and V<sub>CC</sub>/2 (for V<sub>CC</sub> < 3 V), and input pulse levels of 0 to 3 V (for V<sub>CC</sub> ≥ 3 V) and 0 to V<sub>CC</sub> (for V<sub>CC</sub> < 3V). Test conditions for the read cycle use the output loading, shown in part (a) of Figure 11 on page 8, unless specified otherwise.

18.  $t_{POWER}$  gives the minimum amount of time that the power supply is at stable  $V_{CC}$  until the first memory access is performed.

19. These parameters are guaranteed by design and are not tested.

- 20. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW, CE is HIGH.
- 21. t<sub>HZOE</sub>, t<sub>HZCE</sub>, t<sub>HZWE</sub>, and t<sub>HZBE</sub> are specified with a load capacitance of 5 pF, as shown in part (b) of Figure 11 on page 8. Hi-Z, Lo-Z transition is measured ±200 mV from steady state voltage.

22. At any temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>, t<sub>HZBE</sub> is less than t<sub>LZBE</sub>, t<sub>HZDE</sub> is less than t<sub>LZDE</sub>, and t<sub>HZWE</sub> is less than t<sub>LZWE</sub> for any device.

23. Tested initially and after any design or process changes that may <u>affect these parameters</u>. 24. The internal write time of the memory is defined by the overlap of  $WE = V_{|L}$ ,  $\overline{CE} = V_{|L}$ , and  $\overline{BHE}$  or  $\overline{BLE} = V_{|L}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.

25. The minimum write pulse width for Write Cycle No. 2 (WE controlled, OE LOW) should be sum of t<sub>HZWE</sub> and t<sub>SD</sub>.



### **Switching Waveforms**





Figure 14. Read Cycle No. 2 of CY7C1061GE (Address Transition Controlled) <sup>[26, 27]</sup>



Notes 26. The device is continuously selected,  $\overline{OE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$ ,  $\overline{BHE}$  or  $\overline{BLE}$  or both =  $V_{IL}$ . 27. WE is HIGH for read cycle.





Figure 15. Read Cycle No. 3 (OE Controlled) <sup>[28, 29, 30]</sup>

Notes

28. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

29. WE is HIGH for read cycle.

30. Address valid prior to or coincident with  $\overline{CE}$  LOW transition.





- 31. For all dual chip enable devices, CE is the logical combination of CE<sub>1</sub> and CE<sub>2</sub>. When CE<sub>1</sub> is LOW and CE<sub>2</sub> is HIGH, CE is LOW; when CE<sub>1</sub> is HIGH or CE<sub>2</sub> is LOW, CE is HIGH.
- 32. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 33. Data I/O is in high-impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ . 34. The minimum write cycle pulse width should be equal to sum of  $t_{HZWE}$  and  $t_{SD}$ .
- 35. During this period the I/Os are in output state. Do not apply input signals.





Figure 18. Write Cycle No. 3 (WE controlled)<sup>[36, 37, 38]</sup>

- 36. For all dual chip enable devices, CE is the logical combination of CE<sub>1</sub> and CE<sub>2</sub>. When CE<sub>1</sub> is LOW and CE<sub>2</sub> is HIGH, CE is LOW; when CE<sub>1</sub> is HIGH or CE<sub>2</sub> is LOW, CE is HIGH.
- 37. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 38. Data I/O is in high-impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ . 39. During this period, the I/Os are in output state. Do not apply input signals.





Figure 19. Write Cycle No. 4 ( $\overline{\text{BLE}}$  or  $\overline{\text{BHE}}$  Controlled) [40, 41, 42]

- 40. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.
- 41. The internal write time of the memory is defined by the overlap of  $\overline{WE} = V_{IL}$ ,  $\overline{CE} = V_{IL}$  and  $\overline{BHE}$  or  $\overline{BLE} = V_{IL}$ . These signals must be LOW to initiate a write, and the HIGH transition of any of these signals can terminate the operation. The input data setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 42. Data I/O is in high-impedance state if  $\overline{CE} = V_{IH}$ , or  $\overline{OE} = V_{IH}$  or  $\overline{BHE}$ , and/or  $\overline{BLE} = V_{IH}$ .
- 43. During this period, the I/Os are in output state. Do not apply input signals.



### **Truth Table**

<b>CE</b> [44]	OE	WE	BLE	BHE	1/0 <sub>0</sub> -1/0 <sub>7</sub>	I/O <sub>8</sub> -I/O <sub>15</sub>	Mode	Power
Н	X <sup>[45]</sup>	X <sup>[45]</sup>	X <sup>[45]</sup>	X <sup>[45]</sup>	High-Z	High-Z	Power down	Standby (I <sub>SB</sub> )
L	L	Н	L	L	Data out	Data out	Read all bits	Active (I <sub>CC</sub> )
L	L	Н	L	Н	Data out	High-Z	Read lower bits only	Active (I <sub>CC</sub> )
L	L	Н	Н	L	High-Z	Data out	Read upper bits only	Active (I <sub>CC</sub> )
L	Х	L	L	L	Data in	Data in	Write all bits	Active (I <sub>CC</sub> )
L	Х	L	Г	Н	Data in	High-Z	Write lower bits only	Active (I <sub>CC</sub> )
L	Х	L	Н	L	High-Z	Data in	Write upper bits only	Active (I <sub>CC</sub> )
L	Н	Н	Х	Х	High-Z	High-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )
L	Х	Х	Н	Н	High-Z	High-Z	Selected, outputs disabled	Active (I <sub>CC</sub> )

### ERR Output – CY7C1061GE

Output <sup>[46]</sup>	Mode			
0	Read operation, no single-bit error in the stored data.			
1	Read operation, single-bit error detected and corrected.			
High-Z	Device deselected or outputs disabled or Write operation			

Notes 44. For all dual chip enable devices,  $\overline{CE}$  is the logical combination of  $\overline{CE}_1$  and  $CE_2$ . When  $\overline{CE}_1$  is LOW and  $CE_2$  is HIGH,  $\overline{CE}$  is LOW; when  $\overline{CE}_1$  is HIGH or  $CE_2$  is LOW,  $\overline{CE}$  is HIGH.

<sup>45.</sup> The input voltage levels on these pins should be either at V<sub>IH</sub> or V<sub>IL</sub>. 46. ERR is an Output pin. If not used, this pin should be left floating.



# **Ordering Information**

Speed (ns)	Voltage Range	Ordering Code	Package Diagram	Package Type (all Pb-free)	Key Features/ Differentiators	ERR Pin/Ball	Operating Range
		CY7C1061G-10BV1XI		48-ball VFBGA	Single Chip Enable	No	
		CY7C1061GE-10BV1XI	51-85150		Address MSB A19 at ball G2	Yes	
		CY7C1061G-10BVJXI			Dual Chip Enable	No	
		CY7C1061GE-10BVJXI	31-03130		Address MSB A19 at ball G2	Yes	
	4.5 V–5.5 V	CY7C1061G-10BVXI			Dual Chip Enable	No	
	4.5 V-5.5 V	CY7C1061GE-10BVXI			Address MSB A19 at ball H6	Yes	
		CY7C1061G-10ZSXI	51-85160		Dual Chip Enable	No	
		CY7C1061GE-10ZSXI	51-65160	54-pin 130F II	Dual Chip Enable	Yes	
		CY7C1061G-10ZXI	51-85183	49 pip TSOD I	Single Chip Enable	No	
10		CY7C1061GE-10ZXI	01-00100	40-pin 130F 1	Single Chip Enable	Yes	
10		CY7C1061G30-10BV1XI		48-ball VFBGA	Single Chip Enable	No	
	2.2 V-3.6 V	CY7C1061GE30-10BV1XI	51-85150		Address MSB A19 at ball G2	Yes	
		CY7C1061G30-10BVJXI			Dual Chip Enable Address MSB A19 at ball G2	No	
		CY7C1061GE30-10BVJXI				Yes	
		CY7C1061G30-10BVXI			Dual Chip Enable Address MSB A19 at ball H6	No	Industrial
		CY7C1061GE30-10BVXI				Yes	
		CY7C1061G30-10ZSXI	54.05400	54-pin TSOP II	Dual Chip Enable	No	
		CY7C1061GE30-10ZSXI	51-85160			Yes	
		CY7C1061G30-10ZXI	54.05400		Single Chip Enable	No	
		CY7C1061GE30-10ZXI	51-85183	40-pin 130F 1	Single Chip Enable	Yes	
		CY7C1061GE18-15BV1XI			Single Chip Enable	Yes	
		CY7C1061G18-15BV1XI			Address MSB A19 at ball G2	No	
		CY7C1061GE18-15BVJXI	51-85150	48-ball VFBGA	Dual Chip Enable	Yes	
		CY7C1061G18-15BVJXI	51-65150	40-Dall VFDGA	Address MSB A19 at ball G2	No	
15	1.65 V–2.2 V	CY7C1061GE18-15BVXI			Dual Chip Enable	Yes	
	1.65 V-2.2 V	CY7C1061G18-15BVXI			Address MSB A19 at ball H6	No	
		CY7C1061GE18-15ZSXI	54.05460			Yes	
		CY7C1061G18-15ZSXI	51-85160	54-pin TSOP II		No	
		CY7C1061GE18-15ZXI	E1 0E100	49 pip TOOD	Single Chin Enchle	Yes	
		CY7C1061G18-15ZXI	51-85183	40-pin 150P1	Single Chip Enable	No	



### **Ordering Code Definitions**





### **Package Diagrams**

Figure 20. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A Package Outline

DIMENSIONS IN INCHES[MM]  $\frac{\text{MIN.}}{\text{MAX.}}$ 

JEDEC # MO-142





### Package Diagrams (continued)



### Figure 21. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Z54-II Package Outline

51-85160 \*E



### Package Diagrams (continued)







NOTE:

PACKAGE WEIGHT: See Cypress Package Material Declaration Datasheet (PMDD) posted on the Cypress web.

51-85150 \*H



### Acronyms

Acronym	Description		
BHE	Byte High Enable		
BLE	Byte Low Enable		
CE	Chip Enable		
CMOS	Complementary metal oxide semiconductor		
I/O	Input/output		
OE	Output Enable		
SRAM	Static random access memory		
TSOP	Thin small outline package		
TTL	Transistor-transistor logic		
VFBGA	Very fine-pitch ball grid array		
WE	Write Enable		

### **Document Conventions**

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	megahertz
μΑ	microampere
μS	microsecond
mA	milliampere
mm	millimeter
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt



# **Document History Page**

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Rev.	ECN No.	Orig. of Change	Submission Date	Description of Change
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