

## Features

- High speed
  - $t_{AA} = 10 \text{ ns}$
- Low active power
  - 990 mW (max)
- Operating voltages of  $3.3 \pm 0.3 \text{ V}$
- 2.0 V data retention
- Automatic power down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with  $\overline{CE}_1$  and  $CE_2$  features
- Available in Pb-free 54-pin thin small outline package (TSOP) II package

## Functional Description

The CY7C1069AV33 is a high performance complementary metal oxide semiconductor (CMOS) static RAM organized as 2,097,152 words by 8 bits. Writing to the device is accomplished by enabling the chip (by taking  $CE_1$  LOW and  $CE_2$  HIGH) and Write Enable ( $\overline{WE}$ ) inputs LOW.

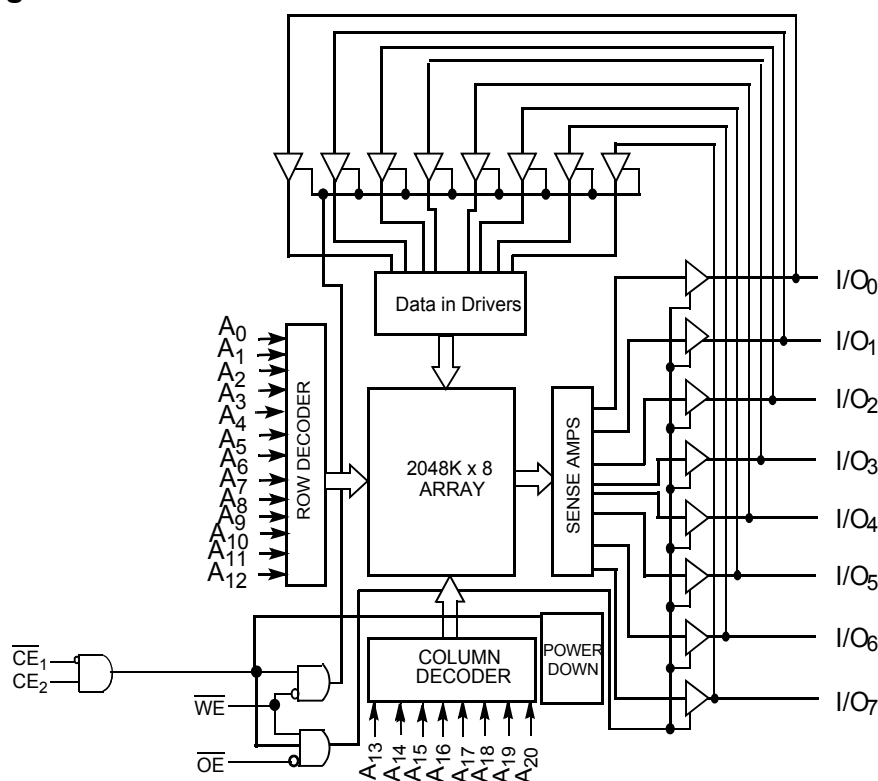
Reading from the device is accomplished by enabling the chip ( $CE_1$  LOW and  $CE_2$  HIGH) as well as forcing the Output Enable ( $\overline{OE}$ ) LOW while forcing the  $\overline{WE}$  HIGH. See [Truth Table on page 9](#) for a complete description of Read and Write modes.

The input/output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $CE_1$  HIGH or  $CE_2$  LOW), the outputs are disabled ( $\overline{OE}$  HIGH), or during a Write operation ( $CE_1$  LOW,  $CE_2$  HIGH, and  $\overline{WE}$  LOW).

The CY7C1069AV33 is available in a 54-pin TSOP II package with center power and ground (revolutionary) pinout.

For a complete list of related documentation, [click here](#).

## Logic Block Diagram



## Contents

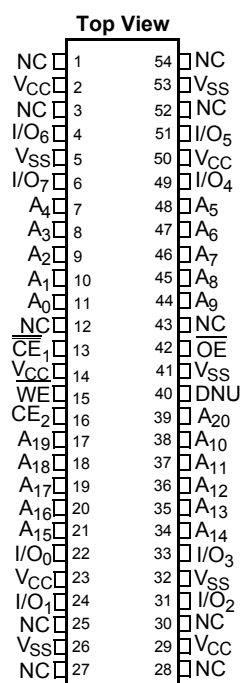
|                                            |           |                                                      |           |
|--------------------------------------------|-----------|------------------------------------------------------|-----------|
| <b>Selection Guide .....</b>               | <b>3</b>  | <b>Package Diagram .....</b>                         | <b>11</b> |
| <b>Pin Configuration .....</b>             | <b>3</b>  | <b>Acronyms .....</b>                                | <b>12</b> |
| <b>Maximum Ratings .....</b>               | <b>4</b>  | <b>Document Conventions .....</b>                    | <b>12</b> |
| <b>Operating Range .....</b>               | <b>4</b>  | Units of Measure .....                               | 12        |
| <b>DC Electrical Characteristics .....</b> | <b>4</b>  | <b>Document History Page .....</b>                   | <b>13</b> |
| <b>Capacitance .....</b>                   | <b>5</b>  | <b>Sales, Solutions, and Legal Information .....</b> | <b>14</b> |
| <b>AC Test Loads and Waveforms .....</b>   | <b>5</b>  | Worldwide Sales and Design Support .....             | 14        |
| <b>Data Retention Waveform .....</b>       | <b>5</b>  | Products .....                                       | 14        |
| <b>AC Switching Characteristics .....</b>  | <b>6</b>  | PSoC® Solutions .....                                | 14        |
| <b>Switching Waveforms .....</b>           | <b>7</b>  | Cypress Developer Community .....                    | 14        |
| <b>Truth Table .....</b>                   | <b>9</b>  | Technical Support .....                              | 14        |
| <b>Ordering Information .....</b>          | <b>10</b> |                                                      |           |
| Ordering Code Definitions .....            | 10        |                                                      |           |

## Selection Guide

| Description                  | -10 | Unit |
|------------------------------|-----|------|
| Maximum access time          | 10  | ns   |
| Maximum operating current    | 275 | mA   |
| Maximum CMOS standby current | 50  | mA   |

## Pin Configuration

Figure 1. 54-pin TSOP II pinout <sup>[1, 2]</sup>



### Notes

1. NC pins are not connected on the die.
2. DNU pins have to be left floating or tied to V<sub>SS</sub> to ensure proper application.

## Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... -65 °C to +150 °C

Ambient temperature with power applied ..... -55 °C to +125 °C

Supply voltage on  $V_{CC}$  to relative GND <sup>[3]</sup> ..... -0.5 V to +4.6 V

DC voltage applied to outputs

in high Z state <sup>[3]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

DC input voltage <sup>[3]</sup> ..... -0.5 V to  $V_{CC} + 0.5$  V

Current into outputs (LOW) ..... 20 mA

## Operating Range

| Range      | Ambient Temperature | $V_{CC}$      |
|------------|---------------------|---------------|
| Commercial | 0 °C to +70 °C      | 3.3 V ± 0.3 V |
| Industrial | -40 °C to +85 °C    |               |

## DC Electrical Characteristics

Over the Operating Range

| Parameter | Description                                   | Test Conditions                                                                                                                                                                | -10  |                | Unit |
|-----------|-----------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|----------------|------|
|           |                                               |                                                                                                                                                                                | Min  | Max            |      |
| $V_{OH}$  | Output HIGH voltage                           | $V_{CC} = \text{Min}, I_{OH} = -4.0 \text{ mA}$                                                                                                                                | 2.4  | –              | V    |
| $V_{OL}$  | Output LOW voltage                            | $V_{CC} = \text{Min}, I_{OL} = 8.0 \text{ mA}$                                                                                                                                 | –    | 0.4            | V    |
| $V_{IH}$  | Input HIGH voltage                            |                                                                                                                                                                                | 2.0  | $V_{CC} + 0.3$ | V    |
| $V_{IL}$  | Input LOW voltage <sup>[3]</sup>              |                                                                                                                                                                                | -0.3 | 0.8            | V    |
| $I_{IX}$  | Input leakage current                         | $GND \leq V_I \leq V_{CC}$                                                                                                                                                     | -1   | +1             | μA   |
| $I_{OZ}$  | Output leakage current                        | $GND \leq V_{OUT} \leq V_{CC}$ , Output Disabled                                                                                                                               | -1   | +1             | μA   |
| $I_{CC}$  | $V_{CC}$ Operating supply current             | $V_{CC} = \text{Max}, f = f_{MAX} = 1/t_{RC}$                                                                                                                                  | –    | 275            | mA   |
| $I_{SB1}$ | Automatic CE power down current – TTL Inputs  | $CE_2 \leq V_{IL}$ , Max $V_{CC}$ , $\overline{CE}_1 \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{MAX}$                                               | –    | 70             | mA   |
| $I_{SB2}$ | Automatic CE power down current – CMOS inputs | $CE_2 \leq 0.3 \text{ V}$ , Max $V_{CC}$ ,<br>$\overline{CE}_1 \geq V_{CC} - 0.3 \text{ V}$ ,<br>$V_{IN} \geq V_{CC} - 0.3 \text{ V}$ or $V_{IN} \leq 0.3 \text{ V}$ , $f = 0$ | –    | 50             | mA   |

### Note

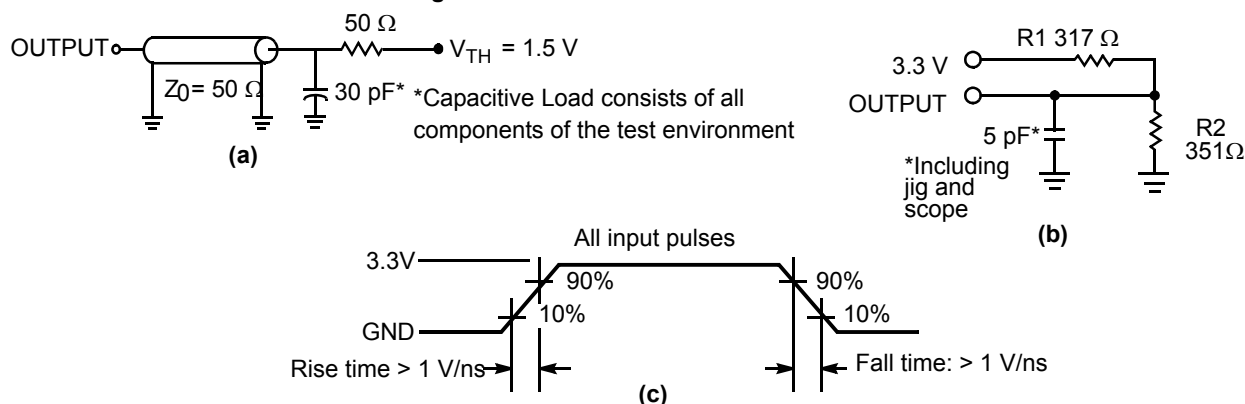
3.  $V_{IL}$  (min.) = -2.0 V for pulse durations of less than 20 ns.

## Capacitance

| Parameter <sup>[4]</sup> | Description       | Test Conditions                                                         | TSOP II | Unit |
|--------------------------|-------------------|-------------------------------------------------------------------------|---------|------|
| $C_{IN}$                 | Input capacitance | $T_A = 25^\circ\text{C}$ , $f = 1\text{ MHz}$ , $V_{CC} = 3.3\text{ V}$ | 6       | pF   |
| $C_{OUT}$                | I/O capacitance   |                                                                         | 8       | pF   |

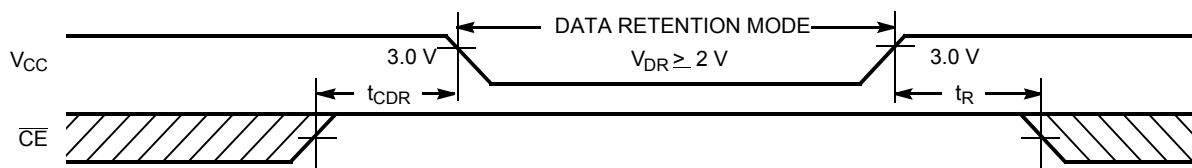
## AC Test Loads and Waveforms

Figure 2. AC Test Loads and Waveforms<sup>[5]</sup>



## Data Retention Waveform

Figure 3. Data Retention Waveform



### Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Valid SRAM operation does not occur until the power supplies have reached the minimum operating  $V_{DD}$  (3.0V). As soon as 1ms ( $T_{power}$ ) after reaching the minimum operating  $V_{DD}$ , normal SRAM operation can begin including reduction in  $V_{DD}$  to the data retention ( $V_{CCDR}$ , 2.0V) voltage.

## AC Switching Characteristics

Over the Operating Range

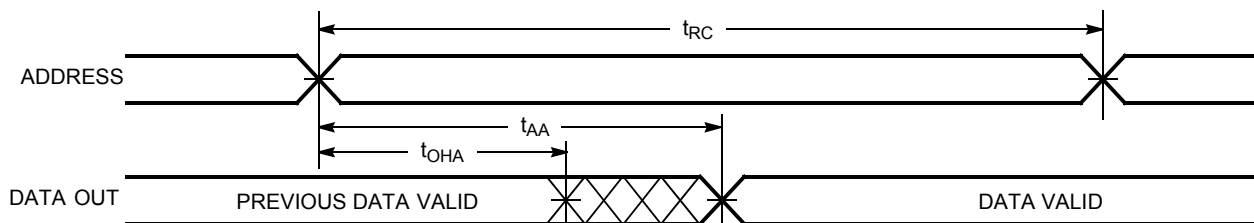
| Parameter <sup>[6]</sup>       | Description                                                                    | -10 |     | Unit |
|--------------------------------|--------------------------------------------------------------------------------|-----|-----|------|
|                                |                                                                                | Min | Max |      |
| Read Cycle                     |                                                                                |     |     |      |
| t <sub>power</sub>             | V <sub>CC</sub> (typical) to the first access <sup>[7]</sup>                   | 1   | –   | ms   |
| t <sub>RC</sub>                | Read cycle time                                                                | 10  | –   | ns   |
| t <sub>AA</sub>                | Address to data valid                                                          | –   | 10  | ns   |
| t <sub>OHA</sub>               | Data hold from address change                                                  | 3   | –   | ns   |
| t <sub>ACE</sub>               | $\overline{\text{CE}}_1$ LOW/CE <sub>2</sub> HIGH to data valid                | –   | 10  | ns   |
| t <sub>DOE</sub>               | $\overline{\text{OE}}$ LOW to data valid                                       | –   | 5   | ns   |
| t <sub>LZOE</sub>              | $\overline{\text{OE}}$ LOW to low Z <sup>[8]</sup>                             | 1   | –   | ns   |
| t <sub>HZOE</sub>              | $\overline{\text{OE}}$ HIGH to high Z <sup>[8]</sup>                           | –   | 5   | ns   |
| t <sub>LZCE</sub>              | $\overline{\text{CE}}_1$ LOW/CE <sub>2</sub> HIGH to low Z <sup>[8]</sup>      | 3   | –   | ns   |
| t <sub>HZCE</sub>              | $\overline{\text{CE}}_1$ HIGH/CE <sub>2</sub> LOW to high Z <sup>[8]</sup>     | –   | 5   | ns   |
| t <sub>PU</sub>                | $\overline{\text{CE}}_1$ LOW/CE <sub>2</sub> HIGH to power up <sup>[9]</sup>   | 0   | –   | ns   |
| t <sub>PD</sub>                | $\overline{\text{CE}}_1$ HIGH/CE <sub>2</sub> LOW to power down <sup>[9]</sup> | –   | 10  | ns   |
| Write Cycle <sup>[9, 10]</sup> |                                                                                |     |     |      |
| t <sub>WC</sub>                | Write cycle time                                                               | 10  | –   | ns   |
| t <sub>SCE</sub>               | $\overline{\text{CE}}_1$ LOW/CE <sub>2</sub> HIGH to write end                 | 7   | –   | ns   |
| t <sub>AW</sub>                | Address setup to write end                                                     | 7   | –   | ns   |
| t <sub>HA</sub>                | Address hold from write end                                                    | 0   | –   | ns   |
| t <sub>SA</sub>                | Address setup to write start                                                   | 0   | –   | ns   |
| t <sub>PWE</sub>               | $\overline{\text{WE}}$ pulse width                                             | 7   | –   | ns   |
| t <sub>SD</sub>                | Data setup to write end                                                        | 5.5 | –   | ns   |
| t <sub>HD</sub>                | Data hold from write end                                                       | 0   | –   | ns   |
| t <sub>LZWE</sub>              | $\overline{\text{WE}}$ HIGH to low Z <sup>[8]</sup>                            | 3   | –   | ns   |
| t <sub>HZWE</sub>              | $\overline{\text{WE}}$ LOW to high Z <sup>[8]</sup>                            | –   | 5   | ns   |

### Notes

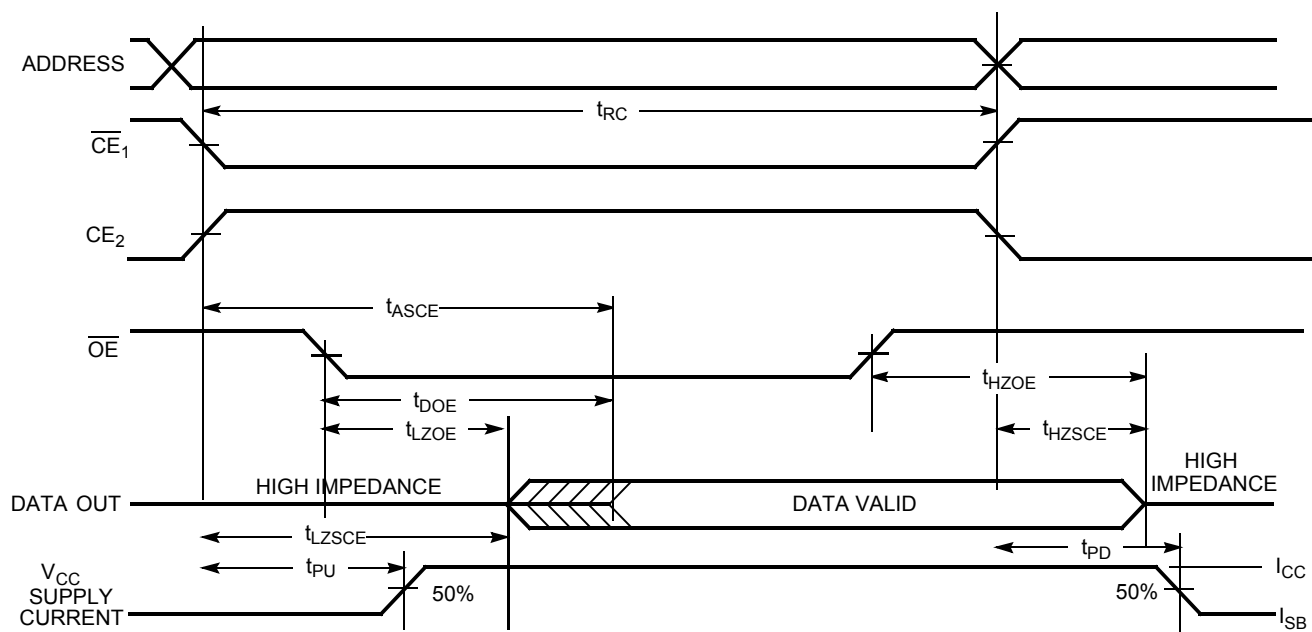
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified  $I_{\text{OL}}/I_{\text{OH}}$  and transmission line loads. Test conditions for the Read cycle use output loading shown in part a) of the AC test loads, unless specified otherwise.
- This part has a voltage regulator which steps down the voltage from 3V to 2V internally.  $t_{\text{power}}$  time has to be provided initially before a Read/Write operation is started.
- $t_{\text{HZOE}}$ ,  $t_{\text{HZCE}}$ ,  $t_{\text{HZWE}}$  and  $t_{\text{LZOE}}$ ,  $t_{\text{LZCE}}$ , and  $t_{\text{LZWE}}$  are specified with a load capacitance of 5 pF as in (b) of AC Test Loads. Transition is measured  $\pm 200$  mV from steady-state voltage.
- These parameters are guaranteed by design and are not tested.
- The internal Write time of the memory is defined by the overlap of  $\overline{\text{CE}}_1$  LOW/ $\text{CE}_2$  HIGH, and  $\overline{\text{WE}}$  LOW.  $\overline{\text{CE}}_1$  and  $\overline{\text{WE}}$  must be LOW along with  $\text{CE}_2$  HIGH to initiate a Write, and the transition of any of these signals can terminate the Write. The input data setup and hold timing should be referenced to the leading edge of the signal that terminates the Write.

## Switching Waveforms

**Figure 4. Read Cycle No. 1** [11, 12]



**Figure 5. Read Cycle No. 2 ( $\overline{OE}$  Controlled)** [12, 13]

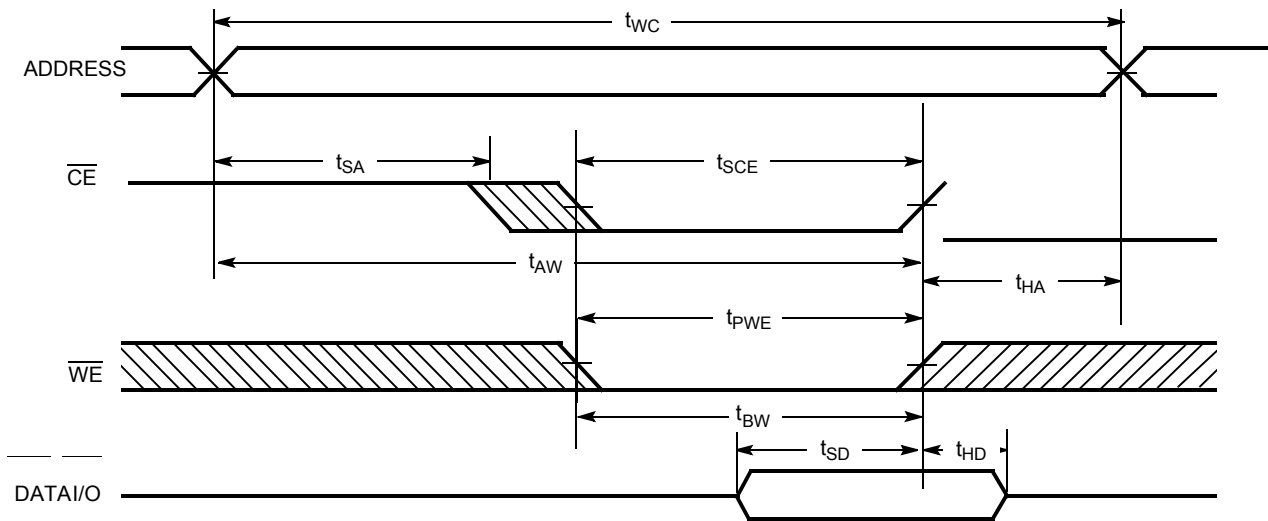


### Notes

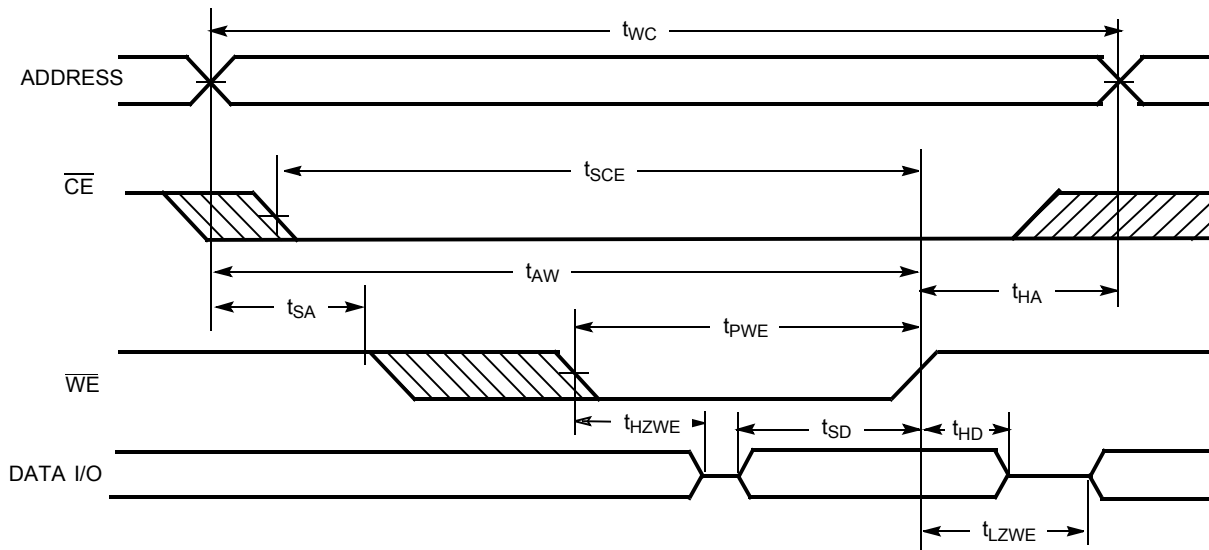
11. Device is continuously selected.  $\overline{CE}_1 = V_{IL}$ ,  $CE_2 = V_{IH}$ .
12.  $\overline{WE}$  is HIGH for Read cycle.
13. Address valid prior to or coincident with  $\overline{CE}_1$  transition LOW and  $CE_2$  transition HIGH.

## Switching Waveforms (continued)

**Figure 6. Write Cycle No. 1 ( $\overline{CE}_1$  Controlled)** [14, 15, 16]



**Figure 7. Write Cycle No. 2 ( $\overline{WE}$  Controlled,  $\overline{OE}$  LOW)** [14, 15, 16]



### Notes

14. Data I/O is high-impedance if  $\overline{OE} = V_{IH}$ .
15. If  $\overline{CE}_1$  goes HIGH/ $\overline{CE}_2$  LOW simultaneously with  $\overline{WE}$  going HIGH, the output remains in a high-impedance state.
16. CE above is defined as a combination of  $\overline{CE}_1$  and  $\overline{CE}_2$ . It is active low.

**Truth Table**

| $\overline{CE}_1$ | $CE_2$ | $\overline{OE}$ | $\overline{WE}$ | I/O <sub>0</sub> –I/O <sub>7</sub> | Mode                       | Power                |
|-------------------|--------|-----------------|-----------------|------------------------------------|----------------------------|----------------------|
| H                 | X      | X               | X               | High Z                             | Power down                 | Standby ( $I_{SB}$ ) |
| X                 | L      | X               | X               | High Z                             | Power down                 | Standby ( $I_{SB}$ ) |
| L                 | H      | L               | H               | Data Out                           | Read all bits              | Active ( $I_{CC}$ )  |
| L                 | H      | X               | L               | Data In                            | Write all bits             | Active ( $I_{CC}$ )  |
| L                 | H      | H               | H               | High Z                             | Selected, outputs disabled | Active ( $I_{CC}$ )  |

## Ordering Information

| Speed (ns) | Ordering Code       | Package Diagram | Package Type             | Operating Range |
|------------|---------------------|-----------------|--------------------------|-----------------|
| 10         | CY7C1069AV33-10ZX C | 51-85160        | 54-pin TSOP II (Pb-free) | Commercial      |

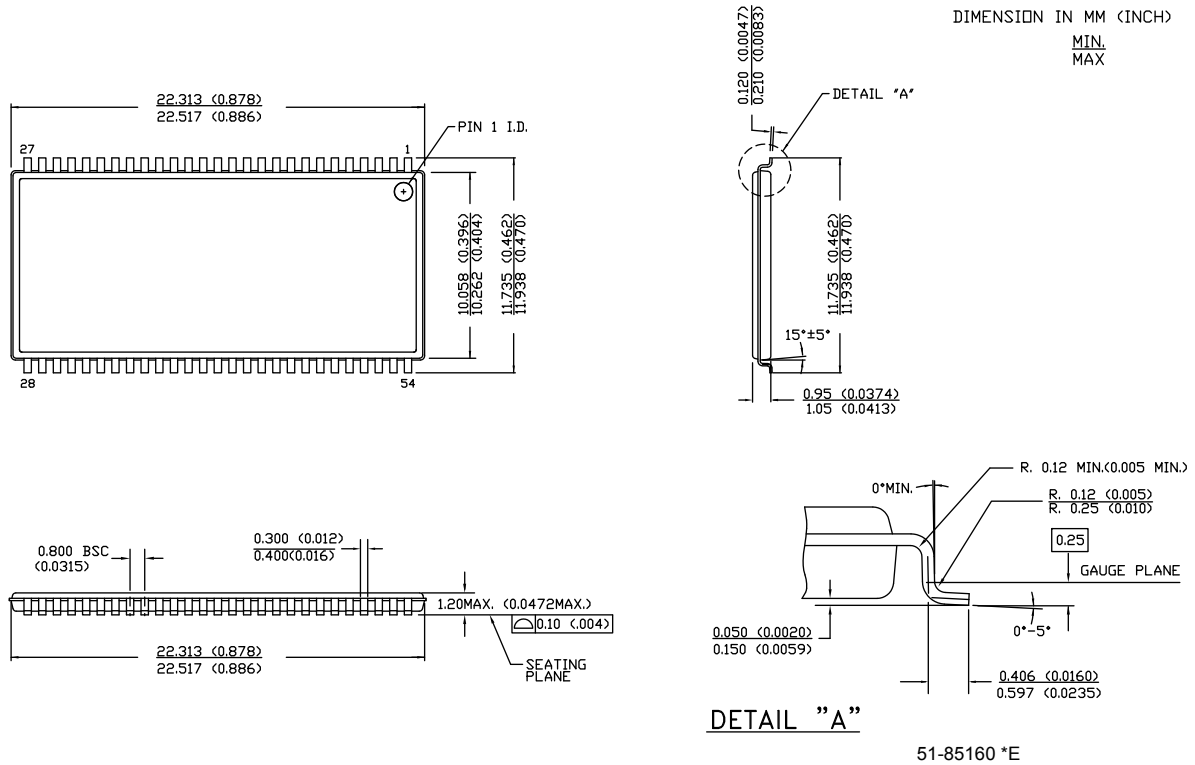
## Ordering Code Definitions

| CY | 7 | C | 1 | 06 | 9 | A | V33 | - | 10 | Z | X | C |                                                |
|----|---|---|---|----|---|---|-----|---|----|---|---|---|------------------------------------------------|
|    |   |   |   |    |   |   |     |   |    |   |   |   | Temperature Range: C = Commercial              |
|    |   |   |   |    |   |   |     |   |    |   |   |   | Pb-free                                        |
|    |   |   |   |    |   |   |     |   |    |   |   |   | Package Type: Z = 54-pin TSOP II               |
|    |   |   |   |    |   |   |     |   |    |   |   |   | Speed Grade: 10 ns                             |
|    |   |   |   |    |   |   |     |   |    |   |   |   | Voltage: V33 = 3.3 V                           |
|    |   |   |   |    |   |   |     |   |    |   |   |   | Process Technology: A = 150 nm                 |
|    |   |   |   |    |   |   |     |   |    |   |   |   | Data width: 9 = × 8-bits                       |
|    |   |   |   |    |   |   |     |   |    |   |   |   | Density: 06 = 16-Mbit density                  |
|    |   |   |   |    |   |   |     |   |    |   |   |   | Family Code: 1 = Fast Asynchronous SRAM family |
|    |   |   |   |    |   |   |     |   |    |   |   |   | Technology Code: C = CMOS                      |
|    |   |   |   |    |   |   |     |   |    |   |   |   | Marketing Code: 7 = SRAM                       |
|    |   |   |   |    |   |   |     |   |    |   |   |   | Company ID: CY = Cypress                       |

## Package Diagram

**Figure 8. 54-pin TSOP II (22.4 × 11.84 × 1.0 mm) Package Outline, 51-85160**

### 54 Lead TSOP TYPE II – STANDARD



## Acronyms

| Acronym                | Description                             |
|------------------------|-----------------------------------------|
| $\overline{\text{CE}}$ | Chip Enable                             |
| CMOS                   | Complementary Metal Oxide Semiconductor |
| I/O                    | Input/Output                            |
| $\overline{\text{OE}}$ | Output Enable                           |
| SRAM                   | Static Random Access Memory             |
| TSOP                   | Thin Small Outline Package              |
| TTL                    | Transistor-Transistor Logic             |
| $\overline{\text{WE}}$ | Write Enable                            |

## Document Conventions

### Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C     | degree Celsius  |
| MHz    | megahertz       |
| μA     | microampere     |
| mA     | milliampere     |
| ms     | millisecond     |
| mV     | millivolt       |
| mW     | milliwatt       |
| ns     | nanosecond      |
| %      | percent         |
| pF     | picofarad       |
| V      | volt            |
| W      | watt            |

## Document History Page

| Document Title: CY7C1069AV33, 2 M × 8 Static RAM<br>Document Number: 38-05255 |         |                 |                 |                                                                                                                                                                                                                                                                                                                                       |
|-------------------------------------------------------------------------------|---------|-----------------|-----------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Rev.                                                                          | ECN No. | Submission Date | Orig. of Change | Description of Change                                                                                                                                                                                                                                                                                                                 |
| **                                                                            | 113724  | 03/27/02        | NSL             | New data sheet                                                                                                                                                                                                                                                                                                                        |
| *A                                                                            | 117060  | 07/31/02        | DFP             | Removed 15-ns bin                                                                                                                                                                                                                                                                                                                     |
| *B                                                                            | 117990  | 08/30/02        | DFP             | Added 8-ns bin<br>Changing I <sub>CC</sub> for 8, 10, 12 bins<br>t <sub>power</sub> changed from 1 μs to 1 ms<br>Load Cap Comment changed (for Tx line load)<br>t <sub>SD</sub> changed to 5.5 ns for the 10-ns bin<br>Changed some 8-ns bin #'s (t <sub>HZ</sub> , t <sub>DOE</sub> , t <sub>DBE</sub> )<br>Removed hz < lz comments |
| *C                                                                            | 120385  | 11/13/02        | DFP             | Final data sheet<br>Added note 4 to "AC Test Loads and Waveforms" and note 7 to t <sub>pu</sub> and t <sub>pd</sub><br>Updated Input/Output Caps (for 48-ball BGA only) to 8 pF/10 pF and for the 54-pin TSOP to 6/8 pF                                                                                                               |
| *D                                                                            | 124441  | 2/25/03         | MEG             | Changed I <sub>SB1</sub> from 100 mA to 70 mA<br>Shaded the 48-ball FBGA product offering information                                                                                                                                                                                                                                 |
| *E                                                                            | 403984  | See ECN         | NXR             | Changed the Logic Block Diagram On page # 1<br>Added notes under Pin Configuration<br>Changed the Package diagram of 51-85162 from Rev *A to Rev *D<br>Changed 48-ball FBGA to 60-ball FBGA in Pin Configuration<br>Updated the Ordering Information                                                                                  |
| *F                                                                            | 492137  | See ECN         | NXR             | Removed 8 ns speed bin from product offering<br>Changed the description of I <sub>IX</sub> from Input Load Current to Input Leakage Current in DC Electrical Characteristics table<br>Updated the Ordering Information                                                                                                                |
| *G                                                                            | 2784946 | 10/12/2009      | VKN / PYRS      | Updated template<br>Corrected typo in footnote 9<br>Updated Ordering Information table                                                                                                                                                                                                                                                |
| *H                                                                            | 2897049 | 03/25/10        | AJU             | Removed inactive parts from the ordering information table.<br>Updated package diagrams.                                                                                                                                                                                                                                              |
| *I                                                                            | 2950666 | 06/11/2010      | VKN             | Removed 12 ns speed bin,<br>Removed 60-ball FBGA package<br>Updated <a href="#">Ordering Information</a><br>Added <a href="#">Acronyms</a> and <a href="#">Ordering Code Definitions</a> .                                                                                                                                            |
| *J                                                                            | 3096933 | 11/29/2010      | PRAS            | Added <a href="#">Units of Measure</a> .<br>Minor edits and updated in new template.                                                                                                                                                                                                                                                  |
| *K                                                                            | 4214675 | 12/09/2013      | VINI            | Updated <a href="#">Package Diagram</a> :<br>spec 51-85160 – Changed revision from *A to *D.<br>Updated in new template.<br>Completing Sunset Review.                                                                                                                                                                                 |
| *L                                                                            | 4574377 | 11/19/2014      | VINI            | Added related documentation hyperlink in page 1.<br>Updated <a href="#">Figure 8</a> in <a href="#">Package Diagram</a> (spec 51-85160 *D to *E).                                                                                                                                                                                     |

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