# 74HC4049

# Hex inverting HIGH-to-LOW level shifter

Rev. 7 — 5 February 2016

**Product data sheet** 

### 1. General description

The 74HC4049 is a hex inverter with over-voltage tolerant inputs. Inputs are overvoltage tolerant to 15 V. This enables the device to be used in HIGH-to-LOW level shifting applications.

### 2. Features and benefits

- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2 000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

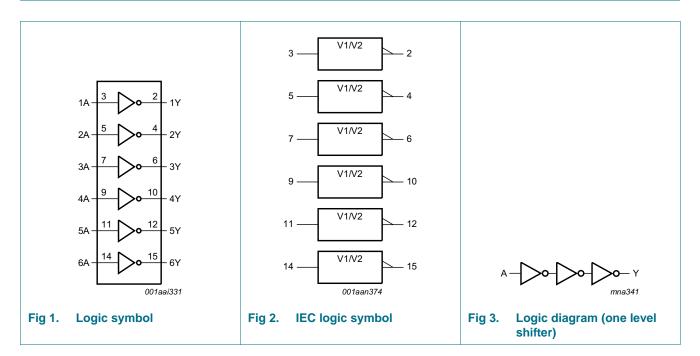
### 3. Ordering information

Table 1. Ordering information

Type number	Package								
	Temperature range	Name	Description	Version					
74HC4049D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1					
74HC4049DB	−40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1					
74HC4049PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1					

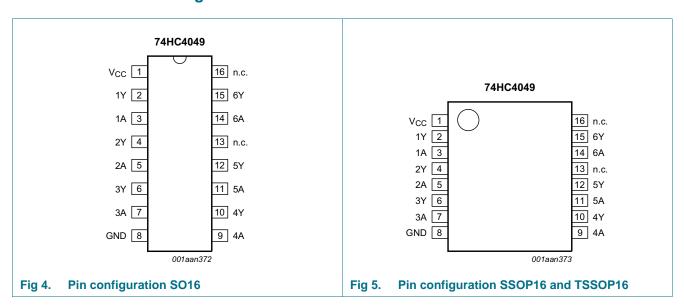


### 4. Functional diagram



### 5. Pinning information

### 5.1 Pinning



### Hex inverting HIGH-to-LOW level shifter

### 5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V <sub>CC</sub>	1	supply voltage
1Y to 6Y	2, 4, 6, 10, 12, 15	output
1A to 6A	3, 5, 7, 9, 11, 14	input
GND	8	ground (0 V)
n.c.	13, 16	not connected

### 6. Functional description

#### Table 3. Function table [1]

Input	Output
nA	nY
L	Н
Н	L

<sup>[1]</sup> H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

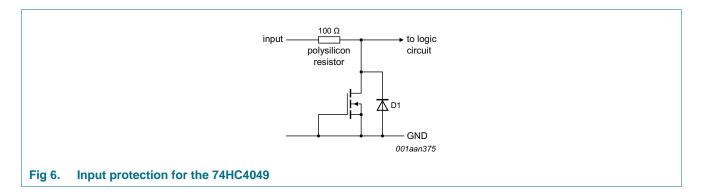
Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V <sub>CC</sub>	supply voltage			-0.5	+7	V
V <sub>IK</sub>	input clamping voltage			-0.5	+16	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V		-20	-	mA
I <sub>OK</sub>	output clamping current	$V_{O} < -0.5 \text{ V or } V_{O} > V_{CC} + 0.5 \text{ V}$		-	±20	mA
Io	output current	$V_{O} = -0.5 \text{ V to } (V_{CC} + 0.5 \text{ V})$		-	±25	mA
I <sub>CC</sub>	supply current			-	+50	mA
I <sub>GND</sub>	ground current			-	-50	mA
T <sub>stg</sub>	storage temperature			-65	+150	°C
P <sub>tot</sub>	total power dissipation	SO16, SSOP16 and TSSOP16 packages	[1]	-	500	mW

<sup>[1]</sup> For SO16 package:  $P_{tot}$  derates linearly with 8 mW/K above 70 °C. For SSOP16 and TSSOP16 packages:  $P_{tot}$  derates linearly with 5.5 mW/K above 60 °C.

### Hex inverting HIGH-to-LOW level shifter



# 8. Recommended operating conditions

 Table 5.
 Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>CC</sub>	supply voltage		2.0	5.0	6.0	V
VI	input voltage		0	-	15	V
Vo	output voltage		0	-	V <sub>CC</sub>	V
T <sub>amb</sub>	ambient temperature		-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	$V_{CC} = 2.0 \text{ V}; V_I = 2.0 \text{ V}$	-	-	625	ns/V
		$V_{CC} = 4.5 \text{ V}; V_I = 4.5 \text{ V}$	-	1.67	139	ns/V
		$V_{CC} = 6.0 \text{ V}; V_I = 6.0 \text{ V}$	-	-	83	ns/V
		$V_{CC} = 6.0 \text{ V}; V_I = 10.0 \text{ V}$	-	-	81	ns/V
		$V_{CC} = 6.0 \text{ V}; V_I = 15.0 \text{ V}$	-	-	83	ns/V

### 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol Parameter		Conditions	T <sub>amb</sub> = 25 °C		T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit	
			Min	Тур	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level	V <sub>CC</sub> = 2.0 V	1.5	1.3	-	1.5	-	1.5	-	V
	input voltage	V <sub>CC</sub> = 4.5 V	3.15	2.4	-	3.15	-	3.15	-	V
		V <sub>CC</sub> = 6.0 V	4.2	3.1	-	4.2	-	4.2	-	V
$V_{IL}$	LOW-level input voltage	V <sub>CC</sub> = 2.0 V	-	0.7	0.5	-	0.5	-	0.5	V
		V <sub>CC</sub> = 4.5 V	-	1.8	1.35	-	1.35	-	1.35	V
		V <sub>CC</sub> = 6.0 V	-	2.3	1.8	-	1.8	-	1.8	V
$V_{OH}$	HIGH-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_{O} = -20 \mu A; V_{CC} = 2.0 V$	1.9	2.0	-	1.9	-	1.9	-	V
		$I_{O} = -20 \mu A; V_{CC} = 4.5 V$	4.4	4.5	-	4.4	-	4.4	-	V
		$I_O = -20 \mu A; V_{CC} = 6.0 V$	5.9	6.0	-	5.9	-	5.9	-	V
		$I_{O} = -4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	3.98	-	-	3.84	-	3.7	-	V
		$I_{O} = -5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	5.48	-	-	5.34	-	5.2	-	V

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### Hex inverting HIGH-to-LOW level shifter

 Table 6.
 Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Tai	T <sub>amb</sub> = 25 °C		T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
			Min	Тур	Max	Min	Max	Min	Max	
$V_{OL}$	LOW-level	$V_I = V_{IH}$ or $V_{IL}$								
	output voltage	$I_O = 20 \mu A; V_{CC} = 2.0 V$	-	-	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5 V$	-	-	0.1	-	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0 V$	-	-	0.1	-	0.1	-	0.1	V
		$I_O = 4.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	-	0.26	-	0.33	-	0.4	V
		$I_{O} = 5.2 \text{ mA}; V_{CC} = 6.0 \text{ V}$	-	-	0.26	-	0.33	-	0.4	V
lı	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0 \text{ V}$	-	-	±0.1	-	±1.0	-	±1.0	μА
		$V_1 = 15 \text{ V}; V_{CC} = 2.0 \text{ V} \text{ to}$ 6.0 V	-	-	±0.5	-	±5.0	-	±5.0	μА
I <sub>CC</sub>	supply current	$V_I = 15 \text{ V or GND}; I_O = 0 \text{ A}; V_{CC} = 6.0 \text{ V}$	-	-	2.0	-	20	-	40	μА
Cı	input capacitance		-	3.5	-	-	-	-	-	pF

# 10. Dynamic characteristics

### Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 pF$  unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions		T <sub>amb</sub> = 25 °C		T <sub>amb</sub> = -40 °C to +85 °C		T <sub>amb</sub> = -40 °C to +125 °C		Unit
		Min	Тур	Max	Min	Max	Min	Max		
t <sub>pd</sub> propagation	nA to nY; see Figure 7									
	delay	V <sub>CC</sub> = 2.0 V	-	28	85	-	105	-	130	ns
	V <sub>CC</sub> = 4.5 V	-	10	17	-	21	-	26	ns	
		$V_{CC} = 5 \text{ V}; C_L = 15 \text{ pF}$	-	8	-	-	-	-	-	ns
		V <sub>CC</sub> = 6.0 V	-	8	14	-	18	-	22	ns
t <sub>t</sub>	transition	Yn; see Figure 7 [2]								
	time	V <sub>CC</sub> = 2.0 V	-	19	75	-	95	-	110	ns
		V <sub>CC</sub> = 4.5 V	-	7	15	-	19	-	22	ns
		V <sub>CC</sub> = 6.0 V	-	6	13	-	16	-	19	ns

#### Hex inverting HIGH-to-LOW level shifter

Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V);  $C_L = 50 \text{ pF}$  unless otherwise specified; for test circuit see Figure 8.

Symbol	Parameter	Conditions	T <sub>an</sub>	<sub>nb</sub> = 25	°C		-40 °C 85 °C		: –40 °C I25 °C	Unit
			Min	Тур	Max	Min	Max	Min	Max	
C <sub>PD</sub>	power dissipation capacitance	$C_L$ = 50 pF; f = 1 MHz; $V_I$ = GND to $V_{CC}$	-	14	-	-	-	-	-	pF

- [1]  $t_{pd}$  is the same as  $t_{PLH}$  and  $t_{PHL}$ .
- [2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .
- [3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ ).

 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$  where:

 $f_i$  = input frequency in MHz;

f<sub>o</sub> = output frequency in MHz;

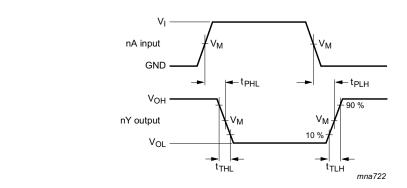
C<sub>L</sub> = output load capacitance in pF;

 $V_{CC}$  = supply voltage in V;

N = number of inputs switching;

 $\sum (C_L \times V_{CC}^2 \times f_0) = \text{sum of outputs.}$ 

### 11. Waveforms



Measurement points are given in Table 8.

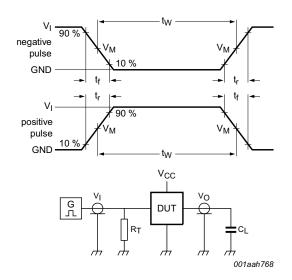
 $V_{\text{OL}}$  and  $V_{\text{OH}}$  are typical voltage output levels that occur with the output load.

Fig 7. The input (nA) to output (nY) propagation delays

Table 8. Measurement points

Туре	Input	Output	
	V <sub>M</sub>	V <sub>M</sub>	
74HC4049	0.5V <sub>CC</sub>	0.5V <sub>CC</sub>	

### Hex inverting HIGH-to-LOW level shifter



Test data is given in Table 9.

Definitions test circuit:

 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

 $C_L$  = Load capacitance including jig and probe capacitance.

 $R_L$  = Load resistance.

S1 = Test selection switch.

Fig 8. Test circuit for measuring switching times

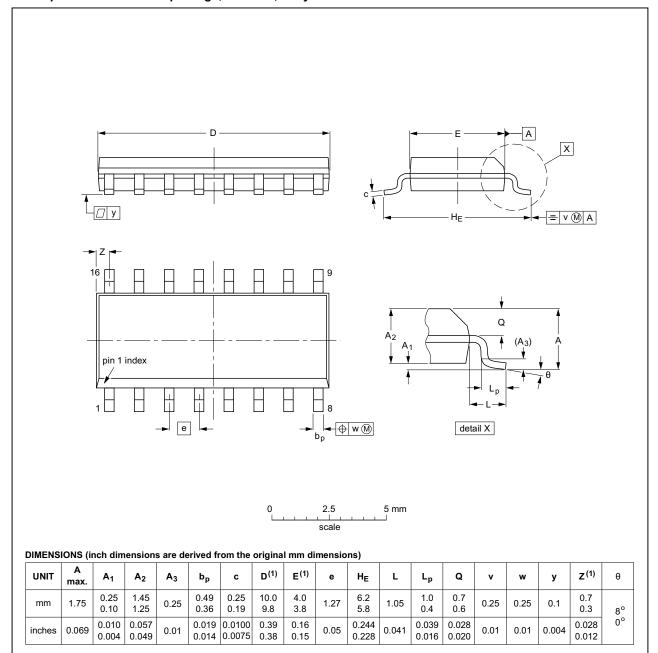
Table 9. Test data

Туре	Input L		Load	Test
	V <sub>I</sub>	t <sub>r</sub> , t <sub>f</sub>	C <sub>L</sub>	
74HC4049	$V_{CC}$	6.0 ns	15 pF, 50 pF	t <sub>PLH</sub> , t <sub>PHL</sub>

### 12. Package outline

#### SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



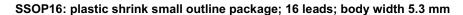
#### Note

<sup>1.</sup> Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

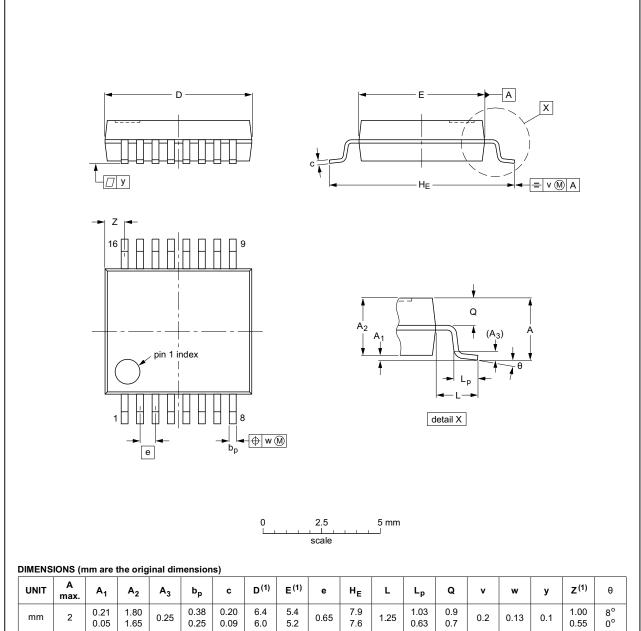
OUTLINE		REFER	ENCES	EUROPEAN	ISSUE DATE
VERSION	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012			<del>99-12-27</del> 03-02-19

Fig 9. Package outline SOT109-1 (SO16)

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SOT338-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	b <sub>p</sub>	С	D <sup>(1)</sup>	E <sup>(1)</sup>	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT338-1		MO-150				<del>99-12-27</del> 03-02-19	

Fig 10. Package outline SOT338-1 (SSOP16)

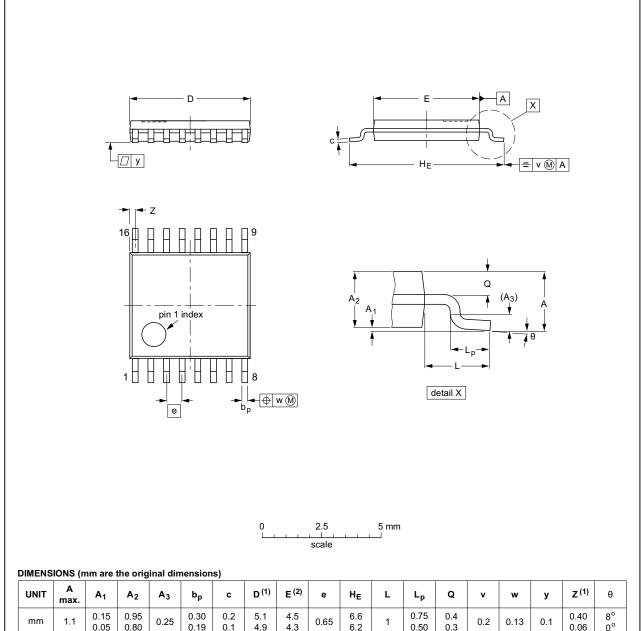
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TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1



UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	<b>A</b> <sub>3</sub>	bp	С	D <sup>(1)</sup>	E (2)	е	HE	L	Lp	Q	v	w	у	Z <sup>(1)</sup>	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

#### Notes

- 1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
- 2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE		REFER	EUROPEAN	ISSUE DATE			
VERSION	IEC	JEDEC	JEITA		PROJECTION	ISSUE DATE	
SOT403-1		MO-153				<del>99-12-27</del> 03-02-18	

Fig 11. Package outline SOT403-1 (TSSOP16)

### Hex inverting HIGH-to-LOW level shifter

### 13. Abbreviations

#### Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MM	Machine Model

# 14. Revision history

### Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC4049 v.7	20160205	Product data sheet	-	74HC4049 v.6
Modifications:	Type num	ber 74HC4049N (SOT38-4	1) removed.	
74HC4049 v.6	20130108	Product data sheet	-	74HC4049 v.5
Modifications:	New gene	ral description.	'	
74HC4049 v.5	20120803	Product data sheet	-	74HC4049 v.4
Modifications:	Measuren	nent points added to figure	7 (errata).	
74HC4049 v.4	20111212	Product data sheet	-	74HC4049 v.3
74HC4049 v.3	20101230	Product data sheet	-	74HC4049_CNV v.2
74HC4049_CNV v.2	19970827	Product specification	-	-

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#### Hex inverting HIGH-to-LOW level shifter

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74HC245PW.112 74HC367D.652 74HC541D.652 74HC541D.653 74HC7541D.112 74HCT367D.652 74HCT541D.653 74LVC244AD.112

74LVC4245AD.112 74LVC541AD.112 74HC240D.652 74HC4049D.653 74HC540D.652 74HCT125D.652 74HCT244D.652

74HCT245PW.112 74HCT367N.652 74HC125D.652 74HC244D.652 74HC245DB.118 HEF4050BT.652 74HC05PW.112 74HC125PW.112

74HC2G16GVH 74LVC06AD.112 74LVC06APW.112 74LVC125APW.112 74LVC126APW.112 74VHC126FT(BE) 7SB3257MUTCG

7SB384MUTCG 7SB384DTT1G 74AHCT245PW.118 74HC126DB.118 74HC240PW.112 74HC241DB.118