

100V N-CHANNEL ENHANCEMENT MODE POWER MOSFET

Features

- 100V, 14.6A
- $R_{DS(ON)} = 100m\Omega$ (max.) @ $V_{GS} = 10V, I_D = 5A$
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- Advanced high cell density Trench technology
- RoHS Compliant & Halogen-Free

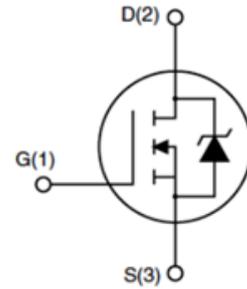
Application

- Synchronous buck converter applications.

Package



TO-252



Absolute Maximum Ratings $T_C=25^\circ C$ unless otherwise specified

Symbol	Parameter	Max.	Units	
V_{DS}	Drain-Source Voltage	100	V	
V_{GS}	Gate-Source Voltage	± 20	V	
I_D	Continuous Drain Current, $V_{GS} @ 10V_{no}$ ^{note1,6}	$T_C = 25^\circ C$	14.6	A
		$T_C = 100^\circ C$	10	A
I_{DM}	Pulsed Drain Current ^{note2}	25	A	
P_D	Power Dissipation ^{note4}	$T_C = 25^\circ C$	30	W
E_{AS}	Single Pulsed Avalanche Energy ^{note3}	0.8	mJ	
$R_{\theta JA}$	Thermal Resistance, Junction to Case ^{note1}	3	$^\circ C/W$	
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to +150	$^\circ C$	

Electrical Characteristics $T_C=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
Off Characteristic						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	100	-	-	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS} = 80V, V_{GS} = 0V$	-	-	10	μA
		$V_{DS} = 80V, T_C = 55^{\circ}\text{C}$	-	-	100	μA
I_{GSS}	Gate to Body Leakage Current	$V_{DS} = 0V, V_{GS} = \pm 20V$	-	-	± 100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	-	2.9	V
$R_{DS(on)}$	Static Drain-Source On-Resistance ^{note2}	$V_{GS} = 10V, I_D = 5A$	-	-	100	m Ω
		$V_{GS} = 4.5V, I_D = 3A$	-	-	110	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5V, I_D = 5A$	-	14	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V,$ $f = 1.0\text{MHz}$	-	450	-	pF
C_{oss}	Output Capacitance		-	55	-	pF
C_{riss}	Reverse Transfer Capacitance		-	16	-	pF
Q_g	Total Gate Charge	$V_{DS} = 50V, I_D = 5A,$ $V_{GS} = 10V$	-	11.9	-	nC
Q_{gs}	Gate-Source Charge		-	2.8	-	nC
Q_{gd}	Gate-Drain("Miller") Charge		-	1.7	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50V, I_D = 5A,$ $R_G = 3.3\Omega, V_{GS} = 10V$	-	3.8	-	ns
t_r	Turn-On Rise Time		-	25.8	-	ns
$t_{d(off)}$	Turn-Off Delay Time		-	16	-	ns
t_f	Turn-Off Fall Time		-	8.8	-	ns
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain to Source Diode Forward Current ^{note1,5}	-	-	14.6	-	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current ^{note2,5}	-	-	25	-	A
V_{SD} ^{note2}	Drain to Source Diode Forward Voltage	$V_{GS} = 0V, I_S = 1A$	-	-	1.2	V

Note :

- The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- The EAS data shows Max. rating . The test condition is $V_{DD}=25V, V_{GS}=10V, L=0.1mH, I_{AS}=50A$
- The power dissipation is limited by 150°C junction temperature
- The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.
- Package limitation current is 85A.

Typical Performance Characteristics

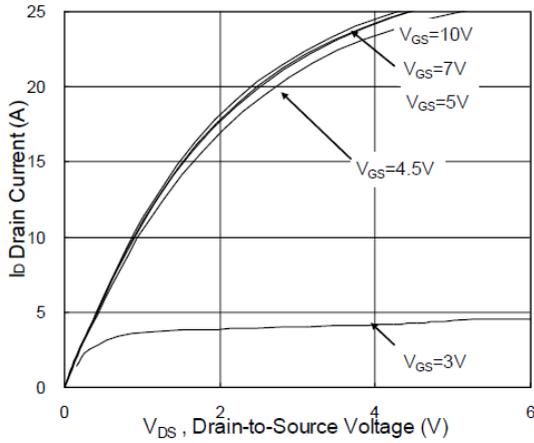


Figure 1. Output Characteristics

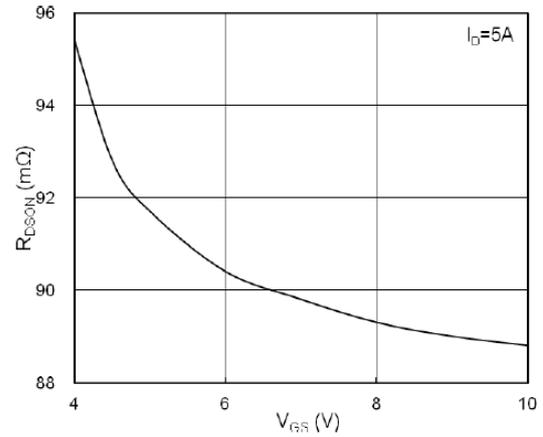


Figure 2. On Resistance vs. Gate-Source Voltage

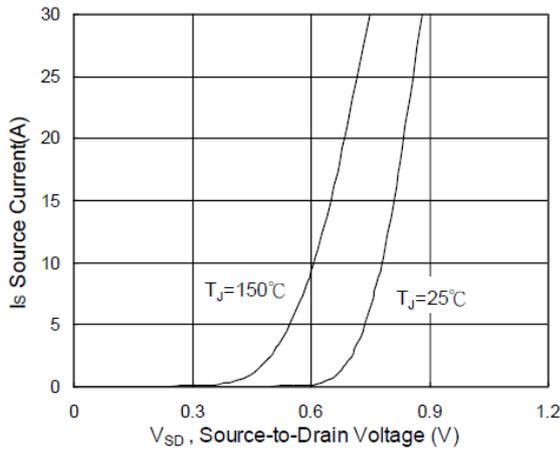


Figure 3. Body Diode Forward Voltage vs. Source Current and Temperature

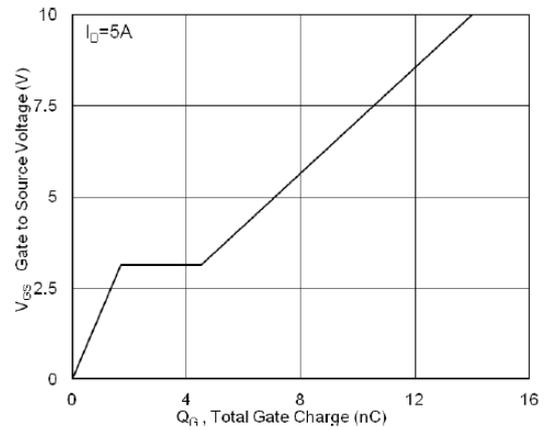


Figure 4. Gate Charge Characteristics

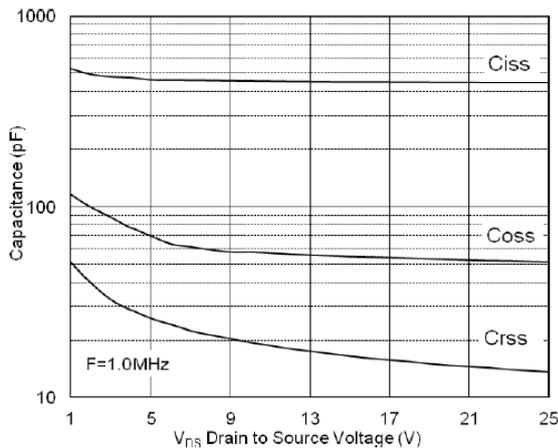


Figure 5. Capacitance Characteristics

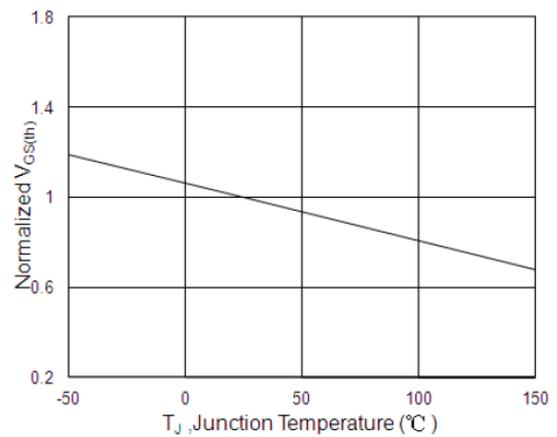


Figure 6. Normalized Threshold Voltage vs. Junction Temperature

N-Channel Enhancement Mode Power MOSFET

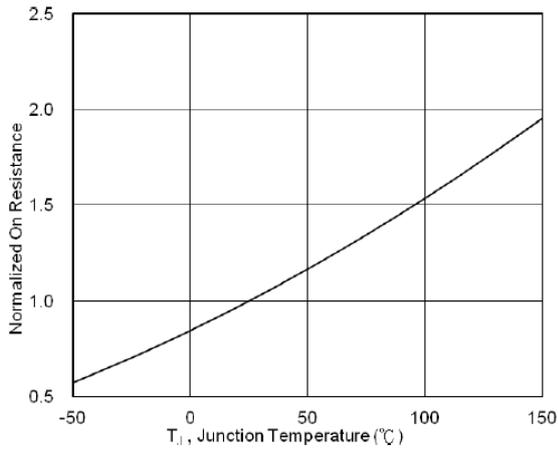


Figure 7. N Normalized On Resistance vs. Junction Temperature

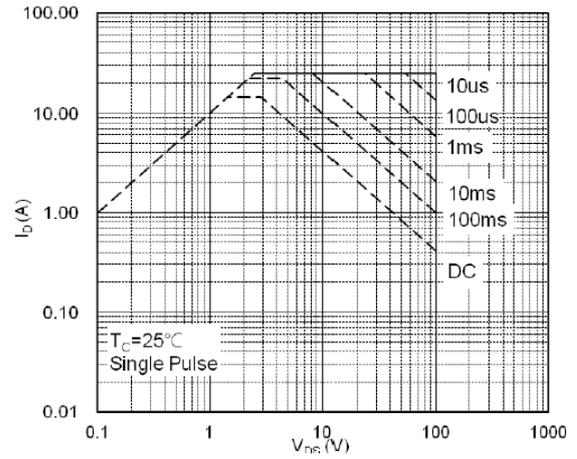


Figure 8. Maximum Safe Operating Area

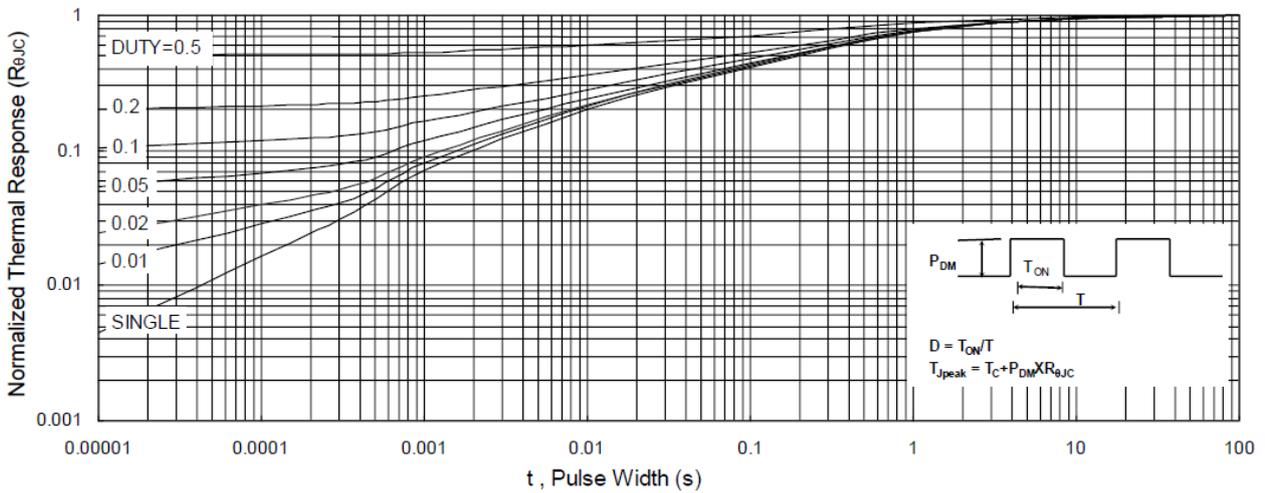


Figure 9. Effective Transient Thermal Impedance

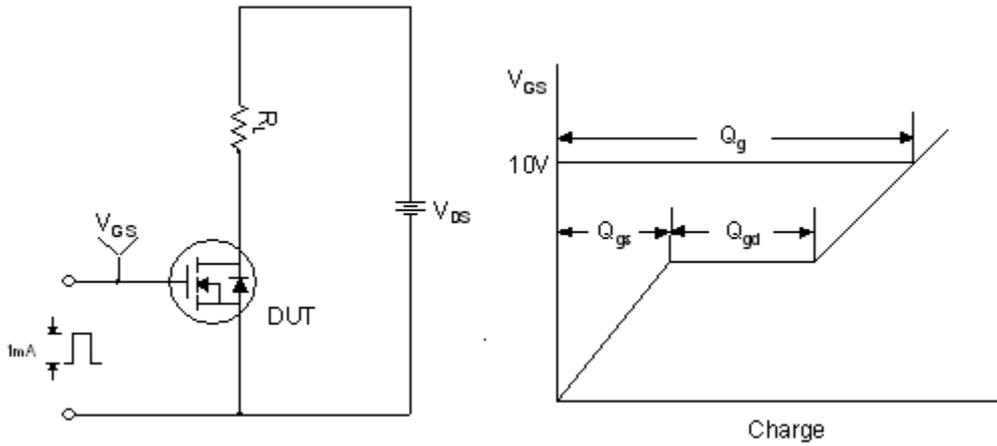


Figure 10. Gate Charge Test Circuit & Waveform

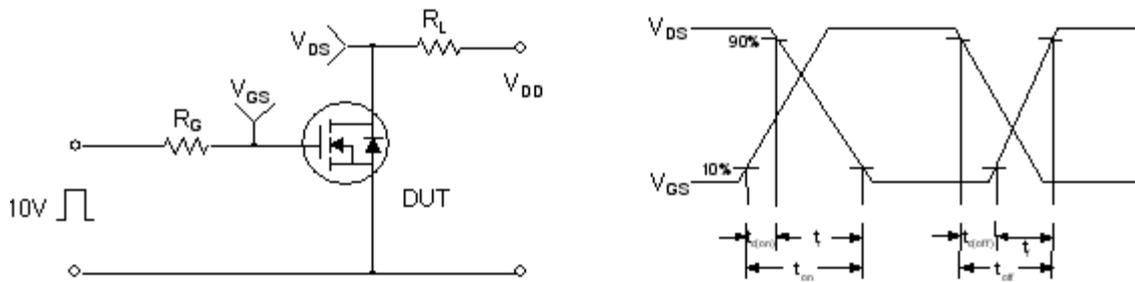


Figure 11. Resistive Switching Test Circuit & Waveforms

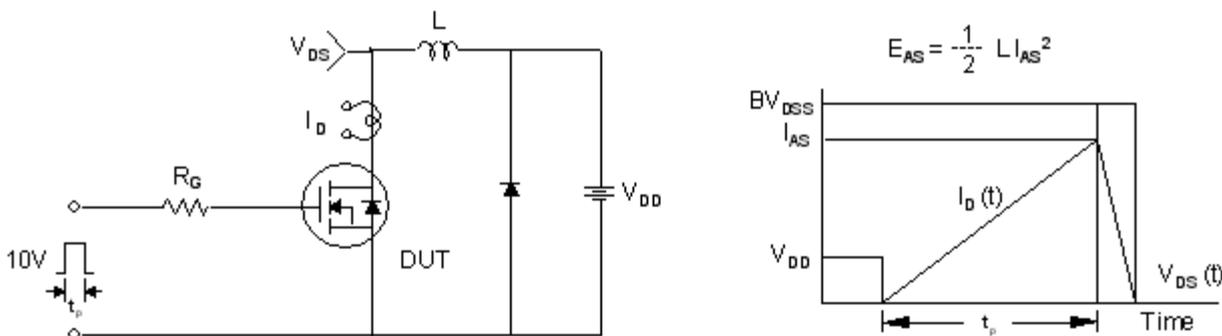


Figure 12. Unclamped Inductive Switching Test Circuit & Waveforms

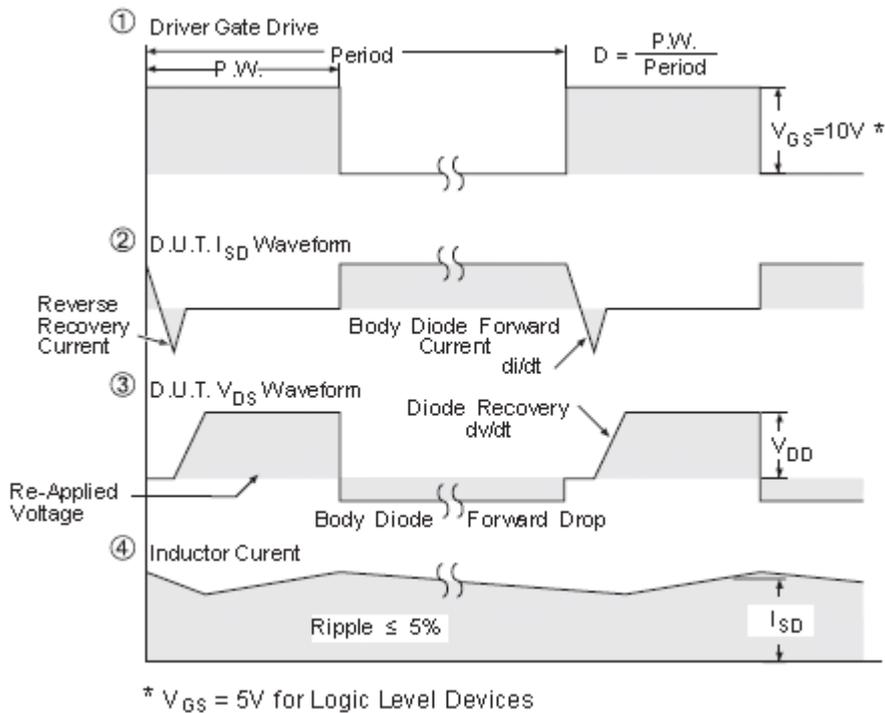
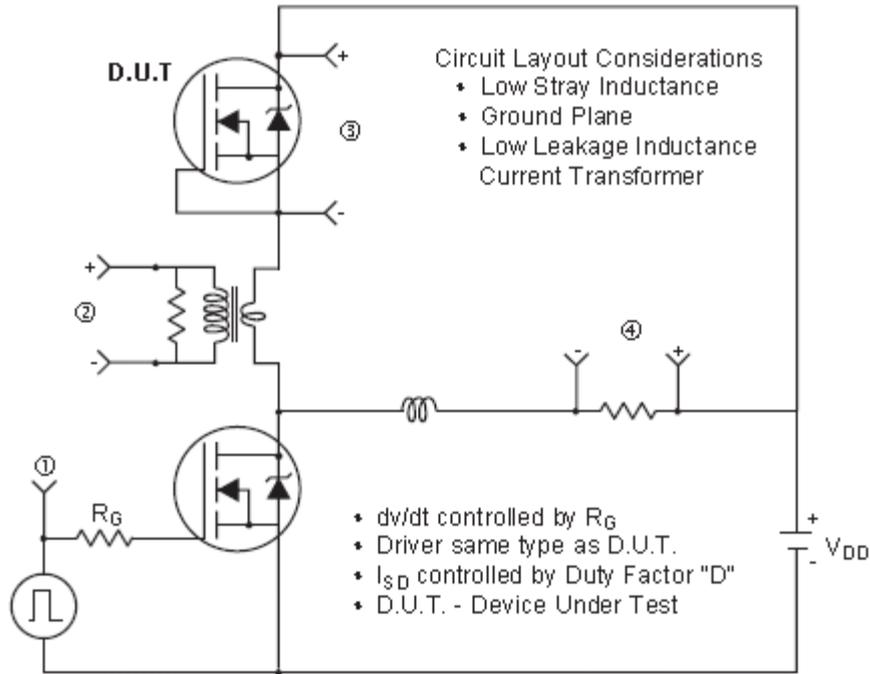


Figure 13. Peak Diode Recovery dv/dt Test Circuit & Waveforms (For N-channel)

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