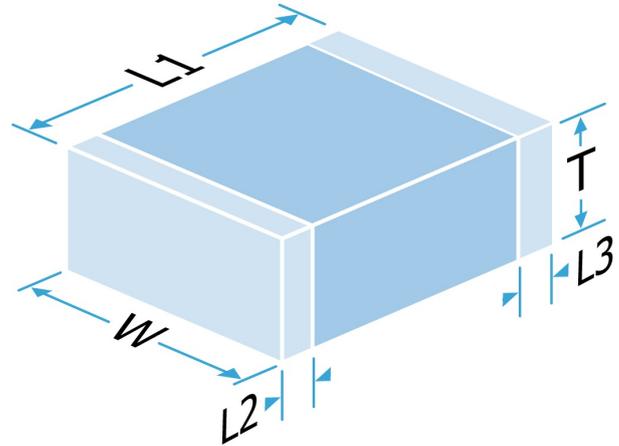


Multilayer Ceramic Chip Capacitor

Part Number: 0603J1000391JAT

Description: 0603 100V 390pF ±5% C0G/NP0 (1B) to AEC-Q200

A range of C0G MLC capacitors fully tested and approved to automotive specification AEC-Q200. Available in 0603 to 3640 chip sizes with capacitance values up to 5.6µF as standard. A variety of termination options are available, including FlexiCap™, the world's first commercially available flexible termination.



Mechanical Specification

Size Code	0603
Length (L1) in mm (")	1.6 ± 0.15 (0.063 ± 0.006)
Width (W) in mm (")	0.8 ± 0.15 (0.032 ± 0.006)
Thickness (T) in mm (")	0.8 Max (0.032 Max)
Minimum Termination Band (L2,L3) in mm (")	0.20 (0.004)
Maximum Termination Band (L2,L3) in mm (")	0.40 (0.016)
Termination Material	Nickel Barrier, Sn Plated Solder (RoHS compliant)
Solderability	IEC-60068-2-58
Packaging	7" Reel Horizontal Orientation, 4000 per reel

General Electrical Specification

Rated Voltage	100Vdc
Nominal Capacitance Value	390pF
Capacitance Tolerance	±5%
Tangent of Loss Angle (Tan δ)	≤0.0015
Capacitance and Tan δ Test Conditions	1.0Vrms @ 1MHz
Voltage Proof	250Vdc
(Voltage applied for 5 secs max. @ 50mA max. charge current)	
Min Insulation Resistance (IR)	100.00GOhm @ 100Vdc
Dielectric Classification	C0G/NP0 (1B) to AEC-Q200
Rated Temperature Range	-55°C / +125°C
Maximum Capacitance Change over Temperature Range	No DC Voltage 0±30ppm/°C Rated DC Voltage -
Climatic Category (IEC)	55/125/56
Ageing Characteristic	Zero

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Date: Friday, January 18, 2019

20190118 06191355UTC

Multilayer Ceramic Chip Capacitor

Part Number: 0603J1000391JAT

Description: 0603 100V 390pF ±5% C0G/NP0 (1B) to AEC-Q200

Environmental

RoHS Compliant to 2011/65/EC as amended by 2015/863/EU	Compliant
REACH Compliant	191 compliant
California Proposition 65	No exposure risk

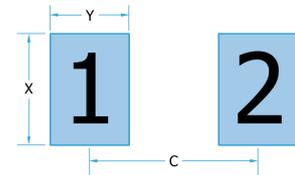
Board Layout

Knowles' conventional 2-terminal chip capacitors can generally be mounted using pad designs in accordance with international specification IPC-7351, Generic Requirements for Surface Mount Design and Land Pattern Standards, but there are some other factors that have been shown to reduce mechanical stress, such as reducing the pad width to less than the chip width. In addition, the position of the chip on the board should be considered.

Some high voltage parts may require modifications to the board layout and/or the addition of a conformal coating to prevent flashover. Refer to application note AN0043 for further information.

IPC-7351 pad design

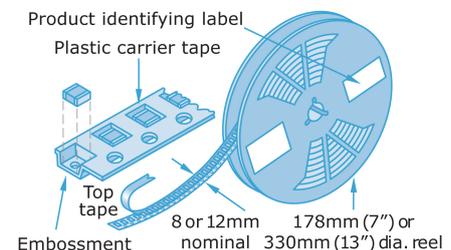
	0603	
C	1.60mm	0.063"
Y	0.85mm	0.033"
X	1.00mm	0.039"



Packaging

Tape packaging information for tape-and-reel parts:

Tape and reel packing of surface mounting chip capacitors for automatic placement are in accordance with IEC60286-3.



Soldering

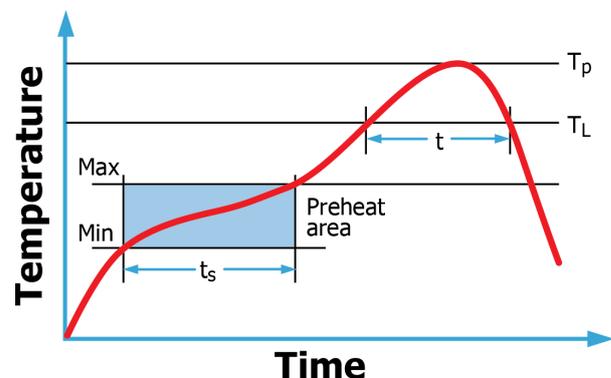
Reflow solder in accordance with IPC-A-610. Recommended reflow profile as laid down in IPC/JEDEC J-STD-020.

Wave soldering is also possible, but care must be taken for case sizes 1210 and larger and component thickness >1.0mm. Trials are encouraged.

Hand soldering is not recommended and can lead to component damage through thermal shock.

PdAg terminations are primarily intended for conductive epoxy attachment - they may be suitable for soldering but trials are recommended.

Application notes with mounting and handling guidance are available on request.



Compex

DLI

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