



PSMN1R0-25YLD

N-channel 25 V, 1.0 mΩ, 240 A logic level MOSFET in LPAK56 using NextPowerS3 Technology

19 April 2016

Product data sheet

1. General description

Logic level gate drive N-channel enhancement mode MOSFET in LPAK56 package. NextPowerS3 portfolio utilising NXP's unique "SchottkyPlus" technology delivers high efficiency, low spiking performance usually associated with MOSFETs with an integrated Schottky or Schottky-like diode but without problematic high leakage current. NextPowerS3 is particularly suited to high efficiency applications at high switching frequencies.

2. Features and benefits

- 100% Avalanche tested at $I_{AS} = 100\text{ A}$
- Ultra low Q_G , Q_{GD} and Q_{OSS} for high system efficiency, especially at higher switching frequencies
- Superfast switching with soft-recovery
- Low spiking and ringing for low EMI designs
- Unique "SchottkyPlus" technology; Schottky-like performance with $< 1\text{ }\mu\text{A}$ leakage at $25\text{ }^\circ\text{C}$
- Optimised for 4.5 V gate drive
- Low parasitic inductance and resistance
- High reliability clip bonded and solder die attach Power SO8 package; no glue, no wire bonds, qualified to $175\text{ }^\circ\text{C}$
- Wave solderable; exposed leads for optimal visual solder inspection

3. Applications

- On-board DC:DC solutions for server and telecommunications
- Secondary-side synchronous rectification in telecommunication applications
- Voltage regulator modules (VRM)
- Point-of-Load (POL) modules
- Power delivery for V-core, ASIC, DDR, GPU, VGA and system components
- Brushed and brushless motor control
- Power OR-ing

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$25\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$		-	-	25	V
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ }^\circ\text{C}$; Fig. 2	[1]	-	-	100	A



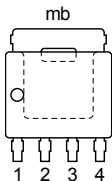
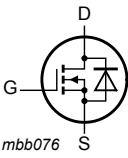
N-channel 25 V, 1.0 mΩ, 240 A logic level MOSFET in LPAK56 using NextPowerS3 Technology

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
P _{tot}	total power dissipation	T _{mb} = 25 °C; Fig. 1		-	-	160	W
T _j	junction temperature			-55	-	175	°C
Static characteristics							
R _{DSon}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	0.89	1	mΩ
		V _{GS} = 4.5 V; I _D = 25 A; T _j = 25 °C; Fig. 10		-	1.19	1.43	mΩ
Dynamic characteristics							
Q _{G(tot)}	total gate charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 10 V; Fig. 12 ; Fig. 13		-	71.8	-	nC
		I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; Fig. 12 ; Fig. 13		-	33.2	-	nC
		I _D = 0 A; V _{DS} = 0 V; V _{GS} = 10 V		-	39.7	-	nC
Q _{GD}	gate-drain charge	I _D = 25 A; V _{DS} = 12 V; V _{GS} = 4.5 V; Fig. 12 ; Fig. 13		-	8	-	nC
Source-drain diode							
S	softness factor	I _S = 25 A; dI _S /dt = -100 A/μs; V _{GS} = 0 V; V _{DS} = 12 V; Fig. 16		-	0.9	-	

[1] Continuous current is limited by package.

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 LPAK56; Power-SO8 (SOT669)	
2	S	source		
3	S	source		
4	G	gate		
mb	D	mounting base; connected to drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN1R0-25YLD	LPAK56; Power-SO8	Plastic single-ended surface-mounted package (LPAK56; Power-SO8); 4 leads	SOT669

7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN1R0-25YLD	1D025L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$		-	25	V
V_{DGR}	drain-gate voltage	$25\text{ °C} \leq T_j \leq 175\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$		-	25	V
V_{GS}	gate-source voltage			-20	20	V
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Fig. 1		-	160	W
I_D	drain current	$V_{GS} = 10\text{ V}$; $T_{mb} = 25\text{ °C}$; Fig. 2	[1]	-	100	A
		$V_{GS} = 10\text{ V}$; $T_{mb} = 100\text{ °C}$; Fig. 2	[1]	-	100	A
I_{DM}	peak drain current	$t_p \leq 10\text{ }\mu\text{s}$; Fig. 3		-	1226	A
T_{stg}	storage temperature			-55	175	°C
T_j	junction temperature			-55	175	°C
$T_{sld(M)}$	peak soldering temperature			-	260	°C
V_{ESD}	electrostatic discharge voltage	HBM		1700	-	V
Source-drain diode						
I_S	source current	$T_{mb} = 25\text{ °C}$	[1]	-	100	A
I_{SM}	peak source current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$		-	1226	A
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 25\text{ A}$; $V_{sup} \leq 25\text{ V}$; $R_{GS} = 50\text{ }\Omega$; $V_{GS} = 10\text{ V}$; $T_{j(\text{init})} = 25\text{ °C}$; unclamped; $t_p = 4.34\text{ ms}$	[2] [3]	-	1762	mJ

[1] Continuous current is limited by package.

[2] Single-pulse avalanche rating limited by maximum junction temperature of 175 °C.

[3] Refer to application note AN10273 for further information.

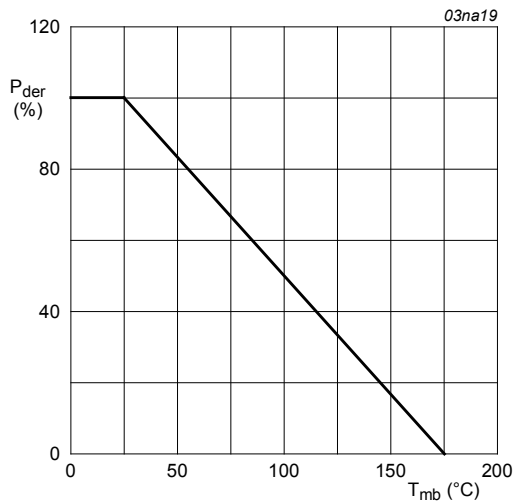
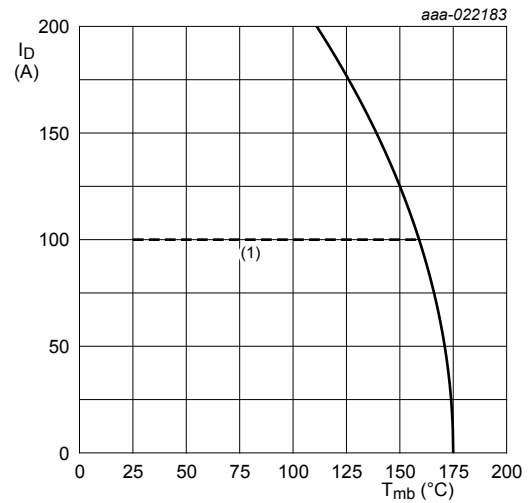


Fig. 1. Normalized total power dissipation as a function of mounting base temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}\text{C})}} \times 100\%$$

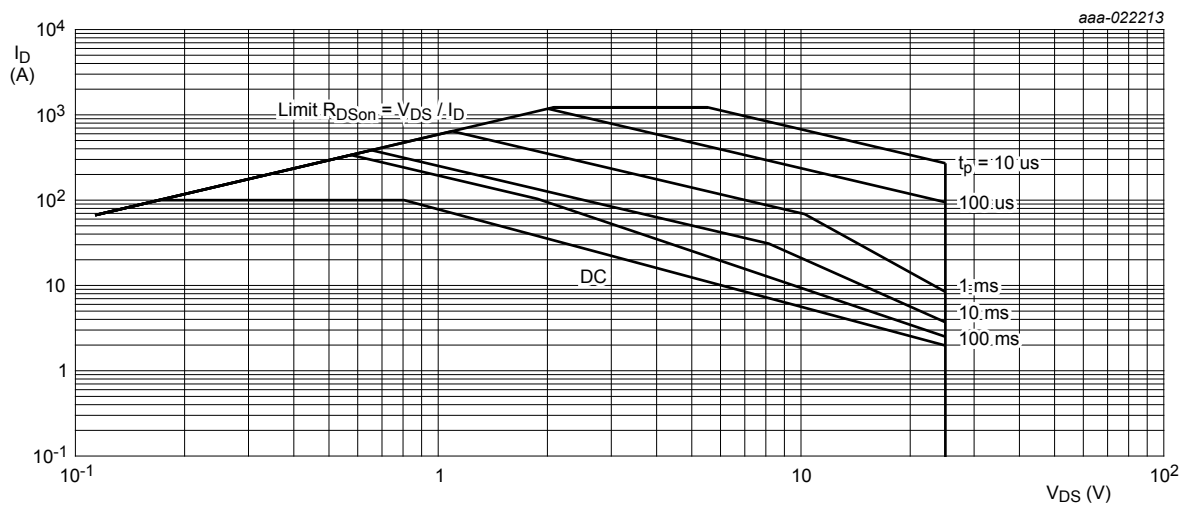


$V_{GS} \geq 10\text{ V}$

(1) Capped at 100A due to package

Fig. 2. Continuous drain current as a function of mounting base temperature

$$I_D = 306\text{A} \times \sqrt{\frac{175^{\circ}\text{C} - T_{mb}}{150^{\circ}\text{C}}} \quad \text{for } T_{mb} \geq 25^{\circ}\text{C}$$



$T_{mb} = 25^{\circ}\text{C}$; I_{DM} is a single pulse

Fig. 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4		-	0.68	0.94	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	Fig. 5		-	50	-	K/W
		Fig. 6		-	125	-	K/W

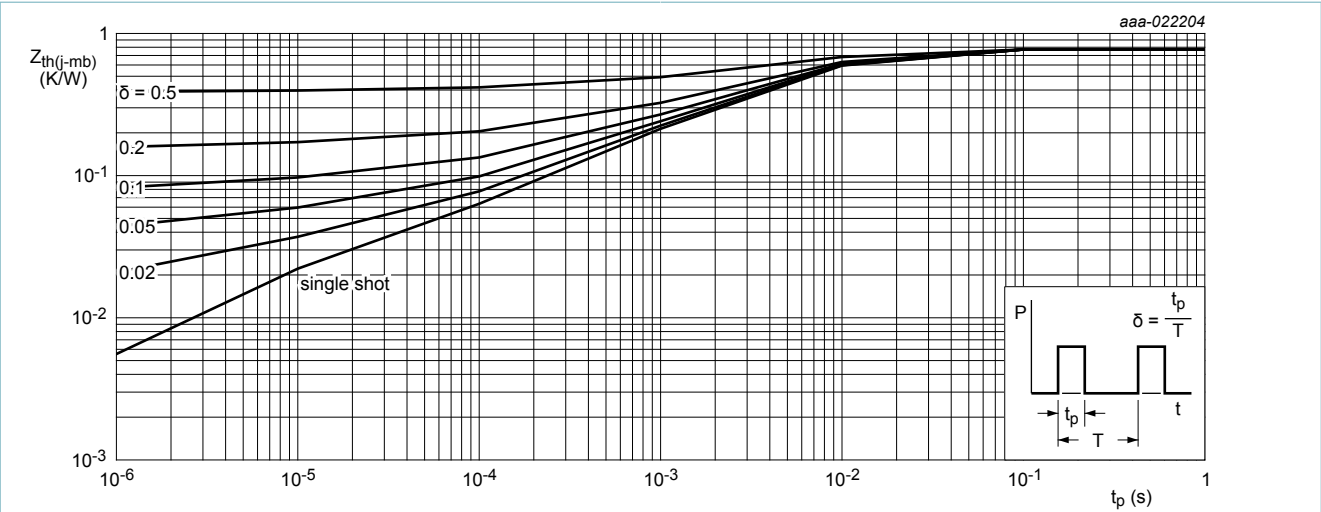


Fig. 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

Fig. 5. PCB layout for thermal resistance junction to ambient 1" square pad; FR4 Board; 2oz copper

Fig. 6. PCB layout for thermal resistance junction to ambient minimum footprint; FR4 Board; 2oz copper

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	25	-	-	V
		$I_D = 250\ \mu A$; $V_{GS} = 0\ V$; $T_j = -55\ ^\circ C$	22.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\ mA$; $V_{DS} = V_{GS}$; $T_j = 25\ ^\circ C$	1.2	1.75	2.2	V
$\Delta V_{GS(th)}/\Delta T$	gate-source threshold voltage variation with temperature	$25\ ^\circ C \leq T_j \leq 175\ ^\circ C$	-	-5	-	mV/K
I_{DSS}	drain leakage current	$V_{DS} = 20\ V$; $V_{GS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	1	μA
		$V_{DS} = 20\ V$; $V_{GS} = 0\ V$; $T_j = 125\ ^\circ C$	-	29.7	-	μA
I_{GSS}	gate leakage current	$V_{GS} = 20\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	100	nA
		$V_{GS} = -20\ V$; $V_{DS} = 0\ V$; $T_j = 25\ ^\circ C$	-	-	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 25\ ^\circ C$; Fig. 10	-	0.89	1	mΩ
		$V_{GS} = 10\ V$; $I_D = 25\ A$; $T_j = 175\ ^\circ C$; Fig. 10 ; Fig. 11	-	-	1.7	mΩ
		$V_{GS} = 4.5\ V$; $I_D = 25\ A$; $T_j = 25\ ^\circ C$; Fig. 10	-	1.19	1.43	mΩ
		$V_{GS} = 4.5\ V$; $I_D = 25\ A$; $T_j = 175\ ^\circ C$; Fig. 10 ; Fig. 11	-	-	2.43	mΩ
R_G	gate resistance	$f = 1\ MHz$	-	1.14	-	Ω
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$I_D = 25\ A$; $V_{DS} = 12\ V$; $V_{GS} = 10\ V$; Fig. 12 ; Fig. 13	-	71.8	-	nC
		$I_D = 25\ A$; $V_{DS} = 12\ V$; $V_{GS} = 4.5\ V$; Fig. 12 ; Fig. 13	-	33.2	-	nC
		$I_D = 0\ A$; $V_{DS} = 0\ V$; $V_{GS} = 10\ V$	-	39.7	-	nC
Q_{GS}	gate-source charge	$I_D = 25\ A$; $V_{DS} = 12\ V$; $V_{GS} = 4.5\ V$; Fig. 12 ; Fig. 13	-	12.9	-	nC
$Q_{GS(th)}$	pre-threshold gate-source charge		-	7.8	-	nC
$Q_{GS(th-pl)}$	post-threshold gate-source charge		-	5.1	-	nC
Q_{GD}	gate-drain charge		-	8	-	nC
$V_{GS(pl)}$	gate-source plateau voltage	$I_D = 25\ A$; $V_{DS} = 12\ V$; Fig. 12 ; Fig. 13	-	2.7	-	V

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Symbol	Parameter	Conditions		Min	Typ	Max	Unit
C_{iss}	input capacitance	$V_{DS} = 12\text{ V}; V_{GS} = 0\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^{\circ}\text{C};$ Fig. 14		-	5308	-	pF
C_{oss}	output capacitance			-	1979	-	pF
C_{rss}	reverse transfer capacitance			-	342	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 12\text{ V}; R_L = 0.6\text{ }\Omega; V_{GS} = 4.5\text{ V};$ $R_{G(ext)} = 5\text{ }\Omega$		-	30.3	-	ns
t_r	rise time			-	36	-	ns
$t_{d(off)}$	turn-off delay time			-	34	-	ns
t_f	fall time			-	24.5	-	ns
Q_{oss}	output charge	$V_{GS} = 0\text{ V}; V_{DS} = 12\text{ V}; f = 1\text{ MHz};$ $T_j = 25\text{ }^{\circ}\text{C}$		-	36.4	-	nC
Source-drain diode							
V_{SD}	source-drain voltage	$I_S = 25\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^{\circ}\text{C};$ Fig. 15		-	0.79	1.2	V
t_{rr}	reverse recovery time	$I_S = 25\text{ A}; dI_S/dt = -100\text{ A}/\mu\text{s}; V_{GS} = 0\text{ V};$ $V_{DS} = 12\text{ V};$ Fig. 16		-	36.9	-	ns
Q_r	recovered charge		[1]	-	36.7	-	nC
t_a	reverse recovery rise time			-	19.2	-	ns
t_b	reverse recovery fall time			-	17.7	-	ns
S	softness factor			-	0.9	-	

[1] includes capacitive recovery

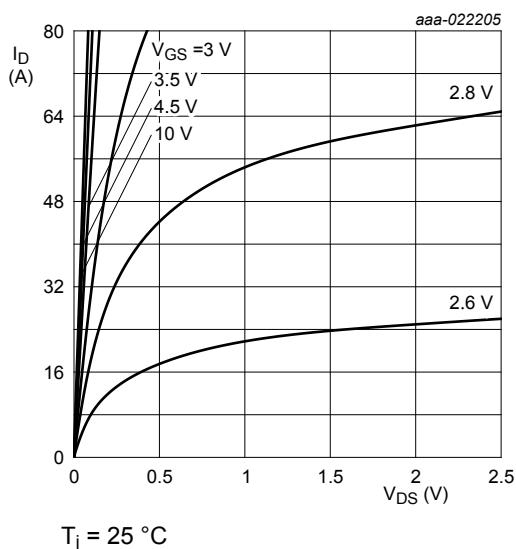


Fig. 7. Output characteristics; drain current as a function of drain-source voltage; typical values

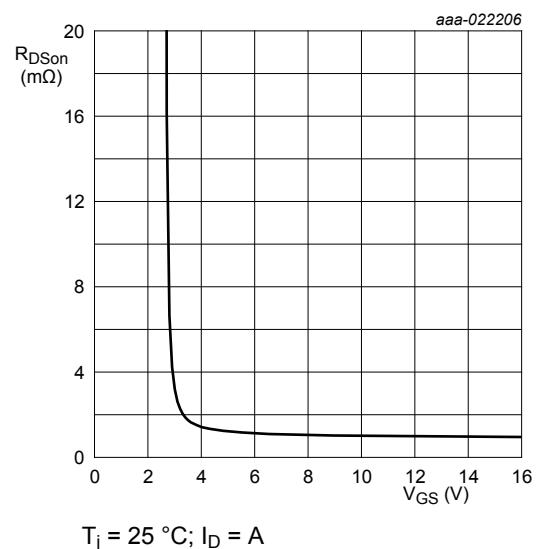
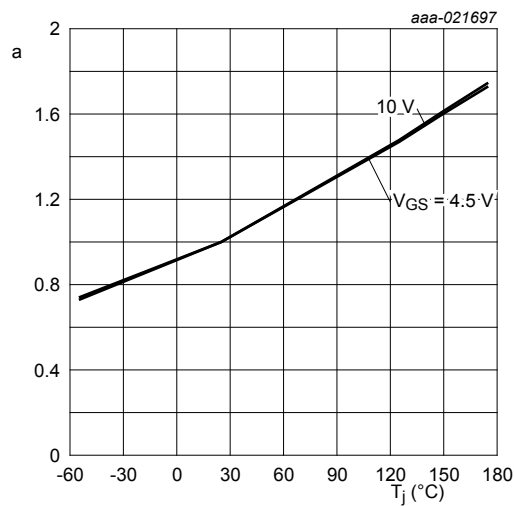
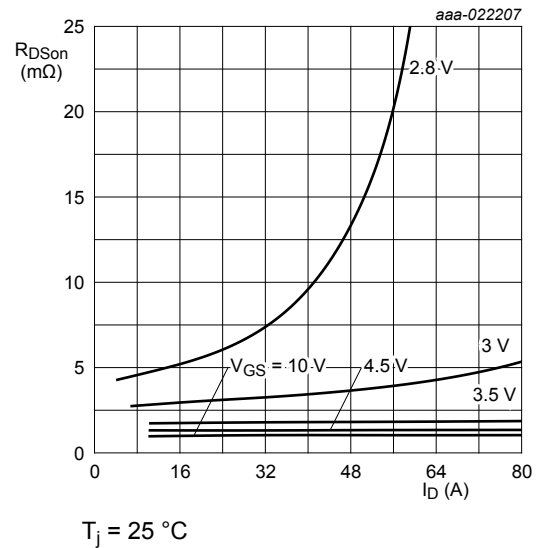
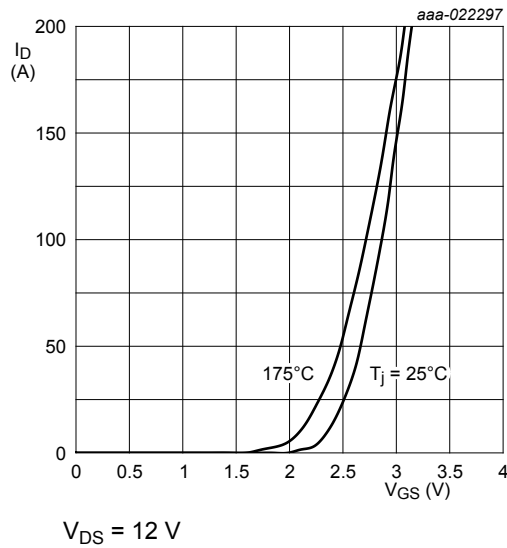
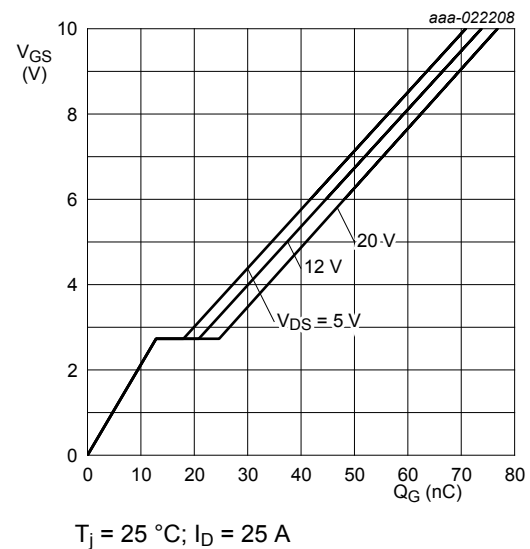


Fig. 8. Drain-source on-state resistance as a function of gate-source voltage; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^{\circ}\text{C})}$$



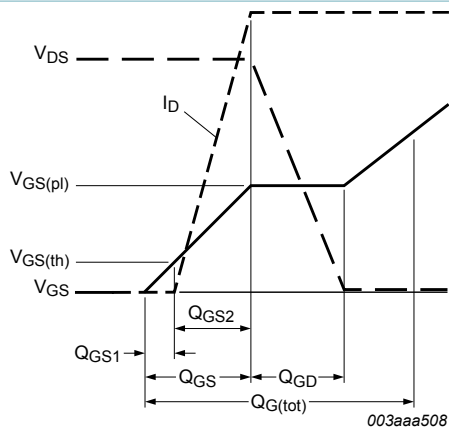
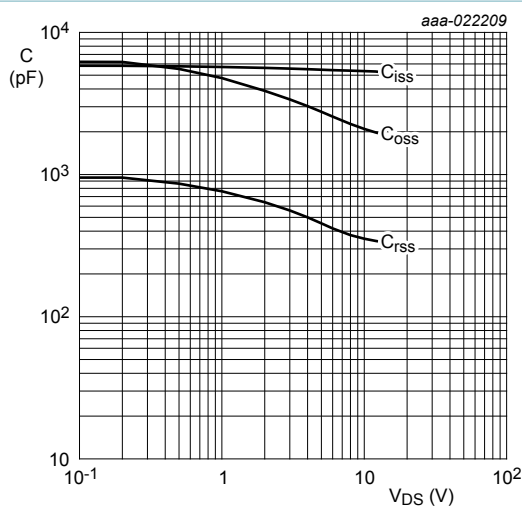
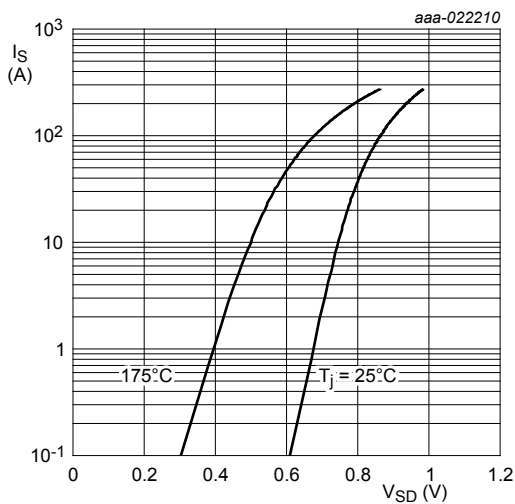


Fig. 13. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$; $f = 1 \text{ MHz}$

Fig. 14. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0 \text{ V}$

Fig. 15. Source-drain (diode forward) current as a function of source-drain (diode forward) voltage; typical values

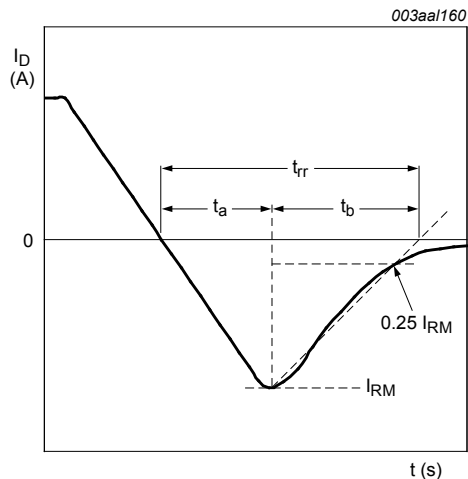


Fig. 16. Reverse recovery timing definition

11. Package outline

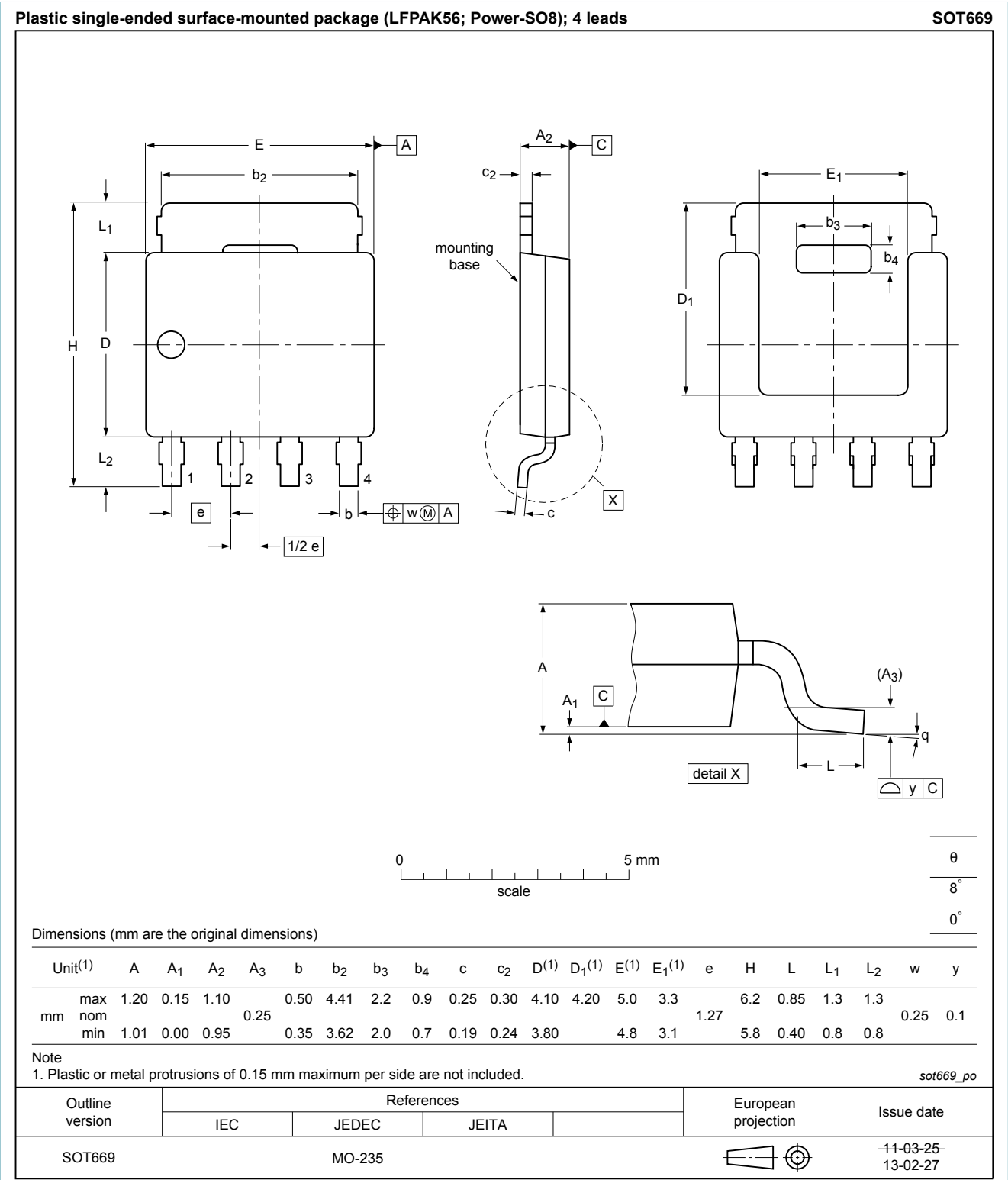


Fig. 17. Package outline LPAK56; Power-SO8 (SOT669)

12. Legal information

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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[BZT52H-B9V1.115](#) [BZV85-C3V9.113](#) [BZX79-C47.113](#) [P5020NSE7VNB](#) [S12ZVML12EVBLIN](#) [SCC2692AC1N40](#) [LPC1785FBD208K](#)
[LPC2124FBD64/01](#) [LS1020ASN7KQB](#) [LS1020AXN7HNB](#) [LS1020AXN7KQB](#) [LS1043ASE7PQA](#) [T1023RDB-PC](#)