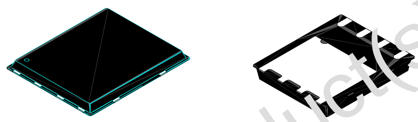
# STL55NH3LL

## N-channel 30 V, 0.0079 Ω, 15 A, PowerFLAT™ (6x5) ultra low gate charge STripFET™ Power MOSFET

## Features

| Type | $V_{DSS}$ | $R_{DS(on)}$ max | $I_D$ |
|---|---|---|---|
| STL55NH3LL | 30 V | < 0.0088 Ω | 15 A |

- Improved die-to-footprint ratio
- Very low profile package (1mm max)
- Very low thermal resistance
- Very low gate charge
- Low threshold device



PowerFLAT™(6x5)

## Application

- Switching applications

## Description

This application specific Power MOSFET is the latest generation of STMicroelectronics unique “STripFET™” technology. The resulting transistor is optimized for low on-resistance and minimal gate charge. The chip-scaled PowerFLAT™ package allows a significant board space saving, still boosting the performance.

**Figure 1. Internal schematic diagram**

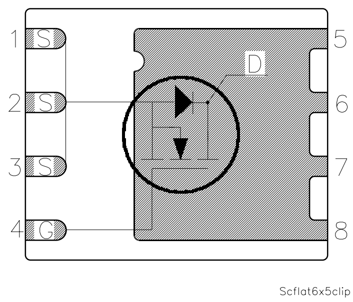





**Table 1. Device summary**

| Order code | Marking | Package | Packaging |
|---|---|---|---|
| STL55NH3LL | L55NH3LL | PowerFLAT™ (6x5) | Tape and reel |

# Contents

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $V_{DS}$ | Drain-source voltage ($V_{GS}$ = 0) | 30 | V |
| $V_{GS}$ (1) | Gate-source voltage | ± 16 | V |
| $V_{GS}$ (2) | Gate-source voltage | ± 18 | V |
| $I_D$ (3) | Drain current (continuous) at $T_C$ = 25 °C | 55 | A |
| $I_D$ (3) | Drain current (continuous) at $T_C$=100 °C | 36 | A |
| $I_{DM}$ (4) | Drain current (pulsed) | 60 | A |
| $I_D$ (5) | Drain current (continuous) at $T_C$ = 25 °C | 15 | A |
| $I_D$ (5) | Drain current (continuous) at $T_C$=100 °C | 9.4 | A |
| $P_{TOT}$ (5) | Total dissipation at $T_C$ = 25 °C | 4 | W |
| $P_{TOT}$ (3) | Total dissipation at $T_C$ = 25 °C | 60 | W |
| | Derating factor | 0.03 | W/°C |
| $T_J$<br>$T_{stg}$ | Operating junction temperature<br>Storage temperature | -55 to 150 | °C |

1. Continuous mode
2. Guaranteed for test time ≤ 15 ms
3. The value is rated according $R_{thj-case}$
4. Pulse width limited by safe operating area
5. The value is rated according $R_{thj-pcb}$

**Table 3. Thermal resistance**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{thj-case}$ | Thermal resistance junction-case (drain) | 2.08 | °C/W |
| $R_{thj-pcb}$ (1) | Thermal resistance junction-ambient | 31.3 | °C/W |

1. When mounted on FR-4 board of 1inch², 2oz Cu, t < 10 sec

**Table 4. Avalanche data**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $I_{AV}$ | Not-repetitive avalanche current<br>(pulse width limited by Tj Max) | 7.5 | A |
| $E_{AS}$ | Single pulse avalanche energy<br>(starting Tj = 25 °C, $I_D$=$I_{AV}$, $V_{DD}$ = 24 V, L=6 mH) | 150 | mJ |

# 2 Electrical characteristics

($T_{CASE}$=25°C unless otherwise specified)

**Table 5. On/off states**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-source breakdown voltage | $I_D$ = 250 µA, $V_{GS}$= 0 | 30 | | | V |
| $I_{DSS}$ | Zero gate voltage drain current ($V_{GS}$ = 0) | $V_{DS}$ = max rating,<br>$V_{DS}$ = max rating @125 °C | | | 1<br>10 | µA<br>µA |
| $I_{GSS}$ | Gate body leakage current ($V_{DS}$ = 0) | $V_{GS}$ = ±16 V | | | ±100 | nA |
| $V_{GS(th)}$ | Gate threshold voltage | $V_{DS}$= $V_{GS}$, $I_D$ = 250 µA | 1 | | 2.5 | V |
| $R_{DS(on)}$ | Static drain-source on resistance | $V_{GS}$= 10 V, $I_D$= 7.5 A<br>$V_{GS}$= 8 V, $I_D$= 7.5 A<br>$V_{GS}$= 4.5 V, $I_D$= 7.5 A | | 0.0079<br>0.0079<br>0.009 | 0.0088<br>0.0088<br>0.0115 | Ω<br>Ω<br>Ω |

**Table 6. Dynamic**

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $C_{iss}$<br>$C_{oss}$<br>$C_{rss}$ | Input capacitance<br>Output capacitance<br>Reverse transfer capacitance | $V_{DS}$ = 25 V, f=1 MHz, $V_{GS}$=0 | | 965<br>285<br>38 | | pF<br>pF<br>pF |
| $Q_g$<br>$Q_{gs}$<br>$Q_{gd}$ | Total gate charge<br>Gate-source charge<br>Gate-drain charge | $V_{DD}$=15 V, $I_D$ = 15 A<br>$V_{GS}$ =4.5 V<br>*(see Figure 16)* | | 9<br>3.7<br>3 | 12 | nC<br>nC<br>nC |
| $Q_{gs1}$<br>$Q_{gs2}$ | Pre $V_{th}$ gate-to-source charge<br>Post $V_{th}$ gate-to-source charge | $V_{DD}$=15 V, $I_D$ = 15 A<br>$V_{GS}$ =4.5 V | | 2.5<br>1.2 | | nC<br>nC |
| $R_G$ | Gate input resistance | f=1 MHz Gate DC Bias = 0<br>Test signal level = 20 mV<br>open drain | 0.5 | 1.5 | 2.5 | Ω |

Table 7. Switching times

| Symbol | Parameter | Test conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{d(on)}$<br>$t_r$<br>$t_{d(off)}$<br>$t_f$ | Turn-on delay time<br>Rise time<br>Turn-off delay time<br>Fall time | $V_{DD}$=15 V, $I_D$= 7.5 A,<br>$R_G$=4.7 Ω, $V_{GS}$=4.5 V<br>*(see Figure 18)* | | 15<br>32<br>18<br>8.5 | | ns<br>ns<br>ns<br>ns |

Table 8. Source drain diode

| Symbol | Parameter | Test conditions | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{SD}$ | Source-drain current | | | | 15 | A |
| $I_{SDM}$(1) | Source-drain current (pulsed) | | | | 60 | A |
| $V_{SD}$(2) | Forward on voltage | $I_{SD}$=15 A, $V_{GS}$=0 | | | 1.3 | V |
| $t_{rr}$<br>$Q_{rr}$<br>$I_{RRM}$ | Reverse recovery time<br>Reverse recovery charge<br>Reverse recovery current | $I_{SD}$=15 A,<br>di/dt = 100 A/µs,<br>$V_{DD}$=20 V, $T_J$=150 °C<br>*(see Figure 17)* | | 24<br>17.4<br>1.45 | | ns<br>nC<br>A |

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300 µs, duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

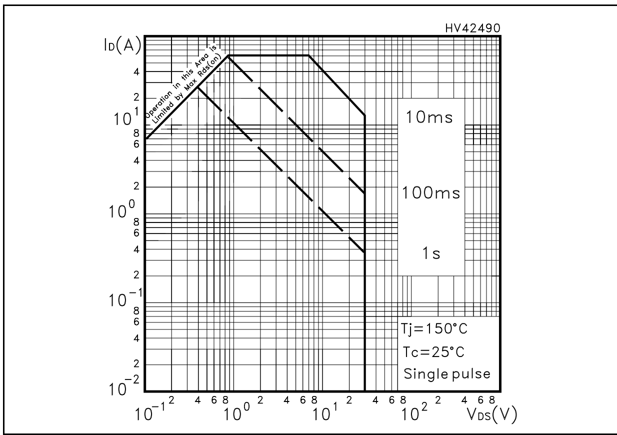



**Figure 2. Safe operating area**

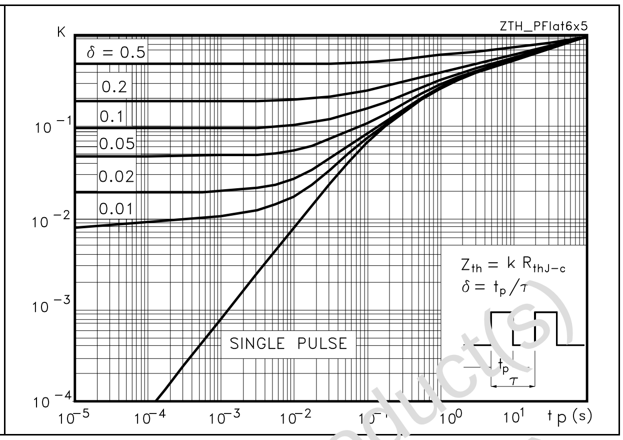



**Figure 3. Thermal impedance**

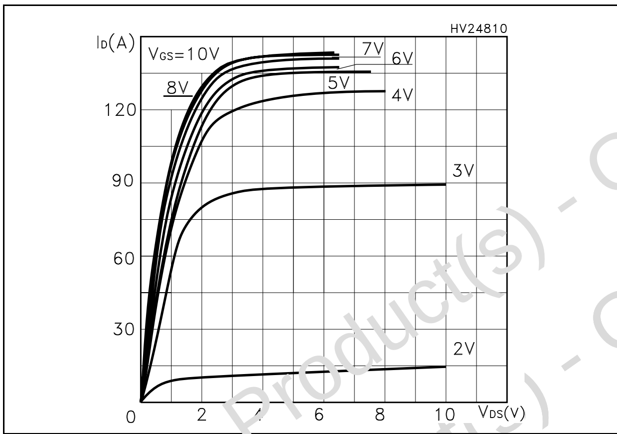



**Figure 4. Output characteristics**

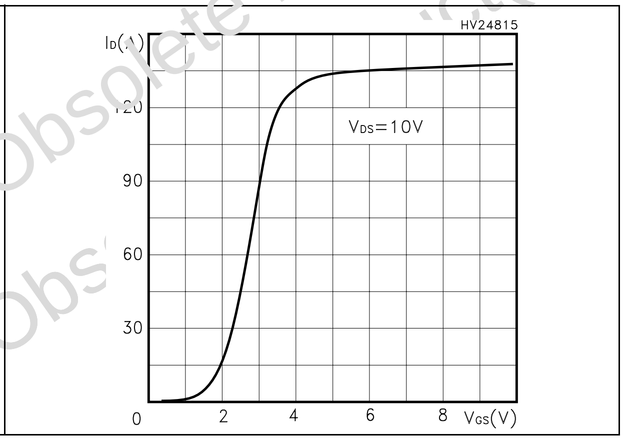



**Figure 5. Transfer characteristics**

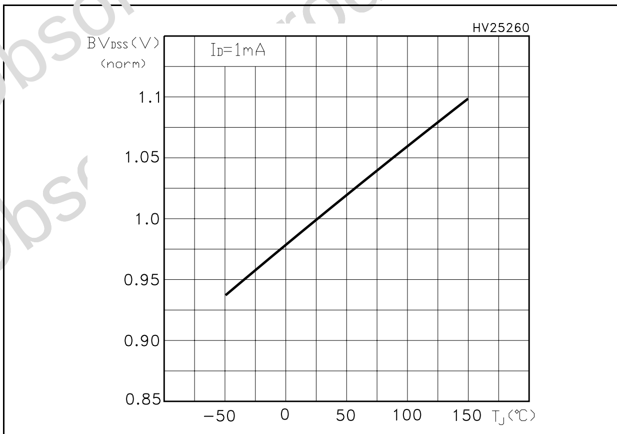



**Figure 6. Normalized $B_{VDSS}$ vs temperature**

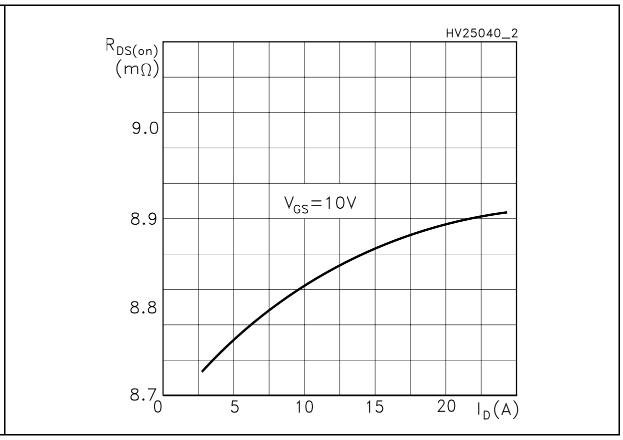



**Figure 7. Static drain-source on resistance**

**Figure 8. Gate charge vs gate-source voltage**

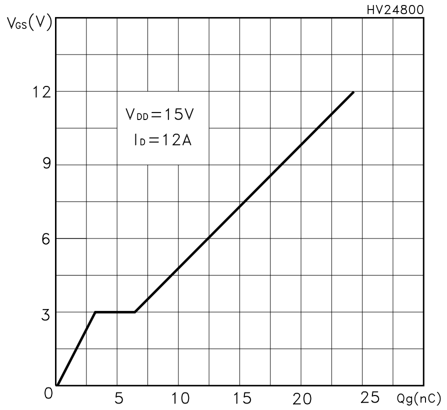



**Figure 9. Capacitance variations**

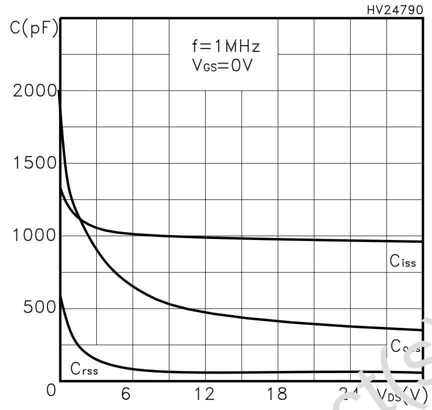



**Figure 10. Normalized gate threshold voltage vs temperature**

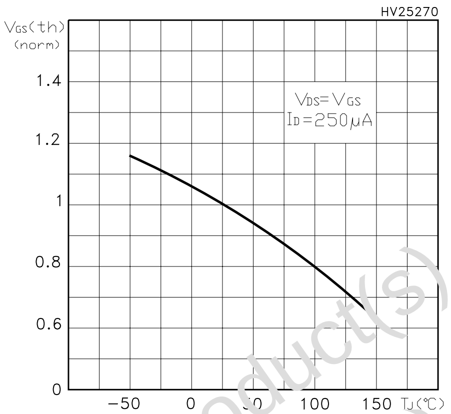



**Figure 11. Normalized on resistance vs temperature**

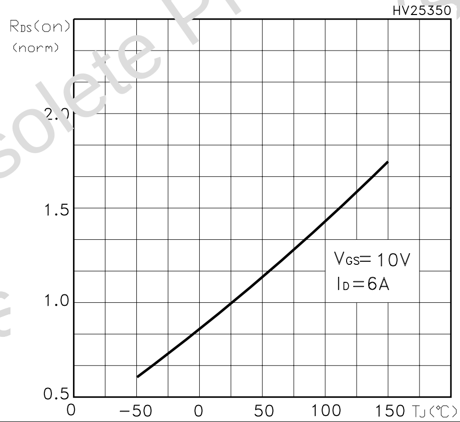



**Figure 12. Source-drain diode forward characteristics**

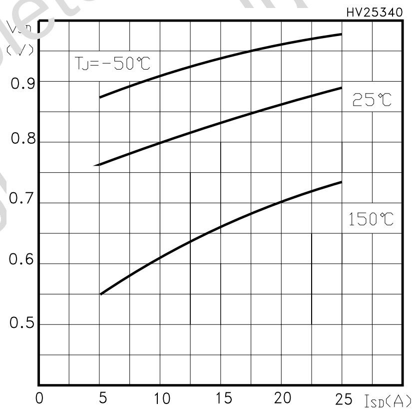



**Figure 13. Avalanche energy vs starting $t_j$**

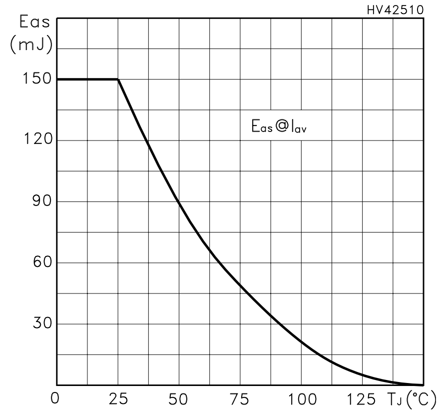
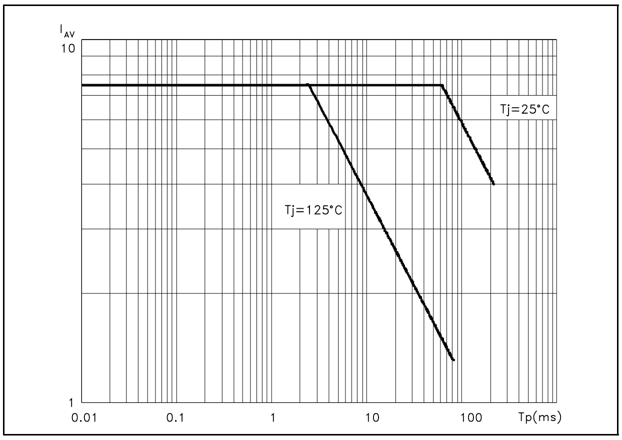


**Figure 14. Allowable $I_{av}$ vs time in avalanche**




The previous curve gives the single pulse safe operating area for unclamped inductive loads, under the following conditions:

$P_{D(AVE)} = 0.5 * (1.3 * B_{VDSS} * I_{AV})$

$E_{AS(AR)} = P_{D(AVE)} * t_{AV}$

Where:

$I_{AV}$ is the allowable current in avalanche

$P_{D(AVE)}$ is the average power dissipation in avalanche (single pulse)

$t_{AV}$ is the time in avalanche

# 3 Test circuits

Figure 15. Switching times test circuit for resistive load

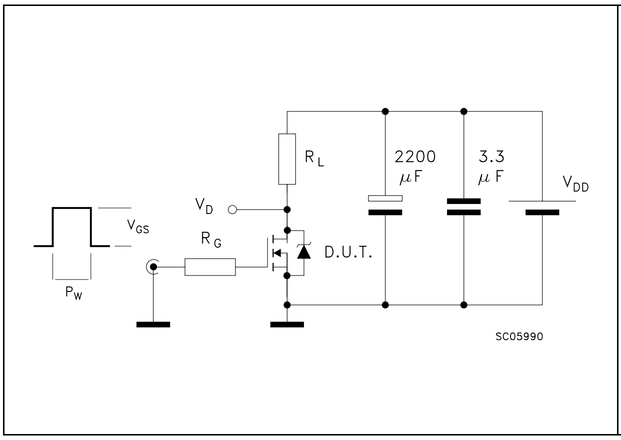



Figure 16. Gate charge test circuit

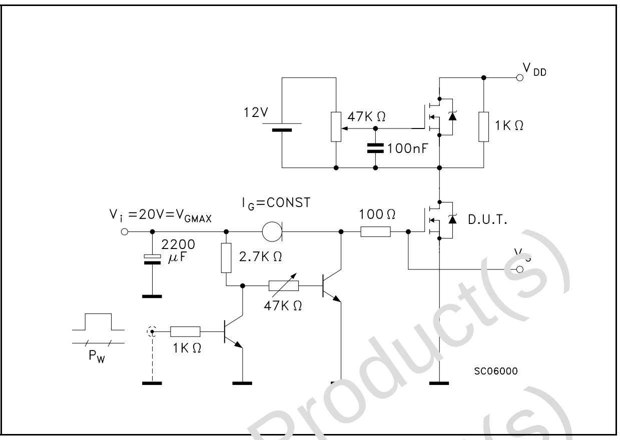



Figure 17. Test circuit for inductive load switching and diode recovery times

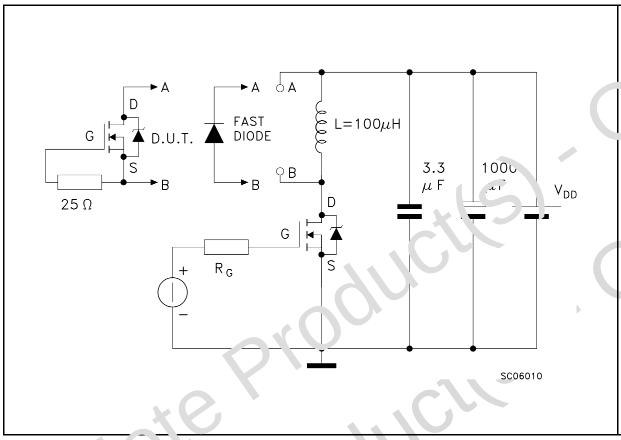



Figure 18. Unclamped inductive load test circuit

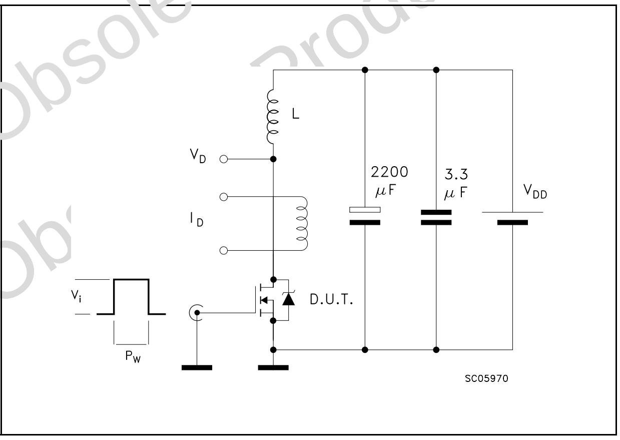



Figure 19. Unclamped inductive waveform

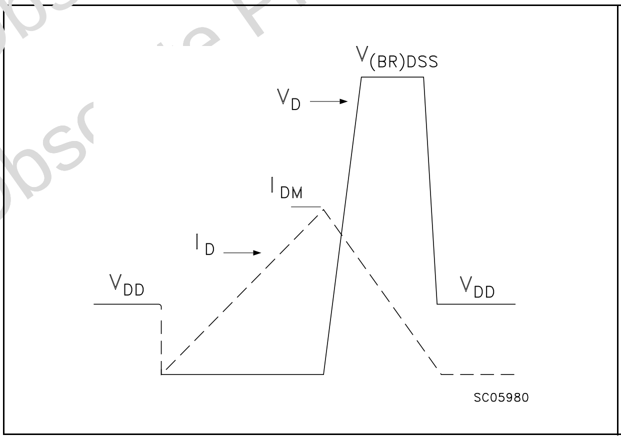



Figure 20. Switching time waveform

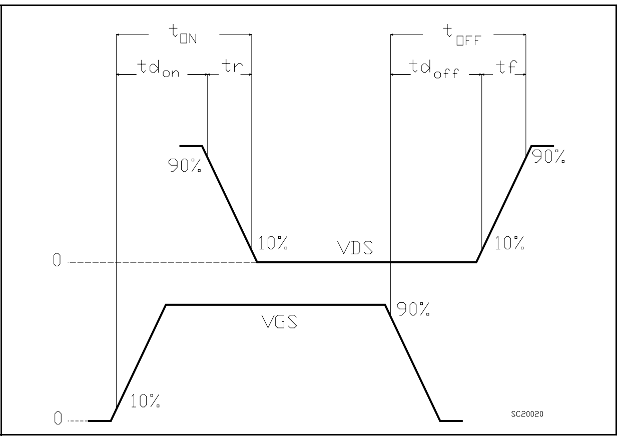
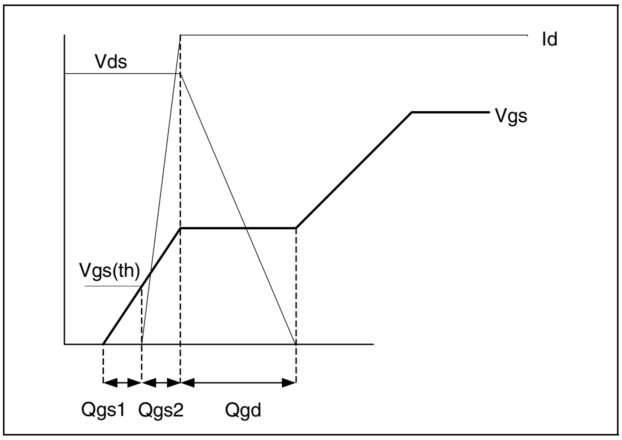


**Figure 21. Gate charge waveform**

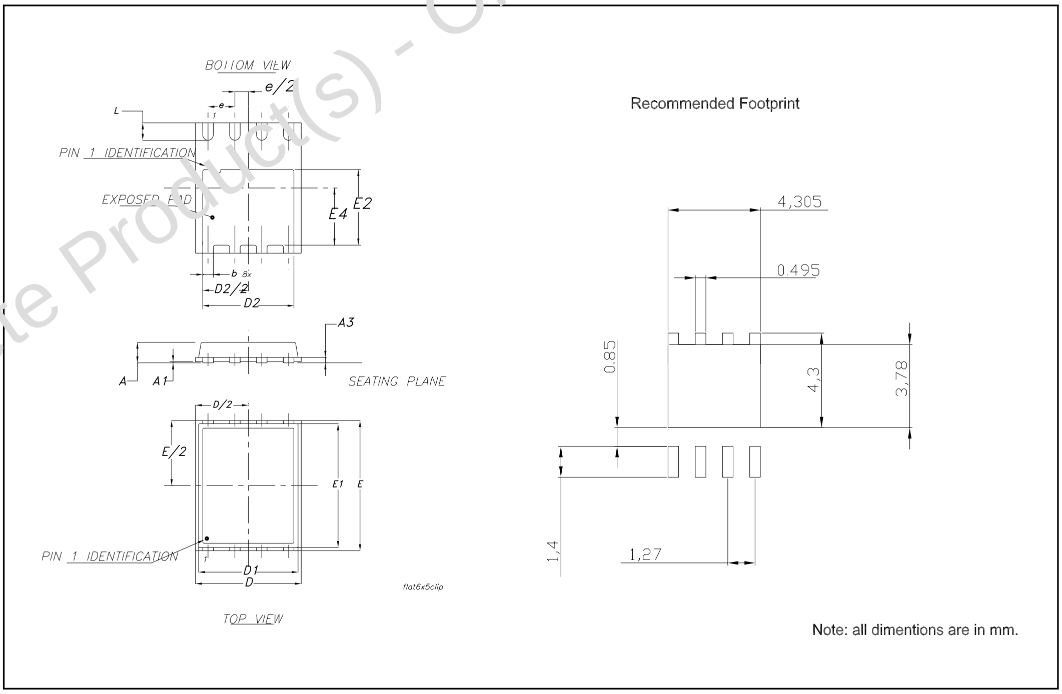


# 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*

## PowerFLAT™ (6x5) MECHANICAL DATA

| DIM. | mm. | | | inch | | |
|---|---|---|---|---|---|---|
| | MIN. | TYP | MAX. | MIN. | TYP. | MAX. |
| A | 0.80 | 0.83 | 0.93 | 0.031 | 0.032 | 0.036 |
| A1 | | 0.02 | 0.05 | | 0.0007 | 0.0019 |
| A3 | | 0.20 | | | 0.007 | |
| b | 0.35 | 0.40 | 0.47 | 0.013 | 0.015 | 0.018 |
| D | | 5.00 | | | 0.196 | |
| D1 | | 4.75 | | | 0.187 | |
| D2 | 4.15 | 4.20 | 4.25 | 0.163 | 0.165 | 0.167 |
| E | | 6.00 | | | 0.236 | |
| E1 | | 5.75 | | | 0.226 | |
| E2 | 3.43 | 3.48 | 3.53 | 0.135 | 0.137 | 0.139 |
| E4 | 2.58 | 2.63 | 2.68 | | 0.103 | 0.105 |
| e | | 1.27 | | | 0.050 | |
| L | 0.70 | 0.80 | 0.90 | 0.027 | 0.031 | 0.035 |



# 5 Revision history

Table 9. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 18-Mar-2008 | 1 | First release. |
| 05-May-2008 | 2 | Corrected *Table 1: Device summary* |
| 07-May-2008 | 3 | Update *Figure 6: Normalized $B_{VDSS}$ vs temperature* |

**Please Read Carefully:**