

# **FMW20N60S1HF**

**FUJI POWER MOSFET** 

## **Super J-MOS series**

#### N-Channel enhancement mode power MOSFET

#### Features

Low on-state resistance Low switching loss easy to use (more controllabe switching dV/dt by Rg)

#### Applications

**UPS** 

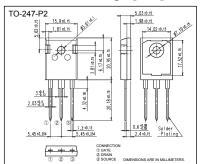
Server

Telecom

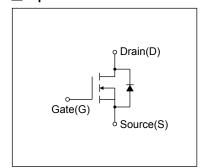
Power conditioner system

Power supply

#### ■ Outline Drawings [mm]



#### ■ Equivalent circuit schematic



#### ■ Maximum Ratings and Characteristics

#### ● Absolute Maximum Ratings at T<sub>c</sub>=25°C (unless otherwise specified)

Description	Symbol	Characteristics	Unit	Remarks	
Dania Carras Valtaria	V <sub>DS</sub>	600	V		
Drain-Source Voltage	VDSX	600	V	V <sub>GS</sub> =-30V	
Continuous Drain Current	lo	±20	Α	Tc=25°C Note*1	
		±12.6	Α	Tc=100°C Note*1	
Pulsed Drain Current	IDP	±60	Α		
Gate-Source Voltage	V <sub>GS</sub>	±30	V		
Repetitive and Non-Repetitive Maximum Avalanche Current	lar	6.6	Α	Note *2	
Non-Repetitive Maximum Avalanche Energy	Eas	472.2	mJ	Note *3	
Maximum Drain-Source dV/dt	dV <sub>DS</sub> /dt	50	kV/μs	V <sub>DS</sub> ≤ 600V	
Peak Diode Recovery dV/dt	dV/dt	15	kV/µs Note *4		
Peak Diode Recovery -di/dt	-di/dt	100	A/µs	Note *5	
Maximum Power Dissipation	Po	2.5	10/	Ta=25°C	
		140	W	Tc=25°C	
Onevetion and Stavens Temperature range	Tch	150	°C		
Operating and Storage Temperature range	T <sub>stg</sub>	-55 to +150	°C		

Note \*1 : Limited by maximum channel temperature.

Note \*2 : Tch≤150°C, See Fig.1 and Fig.2 Note \*3 : Starting Tch=25°C, Ias=2A, L=216mH, Vbb=60V, Rg=50Ω, See Fig.1 and Fig.2

Eas limited by maximum channel temperature and avalanche current. Note \*4 : Ir≤-Ip, -di/dt=100A/µs, Vpp≤400V, Tch≤150°C.

Note \*5 : IF $\leq$ -ID, dV/dt=15kV/ $\mu$ s, VDD $\leq$ 400V, Tch $\leq$ 150°C.

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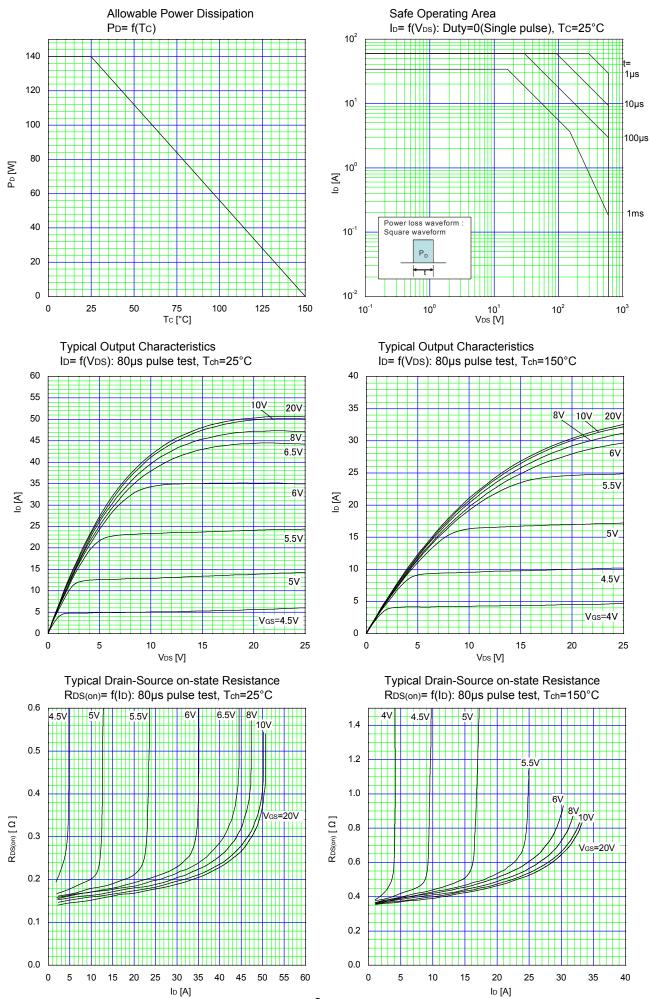
# ● Electrical Characteristics at T₀=25°C (unless otherwise specified) Static Ratings

Description	Symbol	Conditions		min.	typ.	max.	Unit	
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> =250μA V <sub>GS</sub> =0V		600	-	-	V	
Gate Threshold Voltage	V <sub>GS(th)</sub>	I <sub>D</sub> =250μA V <sub>DS</sub> =V <sub>GS</sub>		2.5	3	3.5	V	
Zero Gate Voltage Drain Current		V <sub>DS</sub> =600V V <sub>GS</sub> =0V	T <sub>ch</sub> =25°C	-	-	25	μA	
	Ipss	V <sub>DS</sub> =480V V <sub>GS</sub> =0V	T <sub>ch</sub> =125°C	-	-	250		
Gate-Source Leakage Current	Igss	V <sub>SS</sub> = ± 30V V <sub>DS</sub> =0V		-	10	100	nA	
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	I <sub>D</sub> =10A V <sub>GS</sub> =10V		-	0.161	0.19	Ω	
Gate resistance	Rg	f=1MHz, open drain		-	3.7	-	Ω	
Forward Transconductance	<b>g</b> fs	I <sub>D</sub> =10A V <sub>DS</sub> =25V		8.5	17.5	-	S	
Input Capacitance	Ciss	V <sub>DS</sub> =10V		-	1470	-		
Output Capacitance	Coss	V <sub>GS</sub> =0V f=1MHz		-	3120	-		
Reverse Transfer Capacitance	Crss			-	280	-		
Effective output capacitance, energy related (Note *6)	C <sub>o(er)</sub>	V <sub>GS</sub> =0V V <sub>DS</sub> =0480V		-	90	-	pF	
Effective output capacitance, time related (Note *7)	C <sub>o(tr)</sub>	V <sub>GS</sub> =0V V <sub>DS</sub> =0480V ID=constant		-	305	-		
td(on)	t <sub>d(on)</sub>	V <sub>DD</sub> =400V, V <sub>GS</sub> =10V I <sub>D</sub> =10A, R <sub>G</sub> =27Ω See Fig.3 and Fig.4		-	22	-	ns	
Turn-On Time	tr			-	40	-		
	t <sub>d(off)</sub>			-	162	-		
Turn-Off Time	tr			-	22	-		
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> =480V, I <sub>D</sub> =20A V <sub>GS</sub> =10V See Fig.5		-	48	-	nC	
Gate-Source Charge	Q <sub>GS</sub>			-	12.5	-		
Gate-Drain Charge	Q <sub>GD</sub>			-	15	-		
Drain-Source crossover Charge	Qsw			-	8	-		
Avalanche Capability	lav	L=6.02mH,Tch=25°C See Fig.1 and Fig.2		6.6	-	-	А	
Diode Forward On-Voltage	VsD	I <sub>F</sub> =20A,V <sub>GS</sub> =0V T <sub>ch</sub> =25°C		-	0.9	1.35	V	
Reverse Recovery Time	trr	I <sub>F</sub> =20A, V <sub>GS</sub> =0V V <sub>DD</sub> =400V -di/dt=100A/µs T <sub>ch</sub> =25°C See Fig.6			370	-	ns	
Reverse Recovery Charge	Qrr			-	6.2	-	μC	
Peak Reverse Recovery Current	Irp			-	32	-	А	

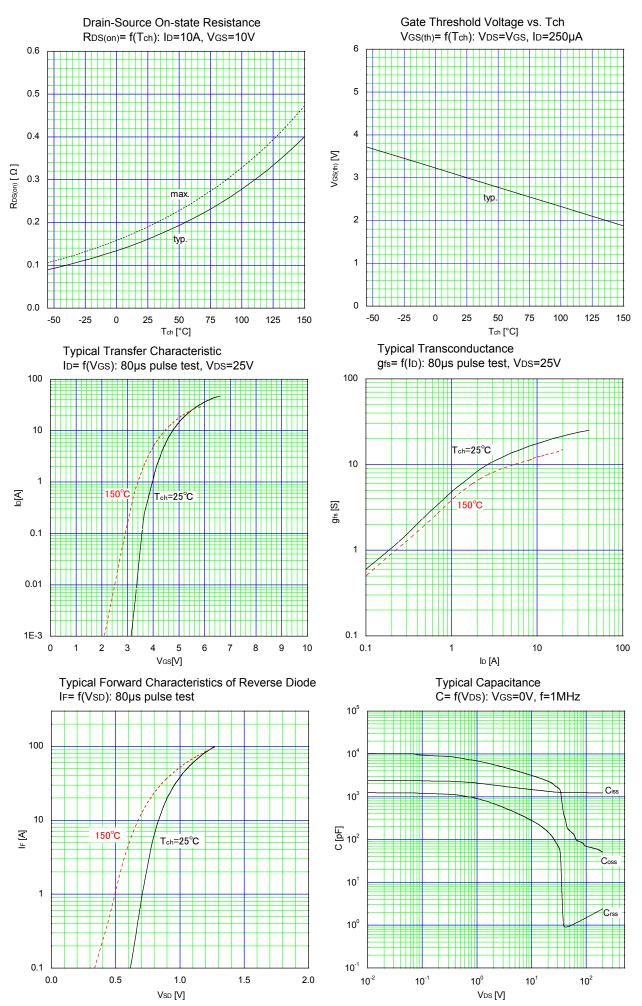
Note  ${}^*6$ :  $C_{o(er)}$  is a fixed capacitance that gives the same stored energy as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80% BVDss. Note  ${}^*7$ :  $C_{o(tr)}$  is a fixed capacitance that gives the same charging times as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80% BVDss.

#### Thermal Characteristics

Description	Symbol	min.	typ.	max.	Unit
Channel to Case	Rth(ch-c)			0.89	°C/W
Channel to Ambient	Rth(ch-a)			50	°C/W

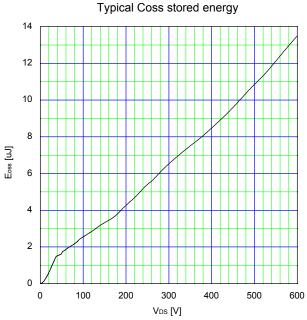


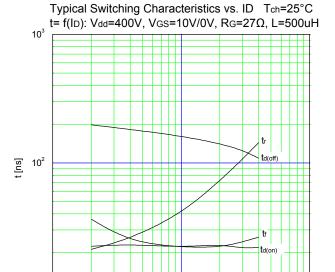
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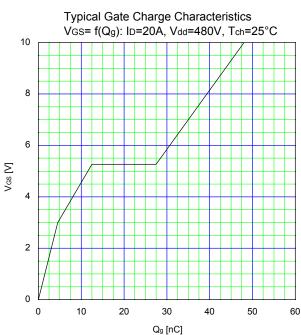


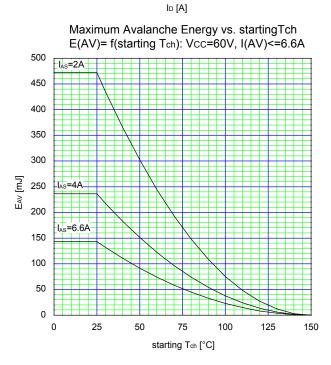


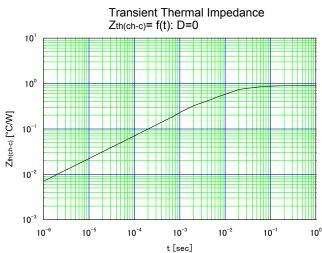
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10<sup>1</sup>

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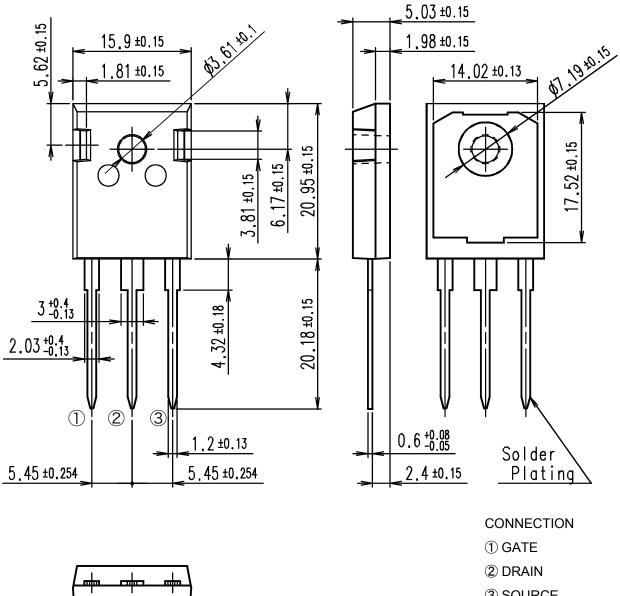






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#### ■ Outview: TO-247-P2 Package

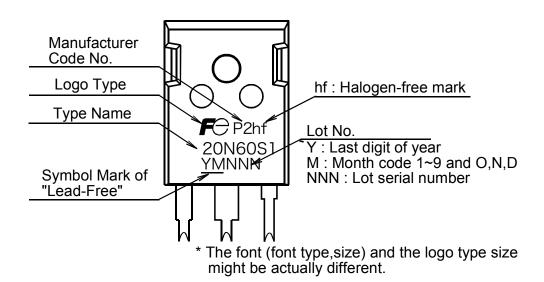


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**③ SOURCE** 

DIMENSIONS ARE IN MILLIMETERS.

#### ■ Marking



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