

# SiT9121

## 1-220 MHz High Performance Differential Oscillator

Preliminary



The Smart Timing Choice™

### Features

- Any frequency between 1 MHz and 220 MHz accurate to 6 decimal places
- LVPECL and LVDS output signaling types
- <0.75ps RMS phase jitter (random) over 12 kHz to 20 MHz bandwidth
- Frequency stability as low as ±10 PPM
- Industrial and extended commercial temperature ranges
- Industry-standard packages: 5.0 mm x 3.2 mm and 7.0 mm x 5.0 mm
- For frequencies higher than 220 MHz, refer to SiT9122 datasheet

### Applications

- SONET, Synchronous Ethernet, SATA, SAS, 10GB Ethernet, Fibre Channel, PCI-Express
- Telecom, networking, broadband, instrumentation



### Electrical Characteristics

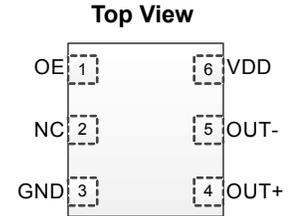
Parameter and Conditions	Symbol	Min.	Typ.	Max.	Unit	Condition
<b>LVPECL and LVDS, Common AC Characteristics</b>						
Output Frequency Range	f	1	–	220	MHz	
Frequency Stability	F_stab	-10	–	+10	PPM	Inclusive of initial tolerance, operating temperature, rated power, supply voltage and load variations
		-25	–	+25	PPM	
		-50	–	+50	PPM	
1-year Aging		-1	–	+1	PPM	First year @ 25°C
10-year Aging		-5	–	+5	PPM	@ 85°C
Operating Temperature Range	T_use	-40	–	+85	°C	Industrial
		-20	–	+70	°C	Extended Commercial
Start-up Time	T_start	–	–	10	ms	
Duty Cycle	DC	45	–	55	%	Contact SiTime for tighter duty cycle
<b>LVPECL, DC and AC Characteristics</b>						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
Current Consumption	Idd	–	61	69	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Supply Current	I_OE	–	–	35	mA	OE = GND
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = GND
Maximum Output Current	I-driver	–	–	30	mA	Maximum average current drawn from OUT+ or OUT-
Output High Voltage	VOH	Vdd-1.1	–	Vdd-0.7	V	See Figure 1
Output Low Voltage	VOL	Vdd-1.9	–	Vdd-1.5	V	See Figure 1
Output Differential Voltage Swing	V_Swing	1.2	1.6	2.0	V	See Figure 1
Rise/Fall Time	Tr, Tf	100	300	500	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	105	ns	f = 220 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Period Jitter	T_jitt	–	1.2	1.7	ps	f = 100 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.5	0.75	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds
<b>LVDS, DC and AC Characteristics</b>						
Supply Voltage	Vdd	2.97	3.3	3.63	V	
		2.25	2.5	2.75	V	
Current Consumption	Idd	–	47	55	mA	Excluding Load Termination Current, Vdd = 3.3V or 2.5V
OE Disable Current	I_OE	–	–	35	mA	OE = Vdd
Output Disable Leakage Current	I_leak	–	–	1	µA	OE = Vdd
Differential Output Voltage	VOD	200	350	500	mV	See Figure 4
VOD Magnitude Change	ΔVOD	–	–	50	mV	See Figure 4
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 4
VOS Magnitude Change	ΔVOS	–	–	50	mV	See Figure 4
Rise/Fall Time	Tr, Tf	360	495	600	ps	20% to 80%
OE Enable/Disable Time	T_oe	–	–	105	ns	f = 220 MHz - For other frequencies, T_oe = 100ns + 3 period
RMS Period Jitter	T_jitt	–	1.2	1.7	ps	f = 100 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 156.25 MHz, VDD = 3.3V or 2.5V
		–	1.2	1.7	ps	f = 212.5 MHz, VDD = 3.3V or 2.5V
RMS Phase Jitter (random)	T_phj	–	0.5	0.75	ps	f = 156.25 MHz, Integration bandwidth = 12 kHz to 20 MHz, all Vdds

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### Pin Description

Pin	Map		Functionality
1	OE	Input	H or Open: specified frequency output L: output is high impedance
2	NC	NA	Do Not Connect; Leave it floating
3	GND	Power	VDD Power Supply Ground
4	OUT+	Output	Oscillator output
5	OUT-	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage



### Absolute Maximum

Attempted operation outside the absolute maximum ratings of the part may cause permanent damage to the part. Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

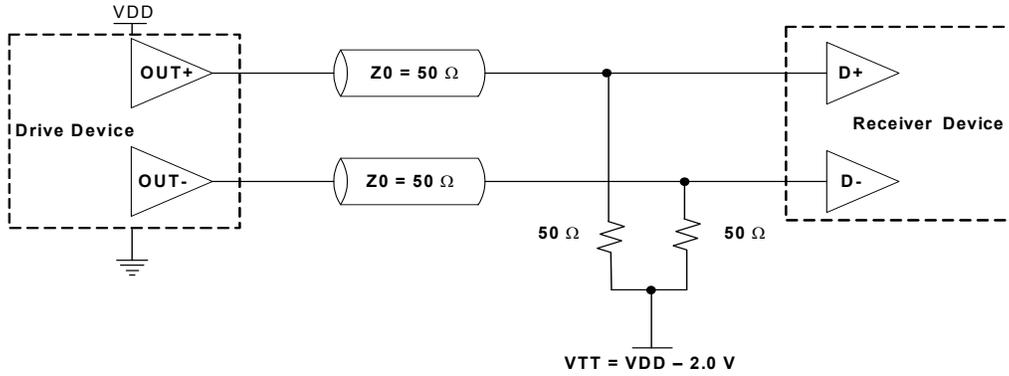
Parameter	Min.	Max.	Unit
Storage Temperature	-65	150	°C
VDD	-0.5	4	V
Electrostatic Discharge	–	2000	V
Soldering Temperature (follow standard Pb free soldering guidelines)	–	260	°C
Program Retention over -40 to 125°C, Process, VDD (0 to 3.65V)	1,000+	–	years

### Environmental Compliance

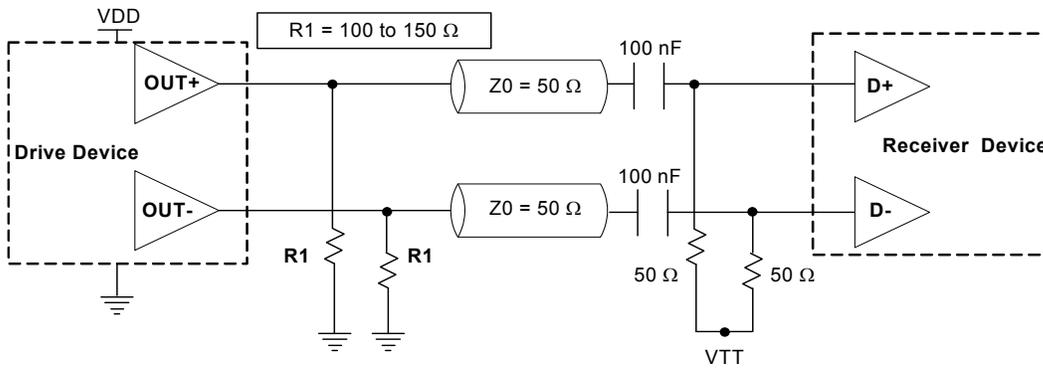
Parameter	Condition/Test Method
Mechanical Shock	MIL-STD-883F, Method 2002
Mechanical Vibration	MIL-STD-883F, Method 2007
Temperature Cycle	JESD22, Method A104
Solderability	MIL-STD-883F, Method 2003
Moisture Sensitivity Level	MSL1 @ 260°C

**Termination Diagrams**

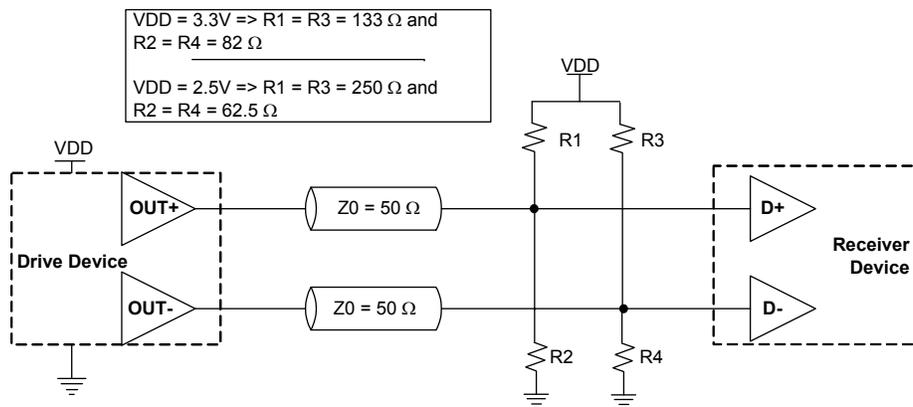
LVPECL:



**Figure 1. LVPECL Typical Termination**



**Figure 2. LVPECL AC Coupled Termination**



**Figure 3. LVPECL with Thevenin Typical Termination**

LVDS:

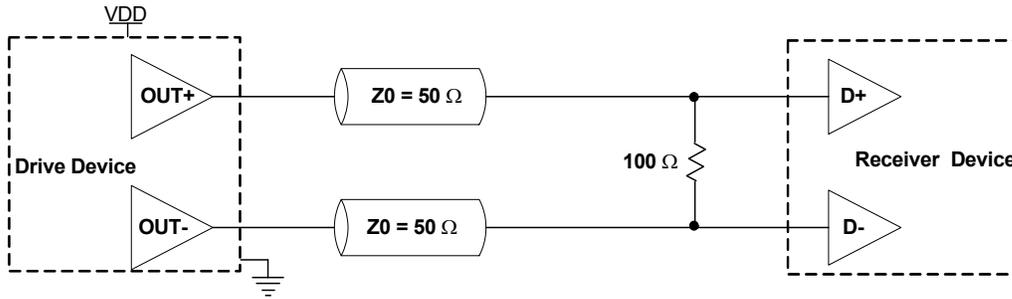
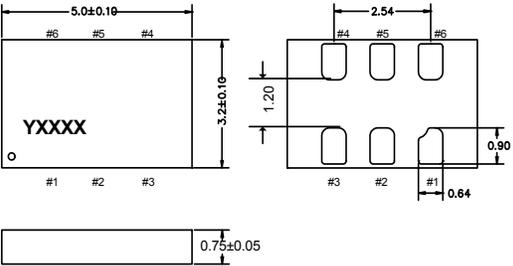
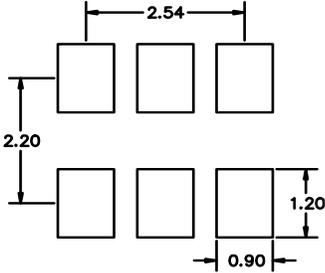
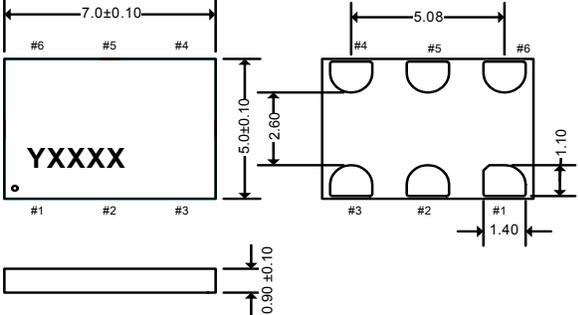
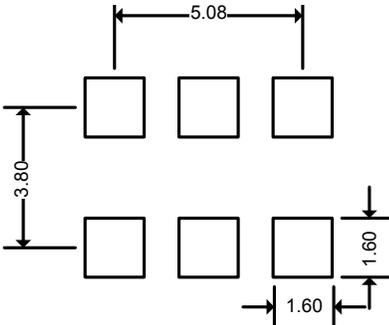


Figure 4. LVDS Single Termination (Load Terminated)

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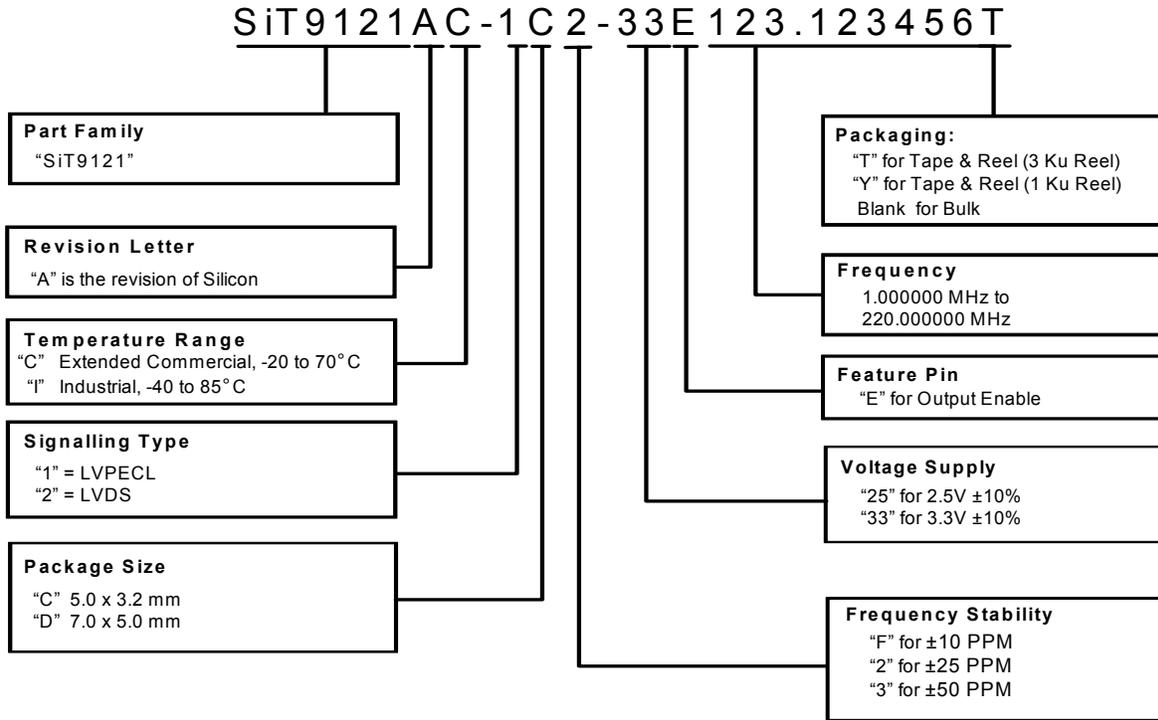
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### Dimensions and Patterns

Package Size – Dimensions (Unit: mm) <sup>[1]</sup>	Recommended Land Pattern (Unit: mm) <sup>[2]</sup>
<p><b>5.0 x 3.2 x 0.75 mm</b></p> 	
<p><b>7.0 x 5.0 x 0.90 mm</b></p> 	

1. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of "Y" will depend on the assembly location of the device.
2. A capacitor of value 0.1  $\mu$ F between Vdd and GND is recommended.

**Ordering Information**



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