BUK9520-100B

N-channel TrenchMOS logic level FET

Rev. 01 — 6 May 2009 | Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product has been designed and qualified to the appropriate AEC standard for use in automotive critical applications.

1.2 Features and benefits

- AEC-Q101 compliant
- Low conduction losses due to low on-state resistance
- Suitable for logic level gate drive sources
- Suitable for thermally demanding environments due to 175 °C rating

1.3 Applications

- 12 V, 24 V and 42 V loads
- Automotive and general purpose power switching
- Motors, lamps and solenoids

1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	-	100	V
I_D	drain current	$V_{GS} = 5$ V; $T_{mb} = 25$ °C; see Figure 1; see Figure 3	-	-	63	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	-	203	W
Avalanche ruggedness						
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 63$ A; $V_{sup} \leq 100$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped	-	-	222	mJ
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = 4.5$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 11; see Figure 12	-	16.4	22.3	mΩ
		$V_{GS} = 5$ V; $I_D = 25$ A; $T_j = 25$ °C; see Figure 12; see Figure 11	-	16.2	20	mΩ

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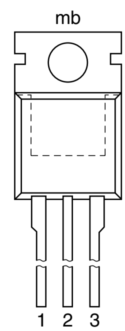
2. Pinning information

Table 2. Pinning information

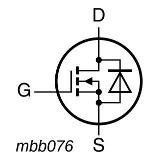
Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate		
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

Simplified outline:



SOT78A (3-lead TO-220AB; SC-46; SFM3)

Graphic symbol:



3. Ordering information

Table 3. Ordering information

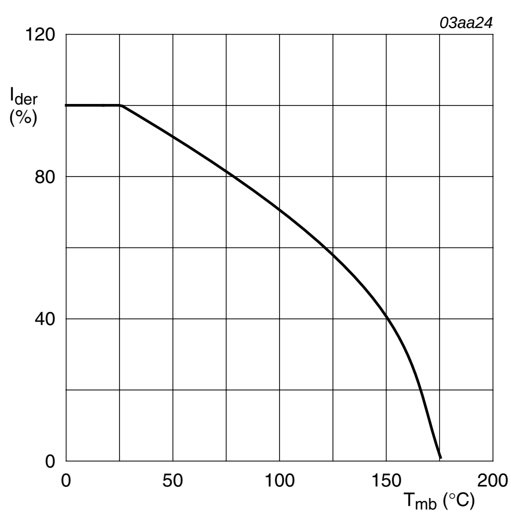
Type number	Package		
	Name	Description	Version
BUK9520-100B	3-lead TO-220AB; SC-46; SFM3	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78A

4. Limiting values

Table 4. Limiting values

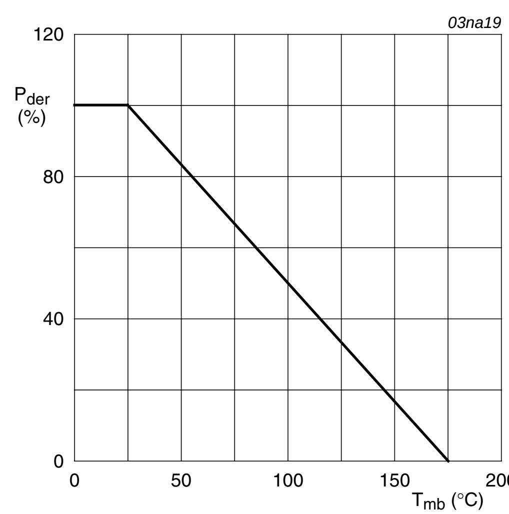
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25$ °C; $T_j \leq 175$ °C	-	100	V
V_{DGR}	drain-gate voltage	$R_{GS} = 20$ kΩ	-	100	V
V_{GS}	gate-source voltage		-15	15	V
I_D	drain current	$T_{mb} = 25$ °C; $V_{GS} = 5$ V; see Figure 1; see Figure 3	-	63	A
		$T_{mb} = 100$ °C; $V_{GS} = 5$ V; see Figure 1	-	45	A
I_{DM}	peak drain current	$T_{mb} = 25$ °C; $t_p \leq 10$ µs; pulsed; see Figure 3	-	253	A
P_{tot}	total power dissipation	$T_{mb} = 25$ °C; see Figure 2	-	203	W
T_{stg}	storage temperature		-55	175	°C
T_j	junction temperature		-55	175	°C
Source-drain diode					
I_S	source current	$T_{mb} = 25$ °C	-	63	A
I_{SM}	peak source current	$t_p \leq 10$ µs; pulsed; $T_{mb} = 25$ °C	-	253	A
Avalanche ruggedness					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	$I_D = 63$ A; $V_{sup} \leq 100$ V; $R_{GS} = 50$ Ω; $V_{GS} = 5$ V; $T_{j(init)} = 25$ °C; unclamped	-	222	mJ



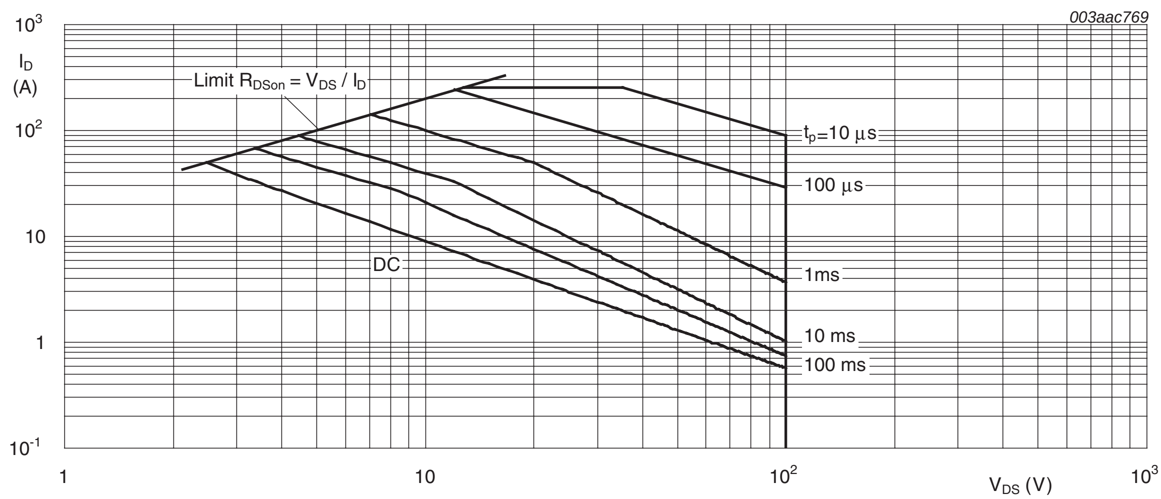
$$I_{der} = \frac{I_D}{I_{D(25°C)}} \times 100\,\%$$

Fig 1. Normalized continuous drain current as a function of mounting base temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25°C)}} \times 100\,\%$$

Fig 2. Normalized total power dissipation as a function of mounting base temperature



$T_{mb} = 25°C; I_{DM}$ is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	see Figure 4	-	-	0.75	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; SOT78 package	-	60	-	K/W

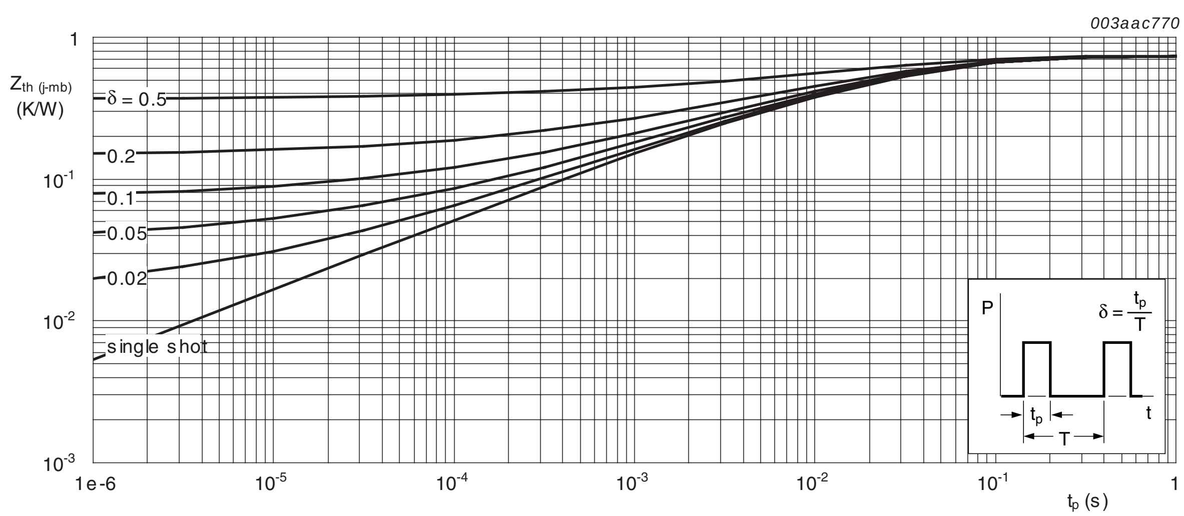


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

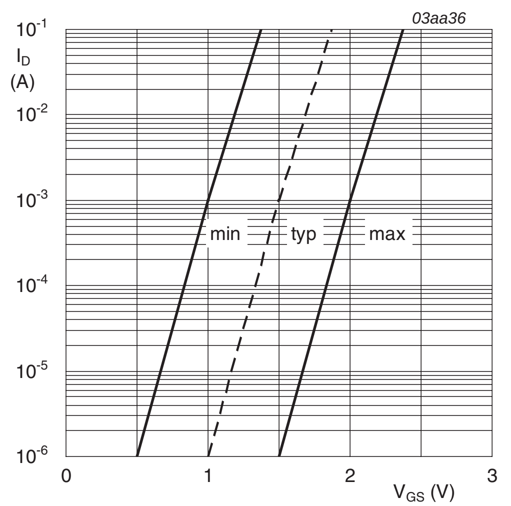
6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 0.25 mA; V_{GS} = 0 V; T_j = 25 °C	100	-	-	V
		I_D = 0.25 mA; V_{GS} = 0 V; T_j = -55 °C	90	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; T_j = 25 °C; see Figure 10	1	1.58	2	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = 175 °C; see Figure 10	0.5	-	-	V
		I_D = 1 mA; V_{DS} = V_{GS}; T_j = -55 °C; see Figure 10	-	-	2.3	V
I_{DSS}	drain leakage current	V_{DS} = 100 V; V_{GS} = 0 V; T_j = 175 °C	-	-	500	µA
		V_{DS} = 100 V; V_{GS} = 0 V; T_j = 25 °C	-	0.05	1	µA
I_{GSS}	gate leakage current	V_{DS} = 0 V; V_{GS} = -10 V; T_j = 25 °C	-	2	100	nA
		V_{DS} = 0 V; V_{GS} = 10 V; T_j = 25 °C	-	2	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 °C; see Figure 11; see Figure 12	-	16.4	22.3	mΩ
		V_{GS} = 10 V; I_D = 25 A; T_j = 25 °C; see Figure 11; see Figure 12	-	15.6	18.5	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 175 °C; see Figure 12; see Figure 11	-	-	50	mΩ
		V_{GS} = 5 V; I_D = 25 A; T_j = 25 °C; see Figure 12; see Figure 11	-	16.2	20	mΩ
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	I_D = 25 A; V_{DS} = 80 V; V_{GS} = 5 V; T_j = 25 °C; see Figure 14; see Figure 15	-	53.4	-	nC
Q_{GS}	gate-source charge		-	9.5	-	nC
Q_{GD}	gate-drain charge		-	21.2	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; T_j = 25 °C; see Figure 16	-	4300	5657	pF
C_{oss}	output capacitance		-	340	411	pF
C_{rss}	reverse transfer capacitance		-	150	201	pF
$t_{d(on)}$	turn-on delay time	V_{DS} = 30 V; R_L = 1.2 Ω; V_{GS} = 5 V; $R_{G(ext)}$ = 10 Ω; T_j = 25 °C	-	45	-	ns
t_r	rise time		-	116	-	ns
$t_{d(off)}$	turn-off delay time		-	173	-	ns
t_f	fall time		-	77	-	ns
L_D	internal drain inductance	from drain lead 6 mm from package to centre of die; T_j = 25 °C	-	4.5	-	nH
		from upper edge of drain mounting base to centre of die; T_j = 25 °C	-	2.5	-	nH
L_S	internal source inductance	from source lead to source bond pad; T_j = 25 °C	-	7.5	-	nH

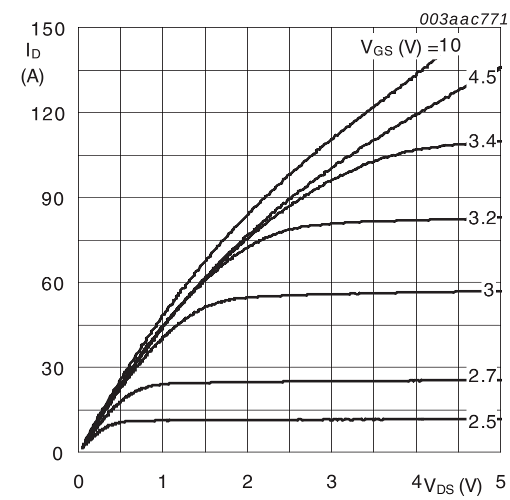
Table 6. Characteristics *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Source-drain diode						
V_{SD}	source-drain voltage	I_S = 25 A; V_{GS} = 0 V; T_j = 25 °C; see Figure 13	-	0.86	1.2	V
t_{rr}	reverse recovery time	I_S = 20 A; dI_S/dt = -100 A/µs; V_{GS} = 0 V; V_{DS} = 30 V; T_j = 25 °C	-	80	-	ns
Q_r	recovered charge		-	272	-	nC



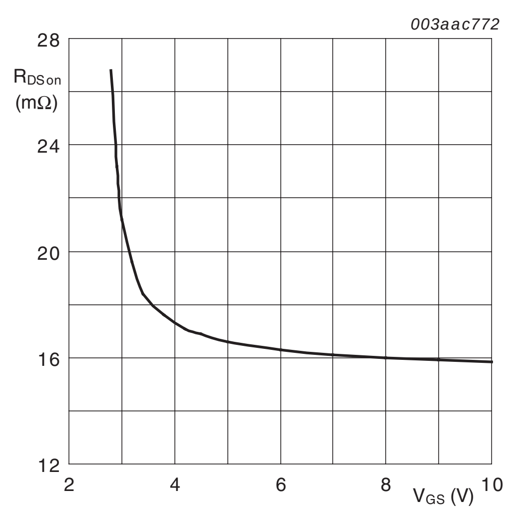
$T_j = 25\,°C; V_{DS} = V_{GS}$

Fig 5. Sub-threshold drain current as a function of gate-source voltage



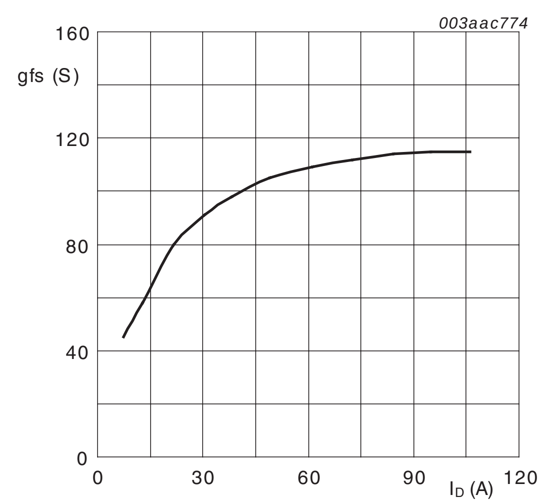
$T_j = 25°C; t_p = 300\mu s$

Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values



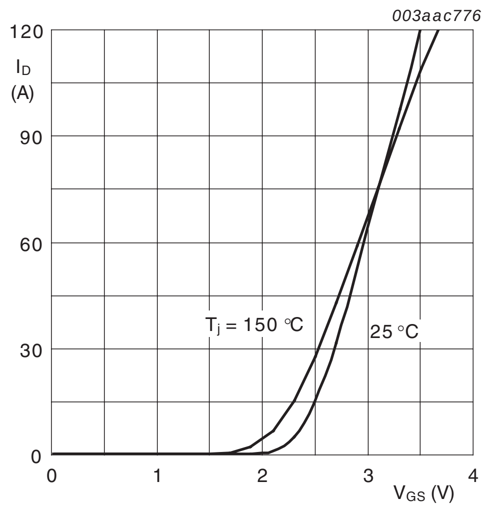
$T_j = 25°C; I_D = 25A$

Fig 7. Drain-source on-state resistance as a function of gate-source voltage; typical values.



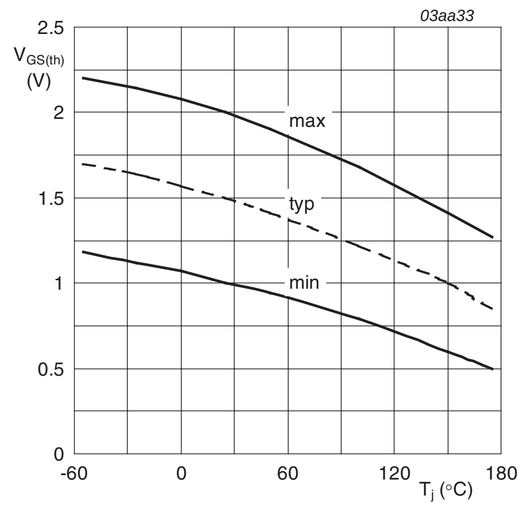
$T_j = 25°C; V_{DS} = 25V$

Fig 8. Forward transconductance as a function of drain current; typical values.



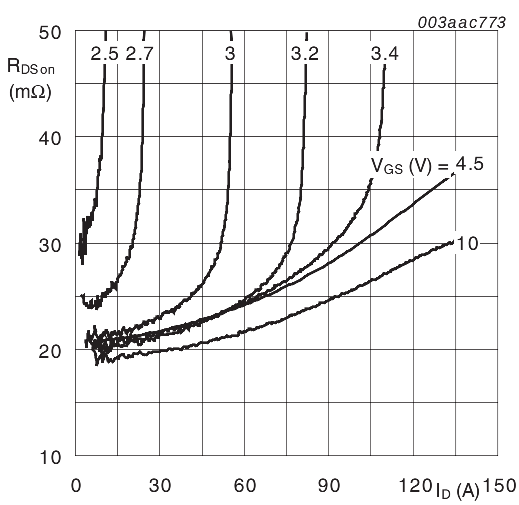
$V_{DS} = 25V$

Fig 9. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



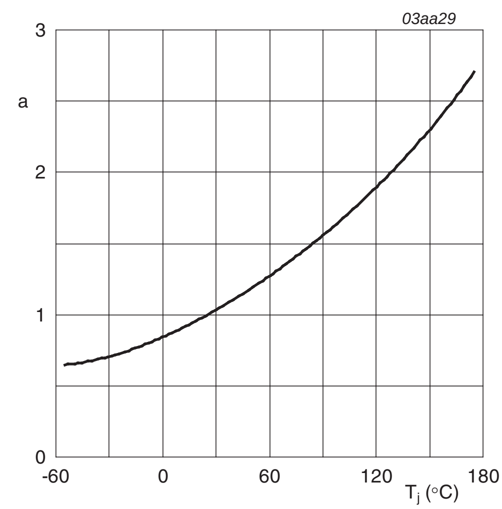
$I_D = 1mA; V_{DS} = V_{GS}$

Fig 10. Gate-source threshold voltage as a function of junction temperature



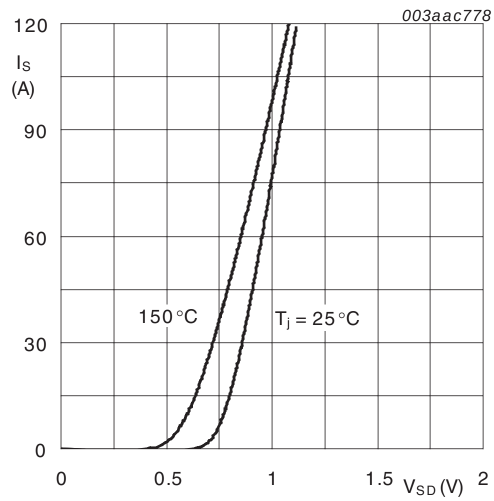
$T_j = 25°C$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature



$V_{GS} = 0V$

Fig 13. Source current as a function of source drain voltage; typical values.

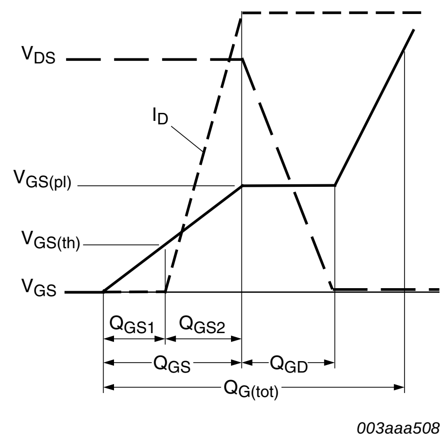
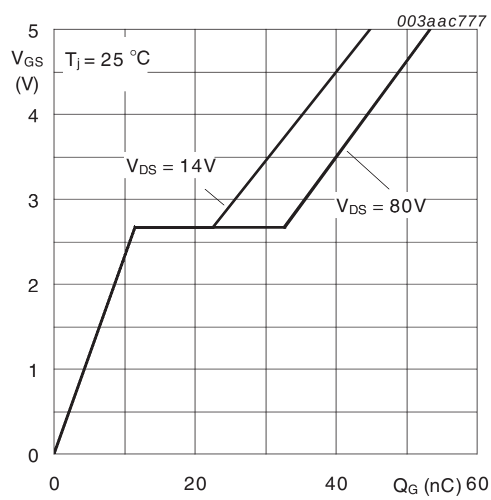
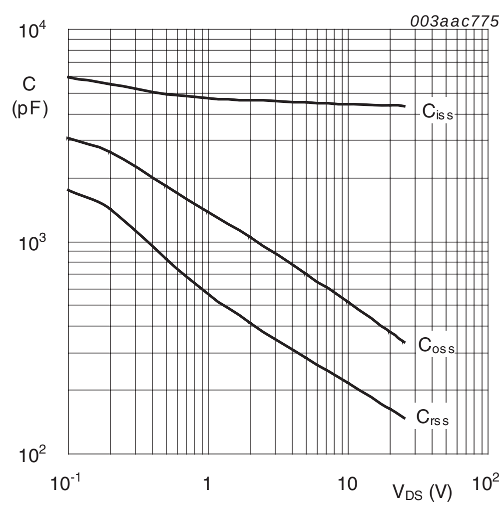


Fig 14. Gate charge waveform definitions



$T_j = 25°C; I_D = 25A$

Fig 15. Gate-source voltage as a function of turn-on gate charge; typical values.

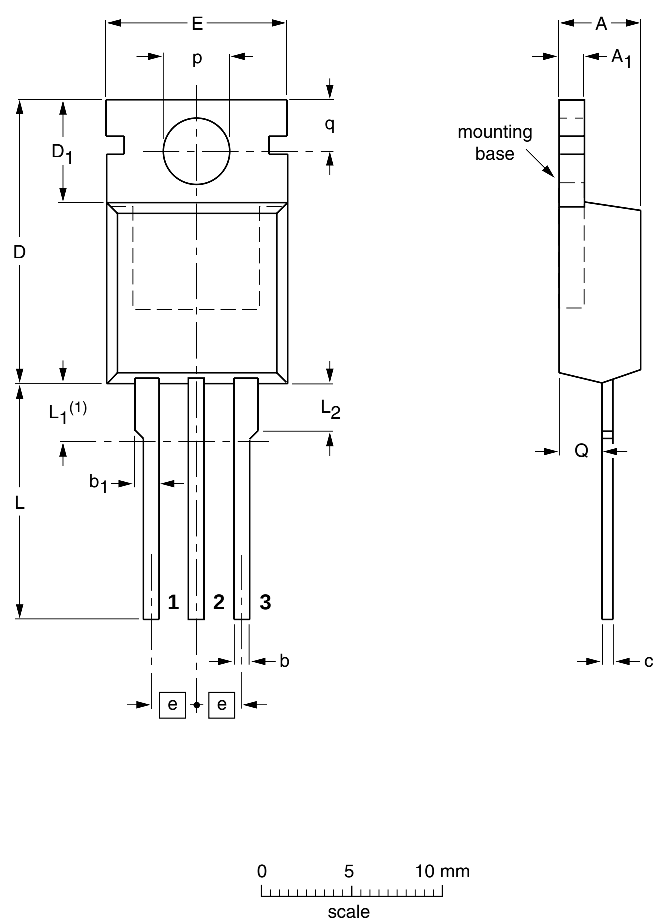


$V_{GS} = 0V; f = 1MHz$

Fig 16. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

7. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78A**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	$L_1^{(1)}$	L_2 max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.6	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

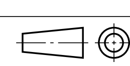
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78A		3-lead TO-220AB	SC-46			~~03-01-22~~ 05-03-14

Fig 17. Package outline SOT78A (3-lead TO-220AB; SC-46; SFM3)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BUK9520-100B_1	20090506	Product data sheet	-	-

9. Legal information

9.1 Data sheet status

Document status [1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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10. Contact information

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For sales office addresses, please send an email to: salesaddresses@nxp.com

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